Assignment - 04

1) Write a VHDL program to implement JK Flip Flop.

Title :- Implementing JK flip flop using VHDL.

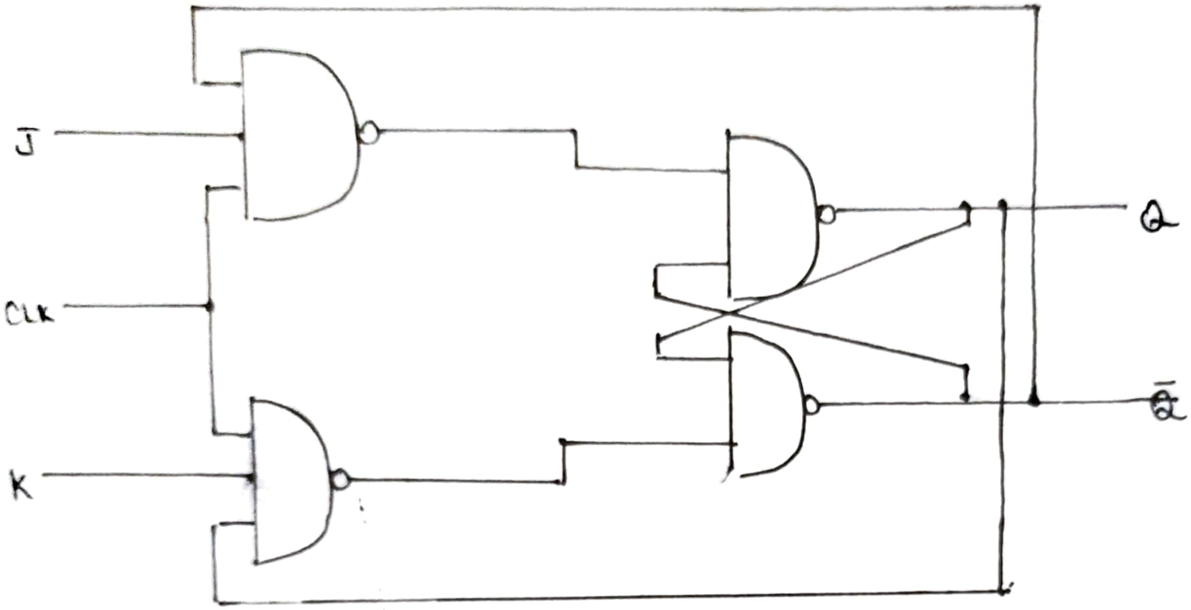
Truth Table

Preset	Clear	CLK	J	K	Q	Q(not)
×	1	×	×	×	0	1
1	×	×	×	×	1	0
0	0	↑	1	0	1	0
0	0	↑	0	1	0	1
0	0	↑	1	1	1*	0
0	0	↑	0	0	1~	0

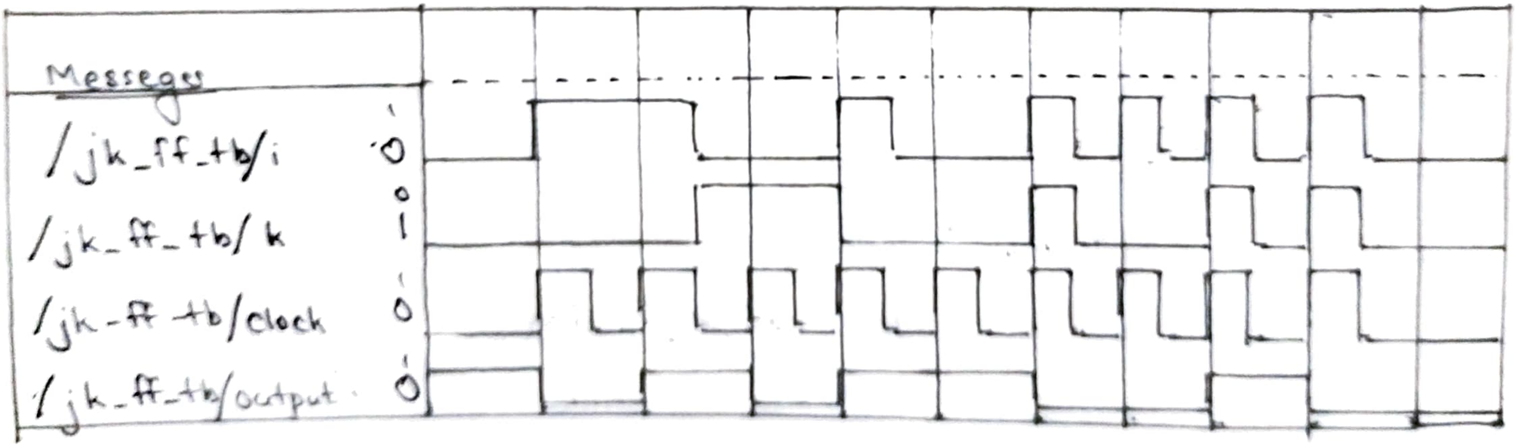
VHDL Programming

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_ARITH.all;
use IEEE.STD_LOGIC_UNSIGNED.all;
entity JK_FF is
 PORT (J, K, CLOCK: in std-logic);
      (Q, QB : out std-logic);
 end JK_FF;
Architecture bhv of JK_FF is
   begin
     PROCESS(CLOCK)
     variable TMP : std-logic;
```

```
begin
    if(CLOCK ='1' and CLOCK'EVENT) then
    if ( J='0' and K= '0') then
            TMP:= TMP;
    elsif ( J='1' ond K='1') then
            TMP := not TMP;
    elsif ( J = '0' ond K = '1') then
            TMP := not TMP;
    else
            TMP := '0';
    else
            TMP := '1';
      end if;
      end if;
            Q <= TMP;
            Q <= not TMP;
            end PROCESS;
            end bhv;
```



Circuit Diagram



Output waveform

2) Write a VHDL program to implement T flip-flop.

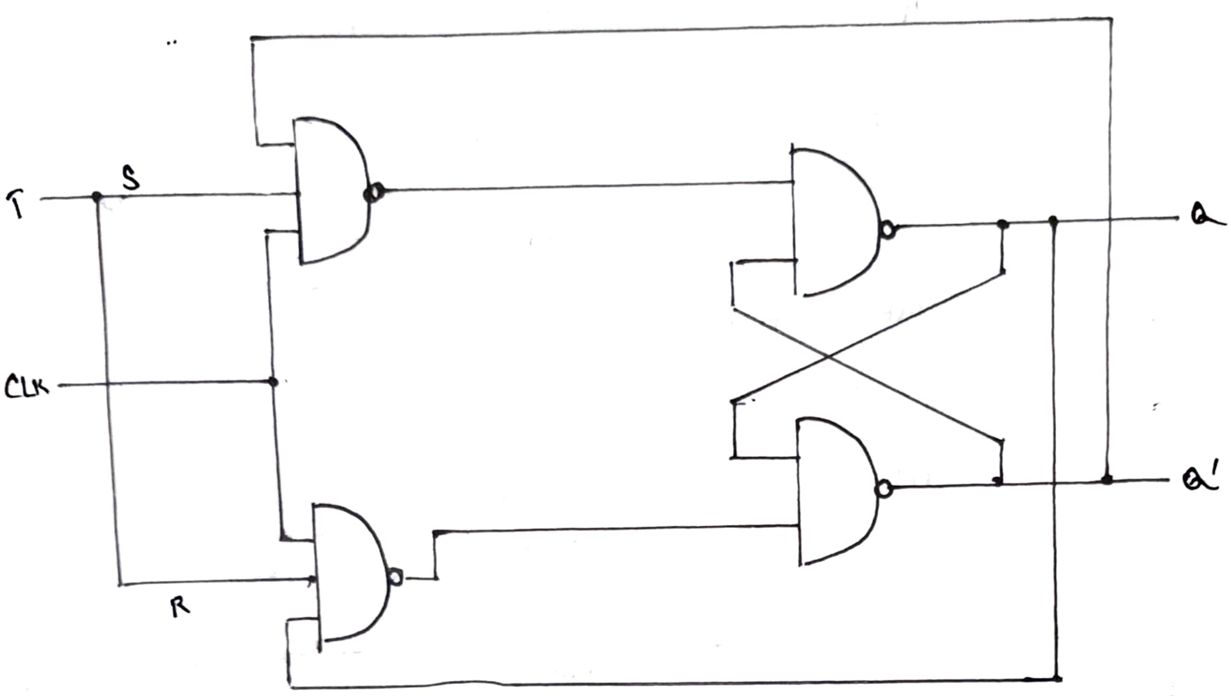
Title: Implementing T- flip-flop using VHDL.

Truth Table

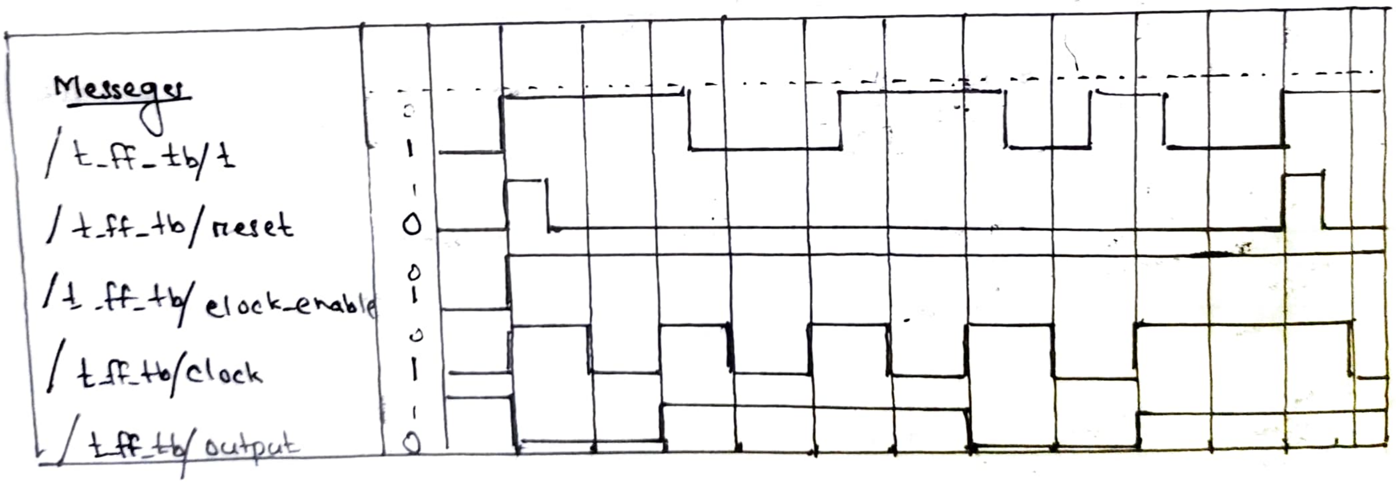
Q	T	Q(T+1)
0	0	0
0	1	1
1	0	1
1	1	0

VHDL Programming

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity T_FF is
 port (T: in std_logic;
       Clock : in std_logic;
         Q : out std_logic);
   end T_FF;
architecture bhv of T_FF is.
   signal tmp : std_logic;
      begin
          process (CLOCK)
      begin
          if Clock 'event and Clock = '1' then
if    T='0' then
        tmp <=tmp;
   elsif  T='1', then
            tmp <= not (tmp);
           end if ;
         end if;
       end  process;
           Q <= tmp;
       end    bhv;
```



Circuit Diagram



Output Waveform