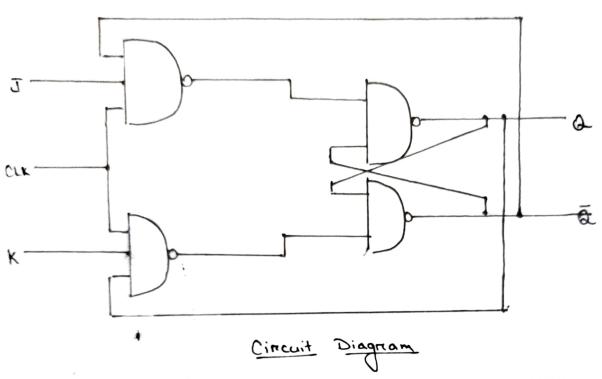
| Assignme | ent - C |)4 | | | PAGE NO. | | | | | | | |
|--|---|--|----------|--|--|--|------------|--|--|--|--|--|
| | | | рподпат | to | implement | Ĵκ | Flip Flop- | | | | | |
| Title: I | | nenting | JK Flip | Flop | using VHD | L. | | | | | | |
| Preset | | Clean | CLK | J | k | a | a(not) | | | | | |
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| VHDL Programming library IEEE; Use IEEE. 8TD-LOGIC-1164-all; | | | | | | | | | | | | |
| use TEEF. STD-LOGIC-ARITHIAII; | | | | | | | | | | | | |
| use Teer-STD_LOGIC_UNSIGNED.all; | | | | | | | | | | | | |
| entity JK-FF is | | | | | | | | | | | | |
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| and the second and the second and the second and second and second and second and second and second and second | | er | d JK- | | | | | | | | | |
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| | | | PROCES | s(CL | ock) | nagarosas (gray) to constituto estáblica a participado de la constitución de la constituc | | | | | | |
| | | | | | IMP: Std_L | ogic; | | | | | | |
| | | | | | | er's Sign | nature | | | | | |

```
if (CLOCK = 'I' and CLOCK' EVENT) then
F(J='0') and K='0') then
    IMP := TMP;
elsif ( J='1' and K='1') then
   TMP := not TMP;
elsif ( ] = 'O' and K = 'I') then
    IMP := not IMP;
else
   TIMP : = 10';
 Plse
    TMP := 1';
 end if;
  end if;
     Q <= TMP;
     a <= not TMP;
     end process;
     end bhvj
```



Messeges

/jk_ff_tb/k

/jk_ff_tb/clock

/jk_ff_tb/clock

/jk_ff_tb/octput

Output waveform

| | | | | PAGE NO. | | | | |
|---------------------------------------|--------------------|------------|---------------|-------------------------|-------|------------------|--|--|
| 2) Write | a VHDL | Prisgran | n to | implemen | 7 + | Flip-flop. | | |
| Title: | Implement Table | ting 7- | Flip-flop | using | NHDL | · | | |
| · · · · · · · · · · · · · · · · · · · | _ | 7 | Q(7+1) | | | | | |
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| VHDL | Programm | ing | | | | | | |
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| | | se TEEE | | GIC -1164 | ·ALL | | | |
| | en | ntity T. | -ff is | | | | | |
| | | pont (7: | in st | d-logicj | | | | |
| | | Cloc | k: in 8 | td-logic; | | | | |
| | | Q | : out s | 3+d-10gic); | | | | |
| , | | end 7 | | | | | | |
| | On (| chitecture | bhu | of T-F | f is. | | | |
| | | Signal | tmp: st | d-logic; | | | | |
| | |) begi | tmp: st | 0 - | | | | |
| | | V | process (| | | | | |
| | | be | , | Service Control Control | | | | |
| | | | J if Clock | event | and | Clock = '1' then | | |
| | | | | | | | | |

end if;

end process;

Q <= tmp;

end bhv;

