Computer Organisation & Architecture Lab	
Assignment - 1	
1) Write a VHDL priogram to implement all the ANT data flow.	D G
Take 710W.	(
Title: Implementation of AND gate using da	ta
Flow modelling. gate using da	
7	
Symbolic Diagram :- A	
\	
8	
Boolean Expression: [A.B]	
- [H. 8]	
Indth Table:	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
0 0	
0 /	
1] 1] 1	
VHDL Code:	
Library TEEE;	
use TEEE. std_lagic_1164.all;	
entity AND-gate is	
part A: in std loois:	
B: in std_logic;	
port (A: in std-logic; B: in std-logic; Y: Out std-logic);	
end AND_gate;	
on chitechture and ania of ania	
begin begin	
Y <= A AND R.	
begin > <= A AND B; end and Logic;	
Output Wayerine	
Inputs	
A :	
3 '	
У '	
$(ns) \rightarrow$	

AND gates using

2) Write a VHDL program to implement all OR Grate using data flow modelling.

Title: Implementation of OR Grate using data flow modelling.

Symbollic Diagnom:

$$A \longrightarrow Y = A+B$$

Boolean Expressions: - (A+B)

Truth	Table	;- :	
	A	В	Y=(A + B)
	٥	٥	0
	0	1	1
	1	0	1
	1	1	1

VHDL Code:

Library TEEE;

use TEEE. Std_logic_1164. all;

entity OR-gate is.

Port (A: in std-logic;

B: in std-logic; Y: Out std-logic);)

end OR-gate;

architechture OR-gatelagic of OR-gate is

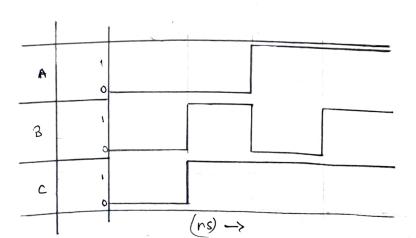
Y <= A AND B;

end OR-gateLogici

begin

Y(= A AND B;

and and Lagic:



3) Write a VHDL Programming to implement oil NOT Grate using data Flow modelling:

Title: Implementation of NOT Grate using data flow modelling.

Symbolic Diogram :-

A Y = A'

Truth Table: -

VHDL Code:

Library IEEE;

entity NOT-gate is

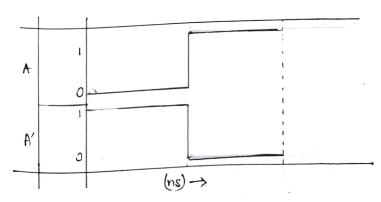
Port (A: in 8td-logic)

Y: Out std-logic);

end Not-gate;

architechture NOTLogic if NOT-gate is

begin Y <= NOT (A); end NOTLogic;



4) Write a VHDL programs to implement all NAND Grate using data flow modelling.

Title: Implementation of NAND Grate using data flow modeling.

Boolean Expression: - Y = AB

Symbolic Diagram: A Do-Y=AB

VHDL Code:

Library IEEE;

Use IEEE_Std_logic_1164.all;

entity NAND_gate is

Pont (A: in std_logic;

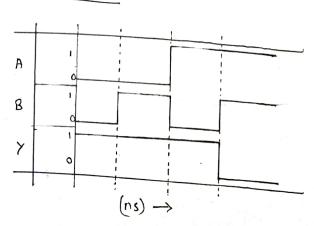
B: in std_logic;

Y: out std_logic;

end NAND_gate;

anchitechture NANDLogic of

architechture NANDLogic of NAND-gate is begin Y (= A NAND B; end NANDLogic;



5) Write a VHDL Arrogram to implement all NOR GATE using data flow modeling

> Title: - Implemention of NOR gate using data flow modeling

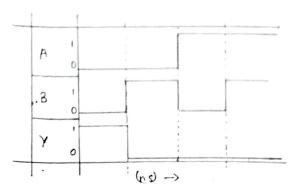
Irruth Table ..

A	В	$y = \overline{A + B}$
0	0	1
٥	ı	0
1	0	0
1	1	0

VHDL Code:

arrehitecture NORLogic of Norgate

erd NorLogie;



6) Write a VHDL program to implement all XOR Grate Using data flow modeling.

Title: - Implementation of xor gate using data flow modeling

Boolean Expression: Y= A B

Symbolic Diagram:

Truth Table :-

A	В	B AA = Y
0	٥	0
O	1	ı
1	0	1
1	1	0

VHDL CODE :-

Library TEEE;

use TEEE_std_lagic_1164 all; entity xorgate is

Port (A: in std-logic;

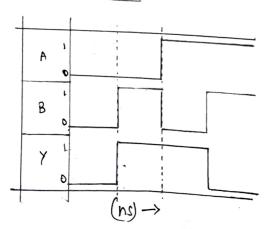
B: in std-logic;

Y: out std-logic);

end XORQ; architechture XORLogic of XORQ is.

begin V <= A xor B;

end xor Logic;



7) Write a VHDL program to implement all xNOR Gate using data flow modeling

> Title: - Implementation of XNOR gate using modeling Flow

Boolean Expression: $Y = Y = A \oplus B$

Inuth Table :-

H	8	Y = A + B
0	٥	1
0	١	٥
١	٥	0
1	1	1

VHDL CODE:

Library TEEE;

use TEEE_std_logic_1164.all; entity xnorg is

entity xnorg is

Port (A: in std-logic;

B: in std-logic;

Y: out std-logic);

end XNORg;

architechture XNORLogic of XNORa is

begin y <= A xnor B;

end XNORLogic;

