Performed transient analysis at 200ns and plotted the graphs.

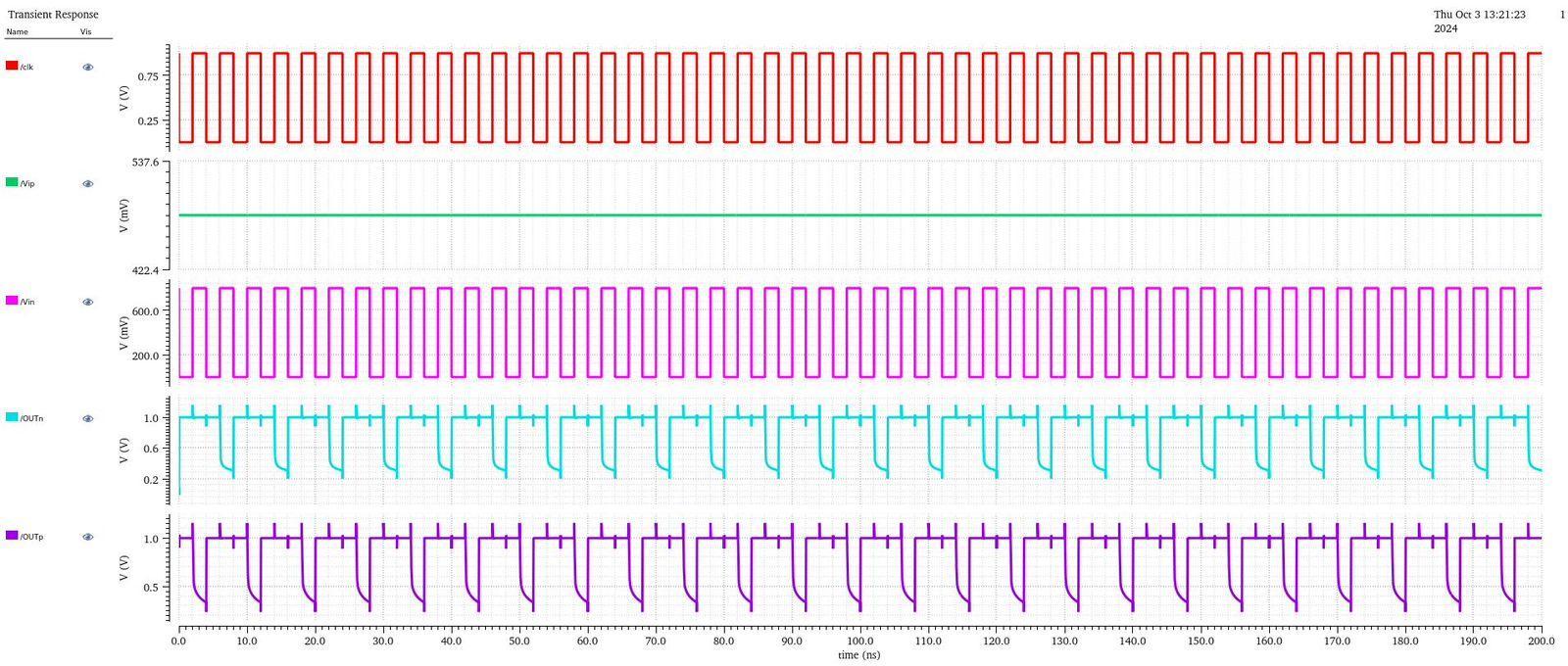


Figure: Output graph

### **Breakdown**

* **clk (Red Waveform):**

This is the **input clock signal**. It's a square wave with a 50% duty cycle, switching between a low voltage (likely 0V) and a high voltage (Vdd, likely around 0.8V). It has a period of approximately 10ns, corresponding to a frequency of 100MHz. This signal serves as the primary timing reference for the entire circuit.

* **vC (Green Waveform):**

This waveform is a constant DC voltage, staying at approximately **537.6mV**. It is a reference voltage used within the circuit and is not a dynamic signal.

* **vOut (Pink/Magenta Waveform):**

This is the **output signal of the circuit**. The voltage levels are roughly 0V and 600mV.

* **clk\_inv (Light Blue/Cyan Waveform):**

This is the **inverted clock signal**. It's a square wave that is a mirror image of the main clock signal (clk). When clk is high, clk\_inv is low, and vice versa. Its voltage levels are between approximately 0.2V and 1.0V. The presence of this signal indicates that an inverter is a part of the circuit design.

* **vOut\_inv (Dark Purple Waveform):**

This is the **inverted output signal**. It's the inverse of the vOut signal. When vOut is high, vOut\_inv is low, and vice versa. Its voltage levels are approximately between 0.5V and 1.0V. The presence of both vOut and vOut\_inv suggests that the circuit output is available in both normal and inverted forms.