# EC lab 7

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## Objective-

(i) To design a Common-Emitter Transistor (n-p-n) Amplifier Circuit
(ii) To obtain the frequency response curve of the amplifier and to determine the mid frequency gain, Amid, lower and higher cut-off frequency of the amplifier circuit.

## Introduction:-

The most common circuit configuration for an n-p-n transistor is that of the Common Emitter Amplifier and that a family of curves known commonly as the Output Characteristics Curves, relates the Collector current (IC), to the output or Collector voltage (VCE), for different values of Base current (IB). All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value. Pre-setting the amplifier circuit to operate between these two maximum or peak values is achieved using a process known as Biasing. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

The single stage common emitter amplifier circuit shown below uses what is commonly called "Voltage Divider Biasing". The Base voltage (VB) can be easily calculated using the simple voltage divider formula below:

$$VB = VCCR2\ R1 + R2$$

Thus the base voltage is fixed by biasing and it is independent of base current as long as the current in the divider circuit is large compared to the base current. Thus assuming IB ≈0, one can do the approximate analysis of the voltage divider network without using the transistor gain, β, in the calculation. Note that the approximate approach can be applied with a high degree of accuracy when the following condition is satisfied:

$$BRE \geq 10R2$$

## Laboratory Report-

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(ii) To obtain the frequency response curve of the amplifier and to determine the mid- frequency gain, Amid, lower and higher cut-off frequency of the amplifier circuit.

Observations: β =100 ,R1= 26 (27)kΩ, R2= 5(4.7+0.22)kΩ, RC = 4 (3.9) kΩ, RE= 1kΩ (RE1=470Ω, RE2=560 Ω), C1= C2= 1μF (2 nos.), CE= 100μF

Table-I:
D.C. Analysis of the circuit (For VCC = 12V)

| Parameter | Computed Value(Theoretical) | Observed Value(Experimental |
|---|---|---|
| VB (in V) | 0 | 0.7 |
| VE (in V) | 0.1 | 0.7 |
| IC~IE (in mA) | 4.58 | 4.63 |
| VCE (in V) | 0.5 | 0 |

DC Q-point is at ( 0. 7 V, 25 mA)

Table-II:
A.C. Analysis of the circuit.

| Parameter | Computed Value(Theoretical) | Observed Value(Experimental |
|---|---|---|
| re ′ (in Ω) | 25 | 3.2 |
| Zin(base) (in Ω) | 3200 | 322 |
| Zin(stage) (in Ω) | 2800 | 2.8 |
| rc (in Ω) | 0 | 5Ω |
| Av | 0.546 | 33.3 |

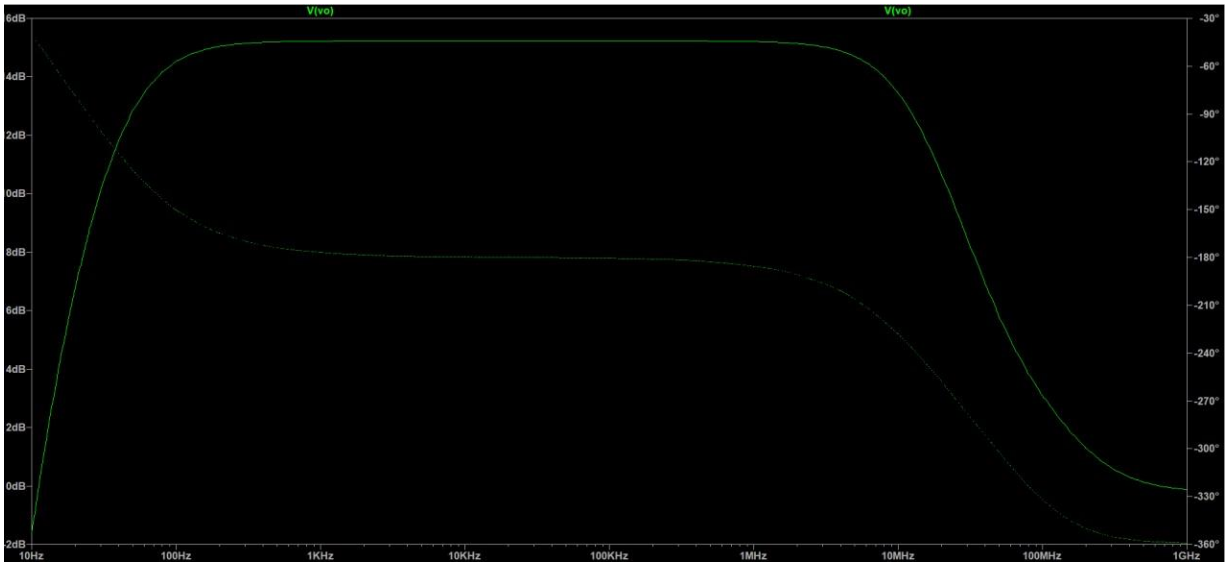
Table-II:

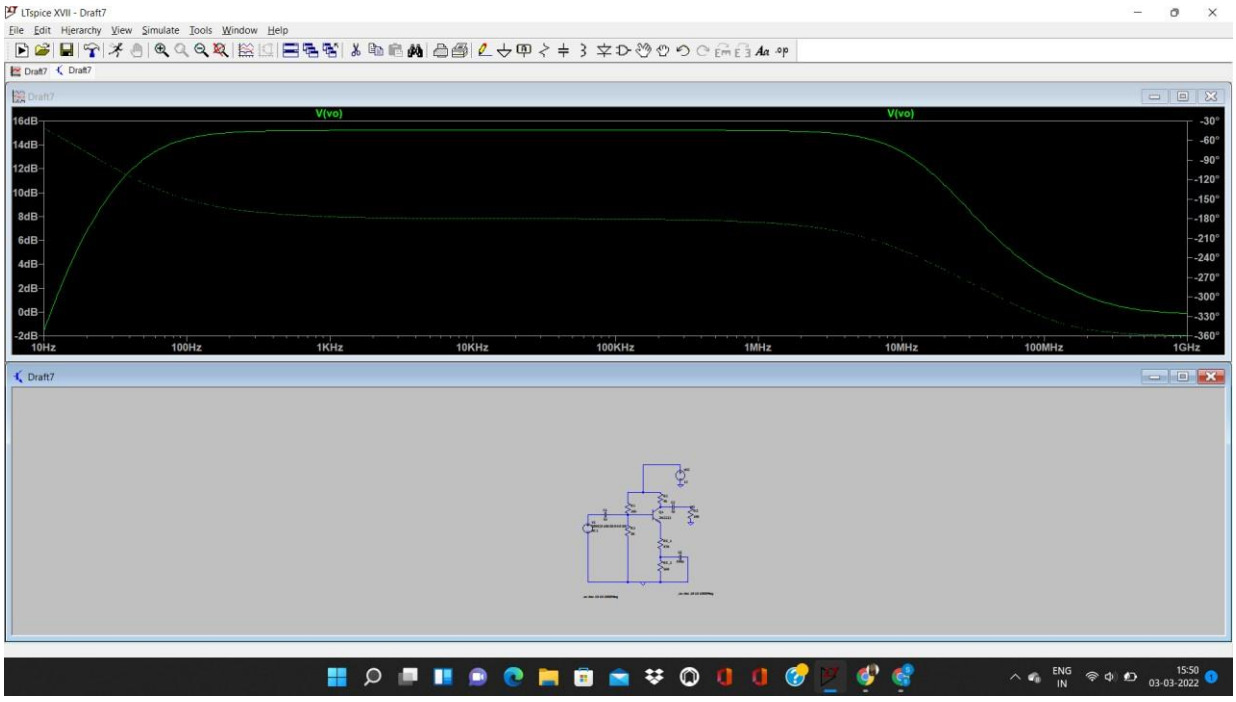
Frequency response: Vi(pp) =12mV

| S. No | Frequency, f (in Hz) | Vo(pp) (V) | Gain ,Av=Vo(pp)/ Vi(pp) | Gain (in dB) |
|---|---|---|---|---|
| 1 | 0 | 0.5 | 0.25 | -6 |
| 2 | 20 | 0.717 | 0.5 | -3 |
| 3 | 50 | 1 | 1 | 0 |
| 4 | 60 | 1.414 | 2 | 3 |

Graph:

Plot the frequency response curve (semi-log plot) and determine the cut-off frequencies, bandwidth and mid- frequency gain.




LTspice XVII - Draft7
File Edit Hierarchy View Simulate Tools Window Help
Draft7
V(vo)
V(vo)
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB
-2dB
-30°
-60°
-90°
-120°
-150°
-180°
-210°
-240°
-270°
-300°
-330°
-360°
10Hz
100Hz
1KHz
10KHz
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1MHz
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100MHz
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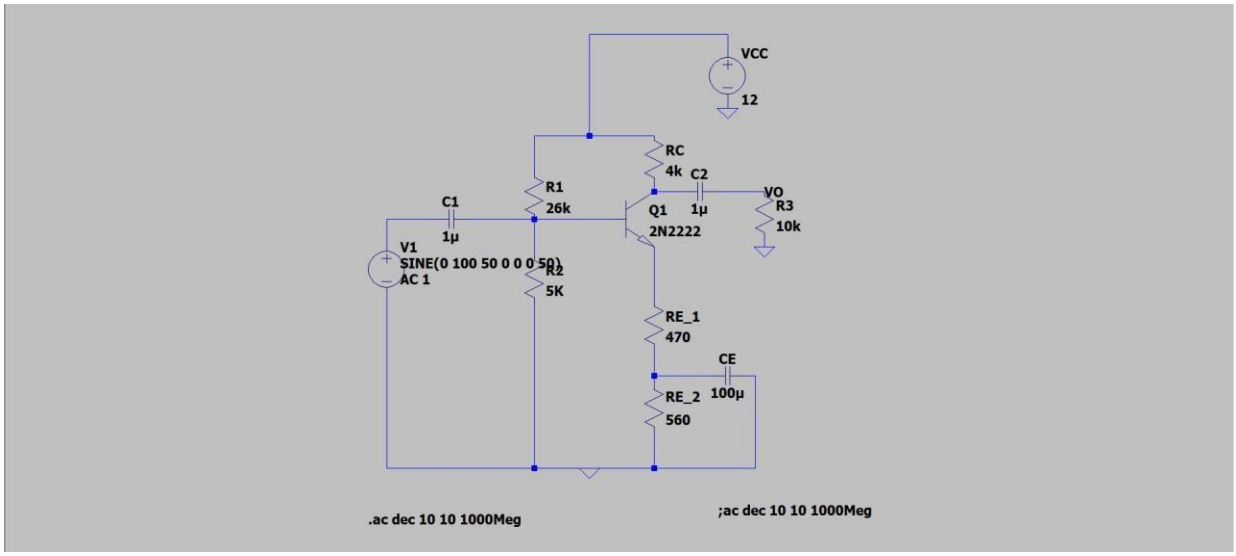
VCC
12
RC
4k
C2
1µ
VO
R3
10k
R1
26k
C1
1µ
Q1
2N2222
V1
SINE(0 100 50 0 0 50)
AC 1
R2
5K
RE_1
470
CE
100µ
RE_2
560
.ac dec 10 10 1000Meg
;ac dec 10 10 1000Meg

# Thank you