Class-D Amplifier — README

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1. Overview

This README documents a practical Class-D audio amplifier design made from common components (timer IC, op-amps, MOSFETs, passive parts). The design avoids dedicated Class-D driver ICs and uses basic building blocks so you can learn how PWM audio switching amplifiers work and reproduce them using hobbyist tools.

Primary features: - Single-ended stereo-ready topology (document focuses on one channel). - Analog input modulation (PWM generated by comparing audio with triangle). - Half-bridge MOSFET output stage. - LC low-pass output filter to recover audio for a loudspeaker. - Emphasis on component selection rationale, PCB layout, and simulation guidance.

2. Design goals & specifications

Target specifications (example, adjustable): - Supply voltage (Vbus): ±12–±24 V recommended (single-supply split or single rail with bootstrapped gate drive). We'll use **+24 V** single supply as a working example. - Output power: up to **50 W** into **4 Ω** (peak currents ≈ 7 A peak, RMS ≈ 5 A — design for 8–10 A margin). - Frequency response: 20 Hz – 20 kHz (after LC filter) - THD+N target: <1–3% depending on layout and filter quality - Switching frequency (carrier): **~300 kHz** (tradeoff between filter size, MOSFET switching losses, and audible artefacts)

Notes: Choose supply and MOSFETs to match the desired power. Lower supply voltages limit max power.

3. Block diagram

Input (RCA / line) → Input conditioning (R, C, gain) → Comparator (PWM): audio vs triangle → Dead-time & gate drive → Half-bridge MOSFETs → LC filter → Speaker

Additionally: power rails, bootstrap or gate driver, logic/gate deadtime, decoupling, and feedback (if feedback used).

4. Component selection — parts list and reasoning

Below are recommended components and the reasoning behind each choice. Where multiple options exist, guidelines are given to choose alternatives.

Active building blocks

- **Triangle carrier oscillator:** Use a timer or op-amp relaxation oscillator. A stable triangle is needed; a good choice is an op-amp integrator fed by a comparator, or a 555 in astable with an integrator to shape triangle. For stability and low distortion, the **op-amp integrator + comparator** approach is preferred.
- Example ICs: general-purpose op-amps such as **LM358 / TL072 / NE5532**. Use a rail-to-rail op-amp (LM358) if using single-supply 24 V.
- Reason: op-amps give better waveform linearity and more controllable frequency than 555-derived triangles.
- **PWM comparator:** high-speed comparator or fast op-amp to compare audio with triangle. Use a comparator with fast slew rate (e.g., LM311 family or a fast op-amp). If using op-amps, ensure bandwidth and slew rate support 300 kHz carrier.
- Example: **LM311** (comparator) or a faster op-amp like **OPA2134** for audio plus a dedicated comparator for high-speed switching.
- **Gate drive & dead-time:** MOSFET gates require proper gate drive levels and dead-time to avoid shoot-through. Ideally use a MOSFET gate driver IC, but since the requirement was to avoid dedicated Class-D ICs, a simple discrete bootstrapped high-side gate drive or transformer driver can be used. For safety and simplicity, it's recommended to use a gate driver IC such as **IR2184** (note: this is a gate driver IC — allowed since it's not a Class-D audio IC). If you strictly want discrete, design a bootstrap using a diode, capacitor and a level-shifting driver made from transistors.
- Reason: MOSFET gates need fast, low-impedance drive to minimize switching losses.
- **MOSFETs (output):** Choose N-channel MOSFETs for half-bridge. Key parameters:
- Vds rating > 1.5×Vbus (for safety). For 24 V choose MOSFETs rated 60 V or 80 V.

- Low Rds(on) ($\leq$ 50 mΩ for high current), low gate charge (Qg) to reduce driver stress.
- Example parts: **IRLR7843**, **IRFZ44N**, **STP55NF06**, or modern logic-level MOSFETs like **STB55NM60N** (choose by needed ratings).
- Reason: low conduction loss and manageable switching losses.

Passive components

- **LC filter:** L and C chosen to set cutoff just above 20 kHz but well below switching frequency.
- Fc = $1/(2\pi\sqrt{(L \cdot C)})$. For a 4 Ω load, typical fc = 25 kHz. Example: L = 30 µH, C = 1 µF (electrolytics + film in parallel). We'll show calculation in section 7.
- **Decoupling capacitors:** Large electrolytic bulk caps (e.g., 470 µF–2200 µF @35V) and multiple ceramics (100 nF, 1 µF) near MOSFET drains and supply pins.
- **Snubbers / RC damping:** small RC across MOSFETs or across transformer to damp ringing. A small RC (e.g., 100 Ω + 100 pF) can help.
- **Gate resistors:** 5–22 Ω series gate resistors to control dv/dt and reduce ringing.
- **Dead-time network:** Simple resistor/cap to delay gate edges if necessary.

Example BOM (single-channel)

- Op-amps: 2 × LM358 (one for triangle oscillator, one for comparator), or 1 × LM358 + 1 × LM311 comparator.
- MOSFETs: 2 × N-channel MOSFETs rated 60 V, Rds(on) $\leq$ 50 mΩ, e.g., IRF3205 or more modern equivalents (2 per half-bridge for paralleling optional).
- Inductor: 30 µH, rated for 10 A DC
- Capacitor (output filter): 1 µF film + 10 µF electrolytic
- Bulk caps: 2 × 1000 µF @ 35 V
- Gate driver: IR2184 (optional, recommended)
- Misc: resistors, ceramics, connectors, heatsink, PCB mounting hardware

5. Circuit description (schematic walkthrough)

(Here we describe the key sub-circuits; include reference netlist in simulation section.)

5.1 Triangle oscillator

Use an op-amp integrator driven by a square wave generator (comparator with hysteresis). The comparator toggles at the carrier frequency; its output charges/discharges the integrator producing a linear triangle. Adjust R and C in integrator to shape slope and amplitude.

5.2 PWM comparator

Audio input (after anti-aliasing and gain stage) is offset to the common-mode of the triangle (if single-supply) and compared with the triangle. Comparator output is a PWM stream containing audio information in pulse width.

5.3 Dead-time & gate drive

Comparator outputs drive gate driver input which produces high-side and low-side gate signals with programmable dead-time (internal to driver or via small RC delays). If using discrete drivers, ensure dead-time to avoid shoot-through.

5.4 Half-bridge output stage

MOSFETs arranged as high-side and low-side N-channel in half-bridge. The switching node (between MOSFET drains) is the PWM output that feeds the LC filter.

5.5 Output LC filter

LC low-pass removes high-frequency carrier, passing audio to speaker. Place L near MOSFETs, C near speaker. Add small damping resistor in series with L if ringing occurs.

6. PWM generation & carrier selection

Carrier frequency choice

- Must be well above audio band so filter can remove carrier. Common range: 200 kHz–600 kHz.
- Higher carrier → smaller filter components but increased switching losses.

Choice for this design: 300 kHz

Triangle amplitude and comparator thresholds

- Triangle amplitude must exceed maximum audio amplitude to generate full-range PWM.
- For single-supply systems, offset audio to mid rail (Vbus/2) or use coupling capacitors and biased comparator mid-level.

Dead-time

- Insert 50–200 ns dead-time depending on MOSFET switching speed. Ensure driver supports dead-time control or implement via RC delays.

7. Output filter design (LC) — example calculations

Design target: fc ≈ 25 kHz with 4 Ω load.

Choose C = 1 µF (film capacitor recommended). Then L = 1/((2π·fc)^2 · C)

Compute L for fc=25 kHz:

L = 1 / ((2π·25e3)^2 * 1e-6) = 1 / ((157079.63)^2 * 1e-6) ≈ 1 / (2.467e10 * 1e-6) ≈ 1 / 2.467e4 ≈ 40.55 µH

So choose L ≈ 33–47 µH (choose a real 30–47 µH part rated for current). We earlier suggested 30 µH; 33–47 µH is acceptable. If using 30 µH, fc increases slightly (~28 kHz) — still acceptable.

Damping and Q factor: - For loudspeaker (low resistance), LC resonates; include series resistor with L or small series ESR in C to control Q and avoid peaking. - Example: small series resistor 0.5–1 Ω in series with L to damp resonance.

8. Power supply considerations

- Bulk capacitance close to MOSFET Vbus rails: 1000 µF+ electrolytic per rail (or per +24 V). Use low-ESR caps.
- Add ceramic decoupling 100 nF and 1 µF near MOSFET drain supply pins.
- Ensure supply traces are thick and short.
- Heatsinking: MOSFETs should be mounted on a heatsink; calculate thermal dissipation from conduction and switching losses.

9. PCB design guidance

9.1 Board size & layers

- **Recommended PCB size (single channel):** ~100 mm × 80 mm (allow 2 channels on a 160 × 100 mm board).
- **Layers:** 2-layer FR4 is OK. For better thermal and EMI performance, use 2 oz copper on the bottom layer with a ground plane. If available, use 4-layer with dedicated power and ground planes.

9.2 Copper thickness & trace width

- Use **2 oz (≈70 µm)** copper for power traces if possible. If using 1 oz (35 µm), increase trace width accordingly.

Estimate trace width for 8 A continuous (approx): - With 1 oz copper, to carry ~8 A safely, you need ≈10–12 mm trace width (on internal/outer layers). For 2 oz, ≈6–7 mm.

Helpful reference (approx): - 1 oz (35 µm): 5 A → ≈5 mm wide; 8 A → ≈10 mm wide. - 2 oz (70 µm): 5 A → ≈3 mm; 8 A → ≈6 mm.

Place MOSFETs close to each other and route the switching node with short, wide traces. Keep the loop area between MOSFETs and decoupling caps minimal.

9.3 Placement guidelines

- Place MOSFETs together along one edge; speaker connector close to LC filter.
- Bulk capacitors near Vbus input and MOSFET drains.

- Triangle oscillator and comparator placed away from noisy switching node; give them a quiet analog ground near the op-amp ground return.
- Use split ground plane: small analog ground region for input and comparator, large power ground region for MOSFETs. Tie them at a single star point near power return/bulk capacitors.
- Place decoupling ceramics as close as possible to MOSFET Vbus pins and gate driver supply pins.

9.4 Thermal & mechanical

- Provide thermal pads and mounting holes for heatsink. Use copper pours under MOSFET pads and multiple vias to spread heat to bottom layer.

9.5 EMI considerations

- Keep PWM traces short. Add small RC snubber between MOSFET drain and source if ringing present.
- Route speaker traces away from the switching node; shield sensitive analog inputs.

10. Simulation setup (LTspice) & netlist

A simulation allows validating PWM generation, dead-time, switching behaviour and LC recovery. Below is a minimal LTspice netlist-style description and guidance to set up.

10.1 Recommended simulator

- **LTspice** (free) — preferred for power electronics and switching simulations.
- Alternatives: Ngspice, PSpice, Multisim.

10.2 Simulation approach

- Simulate the triangle oscillator and PWM comparator at 300 kHz.
- Model gate driver (or ideal gate drive pulses) to switch MOSFETs with realistic gate charge (model MOSFETs with manufacturer SPICE models if available).
- Include parasitic R and L for traces and MOSFETs for more realistic switching.

10.3 Example LTspice netlist (conceptual)

```
* Class-D single channel conceptual netlist
Vin IN 0 AC 1 SIN(0 0.5 1k) ; audio source 1 kHz test
Vbus Vbus 0 DC 24
* Triangle generator: op-amp derived (approx as Vtriangle source for PWM test)
Vtri TRI 0 PULSE(-2 2 0 1u 1u 1.6667u 3.333u) ; approx 300 kHz triangle-ish
(replace with real op-amp subcircuit)
* PWM comparator: behavioral source
Ecomp PWM 0 VALUE={V(IN) > V(TRI)} ; simple comparator
* Gate drive (idealized)
Vgh GH 0 PULSE(0 12 0 10n 10n 50n 3.333u) ; high-side gate
Vgl GL 0 PULSE(12 0 0 10n 10n 50n 3.333u) ; low-side gate (complementary)
* MOSFET half bridge (use generic MOSFET models)
MHS SW Vgh Vbus 0 NMOS ; high side
```

```
MLS 0 Vgl SW 0 NMOS ; low side
.model NMOS NMOS (VTO=4V BETA=50 RS=0.01 CGS=1e-9)
* Output LC
L1 SW Lout 33uH
Cout Lout 0 1u
RLload 0 Lout 4

.tran 0 2m 0 1u
.backanno
.end
```

Important: the above is *conceptual* to show how to wire sources; for realistic switching behavior replace ideal pulses with gate-driver models and MOSFET SPICE models. Use `.measure` statements in LTspice to compute THD, output RMS, and switching losses.

10.4 Simulation checklist

- Verify triangle is stable at chosen amplitude and frequency.
- Confirm comparator produces PWM and that complementary gate signals include dead-time.
- Observe MOSFET drain node (SW) for switching spikes; add snubbers if needed.
- Run FFT of the filtered output node to check audio content and residual carrier.

11. Testing, measurements & expected results

- Test first with an 8 Ω dummy load and low supply voltage (e.g., 12 V) before powering speakers.
- Use scope to probe:
- Triangle and audio signals at comparator inputs.
- Gate voltages to ensure dead-time.
- Switching node (SW) to verify clean transitions and acceptable dv/dt.
- After LC filter, measure audio waveform and spectrum.
- Expected behavior: PWM at 300 kHz on SW node; clean audio at speaker terminal after filter with carrier largely removed.

12. Safety, thermal, and EMC notes

- Always discharge bulk capacitors before touching the board.
- Use fuses on Vbus input and slow-start if possible to prevent inrush damage.
- MOSFETs can get hot — use appropriate heatsinks and thermal pads.
- Class-D switching makes EMI — consider EMI filtering on supply and careful layout.

13. Files included / next steps

This README provides a full conceptual design and simulation guidance. Recommended next steps: 1. Build a breadboard prototype of the oscillator + comparator and validate PWM (low power). 2. Bring up gate driver and single MOSFET switching node (no load) and verify switching and dead-time. 3. Add LC filter and dummy load; tune filter and damping. 4. Design PCB (Gerber) following layout rules here; order PCB and assemble. 5. Iterate and measure thermal performance and THD.

If you'd like, I can also provide: - A full LTspice schematic and ".asc" file for simulation. - Gerber-ready PCB layout in KiCad (schematic and PCB files) sized for two channels. - A parts BOM with alternate part numbers and source suggestions.

Quick references & formulae

- LC cutoff: fc = 1/(2π√(L·C))
- Power into R: P = V^2 / R (for DC RMS equivalents)
- Peak current estimate for P_out into R: I_peak ≈ √(2·P_out / R)
- Trace width: consult IPC-2152 or online calculators; for rough sizing use the guide in Section 9.2.

End of README