A Project Stage – II

on

**CHARACTERISTIC ANALYSIS OF UTB AND NW MODELS OF TUNNEL FIELD EFFECT TRANSISTOR(TFET) FOR LOW POWER APPLICATIONS**

*Submitted in partial fulfillment of the requirements for the award of the degree of*

**BACHELOR OF TECHNOLOGY**

**in**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

by

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**Professor**



**Department of Electronics and Communication Engineering**

**BVRIT HYDERABAD College of Engineering for Women**

**(Approved by AICTE, New Delhi and Affiliated to JNTUH, Hyderabad)**

**Accredited by NBA and NAAC with A Grade**

**Bachupally, Hyderabad – 500090**

**2023-24**

**DECLARATION**

We hereby declare that the work described in this report, entitled **“CHARACTERISTIC ANALYSIS OF UTB AND NW MODELS OF TUNNEL FIELD EFFECT TRANSISTOR(TFET) FOR LOW POWER APPLICATIONS”** which is being submitted by us in partial fulfillment for the award of the degree of **Bachelor of Technology** in the department of **Electronics and Communication Engineering** at **BVRIT HYDERABAD College of Engineering for Women,** affiliated to **Jawaharlal Nehru Technological University Hyderabad**, Kukatpally, Hyderabad – 500085 is the result of original work carried out by us under the guidance of **Dr. M. Parvathi, Prof, Dept of ECE.**

This work has not been submitted for any Degree/Diploma of this or any other institute/university to the best of our knowledge and belief.

**Place:** Hyderabad

**Date:** 03-05-2024

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**Certificate**

This is to certify that the major/mini project report, entitled **“CHARACTERISTIC ANALYSIS OF UTB AND NW MODELS OF TUNNEL FIELD EFFECT TRANSISTOR(TFET) FOR LOW POWER APPLICATIONS”** is a record of bonafide work carried out by **T Praveenya (20WH1A0477), B Akshaya (20WH1A0479), V Leena (20WH1A0489), K Sneha Bhuvaneshwari (20WH1A04B5)** in partial fulfillment for the award of the degree of **Bachelor of Technology** in the department of **Electronics and Communication Engineering** at **BVRIT HYDERABAD College of Engineering for Women,** affiliated to **Jawaharlal Nehru Technological University Hyderabad**, Kukatpally, Hyderabad – 500085.

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**ABSTRACT**

Tunnel field-effect transistor (TFET), though structurally akin to MOSFETs, offer a distinct switching mechanism based on quantum tunneling, making them promising for low power electronics. Traditional MOSFETs are constrained by thermionic emission, unlike TFETs, which circumvent this limitation. TFETs boast advantages such as minimal subthreshold swing, low leakage current, and a reduced threshold voltage. However, existing TFET models lack comprehensive parameter ranges for ON-state current, subthreshold swing, and power efficiency. Addressing these limitations is crucial for optimizing TFET performance, particularly in conventional and non-isolated heterojunction TFET designs, to meet the demands of efficient low-power applications.

The existing solutions are represented by conventional transistors and TFETs without an isolated heterojunction. These solutions, while functional, demonstrate limitations in achieving optimal ON-state current and subthreshold swing (SS) necessary for efficient low-power applications. These existing TFET designs fall short in meeting the desired performance criteria, prompting the need for innovative approaches to improve their electrical characteristics.

The proposed study involves the design and simulation of Heterojunction Tunnel Field-Effect Transistors (TFETs), incorporating a SiO2 isolation layer between the source and drain regions. Two TFET architectures, namely Ultra-Thin Body (UTB) and Nanowire (NW), are examined to harness their unique advantages crucial for achieving enhanced TFET performance. The study aims to identify typical operating values by analyzing the characteristics of Tunnel Field Effect Transistors through graphs depicting Ids vs. Vgs and assessing the resulting model suitability for low-power applications. Additionally, the research extends to the design and development of a TFET-based inverter using observed operating values, facilitated by the Silvaco tool.

The anticipated outcomes of the study and analysis encompass the identification of key parameters for optimized performance, tailored for low-power applications. This includes pinpointing the optimal range of threshold voltage, determining the minimum and maximum operable currents, analyzing the impact of doping variations, evaluating the influence of channel length, and assessing how the thickness of oxide and channel contribute to the overall device performance. Through these investigations, the study aims to provide comprehensive insights into the critical factors shaping the behavior and efficiency of the device.

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1. **OPTIMIZED ANALYSIS OF TUNNEL FIELD**

**EFFECT TRANSISTOR**

**1.1 Introduction**

In the realm of semiconductor technology, Complementary Metal-Oxide-Semiconductor (CMOS) has long been the cornerstone for integrated circuit design due to its efficiency and versatility. However, as the pursuit of energy-efficient electronics intensifies, researchers have turned their attention to emerging alternatives. One such candidate that has garnered significant interest is the Tunnel Field-Effect Transistor (TFET). Unlike conventional CMOS technology, TFET operates on a fundamentally distinct principle, leveraging quantum tunneling for charge carriers, which offers the potential for lower power consumption and enhanced performance.

**1.2 Existing Designs and Limitations**

Design and Analysis of Tunnel FET for Low Power High Performance Applications was published in year 2018 by Umesh Dutta, M. K. Soni, Manisha Pattanaik. The invention discusses the design and analysis of TFETS for low-power, high-performance applications. There were limited discussions were performed of advanced materials and temperature effects.

Design of Heterojunction Tunnel 2021 Field-Effect Transistors with SiO2 Isolation between Source and Drain for Low Power Application was published in year 2021 by S. Chander. The invention introduces SiO2-isolated TFET design with enhanced ON-state current and subthreshold swing (SS). There were limited discussions were performed on temperature effects and practical implementation details.

Impact of Temperature on the Performance of Tunnel Field Effect Transistor was published in year 2021 by Akshit Walia, Priya Kaushal, Gargi Khana. The invention examines the impact of temperature on TFET performance. The limitation is that this focuses on temperature effects without extensive details on other performance metrics.

Quantization, Gate Dielectric, and Channel Length Effect in Double-Gate Tunnel Field-Effect Transistor was published in year 2022 by Kalyan Mondol, Mehedi Hasan, Abdul Hasib Siddique, Sharnali Islam. The invention is that this investigates DG TFETS for improved performance with lower SS. There were limited discussions on temperature effects and practical implementation challenges.

**1.3 Motivation and Objective**

Within the dynamic landscape of semiconductor technology, a paramount emphasis is placed on pioneering advancements that underscore energy efficiency in electronic components. This research initiative embarks on a comprehensive exploration of Tunnel Field-Effect Transistors (TFETs), a transformative class of transistors poised to usher in a new era for low-power applications. The primary thrust of this investigation revolves around elucidating the intrinsic capabilities of TFETs, specifically delving into the nuances of Ultra-Thin Body (UTB) and Nanowire (NW) design methodologies. Augmenting this exploration is the strategic integration of a Silicon Dioxide (SiO2) isolation layer, strategically positioned between the source and drain regions. This research aligns seamlessly with the imperatives of sustainable computing, responding to the escalating demand for cutting-edge, energy-efficient electronic devices.

At the heart of this exploration lies a meticulous comparison between established TFET designs and the proposed UTB and NW TFET architectures. The SiO2 isolation layer introduces an additional dimension to the analysis, with a keen focus on critical performance parameters. ON-state current, subthreshold swing (SS), and overall power consumption emerge as pivotal metrics guiding the assessment process. Graphical representations, ranging from Ids v/s Vgs diagrams, offer a visual narrative of TFET characteristics. This methodical evaluation aims to distill the nuances of TFET behavior, pinpointing configurations that promise optimal efficiency for low-power applications.

The current literature on Tunnel Field-Effect Transistors (TFETs) is marked by restricted parameter ranges, particularly in ON-state current, subthreshold swing (SS), and minimized power consumption—vital factors for efficient low-power applications. Overcoming this challenge involves identifying and implementing optimized TFET performance, necessitating a departure from existing design limitations inherent in both conventional and non-isolated heterojunction TFETs. Navigating beyond established frameworks is imperative, requiring the exploration of innovative solutions that transcend constraints, thus unlocking the full potential of TFETs for heightened efficiency in low-power electronic applications.

The primary objective of this study is to conduct a comparative analysis between established TFET designs and the novel architectures of UTB and NW TFETs, each integrated with an isolation layer. The assessment revolves around key performance metrics, including the ON-state current, subthreshold swing (SS), and overall power consumption, with a keen focus on achieving optimal efficiency for low-power applications. And to design and develop TFET based application using observed operating values using Silvaco tool.

**1.4 Report Organization**

Chapter 1 provides an overview of Introduction, Existing designs and limitations, Motivation and objective.

1. **REVIEW ON TUNNEL FIELD EFFECT TRANSISTOR**

**2.1 NCTFET Device for Low Power VLSI Application [1]**

In 2023 paper "NCTFET Device for Low Power VLSI Application", the authors explored a new transistor design Negative Capacitance Tunnel Field-Effect Transistor (NCTFET) for low-power chips. Simulations show promising results with improved on-current, reduced leakage, and sharper switching characteristics. This is achieved through a special gate design with a negative capacitance material. The study emphasizes the importance of transistor design and material properties for future energy-efficient electronics [1].

**2.2 Design of Heterojunction Tunnel Field-Effect Transistors with SiO2 Isolation between Source and Drain for Low Power Application [2]**

In 2021 paper "Design of Heterojunction Tunnel Field-Effect Transistors with SiO2 Isolation between Source and Drain for Low Power Application", the authors propose a new design for a heterojunction tunnel field-effect transistor (TFET) that utilizes an SiO2 isolation layer between the source and drain regions to enhance its low-power performance. The proposed TFET design exhibits a significantly lower subthreshold swing (SS) and higher ON-current (Ion) compared to conventional TFETs, making it a promising candidate for low-power applications. However, the study acknowledges the need for further experimental validation and optimization of the SiO2 isolation layer thickness to achieve optimal device performance [2].

**2.3 Quantization, Gate Dielectric, and Channel Length Effect in Double-Gate Tunnel Field-Effect Transistor [3]**

In 2023 paper "Quantization, Gate Dielectric, and Channel Length Effect in Double-Gate Tunnel Field-Effect Transistor", the authors investigate the impact of quantization effects, gate dielectric material, and channel length on the performance of double-gate (DG) tunnel field-effect transistors (TFETs). They find that DG TFETs with a short channel length, high dielectric constant gate material, and material with an effective mass equal to or greater than 0.04 free electron mass exhibit promising performance. However, the study acknowledges that further research is needed to optimize DG TFET designs for practical applications and to address challenges such as interface traps and gate leakage current [3].

**2.4 Impact of Temperature on the Performance of Tunnel Field Effect Transistor [4]**

In 2021 paper “Impact of Temperature on the Performance of Tunnel Field Effect Transistor”, the authors studied how temperature affects tunnel field-effect transistors (TFETs). They looked at how TFETs perform under different temperatures using experiments and modeling. The research focused on key measures like current flow and switching efficiency (subthreshold swing) at various temperatures. While the study offers valuable insights, it mainly examined one aspect of TFET performance in detail. Further research is needed to understand how temperature affects other TFET characteristics [4].

**2.5 Design and Analysis of Tunnel FET for Low Power High Performance Applications [5]**

In 2018 paper "Design and Analysis of Tunnel FET for Low Power High Performance Applications", the authors propose a new design for a tunnel field-effect transistor (TFET) that is specifically optimized for low-power and high-performance applications. However, the study has some limitations, including the lack of experimental validation, the limited scope of the analysis, and the lack of consideration of the impact of process variations on device performance [5].

**2.6 Fundamentals of Tunnel Field-Effect Transistors [6]**

In 2016 a book named "Fundamentals of Tunnel Field-Effect Transistors", the authors filled a critical gap by providing a comprehensive introduction to Tunnel Field-Effect Transistors (TFETs). TFETs are a growing area of research due to their potential benefits. The book explains the basics of TFETs, including their unique characteristics, advantages, limitations, and recent improvement techniques. It explores various approaches to optimize TFET performance, emphasizing the importance of design trade-offs. The book also includes simulation examples to help readers explore TFET behavior using industry-standard tools, making TFET research and development more accessible [6].

**2.7 Low-power circuit analysis and design based on heterojunction tunneling transistors (HETTs) [7]**

In 2013 paper "Low-power circuit analysis and design based on heterojunction tunneling transistors (HETTs)", the authors explored using heterojunction tunneling transistors (HETTs) as a lower-power alternative to traditional transistors (MOSFETs) in circuit design. HETTs offer a sharper switching ability (lower subthreshold swing). The study developed a computer model to simulate HETT circuits and showed significant reductions in power consumption compared to MOSFET circuits. They compared HETT and MOSFET performance and proposed a new HETT-based memory design (SRAM cell) with substantially lower leakage power. Overall, the research suggests HETTs as a promising candidate for low-power electronic circuits [7].

**2.8 Universal TFET Model. (Version 1.6.8). nano HUB [9]**

In 2015 paper "Universal TFET Model. (Version 1.6.8). nano HUB " the authors introduced a computer model to simulate the behavior of tunnel field-effect transistors (TFETs) for low-power circuit design. This model considers various TFET aspects like switching efficiency and current behavior across different voltage conditions. It can be used in popular circuit simulation tools, allowing designers to predict TFET performance more accurately. This approach can improve the design process for TFET-based circuits [8].

**2.9 The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor [9]**

In 2022 paper "The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor", the authors proposed a new design for an n-MOSFET transistor that utilizes a tunnel source to achieve superior performance characteristics. The PNPN n-MOSFET design exhibits a steep subthreshold swing, improved Ion current, and reduced susceptibility to short-channel effects compared to conventional MOSFETs. However, the study acknowledges the need for further investigation into potential fabrication challenges and parasitic effects associated with the PNPN structure [9].

**2.10 Switching Characteristic Analysis of Tunnel Field-Effect Transistor (TFET) Inverters [10]**

In 2017 paper “Switching Characteristic Analysis of Tunnel Field-Effect Transistor (TFET) Inverters”, the authors studies and examines how tunnel field-effect transistors (TFETs) perform in inverter circuits compared to traditional transistors (MOSFETs). It considers limitations like a lower flow of tunneling current and a larger capacitance within TFETs. The research explores TFET inverters with similar current levels and capacitance as MOSFET inverters using simulations. Interestingly, the study found that slow switching behavior in TFET inverters wasn't solely due to the limitations mentioned. Instead, other factors like internal current flow patterns seem to play a bigger role. This research helps improve designs for TFET-based circuits by providing insights into the unique characteristics of TFET inverters [10].

**2.11 TFET Inverters with n-/p-Devices on the Same Technology Platform for Low-Voltage/Low-Power Applications [11]**

In 2014 paper "TFET Inverters with n-/p-Devices on the Same Technology Platform for Low-Voltage/Low-Power Applications", the authors explore inverter circuits built with special transistors called n-type and p-type TFETs fabricated together on a single chip. Simulations show these TFET inverters outperform traditional CMOS inverters in terms of power efficiency. The TFET design offers steeper switching and higher current flow, leading to potentially 10 times lower power consumption during operation and 100 times lower standby power usage. This makes TFET inverters a promising candidate for future low-power electronic devices [11].

**2.12 Limitations on Existing Design Models**

The investigated TFET research papers collectively unveil both promise and challenges in the pursuit of efficient electronic devices. The first paper (2023) proposes a NCTFET device but challenges in transistor design and material properties remain unresolved. The second paper (2021) proposes a TFET with SiO2 isolation, showing improved low-power performance but necessitating further validation. In the third paper (2023), promising DG TFET performance is observed, yet ongoing research is essential for practical optimization. The fourth paper (2021) primarily focuses on temperature's impact on TFET performance, leaving other TFET characteristics unexplored. The fifth paper (2018) proposes a new design for TFET that is specifically optimized for low-power and high-performance applications. The sixth paper (2016) focuses on providing a general introduction. The seventh paper (2013) proposes HETTs as a promising candidate for low-power electronic circuits, further research is needed to validate and optimize their implementation. The eighth paper (2015) focuses on model development. The ninth paper (2022) introduces a superior PNPN n-MOSFET design but acknowledges potential fabrication challenges. The tenth paper (2017) limitations like lower flow of tunneling current and a larger capacitance within TFETs is observed. The eleventh paper (2014) TFETs are fabricated together on a single chip. Simulations show these TFET inverters outperform traditional CMOS inverters in terms of power efficiency. These findings collectively underscore the dynamic nature of TFET research, emphasizing the potential benefits alongside the ongoing need for refinement and optimization to overcome challenges for practical implementation.

**3. PROPOSED ANALYSIS ON TUNNEL FIELD EFFECT TRANSISTOR**

The methodology employed in this study entails a meticulous exploration through the design and simulation phases, focusing on Heterojunction Tunnel Field-Effect Transistors (TFETs). A key innovation introduced is the incorporation of a Silicon Dioxide (SiO2) isolation layer strategically positioned between the source and drain regions, imparting an additional layer of sophistication to the TFET architecture. The investigation extends to encompass two distinct TFET design methods: Ultra-Thin Body (UTB) and Nanowire (NW), each offering unique attributes that hold significant promise for elevating TFET performance.

The UTB and NW design methods, chosen for their respective advantages, are integral components of the study. These architectures are anticipated to contribute distinct benefits crucial for achieving enhanced TFET functionality, particularly in the realm of low-power applications. The study unfolds through the comprehensive observation of TFET characteristics, facilitated by graphical representations such as Ids (drain current) versus Vgs (gate-source voltage), EC\_EV\_ON\_State (energy band diagram in the ON state), EC\_EV\_OFF\_State (energy band diagram in the OFF state), and Bandgaps. These graphs serve as visual aides, enabling a nuanced understanding of the TFET behaviors under different conditions.

In this study, we embark on an exploration of novel design approaches for Heterojunction Tunnel Field-Effect Transistors (TFETs), leveraging a strategic integration of a SiO2 isolation layer between the source and drain regions. The investigation encompasses two distinct TFET architectures: Ultra-Thin Body (UTB) and Nanowire (NW), each offering unique advantages crucial for elevating TFET performance. Our focus extends to identifying typical operating values through a detailed analysis of Tunnel Field Effect Transistor characteristics. This involves scrutinizing graphs depicting Ids vs. Vgs, EC\_EV\_ON\_State, EC\_EV\_OFF\_State, Bandgaps, with the ultimate goal of observing the resulting model's suitability for low-power applications.

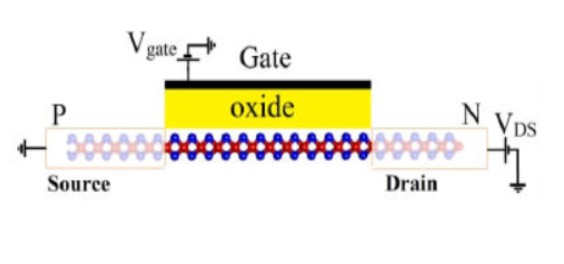
Additionally, the study delves into the practical application domain by employing these observed operating values in the design and development of a TFET-based application, facilitated by the Silvaco tool. This multifaceted exploration seeks to contribute to the advancement of TFET technology, aligning it with the demands of contemporary low-power electronic systems.

**3.1 TFET Models for Proposed Characteristic Analysis**

In the following TFET analysis we use two types of models namely Ultra-thin Body (UTB) and Nano Wire (NW)

**3.1.1 Ultra-Thin Body Tunnel Field Effect Transistor**

**Ultra-Thin Body Tunneling Field-Effect Transistors (UTB-TFETs) represent a novel approach to achieving ultra-low power electronics. Their structure, as depicted in Figure 3.1, incorporates a thin body (channel) positioned between the source and drain electrodes. A crucial element is the gate electrode located on top, responsible for controlling current flow by modulating the tunneling barrier separating the source and channel. This unique combination of a thin body and a gate-controlled tunneling barrier enables UTB-TFETs to achieve both tunneling and drift current mechanisms, resulting in steeper switching characteristics and significantly lower power consumption compared to conventional transistors.**

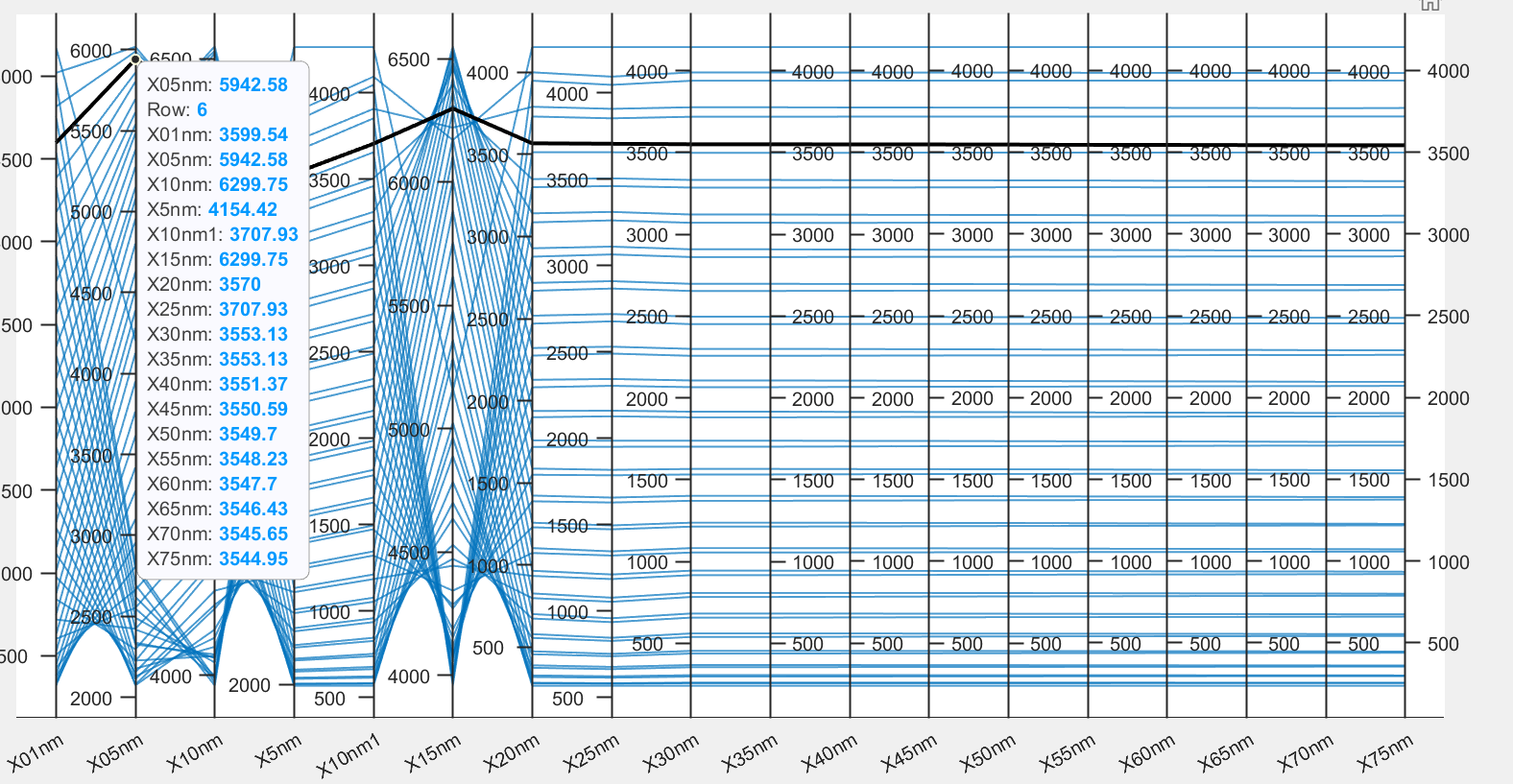
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**Fig 3.1** Ultra-Thin Body Tunnel Field Effect Transistor

**3.1.1.1 Parameters under Consideration for UTB TFET Analysis**

**a) Channel Length(nm)**

The channel length in a UTB (Ultra-Thin Body) TFET (Tunnel Field-Effect Transistor) refers to the distance between the source and drain terminals along the conducting channel. It plays a crucial role in determining the device's performance. A shorter channel length typically enhances the TFET's performance by reducing the resistance along the channel, improving the device's speed and reducing power consumption. Additionally, a shorter channel length can enhance the tunneling probability, leading to better subthreshold swing and thus lower off-state leakage current. However, overly short channel lengths can also introduce challenges such as increased leakage current and fabrication complexity.



**Fig 3.2** Observed typical values of Ids for Channel Length

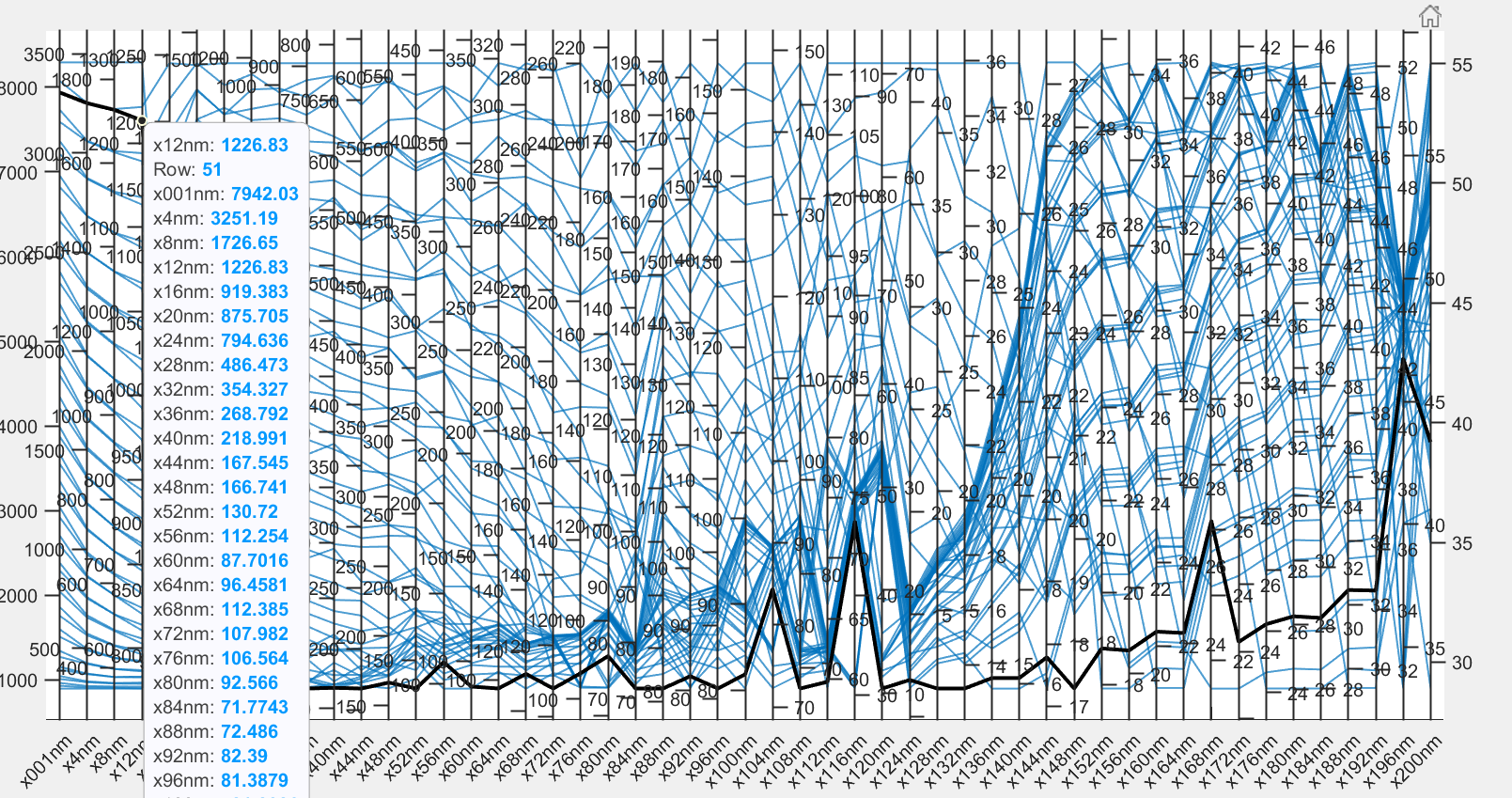
Our analysis encompassed of the channel length ranging from 0.1nm to 75nm, as depicted in Figure 3.2 Our examination focused on identifying the channel length associated with maximum current while simultaneously minimizing leakage current. Through this evaluation, we determined that a channel length of 40nm, 45nm, 50nm exhibits the most favorable characteristics, showcasing lower leakage current alongside minimal threshold voltage and subthreshold swing compared to the reference paper.

**Fig 3.3** Comparing the values of Ids for Channel lengths with base paper

Analysis of the data presented in Figure 3.3 reveals that a channel length of 40nm achieves a high current of 1622.27uA while exhibiting lower subthreshold and threshold frequencies. These parameters collectively indicate the effectiveness of the 40nm channel length in achieving superior performance.

**b) Thickness of the channel(nm):**

The channel thickness in a UTB (Ultra-Thin Body) TFET (Tunnel Field-Effect Transistor) refers to the thickness of the semiconductor material between the source and drain terminals, defining the channel through which current flows. This parameter plays a crucial role in the device's performance. A thinner channel thickness can enhance the tunneling probability, leading to improved subthreshold swing and lower off-state leakage current. It also reduces the resistance along the channel, contributing to faster operation and lower power consumption. However, excessively thin channel thicknesses can pose challenges such as increased leakage current and susceptibility to process variations.



**Fig 3.4** Observed typical values of Ids for channel thickness

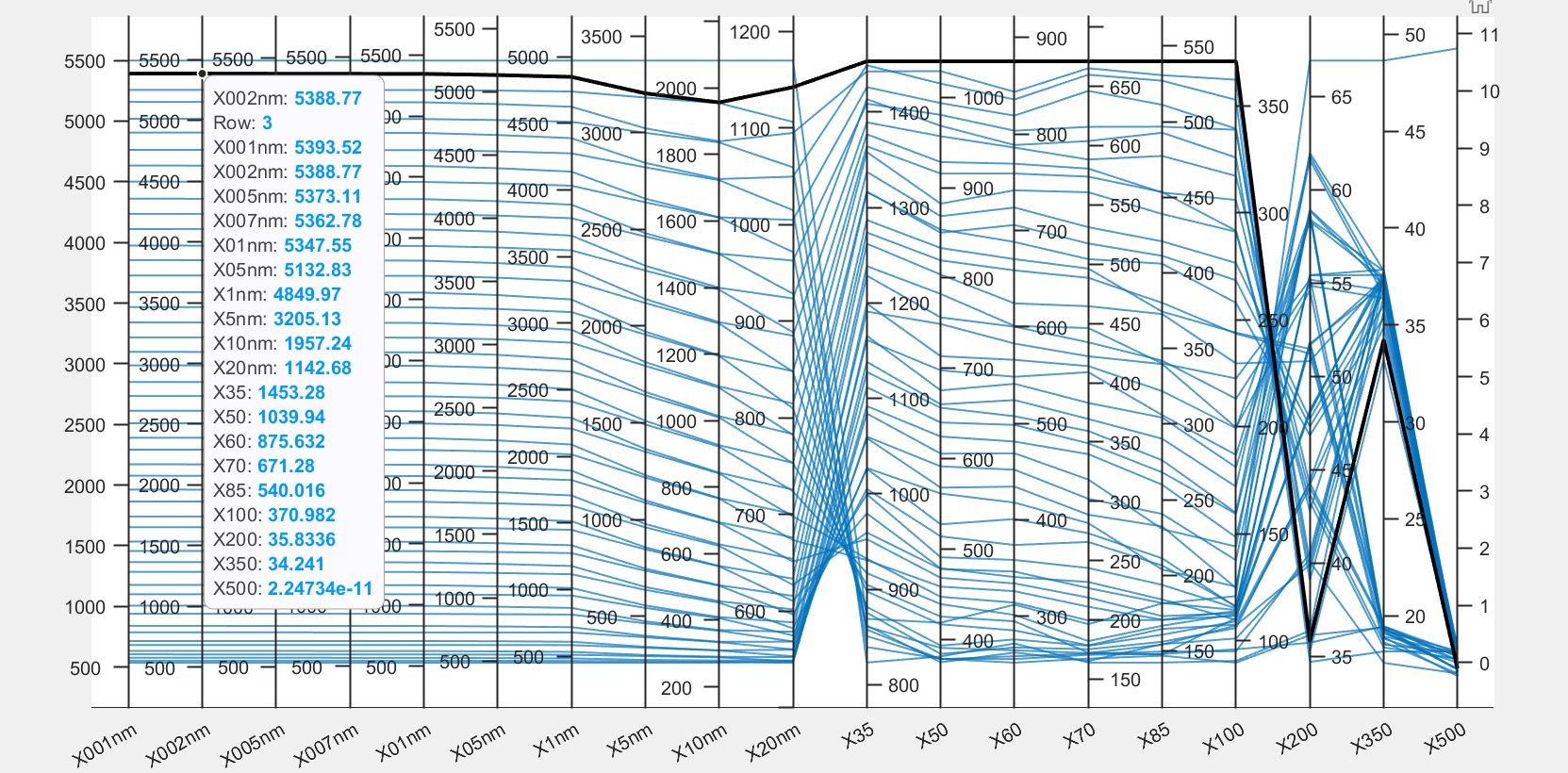
We performed an analysis of channel thickness, ranging from 0.01nm to 200nm, as shown in Figure 3.4 Our aim was to find the optimal thickness for maximizing current while minimizing leakage. From our evaluation, we found that channel thicknesses of 4nm, 8nm, and nm demonstrated the most promising outcomes. These configurations displayed reduced leakage current, as well as minimal threshold voltage and subthreshold swing compared to the reference paper, indicating their favorable performance characteristics.

**Fig 3.5** Comparing the values of Ids for Channel thicknesses with base paper

Analysis of Figure 3.5 reveals that a channel thickness of 4nm exhibits a high current of 1638.42uA, along with lower subthreshold and threshold frequency. These findings indicate the effective performance of the 4nm channel thickness in our study. Therefore, based on these parameters, we conclude that a channel thickness of 4nm is optimal for achieving enhanced performance in UTB-TFETs.

**c) Thickness of the oxide(nm)**

The thickness of the oxide layer in a UTB (Ultra-Thin Body) TFET (Tunnel Field-Effect Transistor) refers to the thickness of the insulating layer separating the channel from the gate electrode. This oxide layer serves as a crucial component in the device's operation. A thinner oxide layer can enhance tunneling probability, facilitating more efficient charge transfer between the channel and the gate. This, in turn, leads to improved subthreshold swing and reduced off-state leakage current. However, overly thin oxide layers may result in increased gate leakage current and susceptibility to gate oxide breakdown. On the other hand, thicker oxide layers offer better insulation and reduced gate leakage but can lead to higher threshold voltages and slower switching speeds.



**Fig 3.6** Observed typical values of Ids for Oxide Thickness

We performed an analysis of the oxide layer thickness, ranging from 0.01nm to 500nm, as shown in Figure 3.6 Our objective was to determine the optimal oxide thickness for maximizing current while minimizing leakage. From our evaluation, we found that oxide thicknesses of 3nm, 8nm, and 10nm exhibited the most favorable characteristics, demonstrating lower leakage current as well as minimal threshold voltage and subthreshold swing compared to the reference paper. These findings suggest that these oxide thicknesses are effective in enhancing the performance of UTB TFETs.

**Fig 3.7** Comparing the values of Ids for Oxide thicknesses with base paper

Analysis of Figure 3.7 indicates that a thickness of 3nm yields the highest current of 0.432mv, coupled with lower subthreshold and threshold frequency. Based on these parameters, we conclude that a 3nm oxide thickness demonstrates effective performance in our study. Therefore, for optimized performance in UTB TFETs, a thickness of 3nm for the oxide layer appears to be advantageous.

**d) Doping**

Doping in the context of semiconductor devices like UTB (Ultra-Thin Body) TFETs involves intentionally introducing impurities into the semiconductor material to modify its electrical properties. The addition of dopants alters the concentration of charge carriers, either increasing (n-type doping) or decreasing (p-type doping) their abundance. In UTB TFETs, doping plays a crucial role in defining the conductivity and operation of the device. Proper doping enables the creation of the source, drain, and channel regions with the desired electrical characteristics. For instance, n-type doping in the source and drain regions facilitates electron injection and extraction, while p-type doping in the channel helps control the tunneling process.

In evaluating the performance of UTB TFETs, we investigated three doping levels: 1e20, 2e20, and 5e20. On analysis of channel length, channel thickness and oxide thickness graphs it revealed that a source doping of 1e20 exhibited superior performance, while a drain doping of 5e20 demonstrated better device performance. These findings indicate the critical role of doping levels in optimizing UTB TFET performance. Therefore, based on this assessment and compared to the reference paper, we conclude that source doping of 1e20 and drain doping of 5e20 are conducive to achieving enhanced device performance.

**Fig 3.8** Comparing the values of Ids for Doping’s with base paper

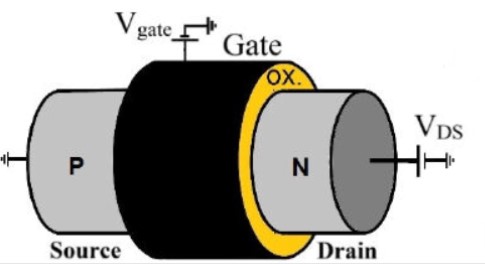
Through analysis of the parameters outlined above, we have identified optimal values Fig 3.8 that result in reduced subthreshold swing, maximal current, and improved threshold voltage. These findings point to enhanced overall device performance, underscoring the significance of parameter optimization in UTB TFET design.

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Channel length(nm) | 40 |
| Channel thickness(nm) | 5 |
| Oxide thickness(nm) | 2 |
| Source doping(cm^-3) | 1e20 |
| Drain doping (cm^-3) | 5e10 |
| Channel doping (cm^-3) | 1e15 |
| Work Function | 4.07 |

**Table 3.9** Device Parameters for UTB-TFET

**3.1.2** **Nanowire Tunnel Field Effect Transistor**

Nanowire Tunneling Field-Effect Transistors (NW-TFETs) represent a revolutionary approach to low-power electronics due to their unique structure, as illustrated in Figure 3.10. Unlike conventional transistors, NW-TFETs feature a nanowire, a very thin semiconductor wire acting as the channel, visible in the figure. This one-dimensional structure allows for superior gate control over the tunneling barrier between the source and drain (also labelled in the figure). The gate electrode, positioned on top of the nanowire, modulates this barrier, significantly impacting current flow. This design enables NW-TFETs to achieve steeper switching characteristics and lower operating voltages compared to conventional transistors

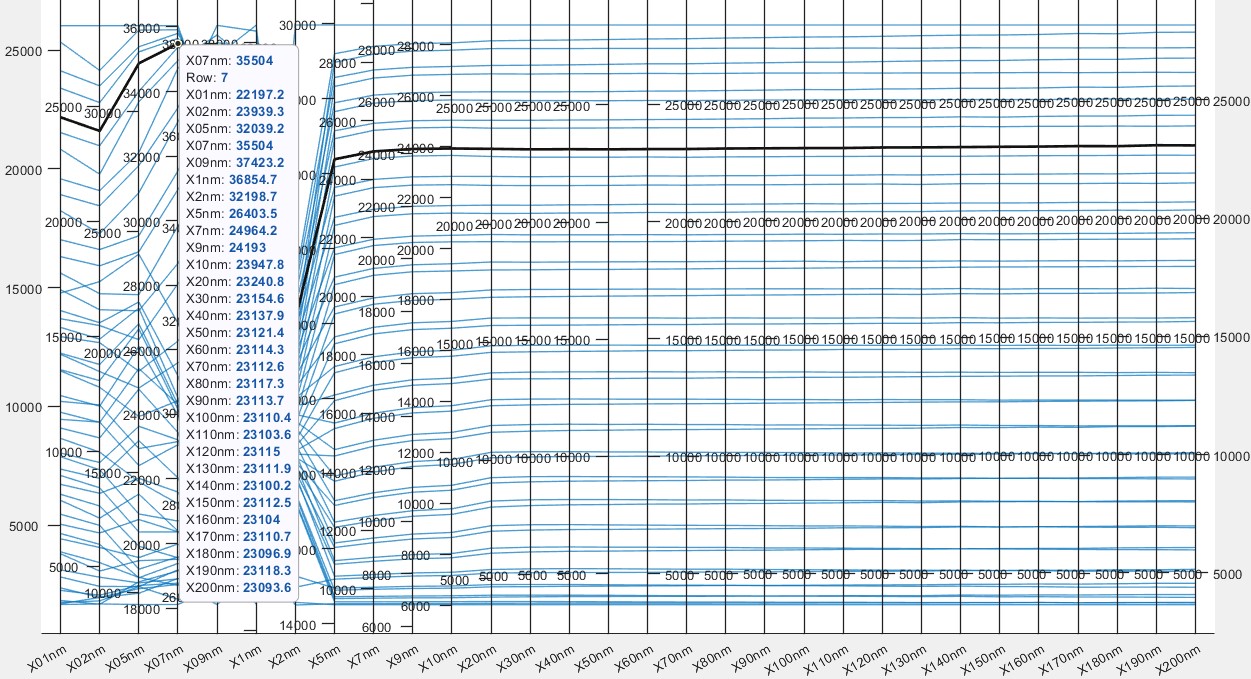
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**Fig 3.10** Nanowire Tunnel Field Effect Transistor

**3.1.2.1 Parameters under Consideration for NW TFET Analysis**

**a) Channel Length(nm)**

The channel length in a Nano wire TFET (NWFET) refers to the distance between the source and drain terminals along the conducting channel within the Nano wire structure. It plays a pivotal role in dictating the device's operational characteristics. A shorter channel length typically enhances the transistor's performance by reducing resistance along the channel, consequently improving speed and minimizing power consumption. Additionally, a shorter channel length can bolster tunneling probability, leading to better subthreshold swing and lower off-state leakage current. However, overly short channel lengths can introduce challenges like increased leakage current and heightened fabrication complexity.



**Fig 3.11** Observed typical values of Ids for Channel Length

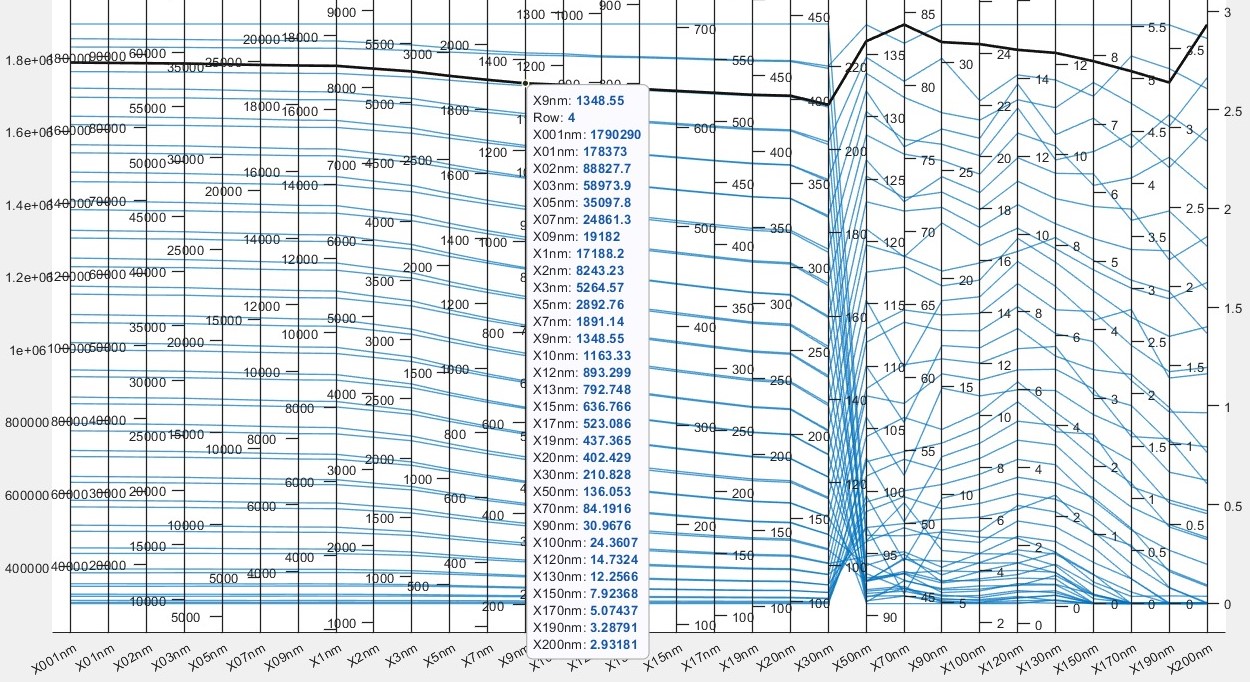
Our analysis encompassed of the channel length ranging from 0.1nm to 200nm, as depicted in Figure 3.11 Our examination focused on identifying the channel length associated with maximum current while simultaneously minimizing leakage current. Through this evaluation, we determined that a channel length of 100nm, 150nm, 180nm exhibits the most favorable characteristics, showcasing lower leakage current alongside minimal threshold voltage and subthreshold swing compared to the reference paper.

**Fig 3.12** Comparing the values of Ids for Channel lengths with base paper

Analysis of the data presented in Figure 3.12 reveals that a channel length of 180nm achieves a high current of \_\_1213.25\_uA while exhibiting lower subthreshold and threshold frequencies. These parameters collectively indicate the effectiveness of the 40nm channel length in achieving superior performance.

**b) Thickness of the channel(nm):**

The channel thickness in a NW (Nano Wire) TFET (Tunnel Field-Effect Transistor) refers to the thickness of the semiconductor material between the source and drain terminals, defining the channel through which current flows. This parameter plays a crucial role in the device's performance. A thinner channel thickness can enhance the tunneling probability, leading to improved subthreshold swing and lower off-state leakage current. It also reduces the resistance along the channel, contributing to faster operation and lower power consumption. However, excessively thin channel thicknesses can pose challenges such as increased leakage current and susceptibility to process variations.



**Fig 3.13** Observed typical values of Ids for Channel Thickness

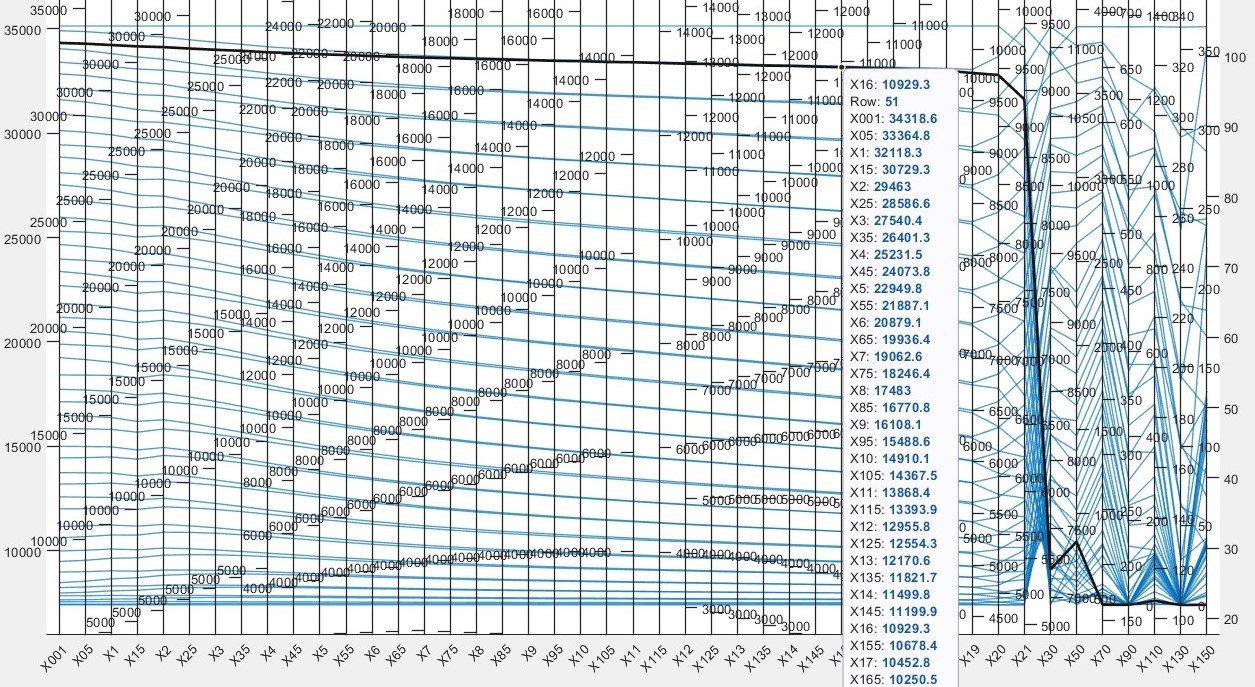
We performed an analysis of channel thickness, ranging from 0.01nm to 200nm, as shown in Figure 3.13 Our aim was to find the optimal thickness for maximizing current while minimizing leakage. From our evaluation, we found that channel thicknesses of 10nm, 15nm, and 20nm demonstrated the most promising outcomes. These configurations displayed reduced leakage current, as well as minimal threshold voltage and subthreshold swing compared to the reference paper, indicating their favorable performance characteristics.

**Fig 3.14** Comparing the values of Ids for Channel thicknesses with base paper

Analysis of Figure 3.14 reveals that a channel thickness of 10nm exhibits a high current of \_1213.25\_\_uA, along with lower subthreshold and threshold frequency. These findings indicate the effective performance of the 10nm channel thickness in our study. Therefore, based on these parameters, we conclude that a channel thickness of 20nm is optimal for achieving enhanced performance in NW-TFETs.

**c)Thickness of the oxide(nm)**

The thickness of the oxide layer in a NW (Nano Wire) TFET (Tunnel Field-Effect Transistor) refers to the thickness of the insulating layer separating the channel from the gate electrode. This oxide layer serves as a crucial component in the device's operation. A thinner oxide layer can enhance tunneling probability, facilitating more efficient charge transfer between the channel and the gate. This, in turn, leads to improved subthreshold swing and reduced off-state leakage current. However, overly thin oxide layers may result in increased gate leakage current and susceptibility to gate oxide breakdown. On the other hand, thicker oxide layers offer better insulation and reduced gate leakage but can lead to higher threshold voltages and slower switching speeds.



**Fig 3.15** Observed typical values of Ids for Oxide Thickness

We performed an analysis of the oxide layer thickness, ranging from 0.01nm to 150nm, as shown in Figure 3.15 Our objective was to determine the optimal oxide thickness for maximizing current while minimizing leakage. From our evaluation, we found that oxide thicknesses of 2nm, 4nm and 8nm exhibited the most favorable characteristics, demonstrating lower leakage current as well as minimal threshold voltage and subthreshold swing compared to the reference paper. These findings suggest that these oxide thicknesses are effective in enhancing the performance of NW TFETs.

**Fig 3.16** Comparing the values of Ids for Oxide Thicknesses with base paper

Analysis of Figure 3.16 indicates that a thickness of 8nm yields the highest current of \_1213.25\_uA, coupled with lower subthreshold and threshold frequency. Based on these parameters, we conclude that a 2nm oxide thickness demonstrates effective performance in our study. Therefore, for optimized performance in NW TFETs, a thickness of 2nm for the oxide layer appears to be advantageous.

**d)Doping**

Doping in the context of semiconductor devices like NW (Nano Wire) TFETs involves intentionally introducing impurities into the semiconductor material to modify its electrical properties. The addition of dopants alters the concentration of charge carriers, either increasing (n-type doping) or decreasing (p-type doping) their abundance. In NW TFETs, doping plays a crucial role in defining the conductivity and operation of the device. Proper doping enables the creation of the source, drain, and channel regions with the desired electrical characteristics. For instance, n-type doping in the source and drain regions facilitates electron injection and extraction, while p-type doping in the channel helps control the tunneling process.

In evaluating the performance of NW TFETs, we investigated three doping levels: 1e20, 2e20, and 5e20. On analysis of channel length, channel thickness and oxide thickness graphs it revealed that a source doping of 1e20 exhibited superior performance, while a drain doping of 5e20 demonstrated better device performance. These findings indicate the critical role of doping levels in optimizing NW TFET performance. Therefore, based on this assessment compared to the reference paper, we conclude that source doping of 1e20 and drain doping of 5e20 are conducive to achieving enhanced device performance.

**Fig 3.17** Comparing the values of Ids for Doping’s with Base paper

Through analysis of the parameters outlined above, we have identified optimal values Fig 3.17 that result in reduced subthreshold swing, maximal current, and improved threshold voltage. These findings point to enhanced overall device performance, underscoring the significance of parameter optimization in NW TFET design.

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Channel length(nm) | 100 |
| Channel thickness(nm) | 10 |
| Oxide thickness(nm) | 2 |
| Source doping(cm^-3) | 1e20 |
| Drain doping (cm^-3) | 2e10 |
| Channel doping (cm^-3) | 1e16 |
| Work function | 4.8 |

**Table 3.18** Device Parameters for NW-TFET

**3.2 Software requirements**

1. nano HUB simulation tool

2. Excel

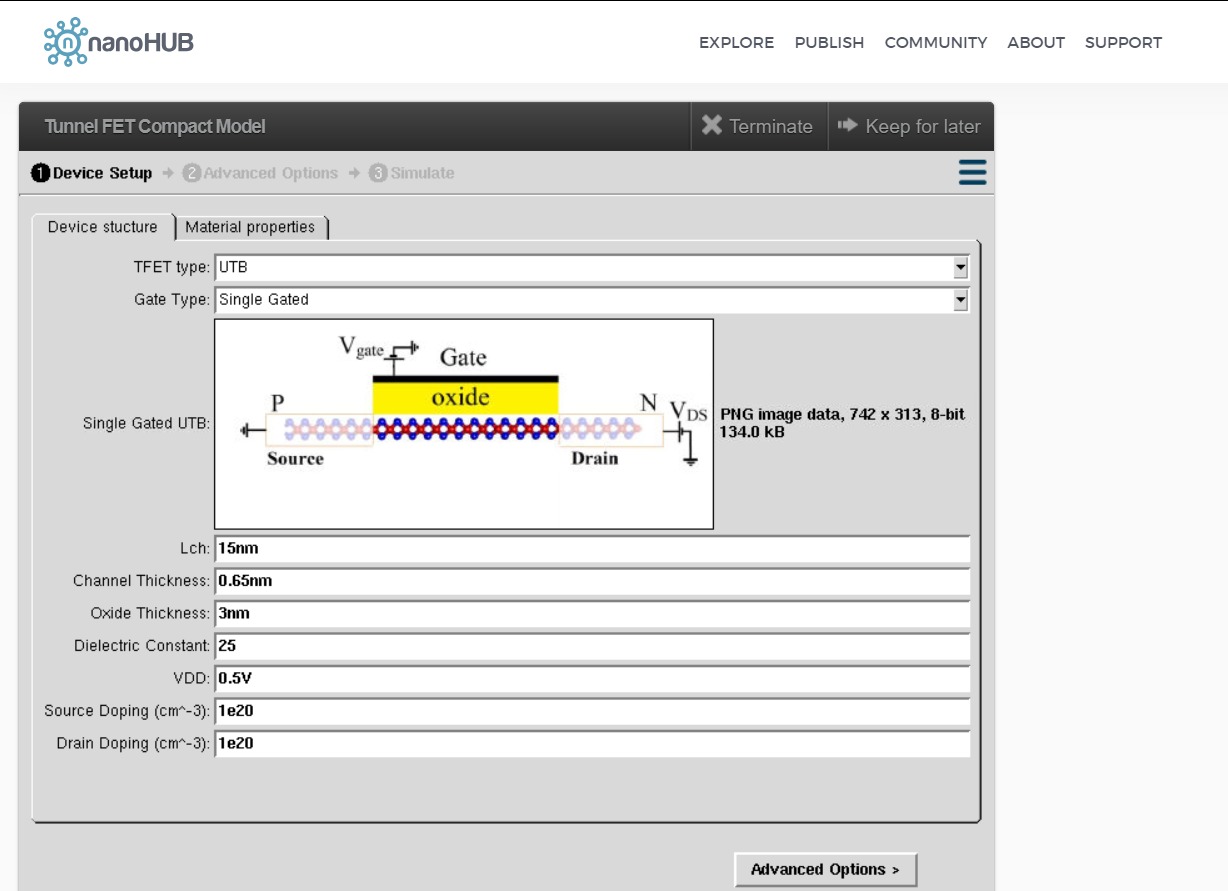
3. MATLAB Simulation Tool

4. Silvaco Tool

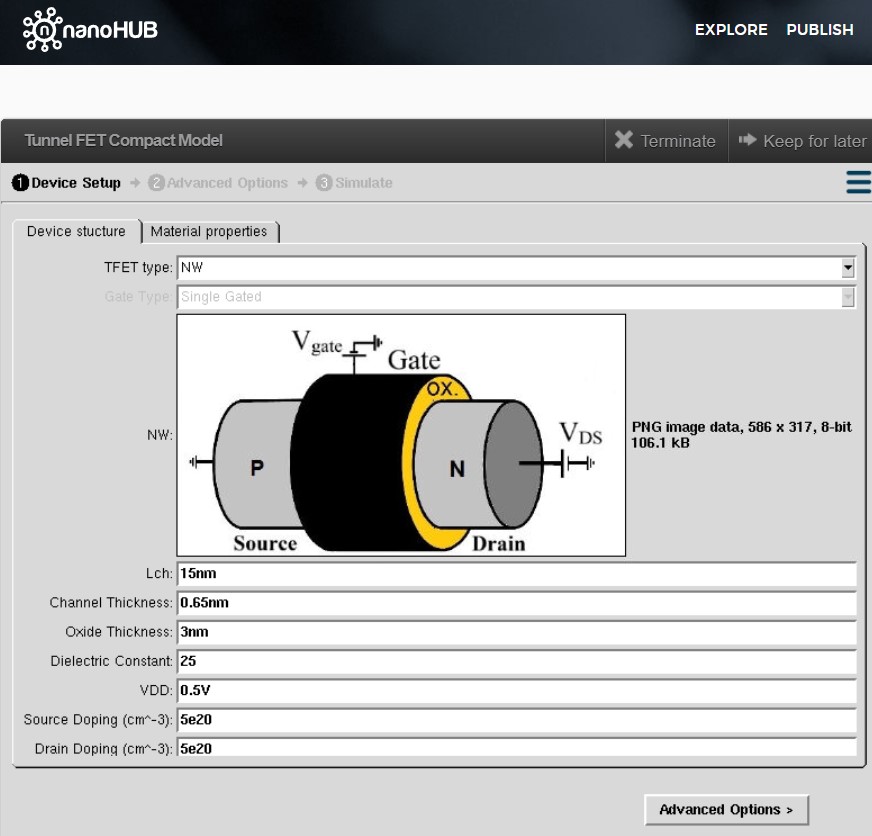
**3.2.1 nano HUB simulation tool**

nanoHUB is a comprehensive online resource for nanotechnology research, education, and collaboration. It provides a wide range of simulation tools, education resources, and a community forum for nanotechnology researchers. nanoHUB is an open-source platform.

nanoHUB provides a wide range of simulation tools for nanotechnology research as shown in Fig 3.19 and Fig 3.20. These tools can be used to model and simulate a variety of nanostructures and devices, including semiconductors, metals, and polymers. The tools are easy to use and can be run online in a web browser.



**Fig 3.19** nano HUB simulation tool for UTB model

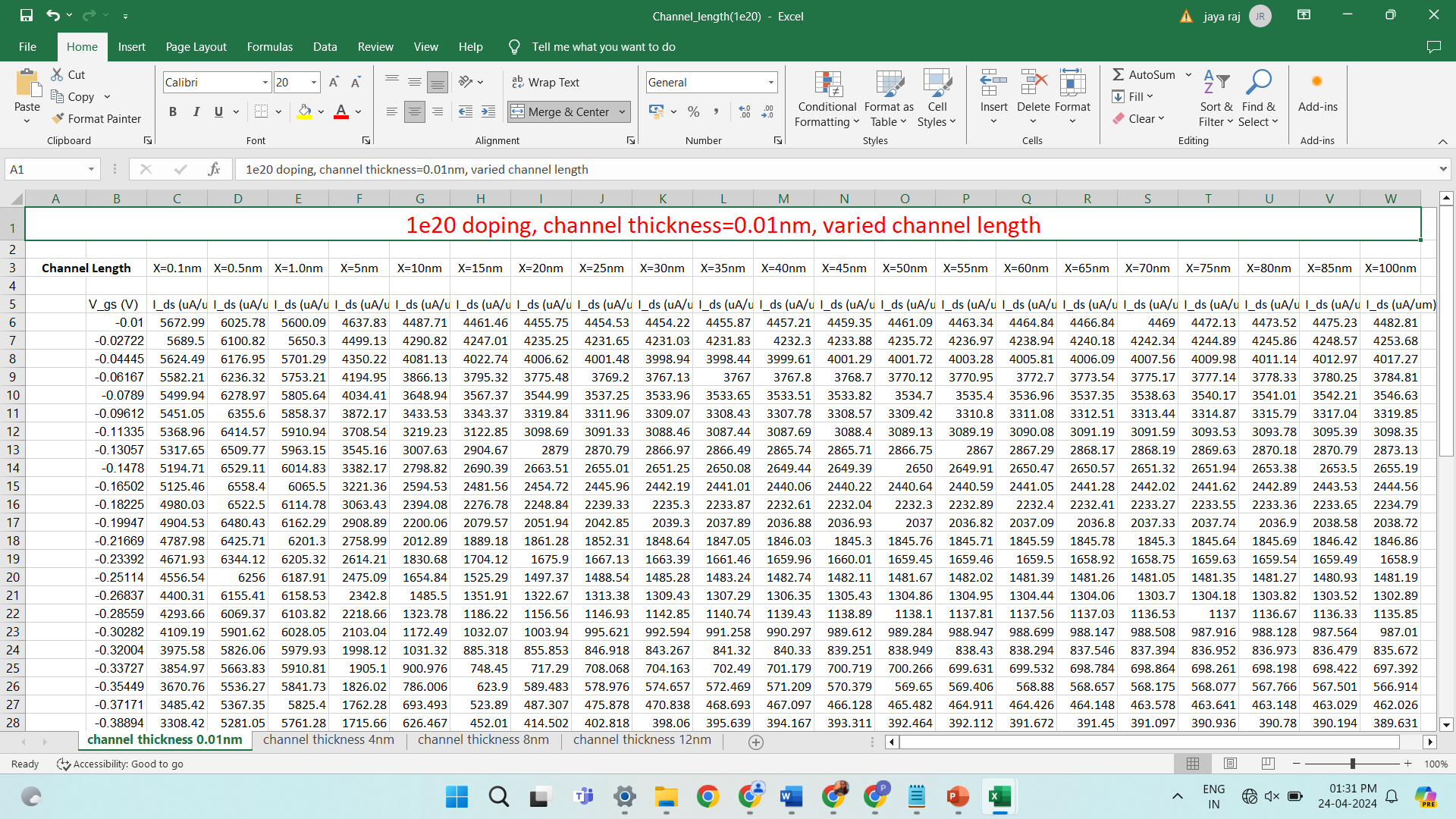


**Fig 3.20** nano HUB simulation tool for NW model

**3.2.2 Characteristic Analysis of Ids vs Vgs**

Microsoft Excel is a spreadsheet program developed by Microsoft that is part of the Microsoft Office suite of productivity software. It is a powerful and widely used tool for creating, organizing, and analyzing data in a tabular format. Excel is particularly popular for its grid of cells arranged in rows and columns, where users can input, manipulate, and perform calculations on data.

Its user-friendly interface, coupled with features like charts and graphs, enhances data visualization, aiding users in interpreting and presenting information effectively. Excel's versatility extends beyond basic data management, as it supports advanced data analysis, pivot tables, and macros, catering to the diverse needs of businesses, researchers, and educators alike.



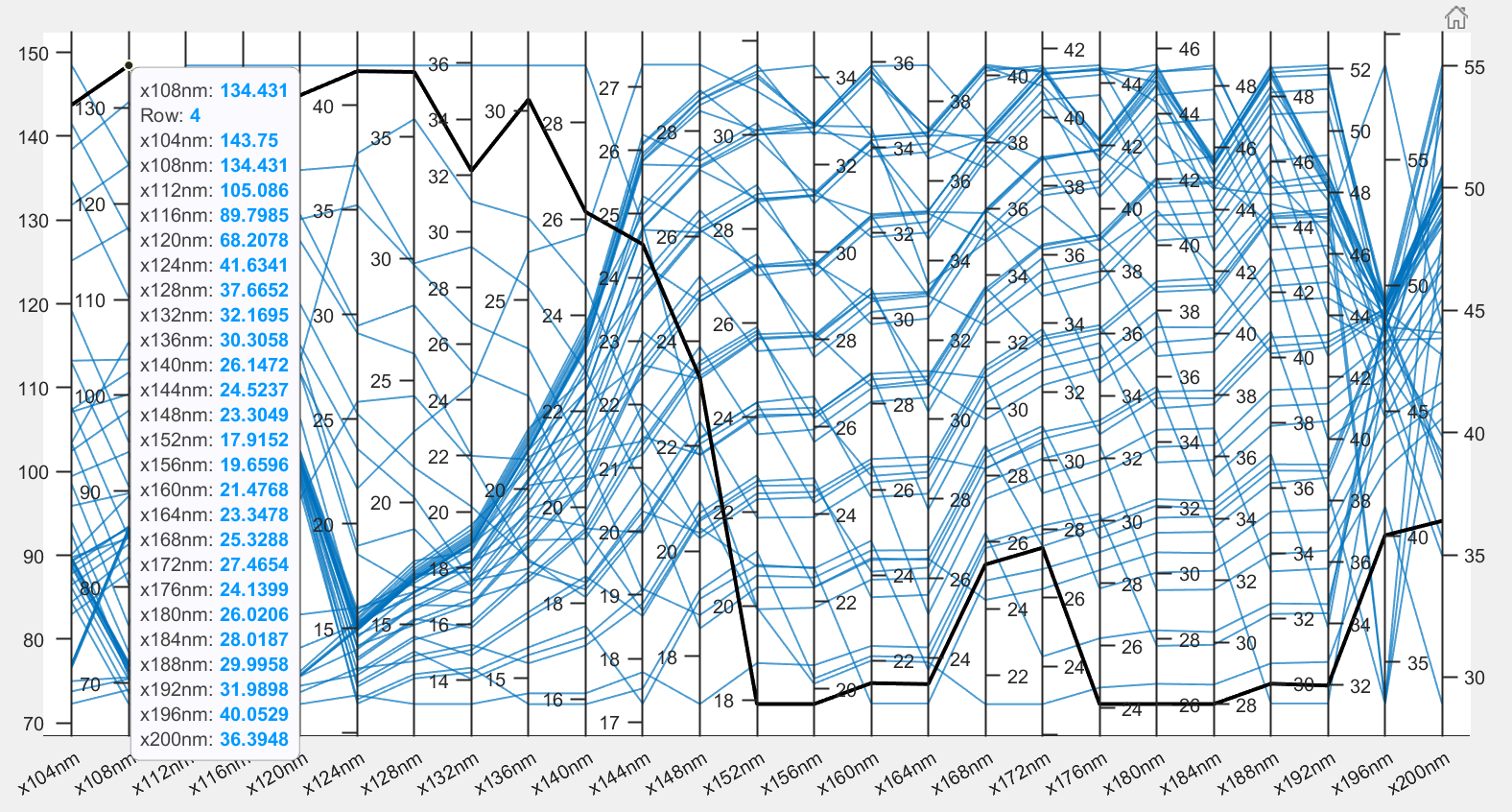
**Fig 3.21** Excel Sheet of Vgs(V) vs Ids(uA/um)

In our analysis, we use Excel to create the datasets as shown in Fig 3.21 by varying the parameters in nanoHUB.

**3.2.3 MATLAB Simulation Tool**

MATLAB is a powerful tool for generating graphs, especially when dealing with complex datasets and varied parameters. It simplifies the process by easily importing data from Excel sheets using functions like `xlsread` or `readtable`. Once the data is imported, MATLAB offers a wide range of plotting functions to create different types of graphs, such as line plots and histograms. It also allows for easy analysis of how changing parameters affect the data, thanks to its scripting capabilities. This makes it straightforward to iterate over different parameter values and visualize the results effectively.

In addition, MATLAB provides customization options for enhancing the appearance of graphs, such as adding legends, labels, and interactive features for better readability. It also enables the export of graphs in various formats, making it convenient to include them in project reports. With its documentation capabilities, MATLAB ensures transparency and reproducibility by allowing the inclusion of code directly into reports alongside formatted text and graphical output. Overall, MATLAB simplifies the process of analyzing data, visualizing results, and presenting findings in a clear and concise manner.



**Fig 3.22** MATLAB Analysis Example

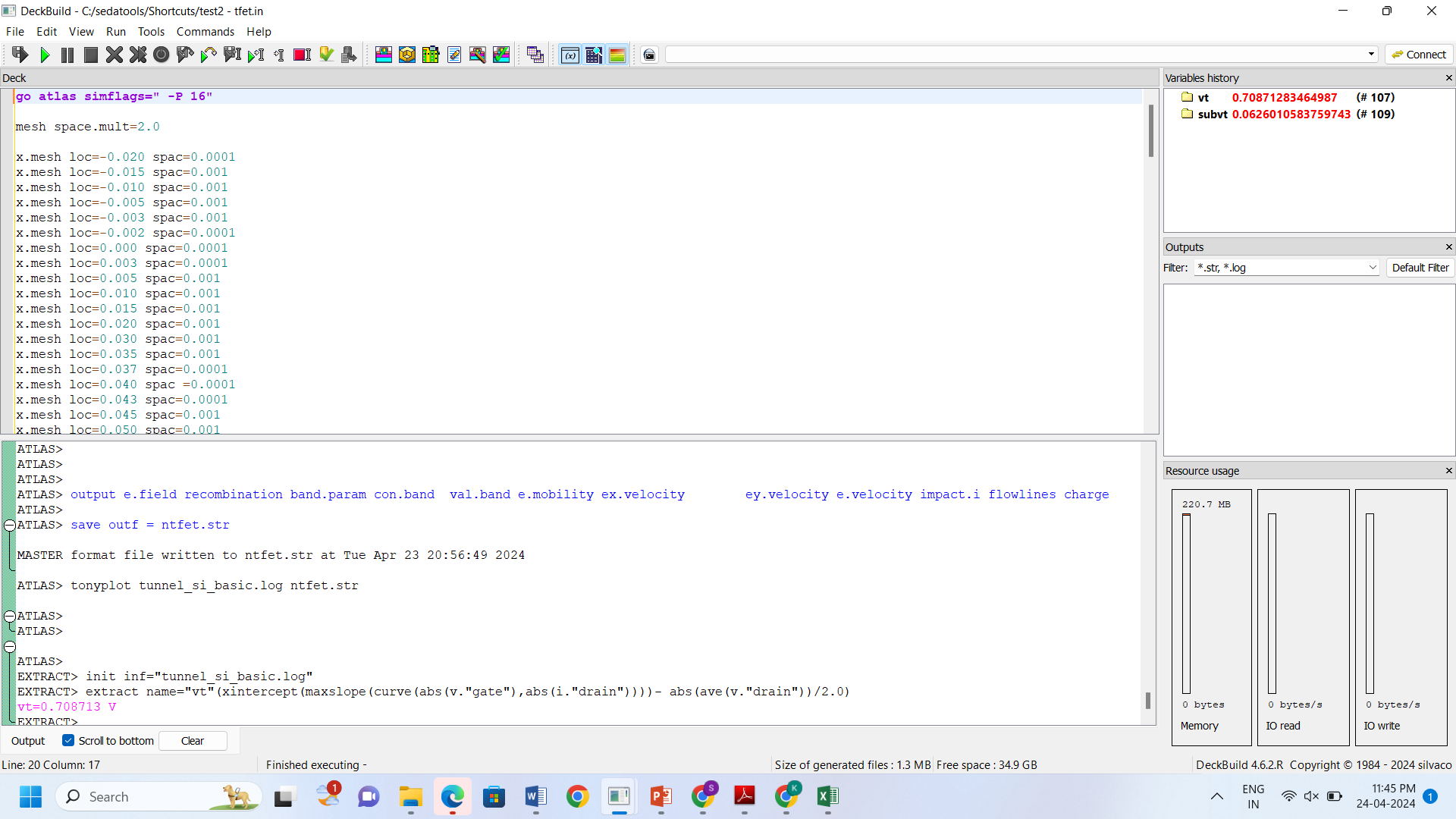
In our analysis we use MATLAB Simulation tool to analyze the datasets as shown in Fig 3.22 by varying the parameters in nano HUB.

**3.2.4 Silvaco**

Silvaco stands out as a premier provider of Electronic Design Automation (EDA) software and semiconductor design tools. Renowned for its comprehensive suite of solutions, Silvaco serves the semiconductor industry with tools spanning various design, simulation, and verification aspects. Among its key offerings, Silvaco's TCAD (Technology Computer-Aided Design) tools hold significance. These tools empower semiconductor engineers to simulate process and device behaviors at the physical level, facilitating the optimization of device performance and manufacturing processes.

Silvaco is a software suite widely used for semiconductor device simulation and process modeling. It provides tools for designing, simulating, and optimizing various semiconductor devices, including TFETs (Tunnel Field-Effect Transistors).

TFETs are a type of transistor that operate on the principle of quantum tunneling. Silvaco offers several features that can be helpful for generating TFET structures including device simulation, process modelling, quantum mechanical simulation, parameter extraction, optimization tools.

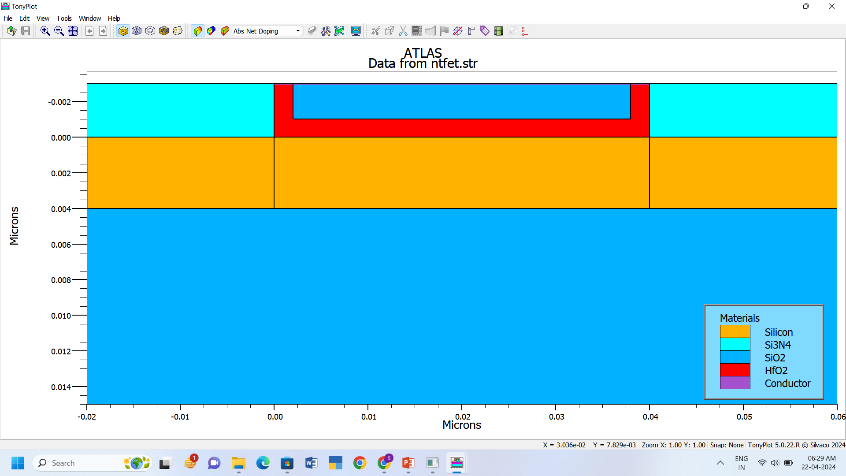
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Overall, Silvaco plays a crucial role in the design, simulation, and optimization of TFET structures by providing a comprehensive suite of tools tailored for semiconductor device engineering.

**4. RESULTS OF TUNNEL FIELD EFFECT TRANSISTOR SIMULATION ANALYSIS**

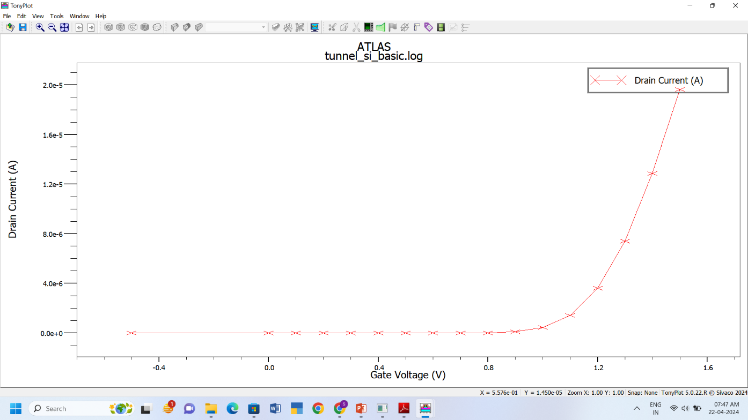
**4.1 UTB-TFET Output**

The UTB TFET has been meticulously designed within the Silvaco tool, guided by thorough analysis of parameters such as channel length, channel thickness, oxide thickness, and doping. As a result of our experimentation, the structure depicted in Figure 4.1 exemplifies our successful implementation.



**Fig 4.1** UTB-TFET Structure

The transfer characteristic curve is also generated for UTB-TFET as shown in Fig 4.2. After the transistor structure is created in Silvaco, the program can be used to simulate its transfer characteristics, electrical characteristics etc. The IDS-VGS plot shows the drain current (Ids) of the transistor as a function of the gate voltage (Vgs).



**Fig 4.2** Transfer Characteristics of UTB-TFET Model

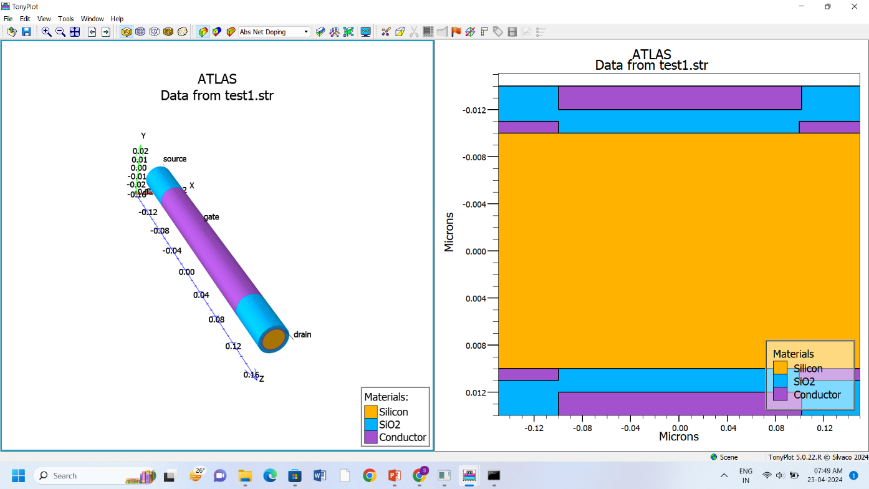
Upon analyzing the IDS and VGS characteristics from Figure 4.2, we have determined that the threshold voltage (VT) measures at 0.709V, showcasing a subthreshold swing of 62 mV/dec. Additionally, our experimental findings reveal a maximum current of 2.53A, demonstrating the performance parameters of our design in the Table 4.3.

|  |  |
| --- | --- |
| **UTB Tunnel FET device** | Values |
| Threshold voltage (Vt) | 0.709V |
| Sub threshold swing (SS) | 62 mV/dec |
| Max Ids | 2.53e-13 |

**Table 4.3** Device Performance Parameters of UTB-TFET Model

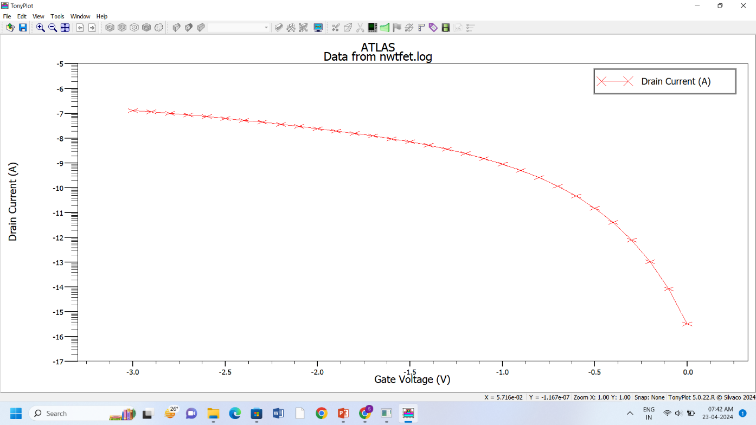
**4.2 NW-TFET Output**

The NW TFET has been meticulously designed within the Silvaco tool, guided by thorough analysis of parameters such as channel length, channel thickness, oxide thickness, and doping. As a result of our experimentation, the structure depicted in Figure 4.4 exemplifies our successful implementation.



**Fig 4.4** NW-TFET Structure

The transfer characteristic curve is also generated for NW-TFET as shown in Fig 4.5. After the transistor structure is created in Silvaco, the program can be used to simulate its transfer characteristics, electrical characteristics etc. The IDS-VGS plot shows the drain current (Ids) of the transistor as a function of the gate voltage (Vgs).



**Fig 4.5** Transfer Characteristics of NW-TFET Model

Upon analyzing the IDS and VGS characteristics from Figure 4.2, we have determined that the threshold voltage (VT) measures at 2.0958V, showcasing a subthreshold swing of 62 mV/dec. Additionally, our experimental findings reveal a maximum current of 1.272A, demonstrating the performance parameters of our design in the Table 4.6.

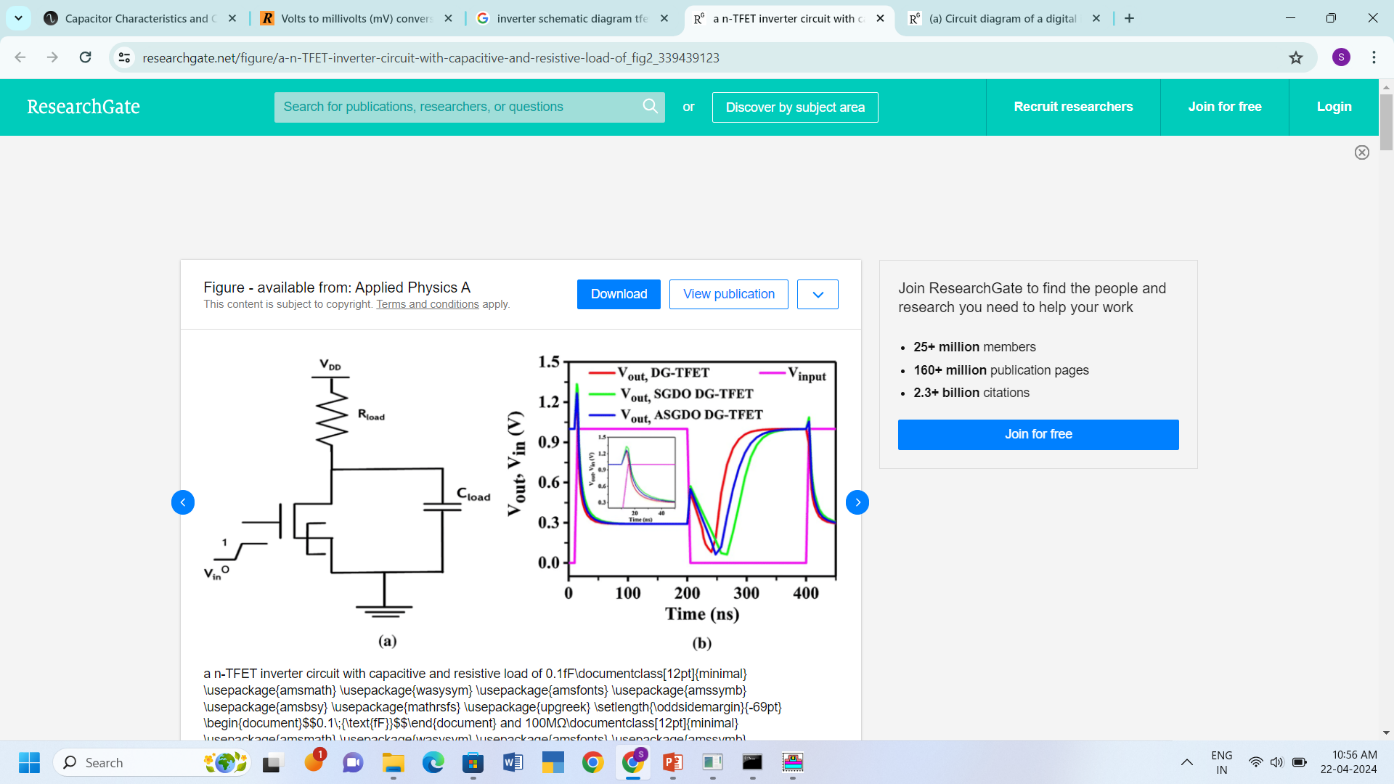
|  |  |
| --- | --- |
| **Tunnel FET device** | **Values** |
| Threshold voltage (Vt) | 2.0958V |
| Sub threshold swing (SS) | 62 mV/dec |
| Max Ids | 1.2727e-07 |

**Table 4.6** Device Performance Parameters of NW-TFET Model

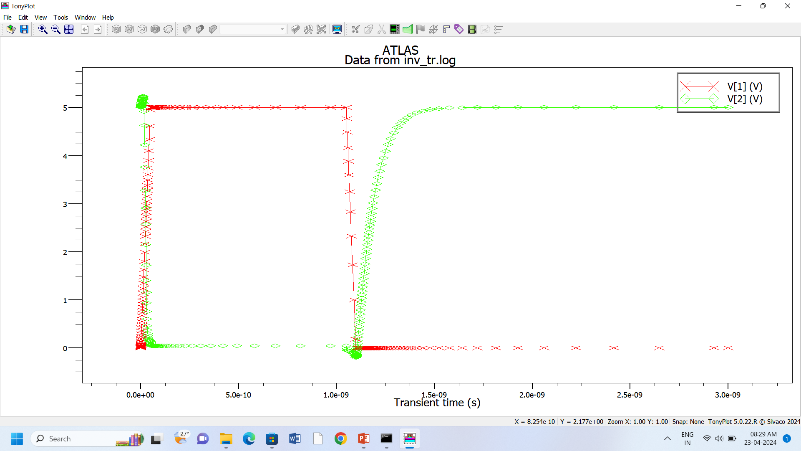
**4.3 Design of Inverter using TFET**

The inverter, a fundamental building block in digital electronics, serves as a critical component in countless electronic systems. At its core, an inverter is a device that converts one logic level to its opposite, typically transforming a high voltage input into a low voltage output, and vice versa. This function is pivotal in digital circuits, where it enables the creation of logical operations such as NOT gates, essential for data processing and signal control. Moreover, inverters play a central role in power electronics, facilitating the conversion of direct current (DC) to alternating current (AC), which is indispensable in various applications, including renewable energy systems, uninterruptible power supplies (UPS), and motor drives. As the demand for efficient energy management and reliable power conversion continues to grow, the significance of inverters in modern technology becomes increasingly evident, highlighting their pivotal role across diverse sectors ranging from telecommunications to renewable energy integration.

The inverter, implemented using our designed NT-FET connected with an RC combination circuit as shown in the Fig 3.1, functions as follows: When the gate voltage is 0V, the NT-FET remains in the off state, resulting in maximum output current. Conversely, when the gate voltage is 5V, the NT-FET switches to the ON state, leading to minimum output current. This operational behavior of the designed inverter demonstrates its intended functionality.



The graph shown in Fig.3.1 depicts the relationship between the output voltage (Vout) and the input voltage (Vin), with Vin (V) plotted on the x-axis and Vout (V) on the y-axis. It exhibits typical inverter behavior, indicating an inverted output voltage relative to the input voltage. Specifically, when Vin is high (positive), Vout is low (negative), and vice versa, confirming the expected behavior of an inverter circuit employing a TFET (Tunneling Field-Effect Transistor). The graph effectively captures the inversion characteristic inherent to the designed inverter, validating its functionality



**Conclusion**

In conclusion, our proposed study focused on the design and simulation of Heterojunction Tunnel Field-Effect Transistors (TFETs), considering parameters such as channel length, channel thickness, oxide thickness, and doping. We investigated two TFET architectures: Ultra-Thin Body (UTB) and Nanowire (NW) designs. Through observation of the characteristics of TFETs via graphs of Ids v/s Vgs, we aimed to identify typical operating values and determine the model best suited for low power applications.

Our analysis revealed that our designed TFETs exhibited promising characteristics. The UTB TFET demonstrated a threshold voltage of 0.709V, while the NW TFET showed a threshold voltage of 2.095V. Additionally, both UTB and NW TFETs exhibited a subthreshold voltage of 62mV/dec. Furthermore, the NW TFET achieved a maximum current of 1.27mA, whereas the UTB TFET reached a maximum current of 2.53mA.

Based on these findings, we proceeded to design and develop a TFET-based inverter, leveraging the observed operating values. This inverter holds significant potential for applications requiring low power consumption, aligning with the current trend towards energy-efficient electronics. Overall, our study contributes to the advancement of TFET technology and its practical implementation in various electronic systems, promising enhanced performance and energy efficiency.

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