Snehadeep Gayen | CS21B078

B. Tech Computer Science and Engineering

Minor in Mathematics

Indian Institute of Technology, Madras

EDUCATION

B. Tech CSE | **CGPA 9.94** — Jul '21 - Present
Indian Institute of Technology Madras — Chennai, TN

HSC Class 12th | **98.17%** — Apr '20 - Apr '21
Pace Junior Science College — Mumbai, MH

ICSE Class 10th | **98.80%** — Apr '18 - Apr '19
Lilavatibai Podar High School — Mumbai, MH

EXPERIENCE

Software Internship at Optiver Amsterdam — May'24 - Jul'24

- Worked in the Quant Research & Data Team of Optiver Delta1
- Added functionality to create TCP/IP filters from session configuration files for the Network Parser and optimised them for performance.
- Added functionality to convert timestamps across timezones, accounting for Daylight Saving Time changes
- Analysed SQL queries and designed a new OneTick database with Schema to replace a saturated PostGres time series database.

Team Avishkar Hyperloop, CFI — Oct '22 - Present

- Part of Embedded Software Team of the **Main Control Unit** and **Navigation Unit** of our Hyperloop Pod.
- Used **RTOS, threading** and communication protocols like MQTT, CAN, etc. to collect and store data from over 20 sensors at **low latency**, **handling errors** appropriately.
- Participated in the prestigious **European Hyperloop Week - Scotland 2023**, among over 25 teams globally to represent the country.

Undergraduate Research - WiFi Sensing for IoT — Jan'24 - May'24

- Created an end-to-end IoT pipeline for Human Activity Recognition using WiFi CSI (Channel State Information) Sensing
- Analysed the effect of compression on CSI data and its tradeoffs on the Network Bandwidth, Energy Consumption & Sensing Accuracy.
- Submitted part of the work in AIoT workshop organised in Athens, Greece.

Undergraduate Research - Custom Protocol Headers with P4 for Network Application Support — Ongoing

- Ideation of a custom protocol header to improve network telemetry or security using P4 switch data plane programming language.
- Implementation with be done on Intel Tofino switches

Tutor & Contributor, NPTEL — March '23 - Present

- Created **YouTube tutorials** for previous years' GATE CS questions
- These tutorials aim to support applicants who may have limited access to resources

SOFTWARE SKILLS

- **Languages**: C++, C, HDL (Verilog), OCaml, Python, Java, Prolog, SQL, x86, MIPS and 8085 ASM, HTML & CSS, R
- **Tools**: TI CCS, Git, LaTeX, AutoCAD, GDB
- **Libraries**: TI RTOS, NumPy, PyLops, Matplotlib

EXTRACURRICULAR ACTIVITIES

- **Sports:** Awarded 13 medals in various Track & Field events and Best Athlete U14 in High School, Taekwondo Red Dan II Belt, NSO Athlete at IITM
- Mentored freshmen, personally and academically, under **Saathi, IIT Madras**

SCHOLASTIC ACHIEVEMENTS

- Awarded Sri V Ramachandran Prize for **Highest CGPA** in Semesters 3 & 4 of B.Tech and Dual Degree in Computer Science
- Secured **AIR 5** in JEE Mains '19 out of 1 million students
- Secured **AIR 161** in JEE Advanced '19
- Secured **AIR 10** in Indian Statistical Institute Exam
- Secured **AIR 21** in INChO and attended Orientation Camp for International Chemistry Olympiad
- Awarded KVPY Fellowship '21 with **AIR 338**
- Winner of Mimamsa '22 at IISER Pune | 4^{th} place in Chemenigma '22 at IISC Bangalore | Won Silver Medal in Homi Bhabha Science Competition (conducted in Maharashtra)

PROJECTS

Java Compiler Design — *Java, C*

CS3300 Course Project - Prof. Krishna Nandivada — Jan-May '23

- Implemented a MIPS compiler for a subset of Java with Lexical Analyser, Parsing, Type Checking, IR Generation, Register Allocation, Stack Handling, and MIPS code generation

OS Scheduler and Memory Management Unit Design — *Java*

CS3500 Course Project - Prof. Prashant LA — Jan-May '23

- Implemented a Memory Management Unit with LRU Page replacement Policy
- Implemented a Multi-Level Feedback Queue Scheduler for processes

CPU Design — *Verilog*

CS2610 Course Project - Prof. C. Chandra Sekhar — Jan-May '23
CS2310 Course Project - Prof. Ayon Chakraborty — Jul-Nov '22

- Implemented a CPU with **Register file** and **ALU** with instructions to perform Arithmetic and Logical operations on both 8-bit integers and 12-bit floating-point numbers
- Built a combinational 8-bit CPU with structural gate-level Verilog

Closeness Centrality Algorithm — *C++*

Project under Prof. Manikandan Narayanan — May-Jun '23

- Implemented the CENDY algorithm, an on-line algorithm for updating Average Path Length and Closeness Centrality in a Dynamic Graph, based on this paper.

COURSES & LABS

Computer Science

- Hi
- Hi

Mathematics

- Hi
- Hi

Economics

- Hi
- Hi