No. of Pages : 02 M.Tech and PhD

1st Semester (End Sem) Examination December 2023

Research Methodology (RM)

Time 2 and 1/2 Hours Max Marks : 50

Answer any five questions

Q1

Define Research. Briefly explain the different attributes for true experimental designs with proper examples. [10]

Q2

(a) Explain the meaning of research hypothesis in context of Research design.

(b) Enumerate different methods of data collection with brief note on observation method and interview method of data collection. [5+5]

Q 3

(a) Differentiate between arbitrary review and systematic review? [3]

(b) Explain how research methods are different from research methodology? Write down the different types of research with respect to criteria and types. [4]

(c) What is meta-analysis? Explain how it is related to systematic review [3]

Q4.

State your research problem with respect to your area of research. Briefly explain PRISMA process of paper screening for a new reviews and updated reviews. Explain with a suitable example how it filters out the records over different stages to finally include in meta-analysis. [10]

Q5:

(a) Will a Patent granted in India protect your rights in the USA? Why?

Critically analyze Idea-Expression Dichotomy with some examples.

(b) State whether following inventions qualify for Patent in India? Give reasons if not patentable.

i. A vehicle travelling faster than speed of light

ii. A new composition for a song

iii. A new theory to establish Sun rises in the east

iv. A new procedure for brain surgery that does not need anesthesia

v. A new Programming code for multiplying matrices

[10]

Q6.

What is the need for intellectual property right (IPR)?

What are the different types of IPR, explain who is benefitted from each type of IPR and how?

Hypothetically you are setting a new Electronics equipment manufacturing company with new and innovative machineries. You plan to use your knowledge of IPR to safeguard your new company from old bigshot companies as well as new budding companies. Describe in details, what all rights you will register and how you will benefit out of it.

[10]

Student Id | | | | | | | | |

No. of Pages: 02 M Tech

First Semester (End Sem) Examination 2023

Blockchain and its Applications

Branch: CSE

Time 2hrs 30min Max Marks: 50

Answer any five questions.

Q 1. [4+6]

a) Explain the concept of collision resistance in the context of cryptographic hash functions.

b) Define what a cryptographic hash function is and outline its fundamental properties.

Provide examples of real-world applications where these properties are crucial for ensuring security.

Q 2. [6+4]

a) Describe the basic process of creating and verifying a digital signature. Include the key steps and the cryptographic components involved.

b) How does the use of public and private keys contribute to the security of digital signatures?

Q 3. [6+4]

a) Explain the fundamental principles of the RAFT consensus protocol. How does RAFT ensure fault-tolerance and leader election in a distributed system?

b) Compare RAFT to other consensus algorithms and discuss scenarios where RAFT might be preferred.

Q 4. [6+4]

a) Explore specific use cases where blockchain interoperability is crucial. How does interoperability enhance the functionality and utility of blockchain technology in areas such as finance, supply chain, or healthcare?

b) Differentiate between Hashlock and Timelock in term of blockchain interoperability.

Q 5. [4+6]

a) Discuss the challenges and importance of interoperability in decentralized identity management.

b) How can standards such as Decentralized Identifiers (DIDs) and Verifiable Credentials contribute to achieving interoperability among various identity systems? Explain how these standards enhance the portability of identity information.

Q 6. [3+4+3]

a) Explain the basic concept of smart contracts on the Ethereum blockchain.

b) How do Ethereum smart contracts differ from traditional contracts, and what advantages do they offer in terms of automation and transparency?

c) Provide an example use case where a smart contract on Ethereum could be beneficial.

Q 7. [5+5]

a) Examine some of the common risks that organizations and users face when engaging with blockchain technology.

b) Discuss in detail issues such as 51% attacks, double-spending, and smart contract vulnerabilities. How do these risks pose challenges to the security and reliability of blockchain networks?

.....ALL THE BEST.....

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No. of Pages: 1 **M Tech**

M.Tech End Semester(1st Sem) Examination - December 2023

Data Analytics & Computing

Branch: CSE

Time 2.5 Hours **Max Marks: 50**

Instruction: Attempt any five questions. All questions carry equal marks.

1. A. Explain the group bar plot, stacked bar plot, general bar plot, pie plot and histogram with examples. [5]

   B. What is the difference between KNN and K Means clustering? [5]

2. Describe various types of neural networks - Perceptron, Multilayer Perceptron, ANN, RNN, CNN, GAN and LSTM with examples. What is the difference between trainable parameters and hyperparameters? [7 + 3]

3. A. What do you mean by loss, objective, and cost functions? Describe with examples. [3]

   B. What is the role of p-value in hypothesis testing? Explain various parametric and non-parametric tests. [7]

4. A. What is the difference between overfitting and underfitting? Explain the bias-variance tradeoff. [7]

   B. Can we use decision trees as regressors? Justify with a proper explanation. [3]

5. A. Describe the usages of Activation Functions. And explain sigmoid, RELU, Leaky RELU and SoftMax activation function. [6]

   B. Explain binning and features hashing (Bag of Words) in detail regarding applicability and examples. [4]

6. Explain the difference between filter and wrapper-based feature selection methods with proper explanation. Do you think ROC-AUC is the appropriate measure of computing classification accuracy? Justify with a proper explanation. [6 + 4]

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No. of pages: 3 M. Tech.

First Semester End-Sem Examination - December 2023
Advanced Computer Architecture
Branch: Computer Science and Engineering

Time: $2\frac{1}{2}$ Hours **Maximum Marks: 50**

Answer any five questions.
The figures in the right-hand margin indicate marks.
Your answers must be complete in all relevant respects and also self-explanatory.

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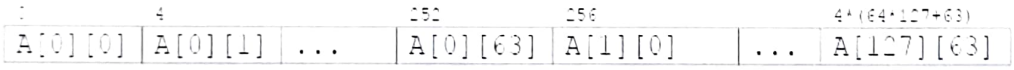
1. (a) Suppose you are given a program which does a fixed amount of work and some fraction s of that work must be done sequentially. The remaining portion of the work is perfectly parallelizable on P processors. Assuming T_1 is the time taken on one processor, derive a formula for T_p the time taken on P processors. Use this to get a formula giving an upper bound on the potential speedup on P processors. Explain why it is an upper bound? (5)

   (b) What is a true data hazard that may occur in an instruction pipeline? Explain with a suitable example and clock cycle diagram. How stalls arising due to true data hazard can be minimized by operand forwarding? (5)

2. (a) Write down the different address mapping schemes that take place between main memory to cache memory with proper examples. (5)

   (b) List out the different cache-writing policies. Mention the advantages and disadvantages of each policy. State the differences between write-allocate and no-write-allocate in the context of write miss in the cache? (5)

3. (a) The matrix A is stored contiguously in memory in row-major order. Row major order means that elements in the same row of the matrix are adjacent in memory as shown in the following memory layout: A[i][j] resides in memory location [4*(64*i + j)]. (5)

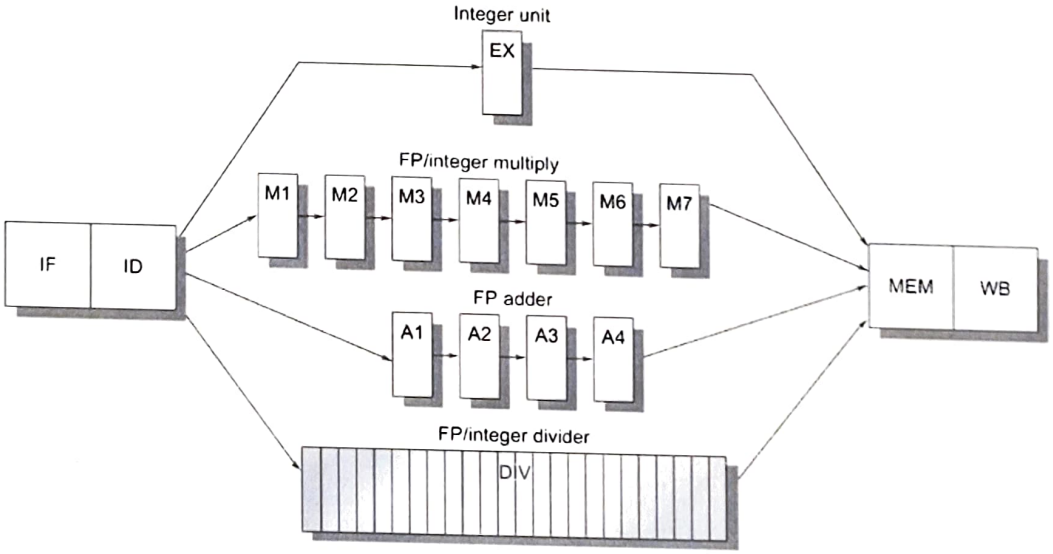


This problem evaluates the cache performances for different loop orderings. You are asked to consider the following two loops, written in C, which calculate the sum of the entries in a 128 by 64 matrix of 32-bit integers:

Loop A	Loop B
sum = 0;	sum = 0;
for(i = 0; i < 128; i++)	for(j = 0; j < 64; j++)
for(j = 0; j < 64; j++)	for(i = 0; i < 128; i++)
sum = sum + A[i][j];	sum = sum + A[i][j];

For the given problem, assume that the caches are initially empty. Also, assume that only accesses to matrix A cause memory references and all other necessary variables are stored in registers. Instructions are in a separate instruction cache. Consider a 4KB direct-mapped data cache with 8-word (32-byte) cache lines. Calculate the number of cache misses that will occur when running Loop A. Calculate the number of cache misses that will occur when running Loop B.

(b) The EXE stage in a classic 5-stage pipelined machine cannot complete an operation in 1 cc always as the nature of operations may vary. The following figure depicts a modification where dedicated hardware units are engaged for the EXE stage for separate operations. In the modified arrangement, the Integer ALU unit takes 1 cc, the Data memory (Integer and Floating-Point loads) takes 2 cc, the Floating-Point adder takes 4 cc, Floating-Point (also Integer) multiplier takes 7 cc, and the Floating-Point (also Integer) divider takes 25 cc to complete the respective operations. Also, except the divider unit all the other units are pipelined. (5)



In this context, define and find out latency and initiation interval of each EXE functional unit. Assuming the other pipe stages complete their execution in 1 cc, provide the clock cycle diagram for the following set of independent instructions execution through this modified instruction pipeline.

Instruction Order	Instruction	Meaning
1	fmul.d	Floating-point multiplication
2	fadd.d	Floating-point addition
3	fdiv.d	Floating-point division
4	fdiv.d	Floating-point division

4. (a) Consider a system with 8-bit addresses and 16-byte pages. A process in this system has 4 logical pages, which are mapped to 3 physical frames in the following manner: logical page (5)

0 maps to physical frame 2, page 1 maps to frame 0, page 2 maps to frame 1, and page 3 is not mapped to any physical frame. The process may not use more than 3 physical frames. On a page fault, the demand paging system uses the LRU policy to evict a page. The MMU has a TLB cache that can store 2 entries. The TLB cache also uses the LRU policy to store the most recently used mappings in cache. Now, the process accesses the following logical addresses in order: 7, 17, 37, 20, 40, 60.

i. Assume that the TLB cache is empty before the accesses begin. Out of the 6 memory accesses, how many result in a TLB miss? Clearly indicate the accesses that result in a miss.

ii. Out of the 6 memory accesses, how many result in a page fault? Clearly indicate the accesses that result in a page fault.

iii. Upon accessing the logical address 60, which physical address is eventually accessed by the system (after servicing any page faults that may arise)? Show suitable calculations.

(b) Consider the page reference string 0, 1, 3, 6, 2, 4, 5, 2, 5, 0, 3, 1, 2, 5, 4, 1, 0. The number of page frames is 4. What would be the number of page faults generated for each of the following algorithms: (5)

i. FIFO

ii. LRU

5. (a) Draw the schematic diagram of a 32 input and output omega network with proper node numbering. Show the routing path for a message between the following sender-receiver node pair: (5)

i. Sender node = 1 and receiver node =25

ii. Sender node = 18 and receiver node = 3

(b) Draw the schematic diagram of a 4-D hypercube network with proper node numbering. Show the routing path for a message between the following sender-receiver node pair using the e-cube routing protocol: (5)

i. Sender node = 1 and receiver node = 10

ii. Sender node = 13 and receiver node = 3

6. (a) What do you mean by cache coherence problem in a multiprocessor system? How this can be dealt with snooping protocol? Explain the different categories of snooping protocols. (5)

(b) What do you mean by coherence misses in symmetric shared-memory multiprocessors? Explain the terms true sharing misses and false sharing misses in connection with the above issue with appropriate examples? (5)

7. (a) State the difference between a thread and a process. List at least four benefits of using threads. What may be the possible disadvantages of threads? (5)

(b) Briefly explain about the following: coarse-grained multithreading, fine-grained multithreading. (5)

IIIT Bhubaneswar

End Semester Examination-2023

MFCS, M & C

M.Tech. & Ph.D. Coursework

F.M.-50 Time-2.5 hr

Group-A (Answer *ANY One* question)

1. (a) Determine the range, kernel, rank, and nullity of the linear transformation $T: V_4 \to V_3$ *by* $T(x_1, x_2, x_3, x_4) = (x_1 - x_4, x_2 + x_3, x_3 - x_4)$. [5]

   (b) Determine the linear map. Given that $T: V_2 \to V_2$ *such that* $T(1,2) = (3,0)$ *and* $T(2,1) = (1,2)$. [5]

2. (a) Solve the system of linear equation by using the row-reduction method:
   $x - y + 3z = 1, 2x + y - z = 2, 3x - y + 2z = 2.$ [5]
   (b) Find the coordinates of the polynomial $3 + 7x + 2x^2$ relative to the order basis $\{1 - x, 1 + x, 1 - x^2\}$ [5]

Group-B (Answer *ANY TWO* questions)

3. Let $A = \begin{bmatrix} 12 & -51 & 4 \\ 6 & 167 & -68 \\ -4 & 24 & -41 \end{bmatrix}$. Using QR decompositions let $A = QR$. Show that the matrix Q is orthogonal. [5]

   (b) Prove that the polynomials $1, x, \frac{3}{2}x^2 - \frac{1}{2}, \frac{5}{2}x^3 - \frac{3}{2}x$ form an orthogonal set in $C[-1,1]$. Also find $f(x)$ such that $||f(x)|| = 1$. [5]

4. (a) If G is the generalised inverse of the matrix $A = \begin{bmatrix} 5 & 1 \\ 4 & 2 \end{bmatrix}$ satisfying the Moore-Penrose conditions, then find the matrix G. [5]

   (b) Let $Q = x_1^2 + 2x_2^2 - 7x_3^2 - 4x_1x_2 + 8x_1x_3$. If $y = x^T Qx$, show that $\frac{\partial^2 y}{\partial x^2} = 2Q$. [3]

   (c) Let $y_1 = x_1^2 - x_2, y_2 = x_3^2 + 3x_2$. If $y = [y_1\ y_2]^T, x = [x_1\ x_2 x_3]^T$, obtain $\frac{\partial y}{\partial x}$. [2]

5. Using singular value decomposition of the matrix, solve the system of equations:
   $x_1 + x_2 + 2x_3 = 5, -x_1 + 2x_2 + x_3 = 9.$ [10]

Group-C (Answer *ANY One* question)

6. Use Kuhn-Tucker conditions to solve the following NLP:
   $\max z = 7x_1^2 - 6x_1 + 5x_2^2,\ s.t.\ x_1 + 2x_2 \leq 10, x_1 - 3x_2 \leq 9, x_1, x_2 \geq 0.$ [10]

7. Solve the following NLP:

   Minimize $Z = 4x_1^2 + 2x_2^2 + x_3^2 - 4x_1x_2$ s.t. $x_1 + x_2 + x_3 = 15, 2x_1 - x_2 + 2x_3 = 20.$ [10]

Group-D (Answer *ANY One* question)

8. (a) Suppose 36% of families own a dog, 30% of families own a cat, and 22% of the families that have a dog also have a cat. A family is chosen at random and found to have a cat. What is the probability they also own a dog? [5]

(b) Given the CDF F(x) for the discrete random variable X, Find: (a) $P(X = 3)$ (b) $P(X < 4)$

X	1	2	3	4	5
$F(X)$	0.2	0.32	0.67	0.9	1

[5]

9. (a) A biased die is thrown 30 times and the number of sixes shown is eight. If the die is thrown further 12 times find:

i) The probability that a six will occur exactly twice.
ii) The expected number of sixes.
iii) The variance of the number of sixes.

[5]

(b) The mean weight of 500 male students at a certain college is 151 lb and the standard deviation is 15 lb. Assuming that the weights are normally distributed, find how many students weigh (a) between 120 and 155 lb, (b) more than 185 lb. [5]

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