University of Applied Sciences Western Switzerland
MSE - Software Engineering

Deepening project

KlugHDL : A VHDL language generator

Specifications

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1 Context

SpinalHDL is a programming language to describe digital hardware and generate the corresponding VHDL/Verilog file[1]. SpinalHDL is written in Scala as a DSL (Domain Specific Language) and has multiple advantages[1] from that :

- No restriction to the genericity of your hardware description by using Scala constructs
- No more endless wiring. Create and connect complex buses like AXI in one line.
- Evolving capabilities. Create your own buses definition and abstraction layer.
- Reduce code size by a high factor, especially for wiring. Allowing you to have a better visibility, more productivity and fewer headaches.
- Free and user friendly IDE. Thanks to scala world for auto-completion, error highlight, navigation shortcut and many others
- Extract information from your digital design and then generate files that contain information about some latency and addresses
- Bidirectional translation between any data type and bits. Useful to load a complex data structure from a CPU interface.
- Check for you that there is no combinational loop / latch
- Check that there is no unintentional cross clock domain

The code 1 shows a AND gate written with SpinalHDL with the corresponding generated VHDL code, we could see the similarity between the two code.

```
import spinal.core._

class AND extends Component
{
    val io = new Bundle
    {
        val a = in Bool
        val b = in Bool
        val c = out Bool
    }

    io.c := io.a & io.b
}
```

```
entity AND_1 is
    port(
        io_a : in std_logic;
        io_b : in std_logic;
        io_c : out std_logic
    );
end AND_1;

architecture arch of AND_1 is

begin
  io_c <= (io_a and io_b);
end arch;
```

Listing 1: Example of a AND gate written in SpinalHDL and the corresponding generated VHDL code

2 Goal

The goal of the project is to produce an application which is analysing a spinalhdl program in order to produce a block diagramm of the corresponding hardware description. This application should offer the following activities :

- Display the complete graph of the programm
- Navigate through all the hierarchical level of the programm (Component inside another component)
- The edges should display some information about the signals :
  - type
  - input or output
  - ...
- A Hierarchical view (like in filesystems or in Quartus)
- A filter functionnality in order to view only some specific component

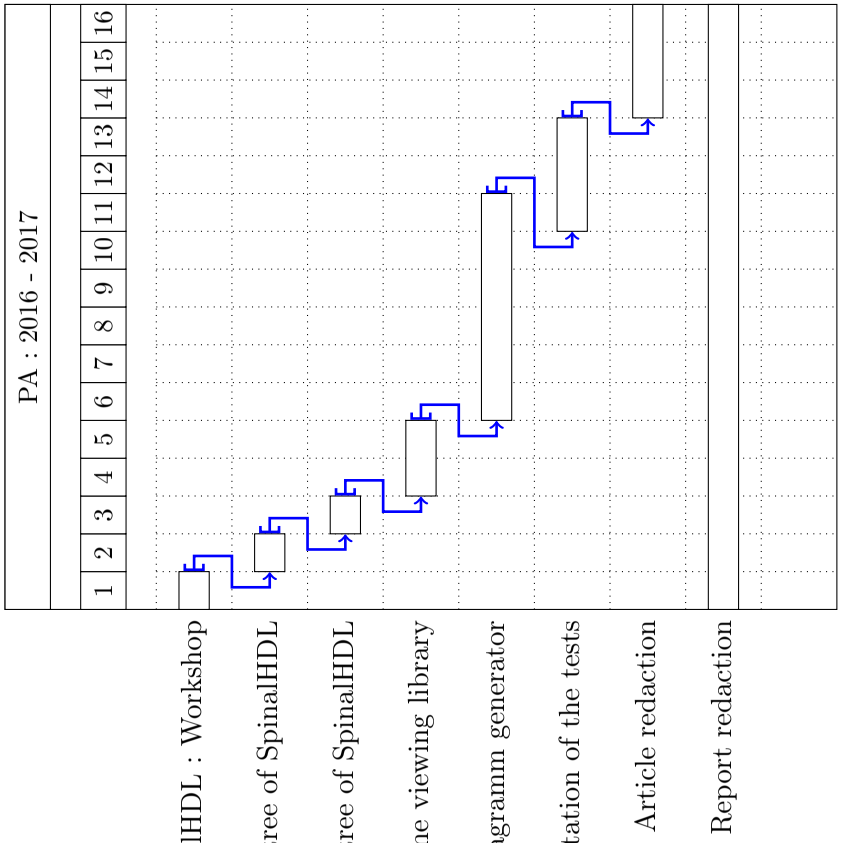
The application is going to be develop, firstable, in a standalone version and next we could develop and plugin version to Eclipse or IntelliJ for example.

3 Activities

The following activities are going to be done during the project :

- Do the Workshop about SpinalHDL in order to understand the basics.
- Analyse of some example to understand the abstract syntax tree of SpinalHDL.
- Generate without computer the blocks from some SpinalHDL/VHDL code.
- Analyse and comparison of some viewing library.
- Specification and implementation of the diagramm generator.
- Specification and implementation of the tests.
- Article redaction.
- Report redaction.

4 Planning


PA : 2016 - 2017
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Hands on with SpinalHDL : Workshop
Analyse and understanding of the abstract syntax tree of SpinalHDL
Generation without computer of some abstract syntax tree of SpinalHDL
Analyse and comparison of some viewing library
Specification and implementation of the diagramm generator
Specification and implementation of the tests
Article redaction
Report redaction

Bibliography

[1] C. Papon, SpinalHDL, **2016**.