Sistemas Digitales
Sistemas Secuenciales

Flip-Flop SR

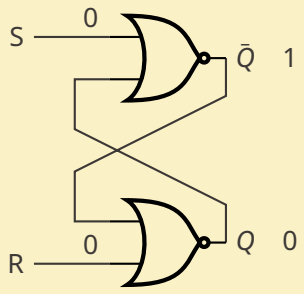


Tabla de verdad

(nunca puede haber *S*&*R*, the effects of *S* or *R* being true persist when returning to the initial state)

S	R	Q	$\bar{Q}$	
0	0			(initial state)
1	0	1	0	
0	1	0	1	
1	1	0	0	(ungodly, now a race condition)

Versión NAND

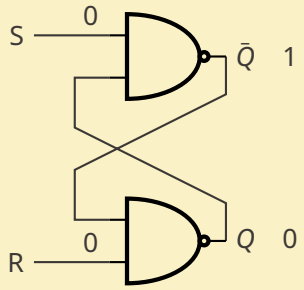


Tabla de verdad

S	R	Q	$\bar{Q}$	
0	0	1	1	(now this ones illegal)
1	0	1	0	
0	1	0	1	
1	1			(now this ones then initial state)

Flip-Flop JK

J_t	K_t	Q_{t+1}	
0	0	Q_t	(La salida se mantiene igual al siguiente ciclo)
0	1	0	
1	0	1	
1	1	$\bar{Q}_t$	(La salida se invierte al siguiente ciclo)

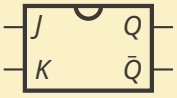
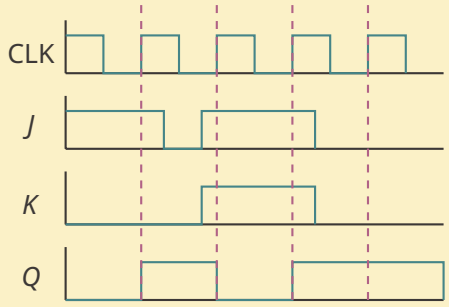
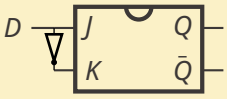


Diagrama de tiempo



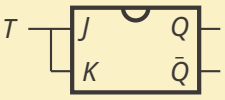
Flip-Flop D

D	Q_{t+1}
0	0
1	1



Flip-Flop T

T	Q_{t+1}
0	Q
1	$\bar{Q}$



Shift registers

S_1	S_0	
0	0	hold
0	1	store left
1	0	store right
1	1	PI??