P-SPI Component

Key Features (Page 2848, Section 70.2.2)

- Minimal CPU overhead with DMA transmit and receive requests supporting FIFO register accesses.
- Support for 32-bit word size.
- Configurable clock polarity and phase.
- Support for 8 peripheral chip selects in Controller mode.
- 4-word transmit and command FIFO.
- 4-word receive FIFO.
- Flexible timing parameters in Controller mode.
- Continuous transfer option to keep PCS asserted across multiple frames.
- Full-duplex and half-duplex transfers.

Block Diagram (Page 2847, Section 70.2.1)

The block diagram of the LPSPI component includes:

- Configuration registers
- Command/TX FIFO
- Control logic
- Shift register
- RX FIFO
- External SPI interface
- Internal chip peripheral bus

Needed Registers and Configuration

Register List (Page 2862, Section 70.6.1)

- Version ID (VERID): Offset 0h, 32 bits, Read-only
- Parameter (PARAM): Offset 4h, 32 bits, Read-only
- Control (CR): Offset 10h, 32 bits, Read/Write
- Status (SR): Offset 14h, 32 bits, Read/Write
- Interrupt Enable (IER): Offset 18h, 32 bits, Read/Write
- DMA Enable (DER): Offset 1Ch, 32 bits, Read/Write
- Configuration 0 (CFGR0): Offset 20h, 32 bits, Read/Write
- Configuration 1 (CFGR1): Offset 24h, 32 bits, Read/Write
- Data Match 0 (DMR0): Offset 30h, 32 bits, Read/Write
- Data Match 1 (DMR1): Offset 34h, 32 bits, Read/Write
- Clock Configuration (CCR): Offset 40h, 32 bits, Read/Write
- Clock Configuration 1 (CCR1): Offset 44h, 32 bits, Read/Write
- FIFO Control (FCR): Offset 58h, 32 bits, Read/Write
- FIFO Status (FSR): Offset 5Ch, 32 bits, Read-only
- Transmit Command (TCR): Offset 60h, 32 bits, Read/Write
- Transmit Data (TDR): Offset 64h, 32 bits, Write-only
- Receive Status (RSR): Offset 70h, 32 bits, Read-only
- Receive Data (RDR): Offset 74h, 32 bits, Read-only
- Receive Data Read Only (RDROR): Offset 78h, 32 bits, Read-only
- Transmit Command Burst (TCBR): Offset 3FCh, 32 bits, Write-only

- Transmit Data Burst (TDBR0 - TDBR127): Offset 400h - 5FCh, 32 bits, Write-only
- Receive Data Burst (RDBR0 - RDBR127): Offset 600h - 7FCh, 32 bits, Read-only

Configuration Details

1. Control Register (CR) (Page 2865, Section 70.6.1.4)
    - MEN: Module Enable
    - RST: Software Reset
    - DBGEN: Debug Enable
    - RTF: Reset Transmit FIFO
    - RRF: Reset Receive FIFO
2. Status Register (SR) (Page 2866, Section 70.6.1.5)
    - TDF: Transmit Data Flag
    - RDF: Receive Data Flag
    - WCF: Word Complete Flag
    - FCF: Frame Complete Flag
    - TCF: Transfer Complete Flag
    - TEF: Transmit Error Flag
    - REF: Receive Error Flag
    - DMF: Data Match Flag
    - MBF: Module Busy Flag
3. Interrupt Enable Register (IER) (Page 2870, Section 70.6.1.6)
    - TDIE: Transmit Data Interrupt Enable
    - RDIE: Receive Data Interrupt Enable
    - WCIE: Word Complete Interrupt Enable
    - FCIE: Frame Complete Interrupt Enable
    - TCIE: Transfer Complete Interrupt Enable
    - TEIE: Transmit Error Interrupt Enable
    - REIE: Receive Error Interrupt Enable
    - DMIE: Data Match Interrupt Enable
4. DMA Enable Register (DER) (Page 2872, Section 70.6.1.7)
    - TDDE: Transmit Data DMA Enable
    - RDDE: Receive Data DMA Enable
5. Configuration 0 Register (CFGR0) (Page 2873, Section 70.6.1.8)
    - HREN: Host Request Enable
    - HRPOL: Host Request Polarity
    - HRSEL: Host Request Select
    - HRDIR: Host Request Direction
    - CIRFIFO: Circular FIFO Enable
    - RDMO: Receive Data Match Only
6. Configuration 1 Register (CFGR1) (Page 2875, Section 70.6.1.9)
    - MASTER: Controller Mode
    - SAMPLE: Sample Point
    - AUTOPCS: Automatic PCS
    - NOSTALL: No Stall
    - PARTIAL: Partial Enable

    - PCSPOL: Peripheral Chip Select Polarity
    - MATCFG: Match Configuration
    - PINCFG: Pin Configuration
    - OUTCFG: Output Configuration
    - PCSCFG: Peripheral Chip Select Configuration
7. Clock Configuration Register (CCR) (Page 2882, Section 70.6.1.12)
    - SCKPCS: SCK-to-PCS Delay
    - PCSSCK: PCS-to-SCK Delay
    - DBT: Delay Between Transfers
    - SCKDIV: SCK Divider
8. Clock Configuration 1 Register (CCR1) (Page 2883, Section 70.6.1.13)
    - SCKSCK: SCK Inter-Frame Delay
    - PCSPCS: PCS to PCS Delay
    - SCKHLD: SCK Hold
    - SCKSET: SCK Setup
9. FIFO Control Register (FCR) (Page 2885, Section 70.6.1.14)
    - TXWATER: Transmit FIFO Watermark
    - RXWATER: Receive FIFO Watermark
10. Transmit Command Register (TCR) (Page 2888, Section 70.6.1.16)
    - CPOL: Clock Polarity
    - CPHA: Clock Phase
    - PRESCALE: Prescaler Value
    - PCS: Peripheral Chip Select
    - LSBF: LSB First
    - BYSW: Byte Swap
    - CONT: Continuous Transfer
    - CONTC: Continuing Command
    - RXMSK: Receive Data Mask
    - TXMSK: Transmit Data Mask
    - WIDTH: Transfer Width
    - FRAMESZ: Frame Size

Additional Useful Information

Functional Description (Page 2849, Section 70.3)

- Controller Mode: Describes how the transmit and command FIFO commands work, including conditions for SPI bus transfers and circular FIFO functionality.
- Peripheral Mode: Details how the LPSPI operates in peripheral mode, including the initialization of the Transmit Command (TCR) and handling of the receive FIFO.

Timing Parameters (Page 2851, Section 70.3.1.3)

- Clock Configuration (CCR): Defines the timing parameters for SPI bus transfers, including SCK setup and hold phases, PCS-to-PCS delay, and SCK-to-SCK delay.

Pin Configuration (Page 2854, Section 70.3.1.4)

- SIN and SOUT Pins: Configuration for half-duplex transfers and direction swapping.

- Output Data Pin Configuration: Specifies whether the output data pin 3-states when PCS is negated.

Clock Loopback (Page 2855, Section 70.3.1.5)

- SCK Clock: Configuration for using the SCK output clock or a delayed version

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Configurations for each register

Control Register (CR) (Page 2865, Section 70.6.1.4)

The Control Register (CR) manages global settings, including module enable/disable and reset operations:

- MEN (Module Enable): Enables or disables the LPSPI module.
    - To enable the module: CR[MEN] = 1
    - To disable the module: CR[MEN] = 0
- RST (Software Reset): Resets all internal logic and registers, except the Control Register.
    - To reset the module: CR[RST] = 1
    - To clear the reset: CR[RST] = 0
- DBGEN (Debug Enable): Enables LPSPI when the CPU is in Debug mode.
    - To enable debug mode: CR[DBGEN] = 1
    - To disable debug mode: CR[DBGEN] = 0
- RTF (Reset Transmit FIFO): Deletes all entries in the transmit FIFO.
    - To reset the transmit FIFO: CR[RTF] = 1
- RRF (Reset Receive FIFO): Deletes all entries in the receive FIFO.
    - To reset the receive FIFO: CR[RRF] = 1

Status Register (SR) (Page 2866, Section 70.6.1.5)

The Status Register (SR):

- TDF (Transmit Data Flag): Indicates whether data can be written to the transmit FIFO.
    - To check if transmit data is requested: SR[TDF] = 1
- RDF (Receive Data Flag): Indicates whether data can be read from the receive FIFO.
    - To check if receive data is ready: SR[RDF] = 1
- WCF (Word Complete Flag): Indicates whether the last bit of a word has been sampled.
    - To check if a word is complete: SR[WCF] = 1
- FCF (Frame Complete Flag): Indicates whether a frame transfer is complete.
    - To check if a frame is complete: SR[FCF] = 1
- TCF (Transfer Complete Flag): Indicates whether all transfers are complete.
    - To check if a transfer is complete: SR[TCF] = 1

- TEF (Transmit Error Flag): Indicates a transmit FIFO underrun error.
    - To check for a transmit error: SR[TEF] = 1
- REF (Receive Error Flag): Indicates a receive FIFO overflow error.
    - To check for a receive error: SR[REF] = 1
- DMF (Data Match Flag): Indicates whether the received data matches the configured data match value.
    - To check for a data match: SR[DMF] = 1
- MBF (Module Busy Flag): Indicates whether the LPSPI module is busy.
    - To check if the module is busy: SR[MBF] = 1

Interrupt Enable Register (IER) (Page 2870, Section 70.6.1.6)

The Interrupt Enable Register (IER) enables interrupts based on data flow and errors:

- TDIE (Transmit Data Interrupt Enable): Enables the transmit data interrupt.
    - To enable the interrupt: IER[TDIE] = 1
    - To disable the interrupt: IER[TDIE] = 0
- RDIE (Receive Data Interrupt Enable): Enables the receive data interrupt.
    - To enable the interrupt: IER[RDIE] = 1
    - To disable the interrupt: IER[RDIE] = 0
- WCIE (Word Complete Interrupt Enable): Enables the word complete interrupt.
    - To enable the interrupt: IER[WCIE] = 1
    - To disable the interrupt: IER[WCIE] = 0
- FCIE (Frame Complete Interrupt Enable): Enables the frame complete interrupt.
    - To enable the interrupt: IER[FCIE] = 1
    - To disable the interrupt: IER[FCIE] = 0
- TCIE (Transfer Complete Interrupt Enable): Enables the transfer complete interrupt.
    - To enable the interrupt: IER[TCIE] = 1
    - To disable the interrupt: IER[TCIE] = 0
- TEIE (Transmit Error Interrupt Enable): Enables the transmit error interrupt.
    - To enable the interrupt: IER[TEIE] = 1
    - To disable the interrupt: IER[TEIE] = 0
- REIE (Receive Error Interrupt Enable): Enables the receive error interrupt.
    - To enable the interrupt: IER[REIE] = 1
    - To disable the interrupt: IER[REIE] = 0
- DMIE (Data Match Interrupt Enable): Enables the data match interrupt.
    - To enable the interrupt: IER[DMIE] = 1
    - To disable the interrupt: IER[DMIE] = 0

DMA Enable Register (DER) (Page 2872, Section 70.6.1.7)

The DMA Enable Register (DER) enables the DMA data flow:

- TDDE (Transmit Data DMA Enable): Enables the transmit data DMA.

    - To enable DMA for transmit data: DER[TDDE] = 1
    - To disable DMA for transmit data: DER[TDDE] = 0
- RDDE (Receive Data DMA Enable): Enables the receive data DMA.
    - To enable DMA for receive data: DER[RDDE] = 1
    - To disable DMA for receive data: DER[RDDE] = 0

Configuration 0 Register (CFGR0) (Page 2873, Section 70.6.1.8)

The Configuration 0 Register (CFGR0) fields to configure LPSPI:

- HREN (Host Request Enable): Enables LPSPI to start a new SPI bus transfer only if the host request input is asserted.
    - To enable host request: CFGR0[HREN] = 1
    - To disable host request: CFGR0[HREN] = 0
- HRPOL (Host Request Polarity): Specifies the polarity of the host request pin or input trigger.
    - To set active high: CFGR0[HRPOL] = 0
    - To set active low: CFGR0[HRPOL] = 1
- HRSEL (Host Request Select): Specifies the source of the host request input.
    - To select HREQ pin: CFGR0[HRSEL] = 0
    - To select input trigger: CFGR0[HRSEL] = 1
- HRDIR (Host Request Direction): Specifies the direction of the HREQ pin.
    - To set as input: CFGR0[HRDIR] = 0
    - To set as output: CFGR0[HRDIR] = 1
- CIRFIFO (Circular FIFO Enable): Enables circular FIFO.
    - To enable circular FIFO: CFGR0[CIRFIFO] = 1
    - To disable circular FIFO: CFGR0[CIRFIFO] = 0
- RDMO (Receive Data Match Only): Enables receive data match.
    - To enable receive data match: CFGR0[RDMO] = 1
    - To disable receive data match: CFGR0[RDMO] = 0

Configuration 1 Register (CFGR1) (Page 2875, Section 70.6.1.9)

The Configuration 1 Register (CFGR1):

- MASTER (Controller Mode): Specifies the LPSPI operating mode.
    - To set as Peripheral mode: CFGR1[MASTER] = 0
    - To set as Controller mode: CFGR1[MASTER] = 1
- SAMPLE (Sample Point): Specifies the SCK clock edge on which LPSPI samples input data.
    - To sample on SCK edge: CFGR1[SAMPLE] = 0
    - To sample on delayed SCK edge: CFGR1[SAMPLE] = 1
- AUTOPCS (Automatic PCS): Enables automatic PCS generation.
    - To enable automatic PCS: CFGR1[AUTOPCS] = 1
    - To disable automatic PCS: CFGR1[AUTOPCS] = 0

- NOSTALL (No Stall): Disables the feature that causes LPSPI to stall transfers when the transmit FIFO is empty or the receive FIFO is full.
    - To enable no stall: CFGR1[NOSTALL] = 1
    - To disable no stall: CFGR1[NOSTALL] = 0
- PARTIAL (Partial Enable): Specifies whether LPSPI stores a partial received word in the receive FIFO or