

# AICD Lab Task PGA

**Group no. 05**

**Course Semester: SoSe 2023**

**Supervisor: Markus Graber**

**Department: Integrierte Elektronische Systeme (IES)**

Advanced Integrated Circuit Design Lab Report by

Huanzheng Zhu, 2888479

Jingang Zhang, 2705413

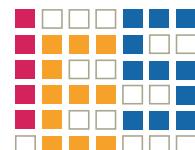
**Prof. Dr.-Ing. Klaus Hofmann**

Darmstadt



TECHNISCHE  
UNIVERSITÄT  
DARMSTADT

Electrical Engineering and  
Information Technology  
Department



# Contents

<b>1</b>	<b>Introduction</b>	.	.	.	<b>4</b>
<b>2</b>	<b>Inverter</b>	.	.	.	<b>5</b>
2.1	Discussion and Design	.	.	.	5
2.2	Schematic	.	.	.	5
2.3	Layout	.	.	.	6
2.4	Waveform	.	.	.	6
<b>3</b>	<b>CMOS-Switch</b>	.	.	.	<b>8</b>
3.1	Discussion and Design	.	.	.	8
3.2	Schematic	.	.	.	8
3.3	Layout	.	.	.	9
3.4	Waveform	.	.	.	10
<b>4</b>	<b>3-Input NAND Gate</b>	.	.	.	<b>11</b>
4.1	Discussion and Design	.	.	.	11
4.2	Schematic	.	.	.	11
4.3	Layout	.	.	.	12
4.4	Post Layout Simulation	.	.	.	13
<b>5</b>	<b>3:8 Multiplexer</b>	.	.	.	<b>14</b>
5.1	Discussion and Design	.	.	.	14
5.2	Schematic	.	.	.	14
5.3	Layout	.	.	.	15
5.4	Post Layout Simulation	.	.	.	16
<b>6</b>	<b>Operational Amplifier (OPAMP)</b>	.	.	.	<b>17</b>
6.1	Discussion and Design	.	.	.	17
6.2	Schematic of OPAMP	.	.	.	17
6.3	Layout of OPAMP	.	.	.	18
6.4	Simulated Waveforms	.	.	.	18
6.5	Schematic vs Post-Layout simulation	.	.	.	20
<b>7</b>	<b>Low Pass Filter</b>	.	.	.	<b>22</b>
7.1	Discussion and Design	.	.	.	22
7.2	Schematic of Low Pass Filter	.	.	.	22
7.3	Layout of Low Pass Filter	.	.	.	23
7.4	Waveform of LPF's Bandwidth	.	.	.	23

---

<b>8 Programmable Gain Amplifier</b>	25
8.1 Discussion and Design	25
8.2 Schematic of PGA	25
8.3 Layout of PGA	26
8.4 Schematic vs Post-Layout simulation	26
<b>9 Summary</b>	27

# 1 Introduction

---

This report focuses on demonstrating how we use Cadence Virtuoso [1], under the guidance of our tutors and with detailed tutorials, for the design and simulation of a programmable gain amplifier (PGA). Based on the progress of the lab, we first designed the schematic and symbol for all individual sub-circuits of the PGA, including inverters, operational amplifiers (OPAMP), and CMOS switches, using electronic components from the UMC65II library. Next, we performed a simulation verification for each sub-circuit using a testbench. Once the simulation met the required specifications, we used our designed sub-circuits along with the electronic components from the UMC65II library for the design, simulation, and verification of the PGA and the low-pass filter (LPF). After the schematic simulation of the PGA met the requirements, we designed the corresponding layout for each sub-circuit based on the specifications and dimensions from the schematic, and conducted post-layout simulation for each sub-circuit. Once the layout of each sub-circuit met the requirements, we assembled them for the PGA layout design and performed post-layout simulation for the entire PGA. By following this standardized design flow, we significantly increase the likelihood of meeting the design requirements, reduce development time, and minimize errors during the design process.

In the following chapters, we will discuss the design principles of each individual sub-circuit comprising the PGA in separate sections. We will demonstrate our corresponding achievements by presenting the schematic, layout, waveform of each circuit.

## 2 Inverter

### 2.1 Discussion and Design

Combining the first tutorial and Professor Hofmann's lecture slides on ADICD, Chapter 5 provides a detailed introduction to the Complementary Metal-Oxide-Semiconductor (CMOS) inverter. We chose a CMOS inverter composed of a pMOS and an nMOS to avoid static power consumption. Since  $\mu_n/\mu_p = 2.5$ , we selected the sizes of the pMOS and nMOS to achieve complete symmetry in the voltage transfer function and balance the performance of both components. The chosen dimensions are:  $(w/l)_p = 1.2 \mu\text{m}/240 \text{ nm} = 5$ ,  $(w/l)_n = 480 \text{ nm}/240 \text{ nm} = 2$ . However, in practical simulations, there is a slight deviation from the theoretical results, which can be observed in the section 3.4 waveform.

### 2.2 Schematic

The figure 3.1 below shows the schematic of the inverter!

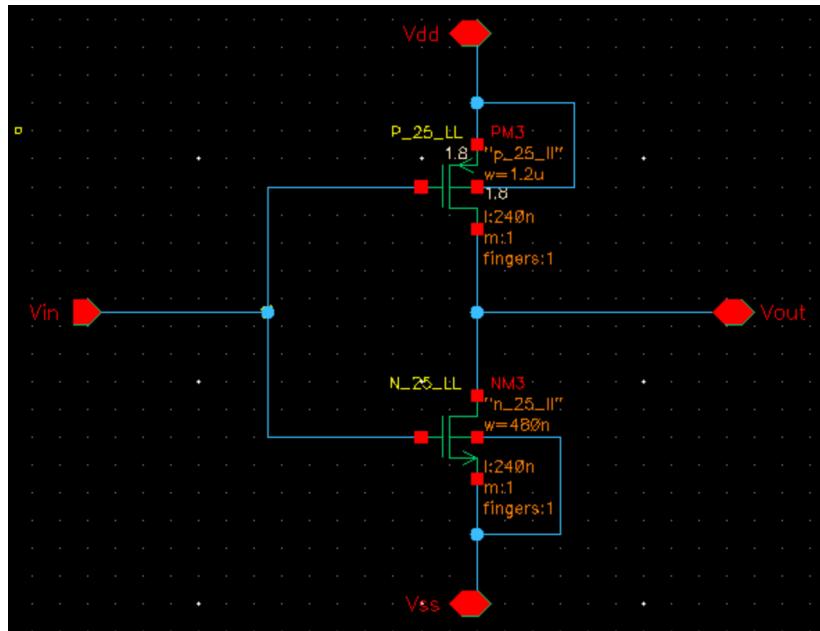


Figure 2.1: Schematic of Inverter

## 2.3 Layout

The figure 2.2 below shows the layout of the inverter. The layout design process is a simple "schematic-driven" approach. The layout of the inverter has a width of  $2.52\mu\text{m}$  and a height of  $5.29\mu\text{m}$ . By calculation, its approximate area is  $13.33\mu\text{m}^2$ .

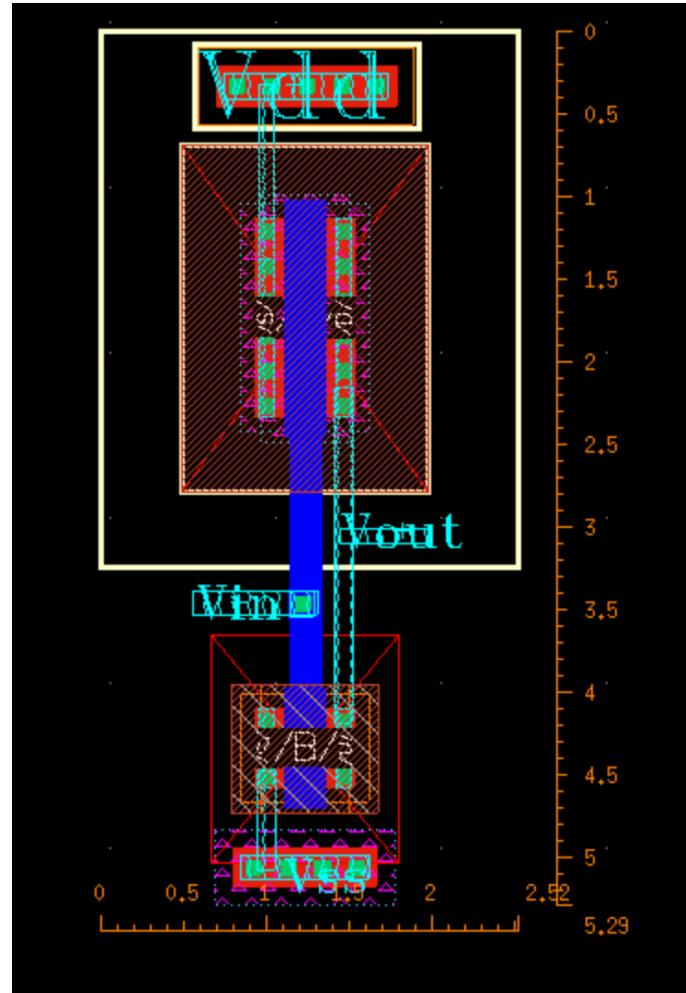
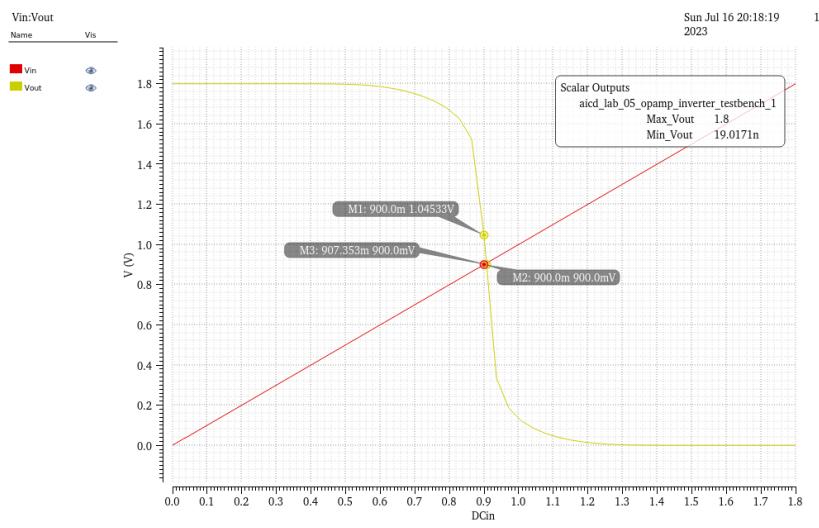


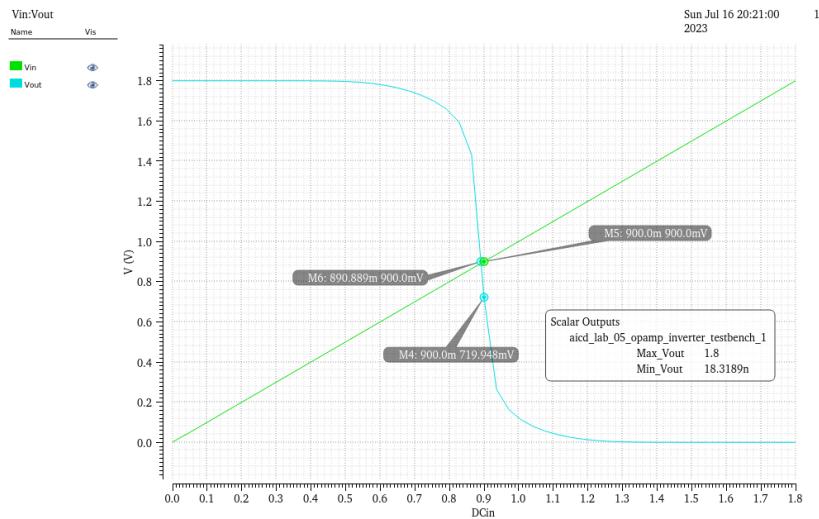
Figure 2.2: Layout of Inverter

## 2.4 Waveform

From the figure 2.3 below, it can be observed that due to the additional parasitic capacitance and resistance introduced by the layout, there are differences in the Vout curves between the two waveforms, despite both being approximately symmetric inverters.



(a) The waveform of the inverter's schematic.



(b) The waveform of the inverter's layout.

Figure 2.3: Comparison of the waveform between the inverter's schematic simulation and post layout simulation

# 3 CMOS-Switch

---

## 3.1 Discussion and Design

---

The design of the CMOS switch is based on the previously introduced inverter and a combination of pMOS and nMOS transistors, forming a CMOS transmission gate (referenced from Professor Hofmann's lecture slides on ADICD, Chapter 8). To achieve an acceptable low on-resistance  $R_{on}$  and an acceptable high off-resistance  $R_{off}$  for the CMOS switch, according to Equation 3.1 [2], it can be observed that as the effective channel width (W) increases, the W/L ratio increases. This leads to a lower on-resistance ( $R_{on}$ ). According to the description of Equation 3.2 in the AICD lecture slides (Chapter 3), in the cutoff state of a CMOS switch, the off-resistance tends to infinity.

$$R_{on} = \frac{1}{K'_n \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})} \quad (3.1)$$

$$I_{off} = 0, \quad R_{off} = \frac{1}{I_{off} \cdot \lambda} = \infty \quad (3.2)$$

So, we chose to design the pMOS and nMOS with the maximum W/L ratio, which is 50 $\mu$ m/240nm (constrained by the UMC65II library).

## 3.2 Schematic

---

The figure 3.1 below shows the schematic of the CMOS-Switch. When the control pin is set to a high voltage (1.8V), the CMOS switch is turned on, and  $V_{in} = V_{out}$ . When the control pin is set to a low voltage (0V), the CMOS switch is turned off, and  $V_{out} = 0$ .

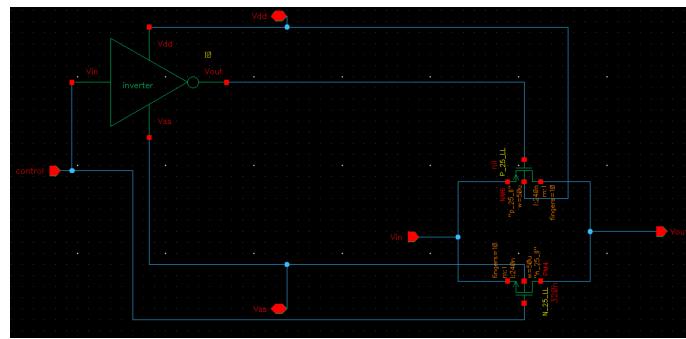


Figure 3.1: Schematic of CMOS-Switch

### 3.3 Layout

The figure 3.2 below shows the layout of the CMOS-Switch. The layout design process is a simple "schematic-driven" approach. The layout of the CMOS-Switch has a width of  $10.225\mu\text{m}$  and a height of  $13.79\mu\text{m}$ . By calculation, its approximate area is  $141\mu\text{m}^2$ .

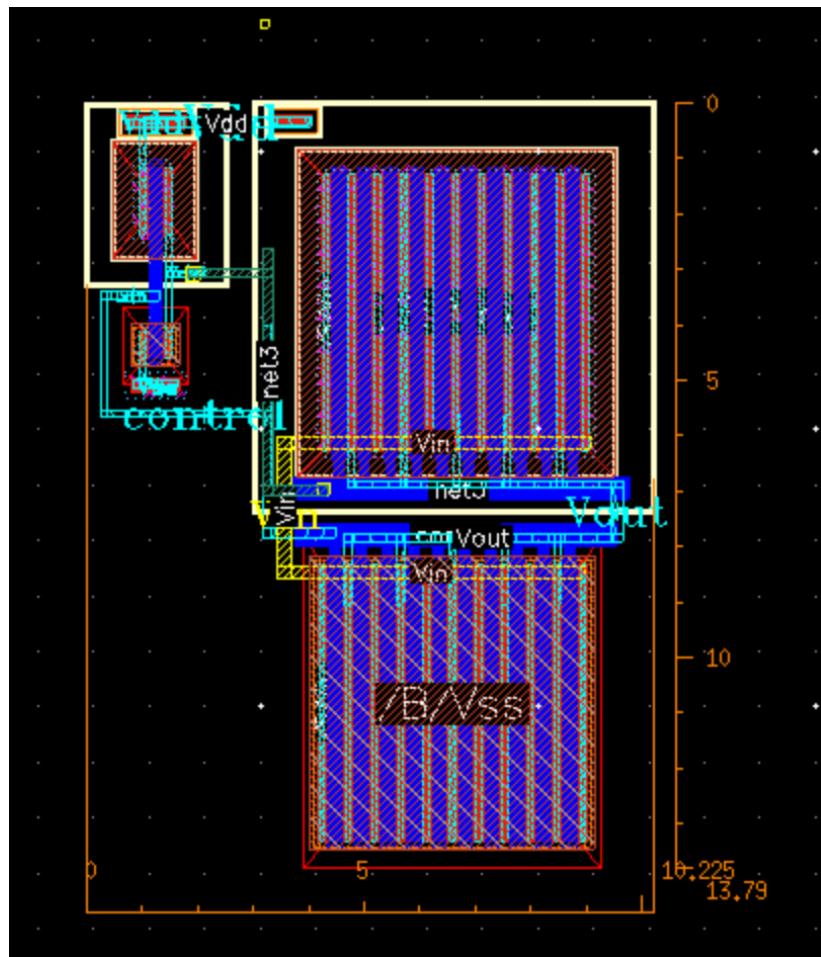


Figure 3.2: Layout of CMOS-Switch

### 3.4 Waveform

The waveform 3.3 below represents the circuit analysis of the CMOS-switch post layout simulation. From the figure, we can observe that  $R_{on}$  gradually increases at a slower rate as the input voltage  $V_{in}$  increases. Simultaneously,  $R_{off}$  gradually decreases as  $V_{in}$  increases. The maximum value of  $R_{on}$  is approximately 198  $\Omega$ , while the minimum value of  $R_{off}$  is around 9 G $\Omega$ . We have also concluded that the CMOS-switch meets the requirements.

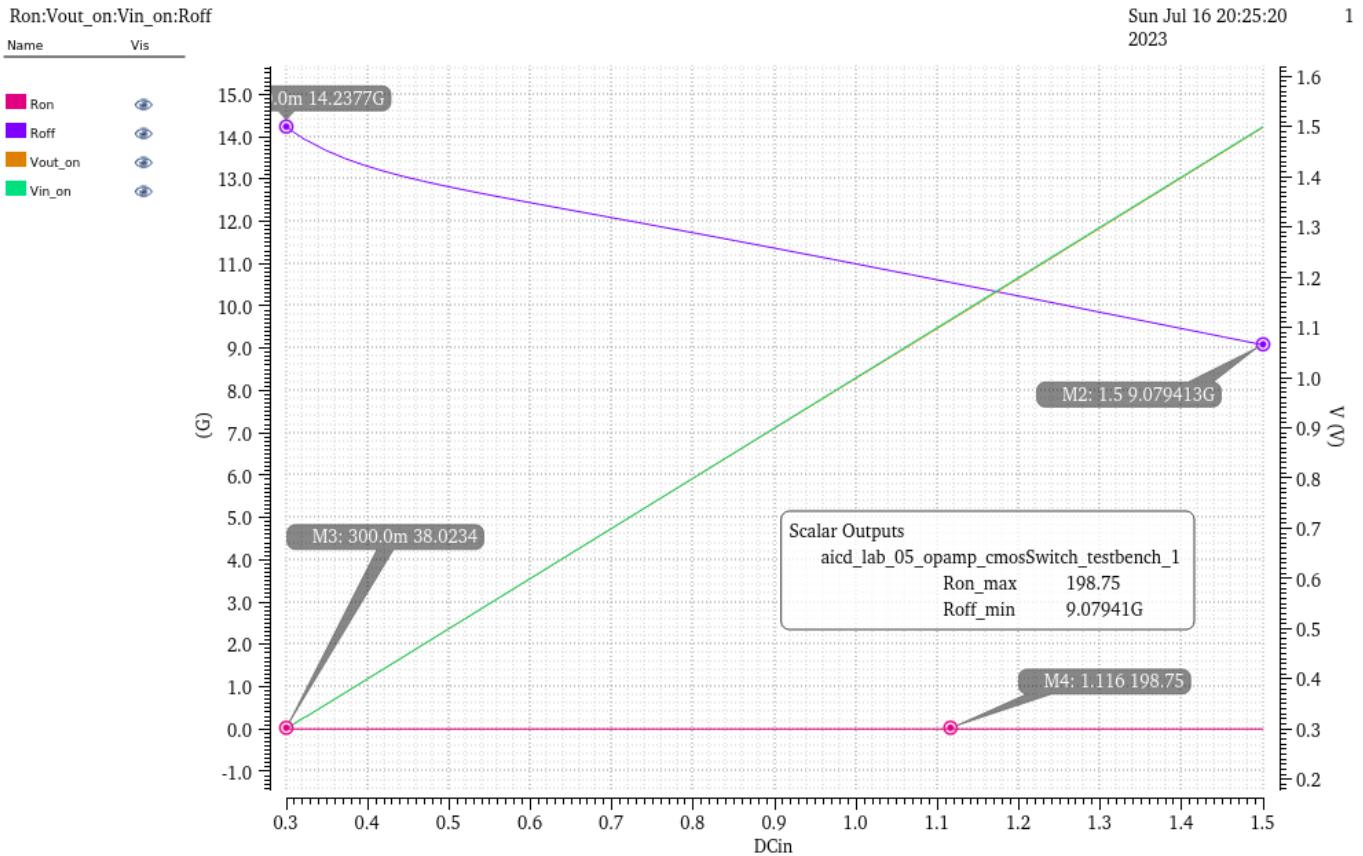


Figure 3.3: Waveform of CMOS-Switch

# 4 3-Input NAND Gate

## 4.1 Discussion and Design

According to the description of CMOS in Chapter 7 of the ADIC script, the 3-input NAND gate should be designed using 3 pMOS transistors with a width-to-length ratio ( $w/l$ ) of 5/1 in parallel and 3 nMOS transistors with a  $w/l$  ratio of 6/1 in series. This configuration theoretically achieves a balanced performance for all MOS transistors. However, due to oversight and time constraints, we used nMOS transistors with a  $w/l$  ratio of 2/1. While this sacrifices some MOS transistor's performance and causes increased logic propagation delay, we still obtain the correct logic result:  $V_{out} = \neg A \& \neg B \& \neg C$  and save the chip area.

## 4.2 Schematic

The schematic 4.1 below represents a 3-input NAND gate. Its working logic is based on the series connection of three inverters. In other words,  $V_{out}$  will be logic 0 only when all three inputs,  $A$ ,  $B$ , and  $C$ , are logic 1. In all other cases,  $V_{out}$  will be logic 1. This behavior can be observed in the section 4.4.

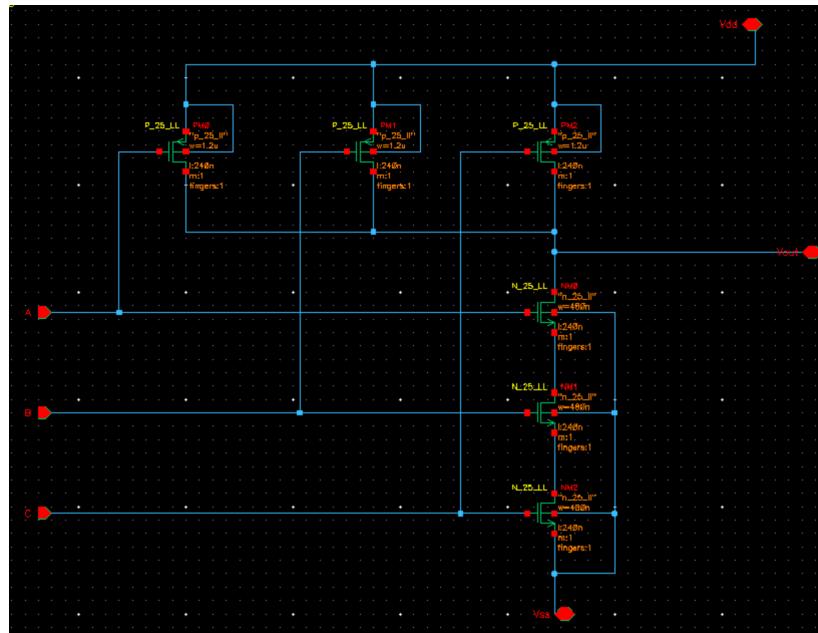


Figure 4.1: Schematic of 3-Input NAND Gate

## 4.3 Layout

The figure 4.2 below shows the layout of the 3-input NAND gate. The layout design process is a simple "schematic-driven" approach. The layout of the 3-input NAND gate has a width of  $7.59\mu\text{m}$  and a height of  $10.08\mu\text{m}$ . By calculation, its approximate area is  $76.46\mu\text{m}^2$ . The area can be further reduced by using Interdigitated Layout and other methods. However, due to time constraints, unfortunately, we won't be able to complete it.

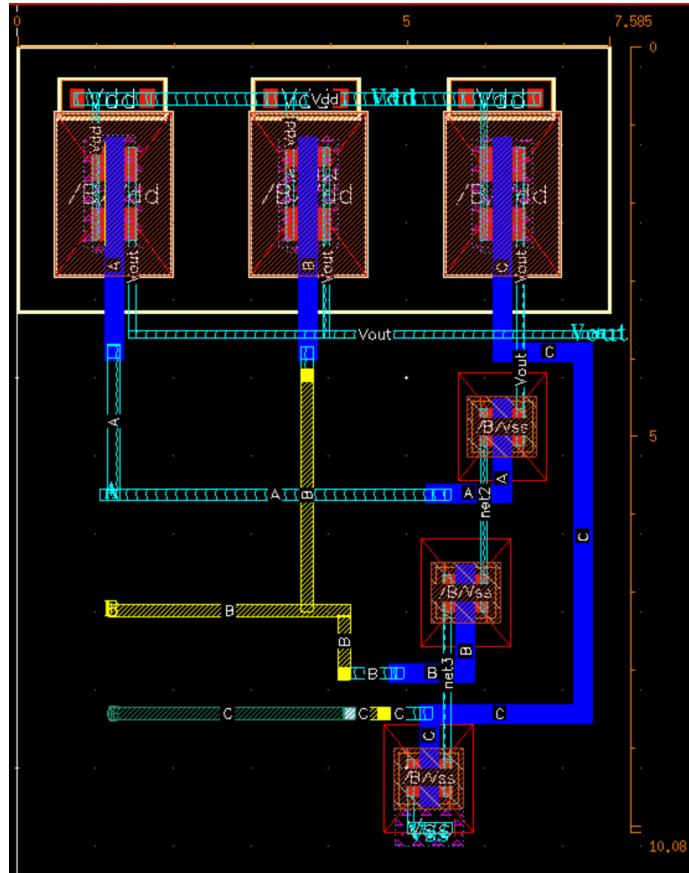


Figure 4.2: Layout of 3-Input NAND Gate

---

## 4.4 Post Layout Simulation

---

The table 4.1 below shows the output results of post layout simulation of a 3-input NAND gate. From the results, it can be verified that this NAND gate fully meets the requirements ( $V_{out} = 1.8V$  represents logic 1,  $V_{out} = 169.5\text{ nV}$  approximately equals 0 representing logic 0).

Table 4.1: Results by post layout simulation for 3-input NAND gate

Inputs ABC	$V_{out}$ [V]
000	1.8
001	1.8
010	1.8
011	1.8
100	1.8
101	1.8
110	1.8
111	169.5E-9

# 5 3:8 Multiplexer

---

## 5.1 Discussion and Design

---

Based on the table 5.1 below, we can see that the 3:8 multiplexer has the function of generating 8 different logic signal combinations from the 3 inputs,  $B_2B_1B_0$ , where each combination corresponds to a specific output logic signal. Therefore, we first need three inverters, each generating a 0 or 1 for the input logic signals (for example, the input 0 results in an output of 1, and vice versa). Then, we require eight 3-input AND gates (constructed by connecting a 3-input NAND gate with an inverter) to receive the 8 different logic signal combinations and produce the corresponding unique output logic signal 1. For example, when  $B_2B_1B_0$  is 110, we connect the logic signal  $B_2B_1!B_0$  (111) to the corresponding 3-input AND gate, resulting in a unique output logic signal where  $S_6$  is 1, while all other output logic signals are 0. This process is repeated for all the combinations.

Table 5.1: The truth table for 3:8 multiplexer

$B_2B_1B_0$	$S_7S_6S_5S_4S_3S_2S_1S_0$
000	00000001
001	00000010
010	00000100
011	00001000
100	00010000
101	00100000
110	01000000
111	10000000

## 5.2 Schematic

---

As shown in the figure 5.1 below, the circuit of a 3:8 multiplexer is composed of three previously created inverters and eight 3-input AND gates. Each 3-input AND gate is formed by connecting a previously created 3-input NAND gate and an inverter in series.

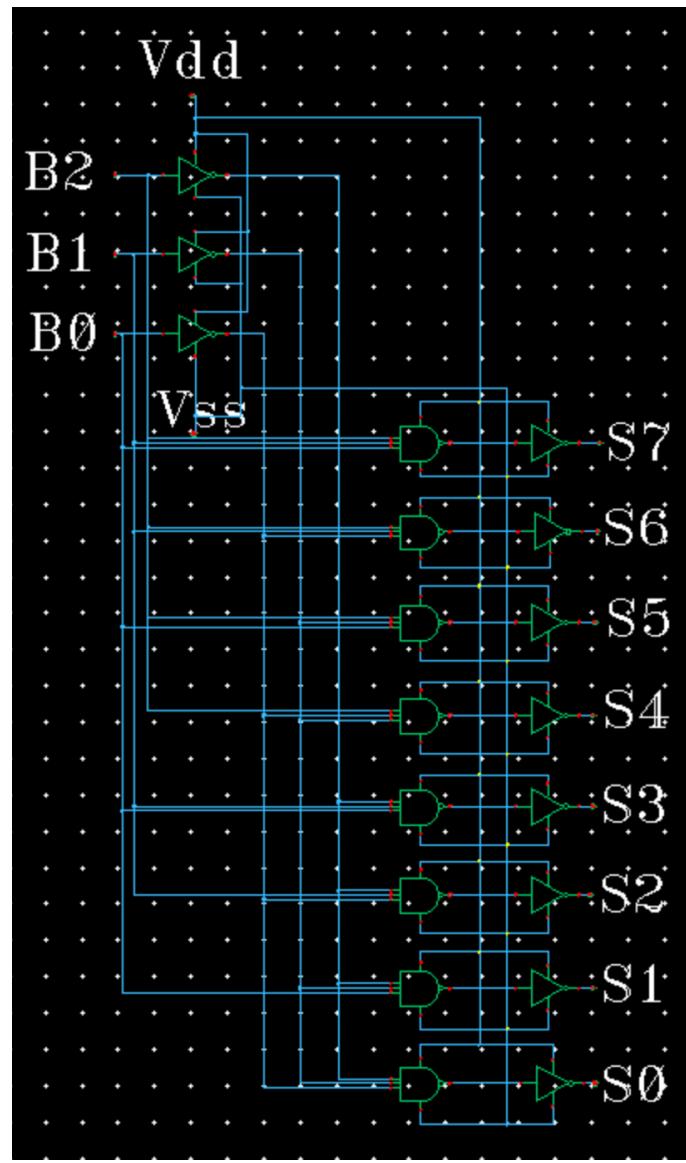


Figure 5.1: Schematic of 3:8 Multiplexer

### 5.3 Layout

The figure 5.2 below shows the layout of 3:8 Multiplexer. The layout design process is a simple "schematic-driven" approach. The layout of the 3:8 Multiplexer has a width of  $94.795\mu\text{m}$  and a height of  $13.42\mu\text{m}$ . By calculation, its approximate area is  $1272\mu\text{m}^2$

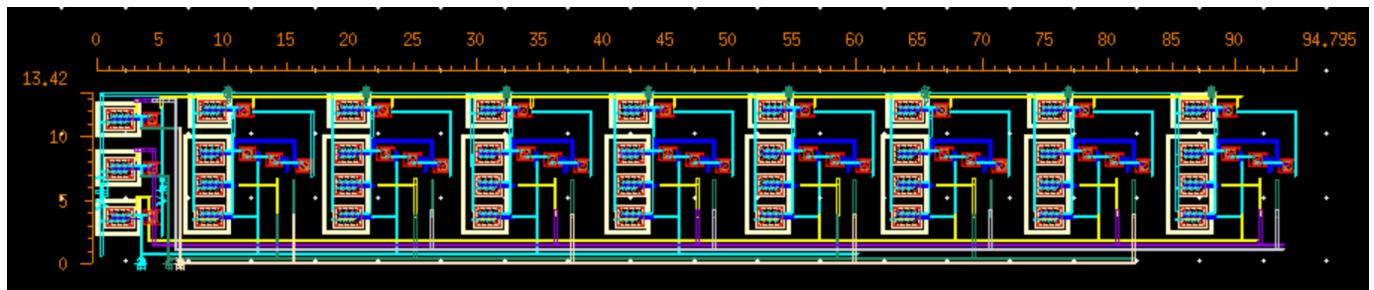


Figure 5.2: Layout of 3:8 Multiplexer

## 5.4 Post Layout Simulation

From the table 5.2 below, we can see that all the output signals of the 3:8 multiplexer match those in the previous table 5.1. In this table, a voltage of 1.8V represents a logic 1, while voltages ranging from 18.74nV to 18.81nV represent a logic 0.

Table 5.2: Results of post layout simulation for the 3:8 Multiplexer

$B_2B_1B_0$	$S_7$ [V]	$S_6$ [V]	$S_5$ [V]	$S_4$ [V]	$S_3$ [V]	$S_2$ [V]	$S_1$ [V]	$S_0$ [V]
000	18.74n	18.77n	18.79n	18.80n	18.80n	18.81n	18.81n	1.8
001	18.74n	18.78n	18.80n	18.80n	18.81n	18.81n	1.8	18.81n
010	18.74n	18.77n	18.79n	18.79n	18.8n	1.8	18.8n	18.81n
011	18.74n	18.77n	18.79n	18.8n	1.8	18.8n	18.8n	18.79n
100	18.74n	18.78n	18.79n	1.8	18.8n	18.8n	18.79n	18.8n
101	18.74n	18.78n	1.8	18.8n	18.8n	18.79n	18.8n	18.79n
110	18.74n	1.8	18.79n	18.79n	18.79n	18.79n	18.79n	18.78n
111	1.8	18.77n	18.79n	18.79n	18.79n	18.79n	18.79n	18.78n

# 6 Operational Amplifier (OPAMP)

## 6.1 Discussion and Design

The input stage of operational amplifier consists of a differential input pair loaded with transistor NMOS M1 and M2, and a common-source amplifier composed of a current mirror across PMOS M3 and M4. NMOS M5 provides a constant bias current for this input stage. The output stage amplifier circuit is composed of M6 and M7. M6 is a common source amplifier, and M7 provides a constant bias current for it and acts as a second-stage output load. The phase compensation circuit is composed of R2 and Cc. R2 is connected between the output of the input stage and the input of the out stage together with the capacitor Cc to form RC Miller compensation. The bias circuit is composed of R1 and NMOS M8.

In another words, M1 and M2 are the first differential transconductance stage that convert differential input voltages into differential currents. M3 and M4 are the first stage loads, which restore the differential mode current to differential mode voltage. M6 is the second transconductance stage, which converts the differential voltage signal into a current, and M7 converts the current signal into a voltage output.

The table 6.1 and 6.2 below shows the parameters of the designed OPAMP. Through the comparison of the tables, it can be seen that there are obvious differences between the manual calculation and the actual design parameters.

Table 6.1: hand calculation

	W/L	W in $\mu\text{m}$	L in $\mu\text{m}$	$L/L_{min}$	
$M_{1/2}$	30.55	11	0.36	1.5	$M_{1/2}$
$M_{3/4}$	31.11	11.2	0.36	1.5	$M_{3/4}$
$M_5$	68.75	16.5	0.24	1	$M_5$
$M_6$	75.83	18.2	0.24	1	$M_6$
$M_7$	63.33	15.2	0.24	1	$M_7$
$M_8$	54.58	13.1	0.24	1	$M_8$
$C_c$ in pF	$I_8$ in $\mu\text{A}$	$I_5$ in $\mu\text{A}$	$I_7$ in $\mu\text{A}$		
1.32	52.8	52.8	75.99		

Table 6.2: schematic design

	W/L	W in $\mu\text{m}$	L in $\mu\text{m}$	$L/L_{min}$
$M_{1/2}$	50	18	0.36	1.5
$M_{3/4}$	9.92	7.14	0.72	3
$M_5$	10	2.4	0.24	1
$M_6$	200	48.125	0.24	1
$M_7$	83.33	20	0.24	1
$M_8$	10	2.4	0.24	1
$C_c$ in pF	$R_1$ in $\text{k}\Omega$	$R_2$ in $\text{k}\Omega$		
0.36	49.98	5.99		

## 6.2 Schematic of OPAMP

The figure 6.1 below shows the schematic of the OPAMP.

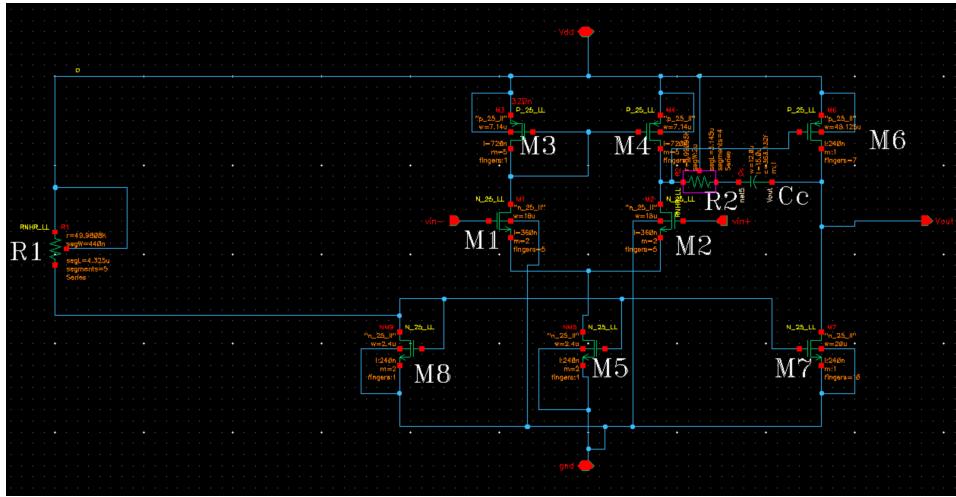


Figure 6.1: Schematic of OPAMP

### 6.3 Layout of OPAMP

When designing layout, we use Interdigitated layout for active load  $M_{3/4}$  and current mirror  $M_{9/5}$ , then use Common centroid layout for differential input  $M_{1/2}$ , which can reduce effects of process variation and mismatch, save space, and effectively reduce noise. The figure 6.2 below shows the layout of the OPAMP. The layout of the OPAMP has a width of  $20.06\mu\text{m}$  and a height of  $46.6\mu\text{m}$ . By calculation, its approximate area is  $934.8\mu\text{m}^2$ .

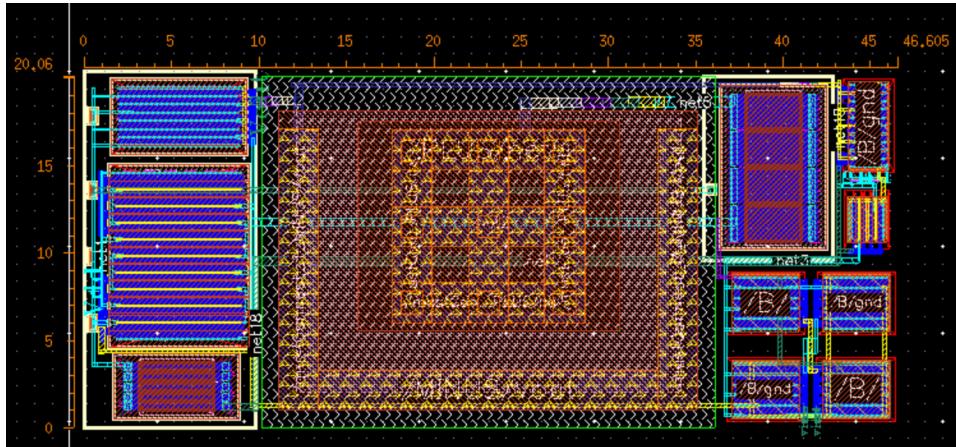


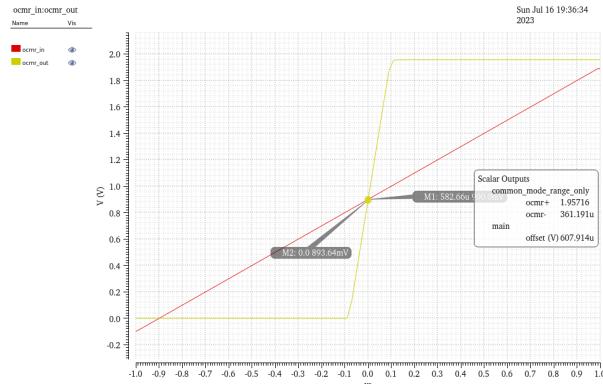
Figure 6.2: Layout of OPAMP

### 6.4 Simulated Waveforms

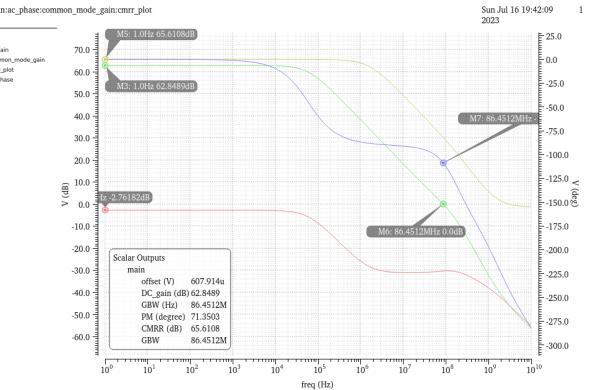
In the figure 6.3(a), it can be observed that the input offset voltage leads to an output voltage equal to zero (bias voltage of  $0.9\text{V}$ ). From Figure 6.3(b), we can observe the values of DC Gain, GBW (Gain-Bandwidth),



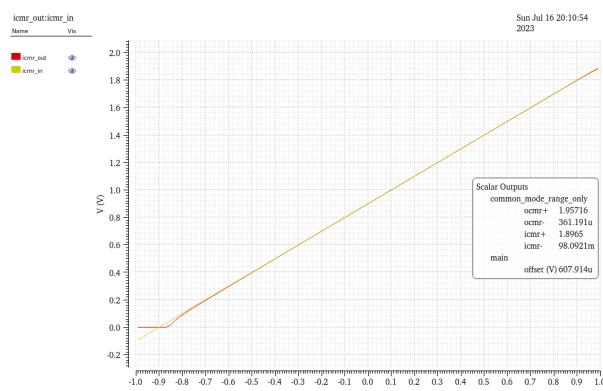
PM (Phase Margin), and CMRR (Common Mode Rejection Ratio). By examining the ICMR (Input Common Mode Range) in Figure 6.3(c) and the voltage swing in Figure 6.3(d), it can be determined that the OPAMP can function as a unit-gain buffer. The SR+ (Rising Slew Rate) and SR- (Falling Slew Rate) in Figures 6.3(e) and 6.3(f) represent the maximum speed at which the OPAMP can charge or discharge its load. In Figure 6.3(g), it can be observed that the input noise decreases gradually as the frequency increases.



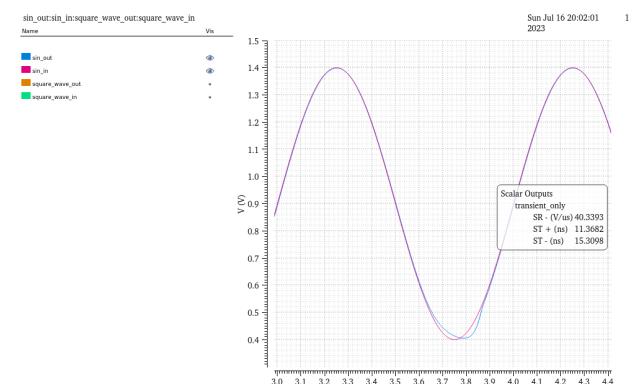
(a) Input Offset Voltage Measurement



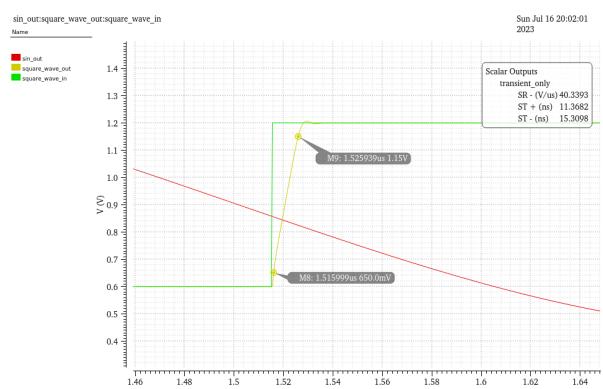
(b) Transfer function (DC gain, GBW, PM, CMRR)



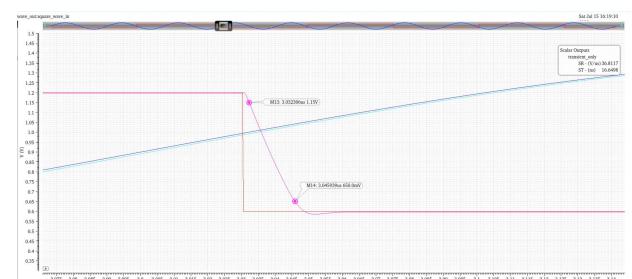
(c) ICMR



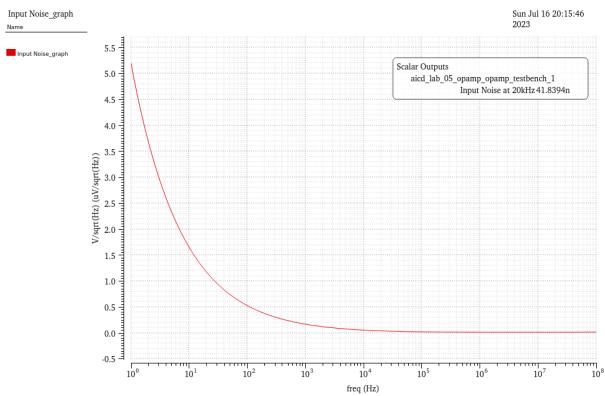
(d) Voltage swing



(e) Rising Slew Rate



(f) Falling Slew Rate



(g) Input Referred Noise

Figure 6.3: The relevant parameters of OPAMP

## 6.5 Schematic vs Post-Layout simulation

The following tables list the comparison of the simulation results of the schematic and post layout parameters.

Table 6.3: OPAMP parameters for  $C_L = 2 \text{ pF}$ , typical corner

Parameter	Specification	Schematic	Post Layout
DC Gain [dB]	$> 50$	62.85	62.79
GBW [MHz]	$\geq 20$	86.45	74.82
Phase Margin [Grad]	$\geq 50$	71.35	66.47
CMRR [dB]	$> 60$	65.61	73.53
Slew Rate(+ve/-ve)[V/ $\mu$ s]	$\geq 15, 15$	50.15/40.16	46.7/36.37
Settling Time (high/low) @5% error [ns]	$\leq 500, 500$	11.42/15.38	12.1/16.85
Input Offset [mV]	$\leq 5$	0.607	2.568
Input Referred Noise @ 20 kHz [nV/ $\sqrt{Hz}$ ]	$\leq 55$	41.83	42.26
Power [mW]	$\leq 0.6$	0.334	0.296
Area [ $\mu\text{m}^2$ ]	—	—	934.9

Table 6.4: OPAMP corner analysis post layout (Schematic) results for  $C_L = 2 \text{ pF}$

Parameter	Specification	Typical	Min	Max	Passed Corner /All Corner
DC Gain [dB]	$> 50$	62.79(62.85)	60.79(60.72)	64.12(64.26)	100%
GBW [MHz]	$\geq 20$	74.82(86.45)	39.51(44.79)	141.7(169.2)	100%
Phase Margin [Grad]	$\geq 50$	66.47(71.35)	55.02(60.01)	77.56(82.13)	100%
Slew Rate(+ve)[V/ $\mu\text{s}$ ]	$\geq 15, 15$	46.7(50.15)	22.45(24.76)	90.01(94.18)	100%
Slew Rate(-ve)[V/ $\mu\text{s}$ ]	$\geq 15, 15$	36.37(40.16)	15.08(16)	67.53(76.16)	100%
Settling Time (high) @5% error [ns]	$\leq 500, 500$	12.1(11.42)	6.51(6.282)	24.65(22.68)	100%
Settling Time (low) @5% error [ns]	$\leq 500, 500$	16.85(15.38)	10.09(8.94)	42.22(41.12)	100%
Input Offset [mV]	$\leq 5$	2.568(0.607)	2.166(0.221)	3.016(1.058)	100%

Table 6.5: OPAMP Monte-Carlo analysis post layout (Schematic) for  $C_L = 2 \text{ pF}$

Parameter	Specification	Min	Max	Mean	Std Dev	Yield (%) (500/500)
DC Gain [dB]	$> 50$	61.5(61.55)	64.09(64.13)	62.81(62.84)	414m(414.8m)	100
GBW [MHz]	$\geq 20$	40.38(48.94)	123.9(133.7)	75.75(87.61)	12.93(15.67)	100
Phase Margin [Grad]	$\geq 50$	55.85(61.59)	74.38(77.57)	66.11(70.87)	2.99(3.038)	100
Slew Rate(+ve)[V/ $\mu\text{s}$ ]	$\geq 15, 15$	25.96(26.12)	81.62(84.97)	47.54(50.99)	8.246(8.737)	100
Slew Rate(-ve)[V/ $\mu\text{s}$ ]	$\geq 15, 15$	21.19(21.15)	51.41(65.26)	36.75(40.38)	5.575(6.419)	100
Settling Time (high) @5% error [ns]	$\leq 500, 500$	7.151(6.935)	21.42(21.49)	12.26(11.56)	2.092(1.961)	100
Settling Time (low) @5% error [ns]	$\leq 500, 500$	11.97(9.513)	28.74(28.85)	17.64(15.72)	2.993(2.615)	100
Input Offset [mV]	$\leq 5$	-6.256(-8.686)	10.38m(10.36m)	2.566(629.5u)	2.978m(3.015m)	78.8(89.6)

# 7 Low Pass Filter

## 7.1 Discussion and Design

As a part of programmable Gain Amplifier(PGA), a low-pass filter (LPF) is a filter that passes signals with a frequency lower than a selected cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency. Our designed low pass filter consists of 1 OPAMP, 1 cmosSwitch, 2 resistors and 1 capacitor. The gain of the operational amplifier is approximately 1 ( $R_2/R_1$ ) by adjusting the values of the two resistors. According to the specifications, the Low Pass Filter (LPF) needs to achieve a Filter Bandwidth (cut-off frequency) of 100MHz. Based on the formula  $BW = \frac{1}{2\pi R_2 C}$ , we have chosen the values of 1M Ohm for  $R_2$  and approximately 1.6pF for the capacitor. This choice is made in order to minimize the size of the capacitor and reduce the chip's area during layout.

## 7.2 Schematic of Low Pass Filter

The figure 7.1 below shows the schematic of the low pass filter.

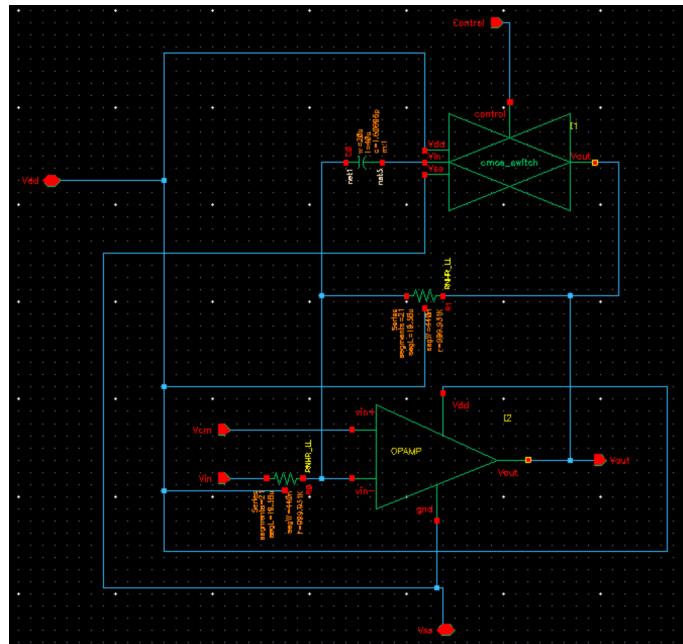


Figure 7.1: Schematic of LPF

## 7.3 Layout of Low Pass Filter

The figure 7.2 below shows the layout of the low pass filter. The layout of the low pass filter has a width of  $75.955 \mu\text{m}$  and a height of  $51.425 \mu\text{m}$ . By calculation, its approximate area is  $3906 \mu\text{m}^2$ .

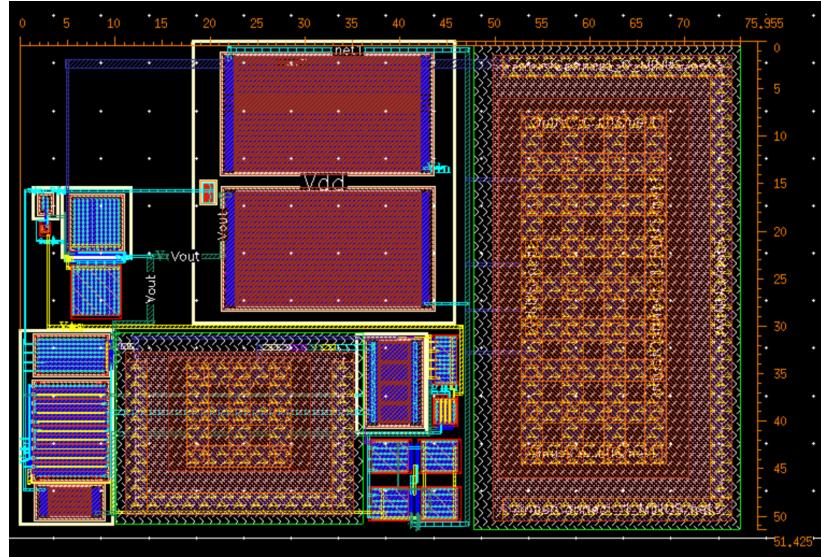


Figure 7.2: Layout of LPF

## 7.4 Waveform of LPF's Bandwidth

According to the below figure 7.3, in the post layout simulation of the design, the obtained Filter Bandwidth is 99.155 KHz, and the Bandwidth Tolerance is 1.62%. This means that the design requirements have been met.

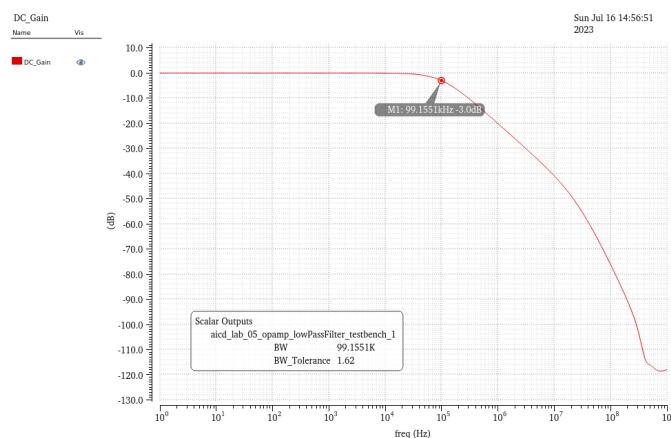


Figure 7.3: Waveform of LPF's Bandwidth

# 8 Programmable Gain Amplifier

## 8.1 Discussion and Design

A programmable-gain amplifier (PGA) is an electronic amplifier (typically based on an operational amplifier) whose gain can be controlled by external digital or analog signals. Based on the required gain specification and the formula  $R_2 = R_1 \cdot 10^{\frac{\text{Gain dB}}{20}}$ , where  $R_1 = 10\text{k}\Omega$ , we manually calculated the resistance values for the remaining resistors.

In our design, PGA consists of 1 OPAMP, 8 cmosSwitch, 1 Low Pass Filter and 1 3:8 Multiplexer. The input signal goes through the operational amplifier. The gain of operational amplifier is achieved through a resistive bridge. The number of gain resistors is determined by the multiplexer to achieve the corresponding gain requirements. The gained signal is passed through a low pass filter to remove low-frequency components.

## 8.2 Schematic of PGA

The figure 8.1 below shows the schematic of the PGA.

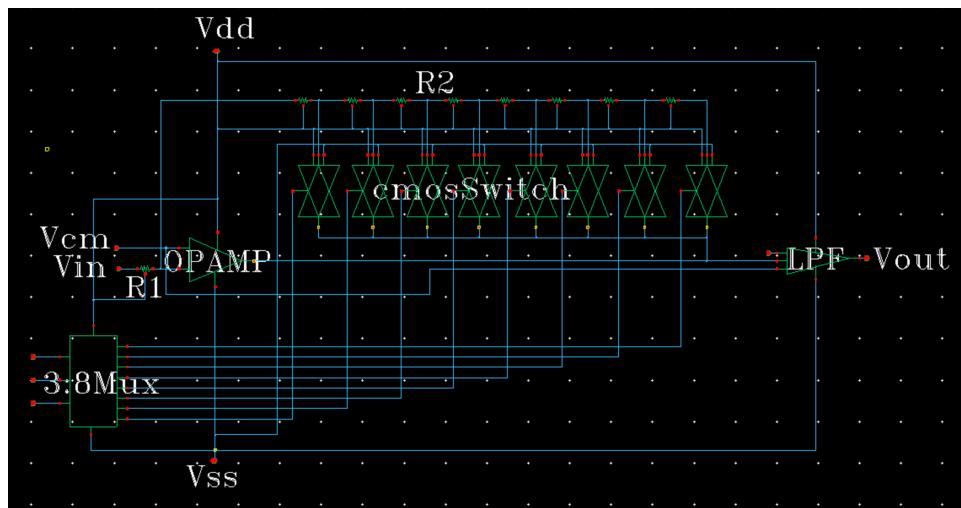


Figure 8.1: Schematic of PGA

## 8.3 Layout of PGA

The figure 8.2 below shows the layout of the PGA. The layout of the PGA has a width of  $194.9 \mu\text{m}$  and a height of  $51.25 \mu\text{m}$ . By calculation, its approximate area is  $9988 \mu\text{m}^2$ .

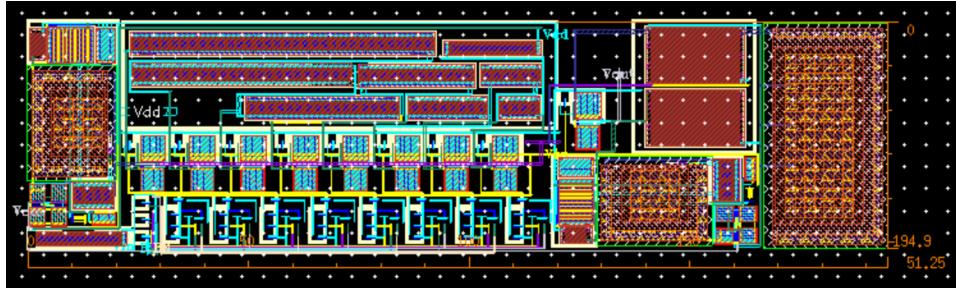


Figure 8.2: Layout of PGA

## 8.4 Schematic vs Post-Layout simulation

The following table 8.1 lists the comparison of the simulation results of the schematic and post layout parameters of PGA. Obviously, all the simulations indicate that the PGA has fully met the design requirements. Additionally, we have also confirmed that the parameters of Gain Differential Non-Linearity (DNL) and Gain Integral Non-Linearity (INL) are both below the specified threshold of 0.5.

Table 8.1: Corner and Monte carlo simulation post layout (Schematic)

Parameter	PGA Gain 000 (dB)	PGA Gain 001 (dB)	PGA Gain 010 (dB)	PGA Gain 011 (dB)	PGA Gain 100 (dB)	PGA Gain 101 (dB)	PGA Gain 110 (dB)	PGA Gain 111 (dB)
Specification Corner	0 $\pm 1.5$	3 $\pm 1.5$	6 $\pm 1.5$	9 $\pm 1.5$	12 $\pm 1.5$	15 $\pm 1.5$	18 $\pm 1.5$	21 $\pm 1.5$
Typical	147.1m(48.32m)	3.108(3.02)	6.091(6.003)	9.064(8.983)	12.06(11.98)	15.04(14.96)	18.02(17.94)	20.99(20.92)
Best Corner	92.47m(22.34m)	3.049(3.028)	6.026(6.036)	8.997(9.033)	11.99(12.04)	14.97(15.03)	17.94(18.02)	20.92(21)
Worst Corner	284.7m(173.9m)	3.231(3.135)	6.207(6.111)	9.172(9.085)	12.17(12.08)	15.14(15.06)	18.12(18.04)	21.1(21.01)
passed corner /all corner	all pass							
Specification Monte Carlo(for std)	0 $\pm 1.5$	3 $\pm 1.5$	6 $\pm 1.5$	9 $\pm 1.5$	12 $\pm 1.5$	15 $\pm 1.5$	18 $\pm 1.5$	21 $\pm 1.5$
Monte Carlo Min	109.4m(-14.53m)	3.007(2.924)	5.971(5.88)	8.905(8.829)	11.85(11.79)	14.82(14.77)	17.8(17.73)	20.78(20.72)
Monte Carlo Max	201.9m(88.4m)	3.198(3.092)	6.216(6.118)	9.242(9.16)	12.28(12.16)	15.26(15.18)	18.26(18.16)	21.23(21.14)
Monte Carlo Mean	149.9m(43.57m)	3.113(3.023)	6.098(6.01)	9.073(8.988)	12.07(11.98)	15.04(14.97)	18.03(17.95)	21.01(20.93)
Monte Carlo Std	21.27m(21.07m)	36.46m(34.42m)	57.29m(51.66m)	70.42m(65.69m)	77.82m(78.29m)	85.85m(83.47m)	89.76m(85.62m)	88.9m(87.99m)
Yield (%)	100	100	100	100	100	100	100	100

## 9 Summary

---

Thanks to the tutors for their help and guidance, which allowed us to learn the integrated circuit design process step by step through this PGA design. Although there may be some shortcomings in the design, such as the calculation error in the W/L ratio of the nMOS in the 3-input NAND and the need for further optimization of its layout and other basic components, such as using Interdigitated Layout to reduce the required area further. However, the final parameters of the OPAMP and PGA have both met the requirements!

# Bibliography

---

- [1] Cadence Virtuoso. <https://www.cadence.com/>.
- [2] Travis N. Blalock Richard C. Jaeger. *Microelectronic circuit design*. 2010.

# List of Figures

2.1 Schematic of Inverter . . . . .	5
2.2 Layout of Inverter . . . . .	6
2.3 Comparison of the waveform between the inverter's schematic simulation and post layout simulation . . . . .	7
3.1 Schematic of CMOS-Switch . . . . .	9
3.2 Layout of CMOS-Switch . . . . .	9
3.3 Waveform of CMOS-Switch . . . . .	10
4.1 Schematic of 3-Input NAND Gate . . . . .	11
4.2 Layout of 3-Input NAND Gate . . . . .	12
5.1 Schematic of 3:8 Multiplexer . . . . .	15
5.2 Layout of 3:8 Multiplexer . . . . .	16
6.1 Schematic of OPAMP . . . . .	18
6.2 Layout of OPAMP . . . . .	18
6.3 The relevant parameters of OPAMP . . . . .	20
7.1 Schematic of LPF . . . . .	22
7.2 Layout of LPF . . . . .	23
7.3 Waveform of LPF's Bandwidth . . . . .	24
8.1 Schematic of PGA . . . . .	25
8.2 Layout of PGA . . . . .	26

# List of Tables

4.1	Results by post layout simulation for 3-input NAND gate . . . . .	13
5.1	The truth table for 3:8 multiplexer . . . . .	14
5.2	Results of post layout simulation for the 3:8 Multiplexer . . . . .	16
6.1	hand calculation . . . . .	17
6.2	schematic design . . . . .	17
6.3	OPAMP parameters for $C_L = 2 \text{ pF}$ , typical corner . . . . .	20
6.4	OPAMP corner analysis post layout (Schematic) results for $C_L = 2 \text{ pF}$ . . . . .	21
6.5	OPAMP Monte-Carlo analysis post layout (Schematic) for $C_L = 2 \text{ pF}$ . . . . .	21
8.1	Corner and Monte carlo simulation post layout (Schematic) . . . . .	26