Solution 1.1

$$
\begin{aligned}
F_1 &= \mathrm{XOR}(A, B) \\
&= \overline{A}B \vee A\overline{B} \\
&= \overline{\overline{\overline{A}B} \wedge \overline{A\overline{B}}}
\end{aligned}
$$

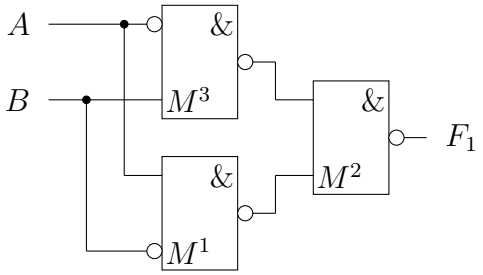


Figure 1.5: XOR(A,B) in NAND

$$
\begin{aligned}
F_2 &= \mathrm{XNOR}(A, B) \\
&= AB \vee \overline{A}\overline{B} \\
&= \overline{\overline{AB} \wedge \overline{\overline{A}\overline{B}}}
\end{aligned}
$$

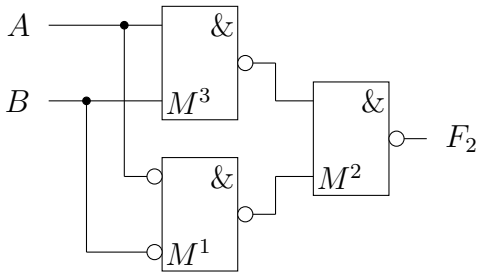


Figure 1.6: XNOR(A,B) in NAND

$$
\begin{aligned}
F_3 &= AS \vee B\overline{S} \\
&= \overline{\overline{AS} \wedge \overline{B\overline{S}}}
\end{aligned}
$$

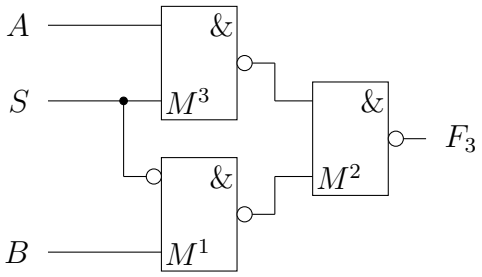


Figure 1.7: MUX(A,B,S) in NAND

Solution 1.2

$$F_1 = \overline{\overline{AC} \vee \overline{BC}}$$
$$= \overline{\overline{AC}} \wedge \overline{\overline{BC}}$$

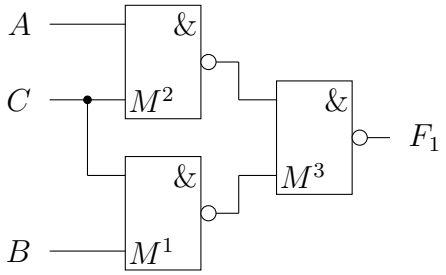


Figure 1.8: Circuit F_1

$$F_2 = \overline{\overline{(A \vee B)(\overline{C} \vee B)}}$$
$$= \overline{\overline{\overline{A \vee B}}\ \overline{\overline{\overline{C} \vee B}}}$$
$$= \overline{\overline{\overline{A}\ \overline{B}}\ \overline{\overline{C}\ \overline{B}}}$$

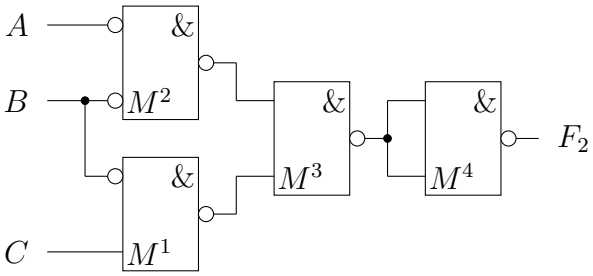


Figure 1.9: Circuit F_2

Solution 1.3

a)

$$
\begin{aligned}
F &= \overline{A}\,\overline{B}\,C \vee \overline{A}\,B\,\overline{C} \vee A\,B\,\overline{C} \\
\overline{F} &= \overline{\overline{A}\,\overline{B}\,C \vee \overline{A}\,B\,\overline{C} \vee A\,B\,\overline{C}} \qquad \text{(deMorgan)} \\
&= \overline{\overline{A}\,\overline{B}\,C} \wedge \overline{\overline{A}\,B\,\overline{C}} \wedge \overline{A\,B\,\overline{C}} \\
&= (A \vee B \vee \overline{C}) \wedge (A \vee \overline{B} \vee C) \wedge (\overline{A} \vee \overline{B} \vee C) \\
&= (A \vee B \vee \overline{C}) \wedge (\overline{B} \vee C)
\end{aligned}
$$

b)

$$
\begin{aligned}
F &= A\,B\,C \vee \overline{A}\,\overline{B}\,C \\
\overline{F} &= \overline{A\,B\,C \vee \overline{A}\,\overline{B}\,C} \\
&= \overline{A\,B\,C} \wedge \overline{\overline{A}\,\overline{B}\,C} \\
&= (\overline{A} \vee \overline{B} \vee \overline{C}) \wedge (A \vee B \vee \overline{C})
\end{aligned}
$$

c)

$$
\begin{aligned}
F &= A\,B\,C \vee A\,B\,\overline{C} \vee A\,\overline{B} \\
&= A\,B \wedge (C \vee \overline{C}) \vee A\,\overline{B} \\
&= A\,B \vee A\,\overline{B} \\
&= A \\
\overline{F} &= \overline{A}
\end{aligned}
$$

Complement of an expression means to dualize the given expression in the operation and negate it in the literal. If possible, the expression should be simplified before it is complemented.

Solution 1.4

a) Structure

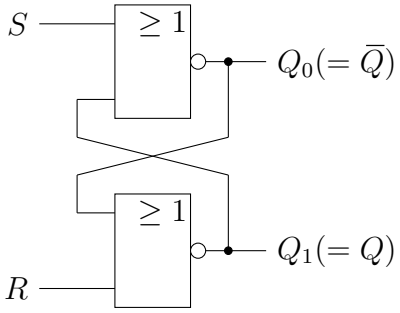


Figure 1.10: Circuit of the RS-Latch (on block level)

b) Logic Automaton Graph

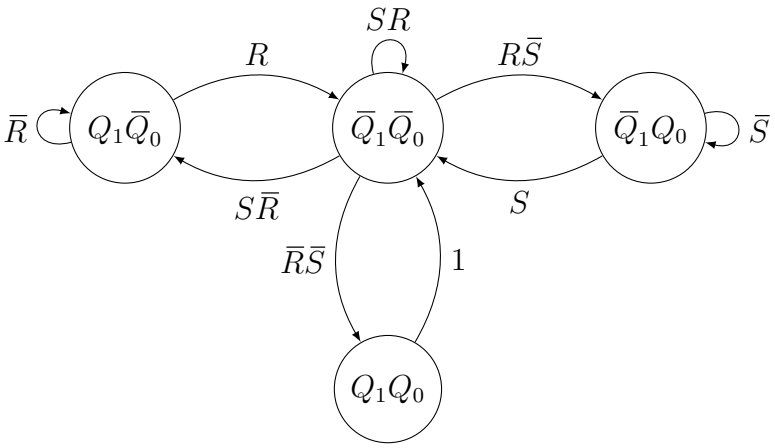


Figure 1.11: Logic automaton of the RS-Latch

c) Reduced Switching Table

S	R	${}^{n}Q$	Comment
1	0	1	set
0	1	0	reset
0	0	${}^{a}Q$	store, if ${}^{a}Q_1 = {}^{a}\overline{Q}_0$
1	1	0	${}^{n}\overline{Q}_1 = {}^{n}\overline{Q}_0$

Table 1.1: Reduced switching table of the RS-Latch

Solution 1.5

a)

${}^{a}Q$	J	K	${}^{n}Q$	${}^{n}\overline{Q}$
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

Table 1.2: Switching table of the JK-FF

b)

J	K	${}^{n}Q$
0	0	${}^{a}Q$
0	1	0
1	0	1
1	1	${}^{a}\overline{Q}$

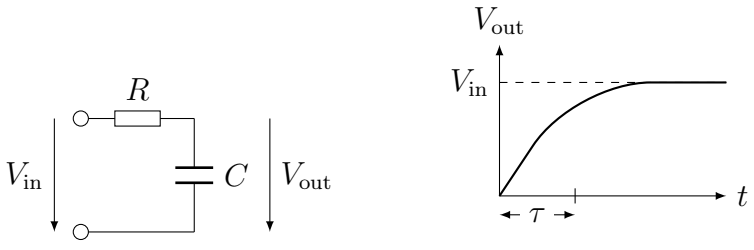
Table 1.3: Reduced switching table of the JK-FF

Solution 1.6

Charge of a capacitance: $Q = C \cdot U$
Current through a capacitance: $I = dQ/dt$

$$I = \frac{dQ}{dt} = \frac{C \cdot \Delta U}{\Delta t} = \frac{25 \cdot 10^{-15}\,\frac{\mathrm{As}}{\mathrm{V}} \cdot 0.6\mathrm{V}}{30 \cdot 10^{-12}\mathrm{s}} = 0.5\mathrm{mA}$$

Solution 1.7



$$\begin{aligned} R &= 12.5\text{k}\Omega \\ C &= 100\text{fF} \\ V_{in} &= 1.2V \end{aligned}$$

Figure 1.12: Structure und function

If a voltage (step V_{in}) is applied to the input, a voltage (step response V_{out}) is generated at the capacitor. The capacitor needs a given time to reach its maximum voltage V_{in}.

$$V_{out} = V_{in}\left(1 - e^{\frac{-t}{\tau}}\right)$$
$$V'_{out} = \frac{V_{in}}{\tau} \cdot e^{\frac{-t}{\tau}}$$

This formula shows the slope (tangent) at each point of the curve.

$$V'_{out}(0) = V_{in}\frac{1}{\tau} \quad \Rightarrow \quad \tau = \frac{V_{in}}{V'_{out}(0)}, \quad \text{mit } \tau = RC = 12.5\text{k}\Omega \cdot 100\text{fF} = 1.25\text{ns}$$

The formula $V_{out} = V_{in}(1 - e^{\frac{-t}{\tau}})$ is resolved to t:

$$t = -\tau \cdot \ln\left(1 - \frac{V_{out}}{V_{in}}\right)$$

a)

$$t_1(V_{out} = 0.6\text{V}) = -1.25\text{ns} \cdot \ln\left(1 - \frac{0.6\text{V}}{1.2\text{V}}\right) = 0.87\text{ns}$$

b)

$$t_2(V_{out} = 1.2\text{V}) = -1.25\text{ns} \cdot \ln\left(1 - \frac{1.2\text{V}}{1.2\text{V}}\right) = \infty$$

c) 10% to 90% from 1.2 V

$$\begin{aligned} t_4 - t_3 &= -1.25\text{ns} \cdot \ln\left(1 - \frac{0.9 \cdot 1.2\text{V}}{1.2\text{V}}\right) - \left(-1.25\text{ns} \cdot \ln\left(1 - \frac{0.1 \cdot 1.2\text{V}}{1.2\text{V}}\right)\right) \\ &\approx 2.75\text{ns} \end{aligned}$$

Solution 1.8

a) With $v(t) = 1.2V\left(1 - e^{-t/RC}\right)$ it follows

$$t_{\mathrm{PLH}} = -\ln\left(1 - \frac{0.6}{1.2}\right) \cdot 30\mathrm{k}\frac{\mathrm{V}}{\mathrm{A}} \cdot 1.0 \cdot 10^{-6}\frac{\mathrm{As}}{\mathrm{V}} = 20.8\mathrm{ms}$$

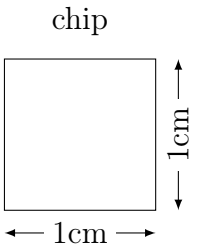
b) With $v(t) = 1.2Ve^{-t/RC}$ follows

$$t_{\mathrm{PHL}} = -\ln\left(\frac{0.6}{1.2}\right) \cdot 12.5\mathrm{k}\frac{\mathrm{V}}{\mathrm{A}} \cdot 1.0 \cdot 10^{-6}\frac{\mathrm{As}}{\mathrm{V}} = 8.66\mathrm{ms}$$

c)

$$\frac{t_{\mathrm{PLH}}}{t_{\mathrm{PHL}}} = \frac{20.8}{8.66} \approx 2.4 \approx \frac{1}{0.4}$$

Solution 1.9



The ratio between two technologies is $0.13\mu\text{m}/0.18\mu\text{m} \sim 0.7$. This also refers to the average edge length of a transistor. The area is $0.7\text{cm} \cdot 0.7\text{cm} \cong 0,5\text{cm}^2$ for the equal number of transistors has halved. When a technology scales by 0.7, then only half the area is needed. In 0.13μm technology, a chip of the same size integrates on average an amount of 100 million transistors.

Solution 1.10

n: Amount of technology generations
2: Doubling the performance of this technology

$$
\begin{aligned}
2 \cdot 10^9\text{Hz} \cdot 2^n &= 10 \cdot 10^9\text{Hz} \\
2^n &= 5 \\
n &= \text{ld}(5) \\
n &= 2.3 \qquad \text{amount of technology generations}
\end{aligned}
$$

Now it takes 3 years to introduce a technology generation:

$$
\begin{aligned}
\Delta n &= \text{ld}(5) \cdot 3 \\
&= 2.3 \cdot 3 \\
&= 6.9
\end{aligned}
$$