Task 8.1

Calculate the power consumption of a pseudo NMOS inverter in its logical zero. Given $V_{\mathrm{OL}} = 0.1\mathrm{V}$ and $W_{\mathrm{N}}/L_{\mathrm{n}} = 9$ in $0.13\mu\mathrm{m}$ technology ($\mu_{\mathrm{n}} = 270\mathrm{cm}^2/\mathrm{Vs}$, $C_{\mathrm{ox}} = 1.6\mu\mathrm{F}/\mathrm{cm}^2$, $V_{\mathrm{TN}} = 0.4\mathrm{V}$, $V_{\mathrm{DD}} = 1.2\mathrm{V}$, $L = 100\mathrm{nm}$, $E_{\mathrm{CN}}L_{\mathrm{N}} = 0.6\mathrm{V}$, $v_{\mathrm{sat}} = 8 \cdot 10^6\mathrm{cm/s}$).

Task 8.2

Calculate the power consumed on a chip:

i) The chip has 10M gates, an activity factor of 10%, $V_{\mathrm{DD}} = 1.8\mathrm{V}$, a clock frequency of 500MHz and an average capacity per node of 20fF.

ii) The chip has 50M gates, an activity factor of 5%, $V_{\mathrm{DD}} = 1.2\mathrm{V}$, a clock frequency of 1GHz and an average capacity per node of 10fF.

Explain which design is the better one and why?

Task 8.3

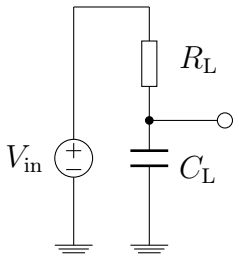

Figure 8.1: RC Circuit

Determine the total energy for the RC circuit in Fig. 8.1. This is transferred from the voltage source to the circuit when there is a jump from 0 to V_{DD}. Calculate the energy stored by the capacitor. What happens to the rest?

Task 8.4

Calculate R_{eqn} and R_{eqp} in $0.13\mu\mathrm{m}$ technology ($\mu_{\mathrm{n}} = 270\mathrm{cm}^2/\mathrm{Vs}$, $\mu_{\mathrm{p}} = 70\mathrm{cm}^2/\mathrm{Vs}$, $C_{\mathrm{ox}} = 1.6\mu\mathrm{F}/\mathrm{cm}^2$, $V_{\mathrm{TN}} = 0.4\mathrm{V}$, $V_{\mathrm{TP}} = -0.4\mathrm{V}$, $V_{\mathrm{DD}} = 1.2\mathrm{V}$, $L = 100\mathrm{nm}$, $E_{\mathrm{CN}}L_{\mathrm{N}} = 0.6\mathrm{V}$, $E_{\mathrm{CP}}L_{\mathrm{P}} = 2.4\mathrm{V}$, $v_{\mathrm{sat}} = 8 \cdot 10^6\mathrm{cm/s}$).

Task 8.5

Determine the worst case capacities for the NAND3 in Fig. 8.2. Consider common areas for source and drain and specify the result depending on C_{g} and C_{eff}.

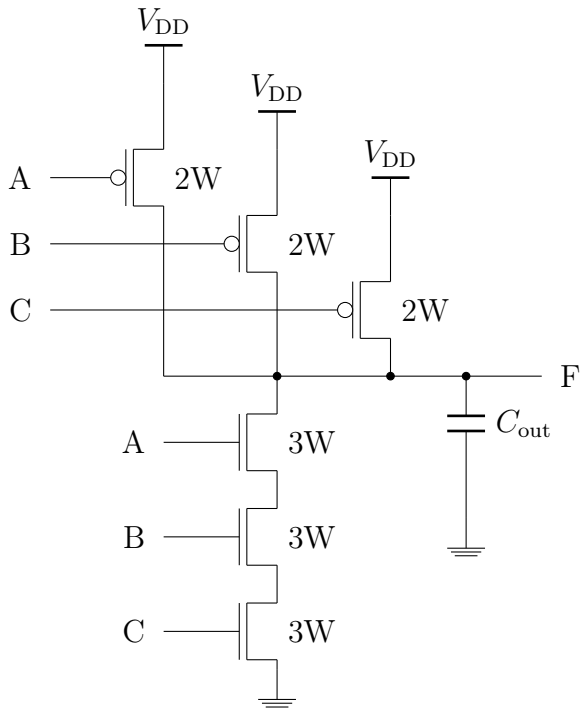

Figure 8.2: NAND3 Gate

Task 8.6

A CMOS inverter has a pull-up transistor with 8λ:2λ and a pull-down transistor with 4λ:2λ. The inverter should be able to drive four identical inverters. Calculate all capacities in 0.18μm technology ($\mu_n = 270\text{cm}^2/\text{Vs}$, $\mu_p = 70\text{cm}^2/\text{Vs}$, $C_{ox} = 1\mu\text{F}/\text{cm}^2$, $V_{TN} = 0.5\text{V}$, $V_{TP} = -0.5\text{V}$, $V_{DD} = 1.8\text{V}, L = 200\text{nm}$, $E_{CN}L_N = 1.2\text{V}$, $E_{CP}L_P = 4.8\text{V}$, $\upsilon_{sat} = 8 \cdot 10^6\text{cm/s}$), line capacities are neglected.

Task 8.7

Specify the structure (schematic of building blocks (gates)) of a positive edge controlled RS-FF. Set up the switching sequence table. In addition, enter a positive edge-controlled D-FF. How can the input capacitance be reduced?