Task 9.1

A CMOS inverter exhibits a pull-up transistor with 8λ:2λ (W/L) and a pull-down transistor with 4λ:2λ (W/L) in 0.18μm technology.

$$(\mu_n = 270\text{cm}^2/\text{Vs}, \quad \mu_p = 70\text{cm}^2/\text{Vs}, \quad C_{ox} = 1.6\mu\text{F}/\text{cm}^2, \quad V_{TN} = 0.5\text{V},$$
$$V_{TP} = \text{-}0.5\text{V}, \quad V_{DD} = 1.8\text{V}, \quad L = 200\text{nm}, \quad E_{CN}L_N = 1.2\text{V},$$
$$E_{CP}L_P = 4.8\text{V}, \quad v_{sat} = 8 \cdot 10^6\text{cm/s})$$

a) Calculate the delay time (FO4) of an inverter for a step at the input. Line capacitances should be neglected.

b) Calculate the delay time (FO1) of four inverters in chain for a step at the input. Consider different rise and fall times.

Task 9.2

Calculate τ_{inv} und γ_{inv} for an inverter in 0.13μm technology.

Task 9.3

Calculate the optimal fanout f for a three-level inverter chain ($C_{load} = 200\text{fF}$ and $C_{in} = 1\text{fF}$). Also calculate the value of f for the optimal number of levels. In both cases, calculate the delay through the inverter chain assuming τ_{inv}=7.5ps and γ_{inv}=0.5.

Task 9.4

Size the gates along the path indicated by the arrow in the circuitry in Fig. 9.1.

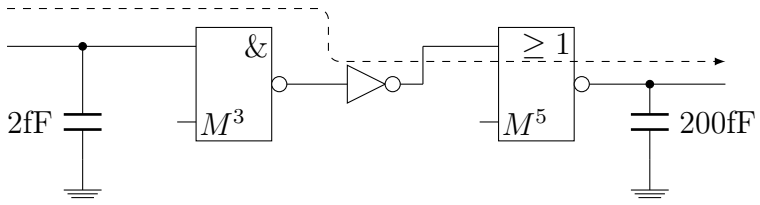

Figure 9.1: Optimum Delay along a Path

Task 9.5

Now size the gates from task 9.4 using Tab. 9.1 and Tab. 9.2 with Logical Effort (LE). Calculate the optimum delay first.

Type of Gate	1 input	2 input	3 input	4 input
INV	1	-	-	-
NAND	-	4/3	5/3	6/3
NOR	-	5/3	7/3	9/3

Table 9.1: Logical Effort (LE) of Simple Gates

Type of Gate	1 input	2 input	3 input	4 input
INV	$P_{\text{inv}} = 1/2$	-	-	-
NAND	-	$2P_{\text{inv}} = 1$	$3P_{\text{inv}} = 3/2$	$4P_{\text{inv}} = 2$
NOR	-	$3P_{\text{inv}} = 3/2$	$4.5P_{\text{inv}} = 9/4$	$6P_{\text{inv}} = 3$

Table 9.2: Parasitics (P) of Simple Gates

Task 9.6

For the specified circuitry in Fig. 9.2, determine the optimal stage effort and total path delay, and size the gates.

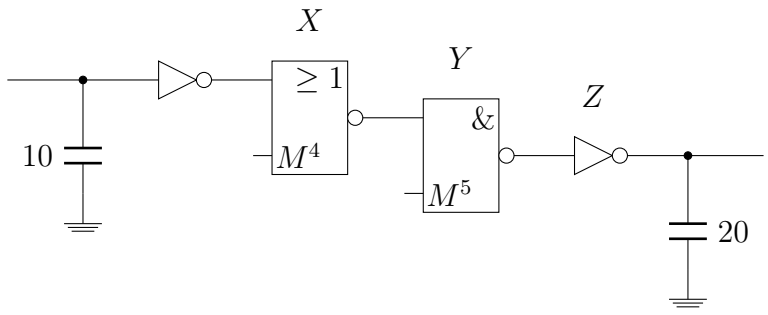

Figure 9.2: Optimal Stage Effort and Path Delay

Task 9.7

For each circuit in Fig. 9.3, determine the inherent capacitance C_{self} for an input step (0.13μm technology).

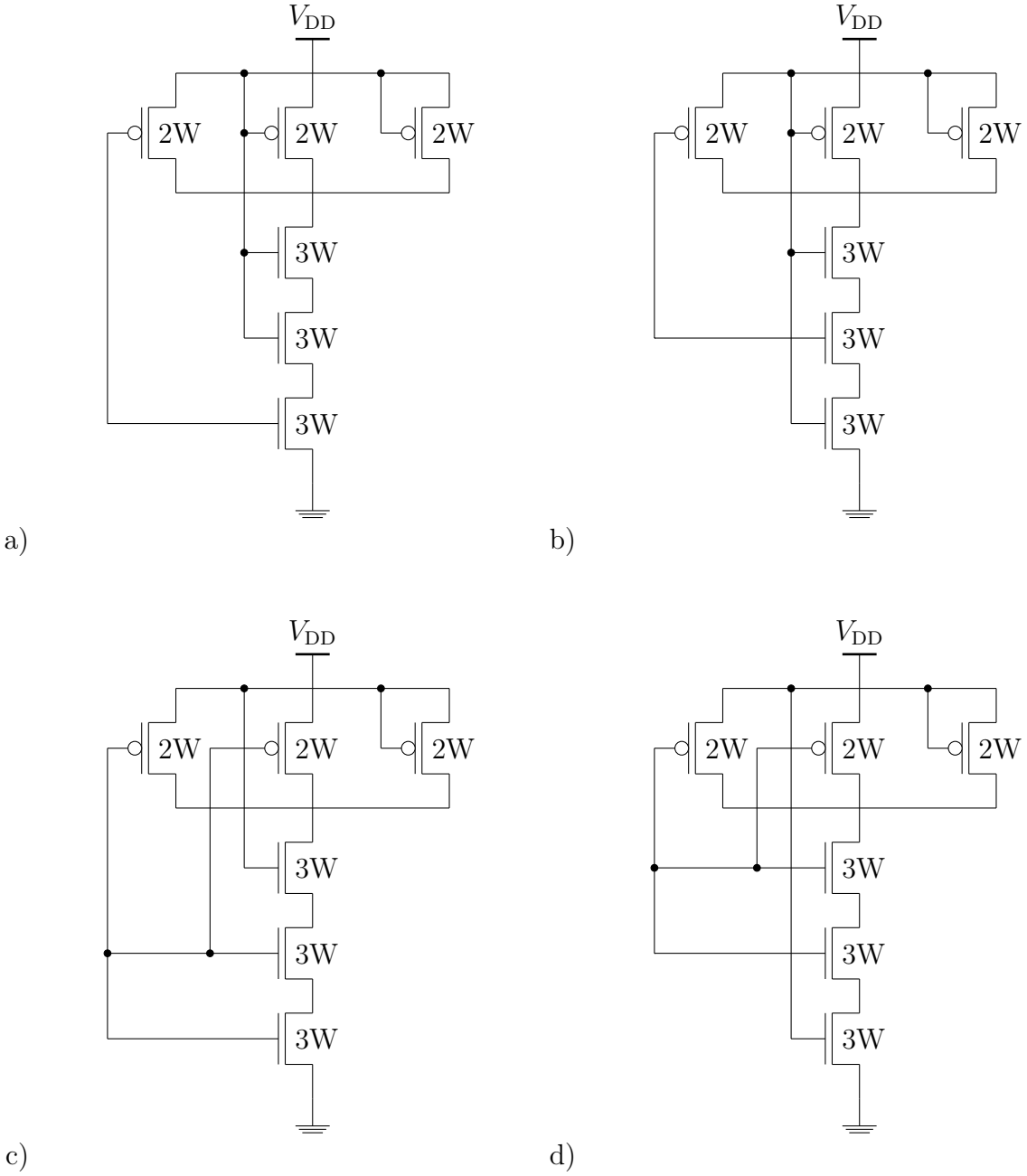

Figure 9.3: Calculation of the Internal Capacitance C_{self}