Task 4.1

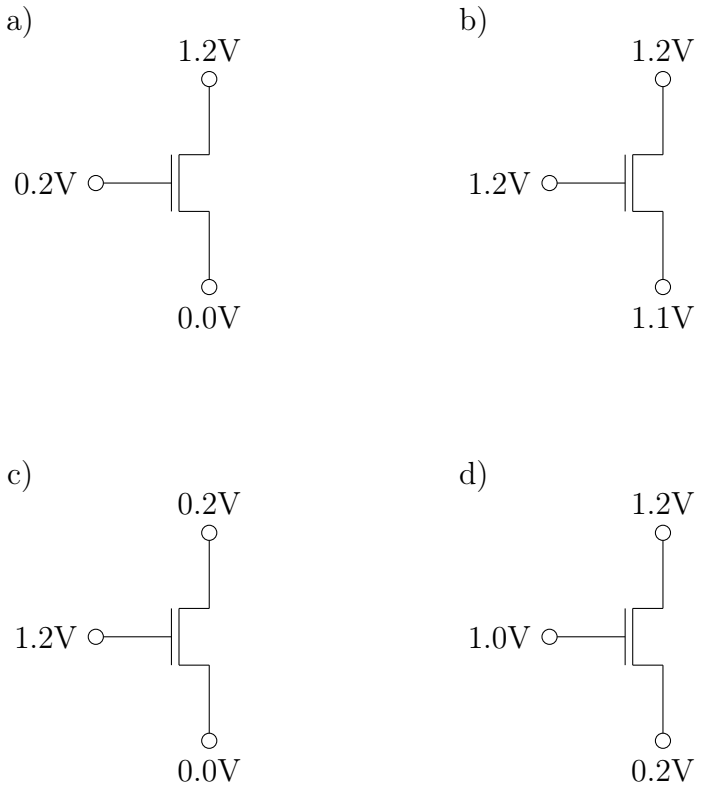

Figure 4.1: Regions of operation (NMOS transistor)

Determine the region of operation for each transistor in Fig. 4.1 ($V_\mathrm{T} = 0.4\mathrm{V}$).

Task 4.2

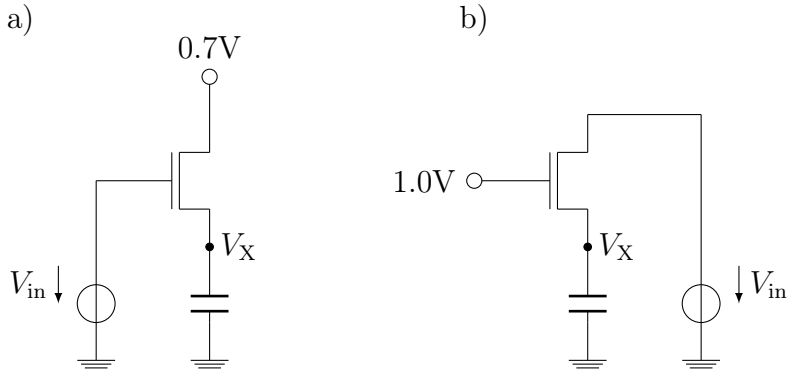

Figure 4.2: Different operating modes of the NMOS transistor

Apply V_X over $0.0\mathrm{V} < V_\mathrm{in} < 1.2\mathrm{V}$ ($V_\mathrm{T} = 0.4\mathrm{V}$) to the circuits of Fig. 4.2.

Task 4.3

For a PMOS transistor, calculate the gate capacitance in the cutoff, linear and saturation region. Given: $t_{ox} = 22$Å, $W = 400$nm, $L = 100$nm
Assumption: $V_{GS} = 0$V in the cutoff area.

Task 4.4

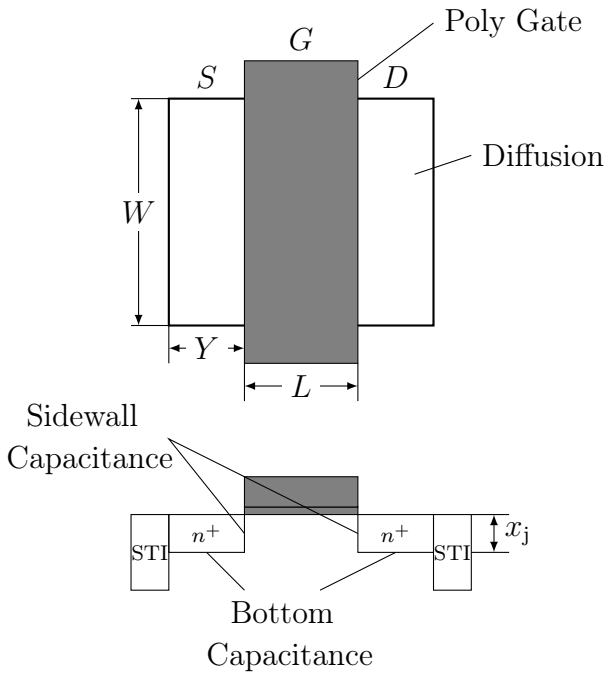

Figure 4.3: Plan view and sectional drawing of an NMOS Transistor

a) Calculate ϕ_B and $C_{jb}(V_J)$ of a n^+p junction. It applies $N_D = 10^{20}\text{cm}^{-3}$ and $N_A = 3 \cdot 10^{17}\text{cm}^{-3}$.

b) Given is $W = 400$nm, $L = 100$nm, $x_j = 50$nm and $Y = 300$nm. Calculate C_J in units [fF] for $V_J = 0$V and $V_J = -1.2$V.

c) Calculate K_{eq} for $V_1 = -1.2$V and $V_2 = 0$V. Specify the C_J effective for large signal behavior.

Task 4.5

Calculate the overlap capacitance C_{ol} for a 0.13μm technology in units [fF/μm].
Given: $T_{poly}/t_{ox} = 100$ and the lateral diffusion $L_D = 10$nm.