INTERNATIONAL EDITION

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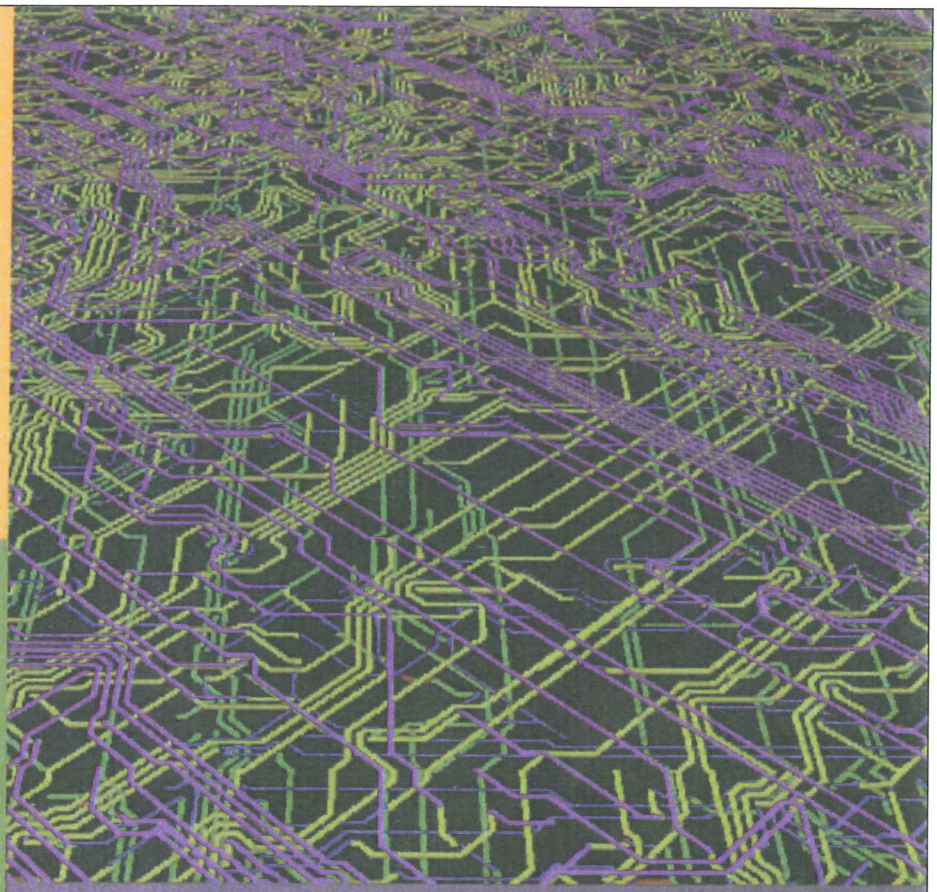

Analysis and Design of Digital Integrated Circuits

In Deep Submicron Technology

Third Edition

Contents

Chapter 1
Deep Submicron Digital IC Design
In the first chapter, we provide a perspective on digital design in the deep submicron era and motivate the topics in the rest of the book. We briefly review important concepts of logic gates primarily to provide notational context for the book, including the ideal logic element, static input-output characteristics, noise margin, and propagation delay time. Then we elaborate on the key issues in deep submicron such as power dissipation, velocity saturated transistors, interconnect resistance, coupling capacitance, and inductance. The role of computer-aided design tools such as SPICE is described. The chapter concludes with the challenges ahead as described in the technology roadmap.

Chapter 2
MOS Transistors
The short-channel device models to be used in the rest of this book are described in this chapter. To begin the treatment, rudimentary device physics concepts are covered to explain the threshold voltage equation and the transistor current equations. Both long- and short-channel models are derived. Then the oxide and junction capacitance models are described to complete the chapter.

Chapter 3
Fabrication, Layout, and Simulation
This chapter describes the relationship between fabrication, layout, and simulation in the integrated circuit design process. The topics of fabrication and layout are important to IC designers and should be well-understood. However, for this course, it serves more as a background for the rest of the text. The more important subject is simulation with SPICE. The model parameters for SPICE are detailed in this chapter. A brief user manual is provided in Appendix A for those unfamiliar with the basics of SPICE. We also provide some advanced material on MOS transistors and fabrication technologies of the future.

Chapter 4
MOS Inverter Circuits
This is a core chapter on MOS digital inverters and introduces concepts of voltage transfer characteristics, noise margins, inverter configurations, and simple timing and power calculations. Analytical equations are derived for noise margin parameters and switching thresholds of inverters for a number of MOS inverters.

Chapter 5
Static MOS Gate Circuits
This is another core chapter of the book. It examines the static design issues for NANDs, NORs, and complex gates. It develops extensions to inverter design to size the transistors in CMOS gates. Sequential elements, such as flip-flops and latches, are described in this chapter. The chapter concludes with a detailed treatment of the various components of power dissipation in logic gates.

Chapter 6
High-Speed CMOS Logic Design
This chapter describes the issues involved in high-speed logic design. It develops useful equations for switching delay calculation for step and ramp inputs. This involves the use of the large-signal on-resistance of gates, and the calculation of the loading capacitance, both of which are detailed. The total capacitance can be computed using two key parameters for input and output capacitance. Gate sizing for equal delay and minimal delay are described. The thrust of the latter half of this chapter is high-speed logic optimization using logical effort.

Chapter 7
Transfer Gate and Dynamic Logic Design
In this chapter, we explore dynamic design techniques using transmission gates and precharged logic. The important concepts of charge-sharing, bootstrapping, feedthrough, and charge leakage are elaborated in this chapter. Domino logic is described in detail as it is the most common form of dynamic logic in use today. These concepts lay the groundwork for the operation of many of the memory circuits discussed in the next two chapters.

Chapter 8
Semiconductor Memory Design
This chapter addresses the analysis and design of VLSI memories, commonly known as semiconductor memories. In this chapter, we classify the different types of memory, examine the major subsystems, and then focus on the static RAM (SRAM) design issues. This topic is particularly suitable for our study of CMOS digital design as it allows us to apply many of the basic concepts presented in earlier chapters. The entire design process for static RAMs is described in detail.

Chapter 9
Additional Topics in Memory Design
This chapter explores a variety of other semiconductor memories, their architectures, access mechanisms, and cell configurations. We begin by examining content-addressable memories, since they are a derivative of the SRAM architecture. We also cover an important application of SRAM cells in the growing market segment of programmable logic called field-programmable gate-arrays (FPGAs). The chapter sequences through dynamic RAMs, mask-programmable ROMs, erasable programmable ROMs, electrically-erasable ROMs and Flash memories, and concludes with a look at memory cells based on ferroelectric materials called FRAMs.

Chapter 10
Interconnect Design
This chapter is devoted to the study of interconnect issues that the IC designer faces when designing in deep submicron technologies. It addresses the issues associated with *RLC* aspects of wires in detail. We begin by re-examining the *RC* delay calculation using the Elmore delay, and address the issue of buffer insertion in long wires.

USEFUL DESIGN PARAMETERS (simplified)

		0.18 μm		0.13 μm		
Name	**Symbol**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**Units**
Channel Length (rounded for convenience)	L	200	200	100	100	nm
Supply Voltage	V_{DD}	1.8	1.8	1.2	1.2	V
Oxide Thickness	t_{ox}	35	35	22	22	Å
Oxide Capacitance	C_{ox}	1.0	1.0	1.6	1.6	μF/cm^2
Threshold Voltage	V_{T0}	0.5	−0.5	0.4	−0.4	V
Body-Effect Term	γ	0.3	0.3	0.2	0.2	V$^{1/2}$
Fermi Potential	$2\lvert\phi_F\rvert$	0.84	0.84	0.88	0.88	V
Junction Capacitance Coefficient	C_{j0}	1.6	1.6	1.6	1.6	fF/μm^2
Built-In Junction Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Grading Coefficient	m	0.5	0.5	0.5	0.5	—
Nominal Mobility (low vertical field)	μ_0	540	180	540	180	cm^2/V-s
Effective Mobility (high vertical field)	μ_e	270	70	270	70	cm^2/V-s
Critical Field	E_c	6×10^4	24×10^4	6×10^4	24×10^4	V/cm
Critical Field × L	E_cL	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eff}	12.5	30	12.5	30	kΩ/□

Name	**Symbol**	**Value**	**Units**
Gate Capacitance Coefficient	C_g	2	fF/μm
Self Capacitance Coefficient	C_{eff}	1	fF/μm
Wire Capacitance Coefficient	C_w	0.1–0.25	fF/μm
Al Wire Resistance	$R_\square$	25–60	mΩ/□
Cu Wire Resistance	$R_\square$	20–40	mΩ/□
Wire Inductance	L_{eff}	40–50	pH/μm

USEFUL PHYSICAL AND MATERIAL CONSTANTS

Name	Symbol	Value	Units
Electron Charge	q	1.6×10^{-19}	C
Boltzmann's Constant	k	1.38×10^{-23}	J/°K
Room Temperature	T	300	°K (27°C)
Thermal Voltage	$V_{th} = kT/q$	26	mV (at 27°C)
Dielectric Constant of Vacuum	ε_0	8.85×10^{-14}	F/cm
Dielectric Constant of Silicon	ε_{si}	$11.7\ \varepsilon_0$	F/cm
Dielectric Constant of SiO_2	ε_{ox}	$3.97\ \varepsilon_0$	F/cm
Intrinsic Carrier Concentration	n_i	1.45×10^{10}	cm^{-3} (at 27°C)
Carrier Saturation Velocity In Silicon	υ_{sat}	8×10^6	cm/s
Aluminum Resistivity	ρ_{Al}	2.7	$\mu\Omega$-cm
Copper Resistivity	ρ_{Cu}	1.7	$\mu\Omega$-cm
Tungsten Resistivity	ρ_W	5.5	$\mu\Omega$-cm

ENGINEERING SCALE FACTORS

G	giga	10^9
M	mega	10^6
k	kilo	10^3
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

METER CONVERSION FACTORS

$1\ \mu m = 10^{-4}\ cm = 10^{-6}\ m$

$1\ m = 10^2\ cm = 10^6\ \mu m$

$0.1\ \mu m = 100\ nm$

$1 Å = 10^{-8} cm = 10^{-10} m$