Task 12.1

Determine the function of the gate in figure 12.1. Which clock feedthrough is generated for the parameters of a 0.13μm technology at internal node X and which worst-case voltage due to charge sharing. Is there a potential risk?

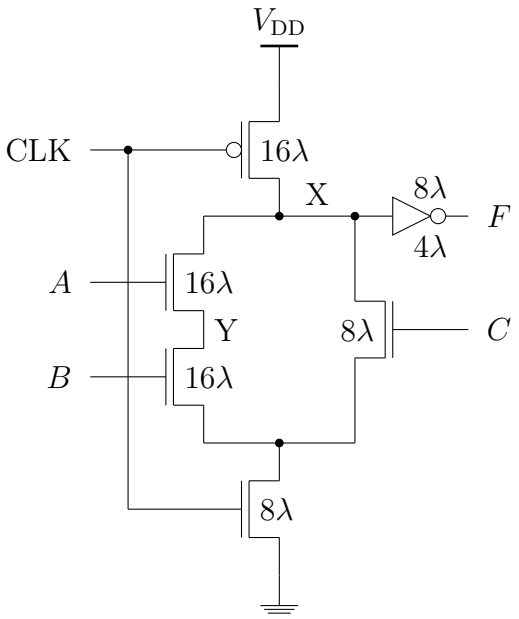

Figure 12.1: Gates in Domino Logic

Task 12.2

Design the minimal XOR/XNOR function in Dual-Rail Domino Logic

Task 12.3

Design minimal logic circuits from transfer gates for the following functions:

a) $F = A \vee BC$

b) $F = AB \vee BC \vee \overline{C}$

c) $F = (\overline{A \vee B \vee C}) \vee \overline{A}B$

d) $F = \left(\overline{\overline{(\overline{A \vee B \vee \overline{C}}) \vee \overline{A}\,\overline{B}}}\right)$

Task 12.4

Describe the function of each circuit in Fig. 12.2 by its truth table.

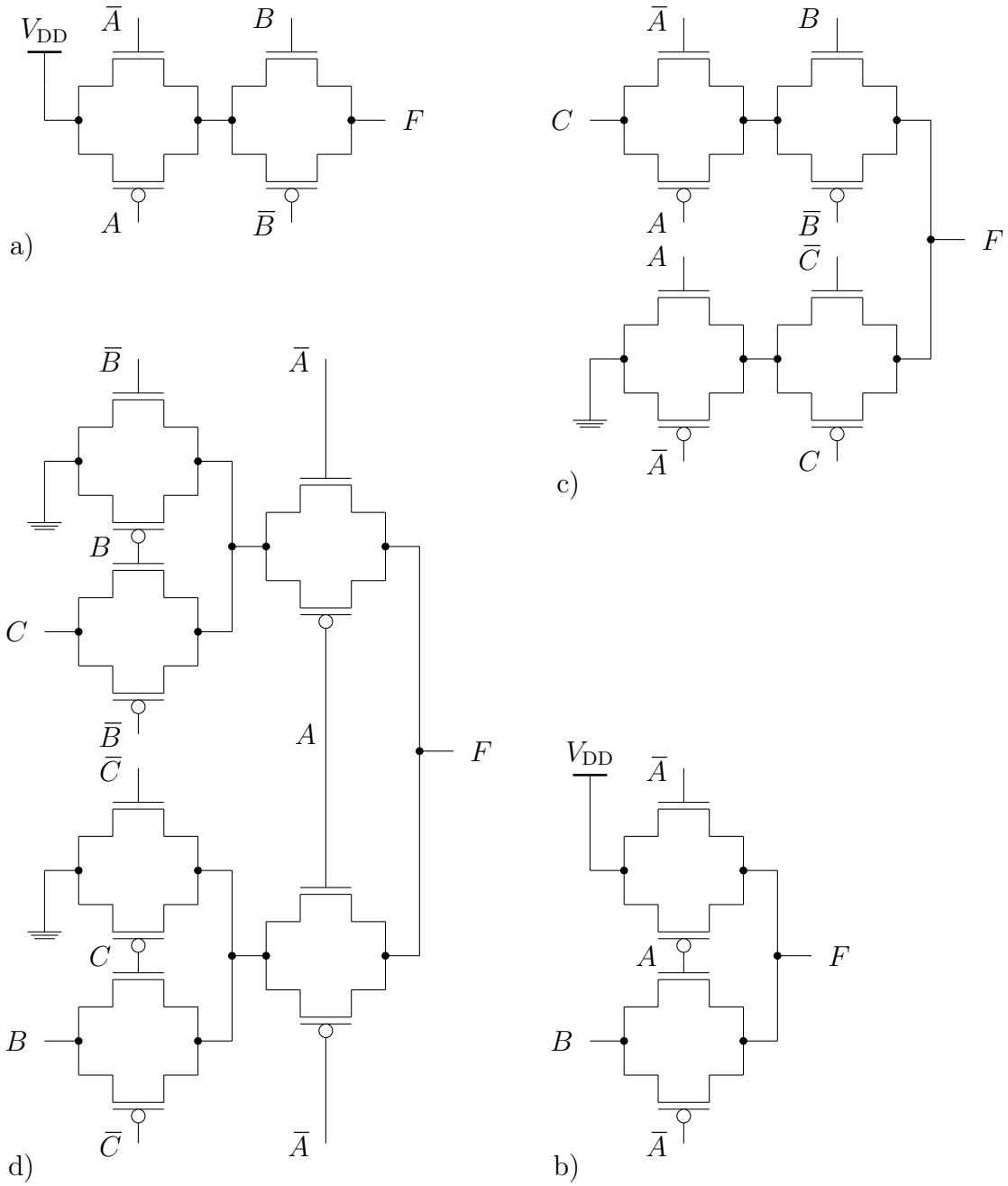

Figure 12.2: Circuits using Transfer Gates

Task 12.5

Design in Domino Logic:

a) $F = \overline{A} \vee \overline{B}C$

b) $F = A\overline{B} \vee BC \vee \overline{C}$

c) $F = (\overline{\overline{A} \vee \overline{B} \vee C}) \vee A\overline{B}$

d) $F = \left(\overline{\overline{(\overline{A} \vee \overline{B} \vee C) \vee \overline{A}B}}\right)$