Solution 3.1

With the process parameters follows the 0.13μm technology:

a) $V_{\mathrm{T0}} = \Phi_{\mathrm{GC}} - 2\Phi_{\mathrm{F}} - Q_{\mathrm{B0}}/C_{\mathrm{ox}} - Q_{\mathrm{ox}}/C_{\mathrm{ox}}$

$$\begin{aligned}
&\text{NMOS:} \quad V_{\mathrm{T0p}} = -0.99\mathrm{V} - (-0.88\mathrm{V}) - (-0.188\mathrm{V}) - 0.06\mathrm{V} = 0.02\mathrm{V} \\
&\text{PMOS:} \quad V_{\mathrm{T0n}} = 0.99\mathrm{V} - (0.88\mathrm{V}) - (0.188\mathrm{V}) - 0.06\mathrm{V} = -0.14\mathrm{V}
\end{aligned}$$

b) $\Phi_{\mathrm{GC}} = \Phi_{\mathrm{F}} - \Phi_{\mathrm{G}}(\mathrm{Gate})$

$$\begin{aligned}
&\Phi_{\mathrm{GC}}|_{\mathrm{NMOS}}(\text{n-gate}) = \Phi_{\mathrm{Fp}} - 0.55, (\phi_{\mathrm{Fp}} < 0) \\
&\Phi_{\mathrm{GC}}|_{\mathrm{PMOS}}(\text{p-gate}) = \Phi_{\mathrm{Fn}} + 0.55, (\phi_{\mathrm{Fn}} > 0) \\
&\Phi_{\mathrm{GC}}|_{\mathrm{PMOS}}(\text{n-gate}) = \Phi_{\mathrm{Fn}} - 0.55, (\phi_{\mathrm{Fn}} > 0)
\end{aligned}$$

The work function is estimated with the intrinsic Fermi level as a reference point. For the threshold voltage of the PMOS transistor (with p^+ doping) the following results in $V_{\mathrm{T0n}} = (-0.11\mathrm{V}) - (0.88\mathrm{V}) - (0.188\mathrm{V}) - 0.06\mathrm{V} = -1.24\mathrm{V}$

c) $N_{\mathrm{I}} = (C_{\mathrm{ox}}/\mathrm{q})\Delta V$

$$\begin{aligned}
&\text{NMOS:} \quad N_{\mathrm{I}} = (10^{+13}\mathrm{V}^{-1}\mathrm{cm}^{-2})(0.4\mathrm{V} - (0.02\mathrm{V})) = 3.8 \cdot 10^{12}\mathrm{cm}^{-2} \\
&\text{PMOS:} \quad N_{\mathrm{I}} = (10^{+13}\mathrm{V}^{-1}\mathrm{cm}^{-2})(-0.4\mathrm{V} - (-0.14\mathrm{V})) = -2.6 \cdot 10^{12}\mathrm{cm}^{-2} \\
&\text{PMOS:} \quad N_{\mathrm{I}} = (10^{+13}\mathrm{V}^{-1}\mathrm{cm}^{-2})(-0.4\mathrm{V} - (-1.24\mathrm{V})) = 8.4 \cdot 10^{12}\mathrm{cm}^{-2}
\end{aligned}$$

d) $|V_{\mathrm{T0}}| < V_{\mathrm{DD}}$, $|V_{\mathrm{T0}}|$ can't be higher than V_{DD}.

e)

$$\begin{aligned}
\mu_{\mathrm{e}} &= \frac{\mu_0}{1 + \left(\dfrac{V_{\mathrm{GS}} - V_{\mathrm{T}}}{\theta \cdot t_{\mathrm{ox}}}\right)^{\eta}} \\
&= \frac{130\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}}{1 + \left(\dfrac{0.8\mathrm{V}}{4 \cdot 10^6\mathrm{Vcm}^{-1} \cdot 22 \cdot 10^8\mathrm{cm}}\right)^{1.85}} \\
&= 71\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}
\end{aligned}$$

Solution 3.2

a) $E_{\mathrm{cn}}L_{\mathrm{n}} = 6 \cdot 10^4 \mathrm{Vcm}^{-1}(0.2\mu\mathrm{m}) \approx 1.2\mathrm{V}$ and $E_{\mathrm{cp}}L_{\mathrm{p}} = 24 \cdot 10^4 \mathrm{Vcm}^{-1}(0.2\mu\mathrm{m}) \approx 4.8\mathrm{V}$

$$\text{NMOS}: \quad V_{\mathrm{Dsat}} = \frac{(V_{\mathrm{GS}} - V_{\mathrm{TN}})(E_{\mathrm{cn}}L)}{(V_{\mathrm{GS}} - V_{\mathrm{TN}} + E_{\mathrm{cn}}L)}$$

$$= \frac{(1.8\mathrm{V} - 0.5\mathrm{V})(1.2\mathrm{V})}{(1.8\mathrm{V} - 0.5\mathrm{V} + 1.2\mathrm{V})} \approx 0.6\mathrm{V}$$

$$\text{PMOS}: \quad V_{\mathrm{Dsat}} = \frac{(V_{\mathrm{SG}} - |V_{\mathrm{TP}}|)(E_{\mathrm{cp}}L)}{(V_{\mathrm{SG}} - |V_{\mathrm{TP}}| + E_{\mathrm{cp}}L)}$$

$$= \frac{(1.8\mathrm{V} - 0.5\mathrm{V})(4.8\mathrm{V})}{(1.8\mathrm{V} - 0.5\mathrm{V} + 4.8\mathrm{V})} \approx 1.0\mathrm{V}$$

b) $E_{\mathrm{cn}}L_{\mathrm{n}} = 6 \cdot 10^4 \mathrm{Vcm}^{-1}(0.1\mu\mathrm{m}) \approx 0.6\mathrm{V}$ and $E_{\mathrm{cp}}L_{\mathrm{p}} = 24 \cdot 10^4 \mathrm{Vcm}^{-1}(0.1\mu\mathrm{m}) \approx 2.4\mathrm{V}$

$$\text{NMOS}: \quad V_{\mathrm{Dsat}} = \frac{(V_{\mathrm{GS}} - V_{\mathrm{TN}})(E_{\mathrm{cn}}L)}{(V_{\mathrm{GS}} - V_{\mathrm{TN}} + E_{\mathrm{cn}}L)}$$

$$= \frac{(1.2\mathrm{V} - 0.4\mathrm{V})(0.6\mathrm{V})}{(1.2\mathrm{V} - 0.4\mathrm{V} + 0.6\mathrm{V})} = 0.34\mathrm{V}$$

$$\text{PMOS}: \quad V_{\mathrm{Dsat}} = \frac{(V_{\mathrm{SG}} - |V_{\mathrm{TP}}|)(E_{\mathrm{cp}}L)}{(V_{\mathrm{SG}} - |V_{\mathrm{TP}}| + E_{\mathrm{cp}}L)}$$

$$= \frac{(1.2\mathrm{V} - 0.4\mathrm{V})(2.4\mathrm{V})}{(1.2\mathrm{V} - 0.4\mathrm{V} + 2.4\mathrm{V})} = 0.6\mathrm{V}$$

c)

$$\text{NMOS}: \quad \frac{I_{\mathrm{DS}}}{W} = \upsilon_{\mathrm{sat}} C_{\mathrm{ox}} \cdot \frac{(V_{\mathrm{GS}} - V_{\mathrm{TN}})^2}{(V_{\mathrm{GS}} - V_{\mathrm{TN}}) + E_{\mathrm{cn}}L}$$

$$= 12.8\mathrm{A(Vcm)}^{-1} \frac{(1.2\mathrm{V} - 0.4\mathrm{V})^2}{(1.2\mathrm{V} - 0.4\mathrm{V}) + 0.6\mathrm{V}} = 585\mu\mathrm{A}/\mu\mathrm{m}$$

$$\text{PMOS}: \quad \frac{I_{\mathrm{DS}}}{W} = \upsilon_{\mathrm{sat}} C_{\mathrm{ox}} \cdot \frac{(V_{\mathrm{SG}} - |V_{\mathrm{TP}}|)^2}{(V_{\mathrm{SG}} - |V_{\mathrm{TP}}|) + E_{\mathrm{cp}}L}$$

$$= 12.8\mathrm{A(Vcm)}^{-1} \frac{(1.2\mathrm{V} - 0.4\mathrm{V})^2}{(1.2\mathrm{V} - 0.4\mathrm{V}) + 2.4\mathrm{V}} = 256\mu\mathrm{A}/\mu\mathrm{m}$$

$$\frac{I_{\mathrm{DsatN}}}{I_{\mathrm{DsatP}}} = \frac{W_{\mathrm{N}}\upsilon_{\mathrm{sat}}C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{TN}})^2/(V_{\mathrm{GS}} - V_{\mathrm{TN}} + E_{\mathrm{cn}}L_{\mathrm{n}})}{W_{\mathrm{P}}\upsilon_{\mathrm{sat}}C_{\mathrm{ox}}(V_{\mathrm{SG}} - |V_{\mathrm{TP}}|)^2/(V_{\mathrm{SG}} - |V_{\mathrm{TP}}| + E_{\mathrm{cp}}L_{\mathrm{p}})} = 2.3$$

Solution 3.3

V_{DD}=1.2V, 1X= W/L (Device Size Ratio), W = 100nm, L = 100nm

a) $I_{\mathrm{DS}} = f(V_{\mathrm{DS}})$
We already know the ratio between 1X devices for NMOS and PMOS transistors:

$$\frac{I_{\mathrm{DsatN}}}{I_{\mathrm{DsatP}}} = 2.3$$

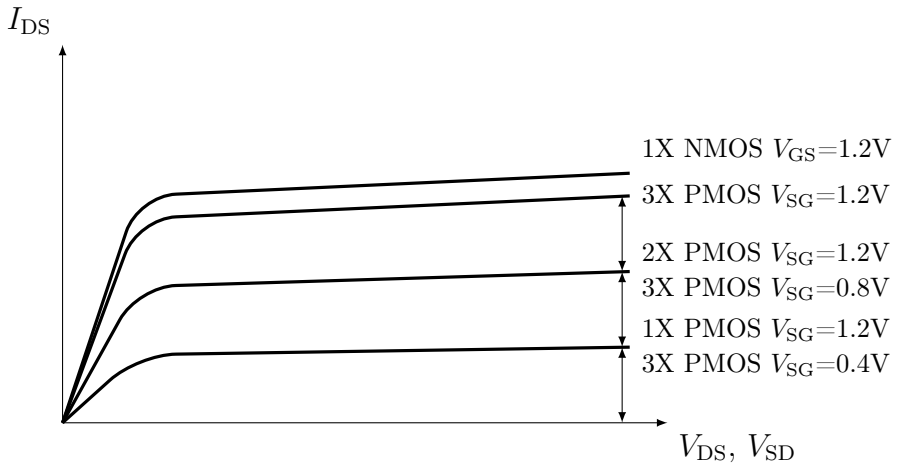

Figure 3.2: Output characteristics of MOS transistors

b) $I_{\mathrm{DS}} = f(V_{\mathrm{GS}})$

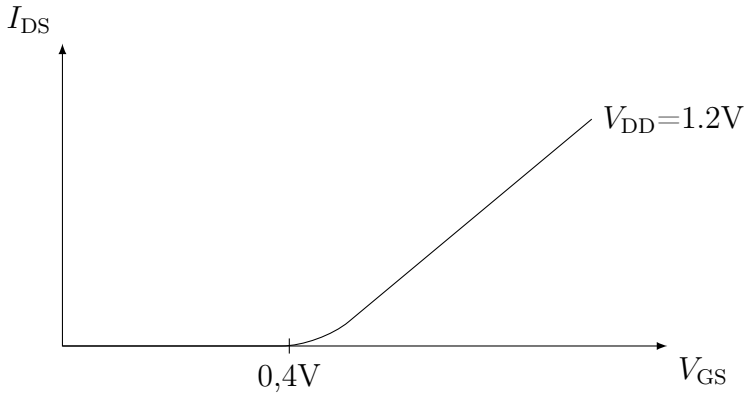

Figure 3.3: Diode characteristic of MOS transistors

Solution 3.4

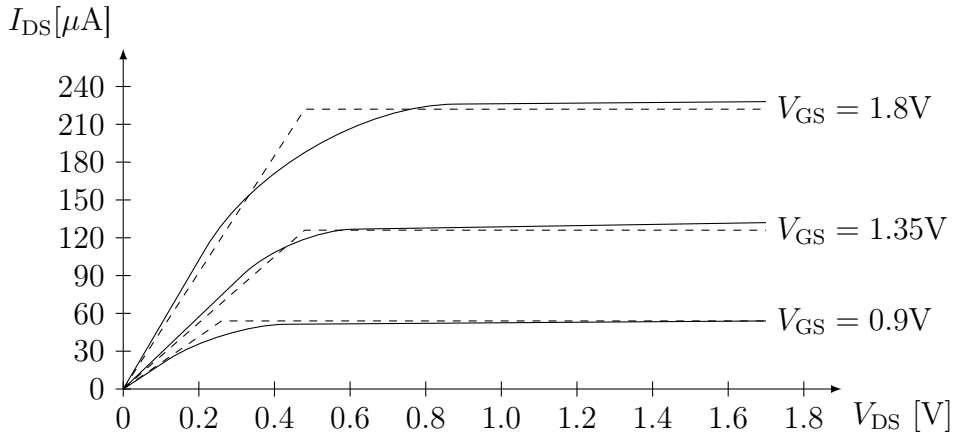

Figure 3.4: I_{DS} versus V_{DS} for NMOS

Using Fig. 3.4 we estimate the saturation value of I_{DS} to $130\mu A$ at $V_{GS} = 1.35V$ and to $220\mu A$ at $V_{GS} = 1.8V$.
The current equation for each measurement is approximated by

$$I_{DS} = K_S \frac{W}{L}(V_{GS} - V_T)^{\alpha} \qquad \text{(Current equation in the saturation range).}$$

It applies:

$$\begin{aligned}
\frac{220\mu A}{130\mu A} &= \frac{K_S(1.8V - 0.5V)^{\alpha}}{K_S(1.35V - 0.5V)^{\alpha}} \\
1.69 &= 1.53^{\alpha} \\
\log 1.69 &= \log 1.53^{\alpha} \\
\log 1.69 &= \alpha \cdot \log 1.53 \\
\alpha &= \frac{\log 1.69}{\log 1.53} = 1.25
\end{aligned}$$

Inserting $\alpha = 1.25$ into the current equation yields

$$\begin{aligned}
130\mu A &= K_S(1.35V - 0.5V)^{1.25} \Rightarrow K_S = 159\frac{\mu A}{V^{1.25}} \\
220\mu A &= K_S(1.8V - 0.5V)^{1.25} \Rightarrow K_S = 158\frac{\mu A}{V^{1.25}} \\
K_S &= 160\mu A/V^{1.25}
\end{aligned}$$

Note that the exponent is near 1. For long channel transistors the exponent is more like 2, for short channel transistors more like 1. To check we calculate the current

$$I_{DS} = 160\frac{\mu A}{V^{1.25}}(0.9V - 0.5V)^{1.25} \approx 50\mu A$$

This value is close to the expected value in Fig. 3.4.