Solution 7.1

We get the sizing in Fig. 7.5. Both inplementations have about the same delay for rising and falling edges as the CMOS inverter.

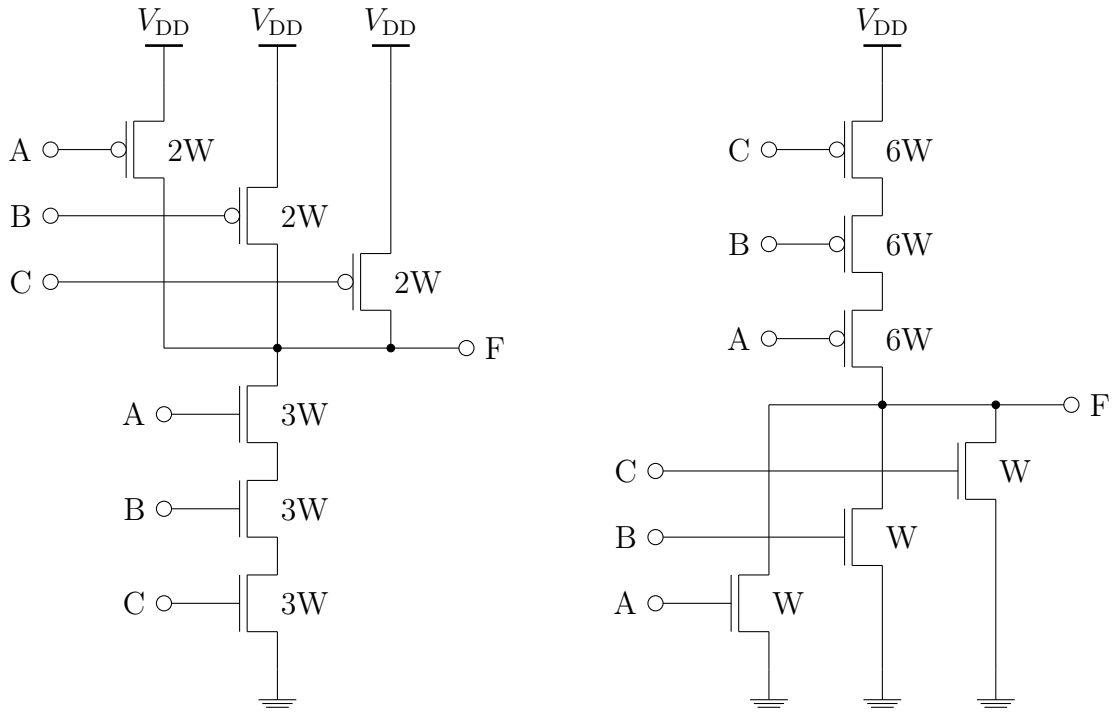

Figure 7.5: NAND3-Gate (a), NOR3-Gate (b)

Solution 7.2

Fig. 7.6 shows the realization of the AND8 function as a two-stage digital circuit. Fig. 7.7 shows the realization of the function AND8 as a three-level digital circuit.

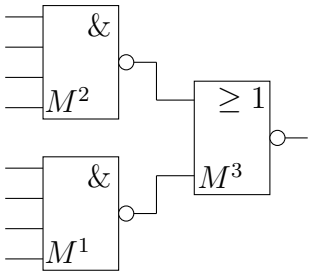

Figure 7.6: NAND4-NOR2

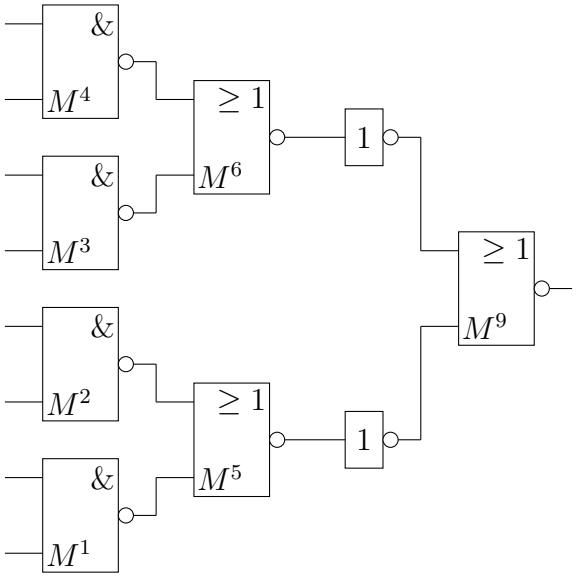

Figure 7.7: NAND2-NOR2-INV-NOR2

Solution 7.3

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a) If one input (i) is at V_{DD} and the other input goes from 0 to V_{DD}, this is equivalent to a pull-up of $W_{\mathrm{P}} = 400\mathrm{nm}$ and a pull-down of $W_{\mathrm{N}} = 400\mathrm{nm}$:

W_{N}=0.4μm W_{P}=0.4μm

$$\chi = \sqrt{\frac{\frac{W_{\mathrm{N}}}{E_{\mathrm{CN}} L_{\mathrm{N}}}}{\frac{W_{\mathrm{P}}}{E_{\mathrm{CP}} L_{\mathrm{P}}}}} = \sqrt{\frac{W_{\mathrm{N}} E_{\mathrm{CP}}}{W_{\mathrm{P}} E_{\mathrm{CN}}}} = \sqrt{\frac{0.4 \cdot 10^{-6}\mathrm{m}(24 \cdot 10^{4}\mathrm{V/cm})}{0.4 \cdot 10^{-6}\mathrm{m}(6 \cdot 10^{4}\mathrm{V/cm})}} = 2.0$$

$$V_{\mathrm{S}} = \frac{V_{\mathrm{DD}} - |V_{\mathrm{TP}}| + \chi V_{\mathrm{TN}}}{1 + \chi} = \frac{1.8\mathrm{V} - |-0.5\mathrm{V}| + 2.0(0.5\mathrm{V})}{1 + 2.0} = 0.77\mathrm{V}$$

If both inputs (ii) go simultaneously from 0 to V_{DD}, this is equivalent to a pull-up of $W_{\mathrm{P}} = 800\mathrm{nm}$ and a pull-down of $W_{\mathrm{N}} = 200\mathrm{nm}$:

W_{N}=0.2μm W_{P}=0.8μm

$$\chi = \sqrt{\frac{\frac{W_{\mathrm{N}}}{E_{\mathrm{CN}} L_{\mathrm{N}}}}{\frac{W_{\mathrm{P}}}{E_{\mathrm{CP}} L_{\mathrm{P}}}}} = \sqrt{\frac{W_{\mathrm{N}} E_{\mathrm{CP}}}{W_{\mathrm{P}} E_{\mathrm{CN}}}} = \sqrt{\frac{0.2 \cdot 10^{-6}\mathrm{m}(24 \cdot 10^{4}\mathrm{V/cm})}{0.8 \cdot 10^{-6}\mathrm{m}(6 \cdot 10^{4}\mathrm{V/cm})}} = 1.0$$

$$V_{\mathrm{S}} = \frac{V_{\mathrm{DD}} - |V_{\mathrm{TP}}| + \chi V_{\mathrm{TN}}}{1 + \chi} = \frac{1.8\mathrm{V} - |-0.5\mathrm{V}| + 1.0(0.5\mathrm{V})}{1 + 1.0} = 0.9\mathrm{V}$$

b) Solution in SPICE:
As expected, the curve with the two connected inputs is on the right side of the transfer characteristic of an inverter. For the transition at A, $V_{\mathrm{S}} = 0.745\mathrm{V}$, for the transition at B, $V_{\mathrm{S}} = 0.721\mathrm{V}$, for A and B is common $V_{\mathrm{S}} \approx 0.9\mathrm{V}$. These values are close to a manual calculation. Hand calculations tend to have slightly higher values due to the approximations for V_{S}. The reason input A returns a slightly

higher value of V_S is because the corresponding transistor has a body effect (V_{SB}) during switching.

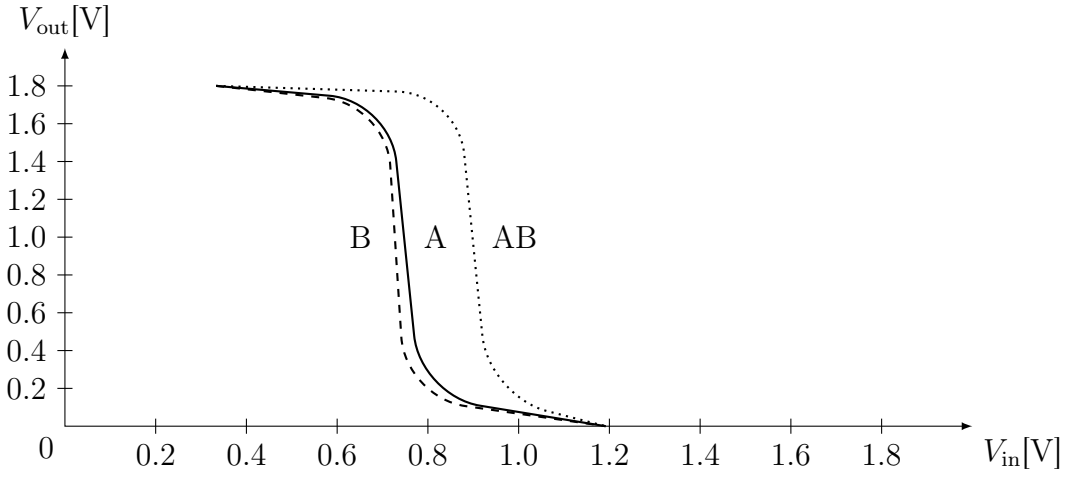

Figure 7.8: Solution in SPICE

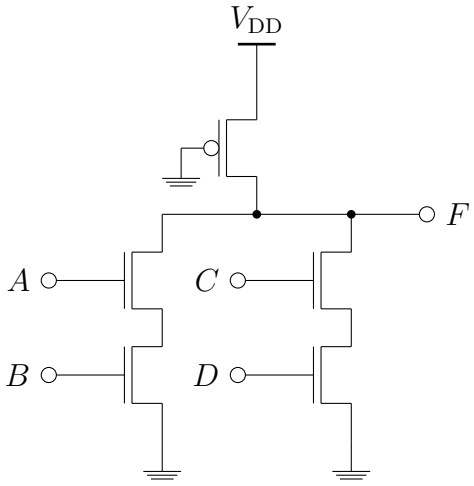

Figure 7.9: Implementation of a Pseudo-NMOS Inverter

Solution 7.4

The n-complex is obtained by coding the zeros as ones.

$$\overline{PD}(A, B, C, D) = AB + CD$$

Thus, two paths with transistors are arranged in series parallel to each other in the n-complex. One path implements AB, the other CD. The dual and component complementary statement of $\overline{PD}$ results in the circuit of the p-complex.

$$PU(A, B, C, D) = (\overline{A} \vee \overline{B})(\overline{C} \vee \overline{D})$$

For the pseudo-NMOS, only the n-complex is needed. The pull-up network consists of a single PMOS transistor. The pseudo-NMOS is therefore more efficient in terms of area than the CMOS (see Fig. 7.9).

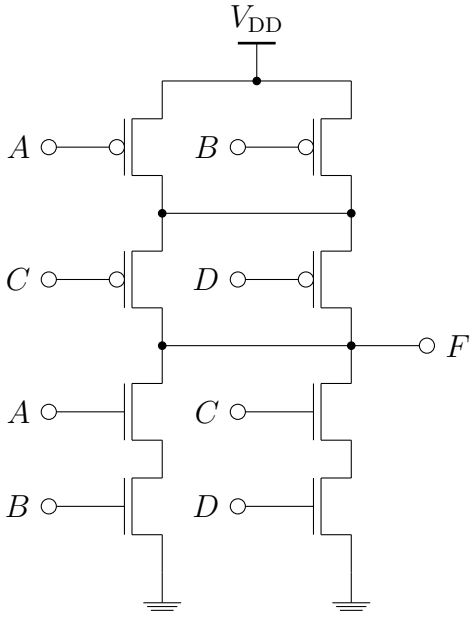

Figure 7.10: Single stage CMOS Complex

Solution 7.5

It applies $V_{OL} = 0\text{V}$ and $V_{OH} = V_{DD}$

A	B	C	D	F
0	0	1	Z	1
0	1	0	0	0
1	0	1	Z	0
1	1	0	0	0

Solution 7.6

In the following, the cross-coupled NOR configuration in Fig. 7.11 is used. To get the desired runtimes we use the relation $t_{PHL} = t_{PLH} = 0.7 R_{eff} C_L$. There is double the runtime from S to Q and from R to $\overline{Q}$. Therefore, we evenly divide the two delays between the two NOR gates. For the n complex, $R_{eqn} = 12.5\text{k}\Omega$ applies.

$$t_{PHL} = 0.7(12.5\text{k}\Omega)\frac{L}{W}(100\text{fF}) = 200\text{ps} \qquad \Leftrightarrow \qquad \frac{W}{L} = 4.4$$

Set $W_N = 440\text{nm}$ for both NMOS gates. For the PMOS gates we then use four times the size of the NMOS gates, $W_P = 1.76\mu\text{m}$.

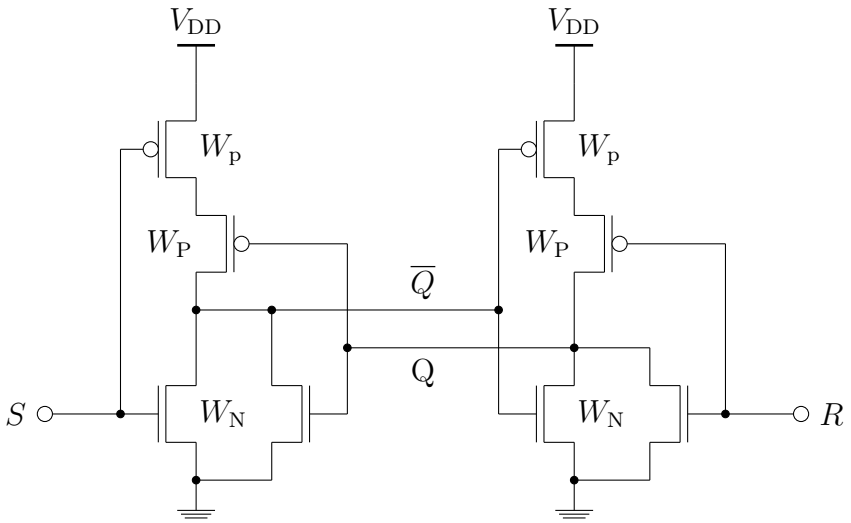

Figure 7.11: Schematic of a RS-Latch

Solution 7.7

Due to the biasing of the NMOS load by the pull-down no VDD-one can be reached.

$$V_{OH} = V_{DD} - V_{TL}(V_{SB}) = V_{DD} - \left(V_{T0} + \gamma\left(\sqrt{V_{SB} + 2|\phi_F|} - \sqrt{2|\phi_F|}\right)\right)$$

Together with $V_{SB} = V_{OH} \neq 0$ bzw. $X = \sqrt{V_{OH} + 2|\phi_F|}$ follows

$$X^2 + 2X\frac{\gamma}{2} + \left(\frac{\gamma}{2}\right)^2 = V_{DD} - V_{T0} + 2|\phi_F| + \gamma\sqrt{2|\phi_F|} + \left(\frac{\gamma}{2}\right)^2$$

with

$$\begin{aligned} V_{DD} - V_{T0} + 2|\phi_F| + \gamma\sqrt{2|\phi_F|} + \left(\frac{\gamma}{2}\right)^2 &= A \\ \left(X + \frac{\gamma}{2}\right)^2 &= A \\ X &= \sqrt{A} - \frac{\gamma}{2} \end{aligned} \tag{7.1}$$

and

$$\begin{aligned} V_{OH} &= \left(\sqrt{A} - \frac{\gamma}{2}\right)^2 - 2|\phi_F| \\ V_{OH} &= A - \gamma\sqrt{A} + \frac{\gamma^2}{4} - 2|\phi_F| \\ V_{OH} &= (V_{DD} - V_{T0}) + \left(\frac{\gamma}{2} + |\sqrt{2|\phi_F|}\right)^2 - \gamma\sqrt{A} + \frac{\gamma^2}{4} - 2|\phi_F| \\ V_{OH} &= (V_{DD} - V_{T0}) + \frac{\gamma}{2}\left(\gamma + 2\sqrt{2|\phi_F|} - 2\sqrt{A}\right) \end{aligned} \tag{7.2}$$

with $B = \gamma + 2\left(\sqrt{2|\phi_F|} - \sqrt{A}\right)$ follows

$$A = 1.2\text{V} - 0.4\text{V} + 0.88\text{V} + 0.2\text{V}^{1/2}\sqrt{0.88\text{V}} + \left(\frac{0.2\text{V}}{2}\right)^2 = 1.8776\text{V}$$

$$B = 0.2\mathrm{V}^{1/2} + 2\left(\sqrt{0.88\mathrm{V}} - \sqrt{1.8776\mathrm{V}}\right) = -0.664\mathrm{V}^{1/2}$$

$$V_{\mathrm{OH}} = 1.2\mathrm{V} - 0.4\mathrm{V} + \frac{0.2\mathrm{V}^{1/2}}{2} \cdot (-0.664\mathrm{V}^{1/2}) = 0.7336\mathrm{V}$$

$$V_{\mathrm{TL}}(V_{\mathrm{OH}}) = 0.4\mathrm{V} + 0.2\mathrm{V}^{1/2}\left(\sqrt{1.8776\mathrm{V}} - \frac{0.2\mathrm{V}^{1/2}}{2} - \sqrt{0.88\mathrm{V}}\right) = 0.4664\mathrm{V}$$

(2nd variant to find V_{OH} see solution 6.1)

$$K_{\mathrm{R}}\frac{\mu_{\mathrm{n}}}{L}\left((V_{\mathrm{DD}} - V_{\mathrm{TI}}) - \frac{V_{\mathrm{OL}}}{2}\right)V_{\mathrm{OL}}\left(\frac{1}{1 + \dfrac{V_{\mathrm{OL}}}{E_{\mathrm{CN}}L}}\right) = \frac{\nu_{\mathrm{sat}}\left(V_{\mathrm{DD}} - V_{\mathrm{OL}} - V_{\mathrm{TL}}\right)^2}{(V_{\mathrm{DD}} - V_{\mathrm{OL}} - V_{\mathrm{TL}}) + E_{\mathrm{CN}}L} \quad (7.3)$$

$$V_{\mathrm{TL}} = V_{\mathrm{T0}} + \gamma\left(\sqrt{V_{\mathrm{OL}} + 2|\phi_{\mathrm{F}}|} - \sqrt{2|\phi_{\mathrm{F}}|}\right) \quad (7.4)$$

Insert V_{OL} in Equ. (7.3) (iterative) and calculate K_{R} (for K_{R}=1 finished)
$\Rightarrow V_{\mathrm{OL}} = 0.165\mathrm{V}$

$$I_{\mathrm{DC}} = W\upsilon_{\mathrm{sat}}C_{\mathrm{ox}}\frac{(V_{\mathrm{DD}} - V_{\mathrm{TL}} - V_{\mathrm{OL}})^2}{(V_{\mathrm{DD}} - V_{\mathrm{TL}} - V_{\mathrm{OL}}) + E_{\mathrm{CN}}L_{\mathrm{N}}}$$

$$I_{\mathrm{DC}} = (0.1 \cdot 10^{-4}\mathrm{cm})(8 \cdot 10^{6}\mathrm{cms}^{-1})(1.6 \cdot 10^{-6}\mathrm{Fcm}^{-2})\frac{(1.2\mathrm{V} - 0.46\mathrm{V} - 0.165\mathrm{V})^2}{(1.2\mathrm{V} - 0.46\mathrm{V} - 0.165\mathrm{V}) + 0.6\mathrm{V}} = 36\mu\mathrm{A}$$

$$P_{\mathrm{DC}} = I_{\mathrm{DC}}V_{\mathrm{DD}} = 36\mu\mathrm{A} \cdot 1.2\mathrm{V} = 43.2\mu\mathrm{W}$$