Task 3.1

	symbol	NMOS	PMOS
n-doping of gate [cm^{-3}]	N_D	$3 \cdot 10^{20}$	-
p-doping of gate [cm^{-3}]	N_A	-	$3 \cdot 10^{20}$
p-doping of substrate [cm^{-3}]	N_A	$3 \cdot 10^{17}$	-
n-doping of well [cm^{-3}]	N_D	-	$3 \cdot 10^{17}$
amount of surface charge [cm^{-2}]	N_SS	$6 \cdot 10^{11}$	$6 \cdot 10^{11}$

Table 3.1: Process parameters in 0.13μm technology

In Tab. 3.1 process parameters of a 0.13μm technology are given.

a) Calculate the non-implanted and non-substrate biased threshold voltages of a NMOS and a PMOS transistor. The thickness of the oxide is $t_\mathrm{ox} = 22\text{Å}$ and the surface charge density at the Si-SiO_2 boundary layer (qN_SS).

b) Normally, a NMOS gate is doped with donors and a PMOS gate is doped with acceptors. How does V_T0 change if a PMOS gate is doped with donors instead of acceptors? Calculate the new V_T0.

c) The threshold voltage of a NMOS transistor and a PMOS transistor is now set to $V_\mathrm{T0p} = 0.4\mathrm{V}$ and $V_\mathrm{T0n} = -0.4\mathrm{V}$. Calculate the implanted threshold voltage level for the two cases in a) and the single case in b).

d) Why do modern technologies have a n^+ gate for NMOS transistors and a p^+ gate for PMOS transistors?

e) Calculate the effective mobility μ_e of a PMOS transistor based on its vertical field. It is $\mu_0 = 130\ \mathrm{cm^2V^{-1}s^{-1}}$, $\theta = 4 \cdot 10^6\mathrm{Vcm^{-1}}$ and $\eta = 1.85$.

Task 3.2

a) Calculate the voltage V_Dsat for NMOS and PMOS transistors in 0.18μm technology ($V_\mathrm{DD} = 1.8\mathrm{V}$, $L = 200\mathrm{nm}$, $V_\mathrm{TN} = 0.5\mathrm{V}$, $V_\mathrm{TP} = -0.5\mathrm{V}$).

b) Calculate V_Dsat for the two transistors in 0.13μm technology ($E_\mathrm{cn}L_\mathrm{n} = 0.6\mathrm{V}$, $E_\mathrm{cp}L_\mathrm{p} = 2.4\mathrm{V}$, $V_\mathrm{DD} = 1.2\mathrm{V}$, $L = 100\mathrm{nm}$, $V_\mathrm{TN} = 0.4\mathrm{V}$, $V_\mathrm{TP} = -0.4\mathrm{V}$).

c) Calculate the ratio of saturation currents for NMOS and PMOS transistors in 0.13μm technology ($T = 400\mathrm{K}$).

Task 3.3

This task concerns I-V characteristics of NMOS and PMOS transistors in 0.13μm technology. Given is the supply voltage $V_{\mathrm{DD}} = 1.2\mathrm{V}$ and the unit dimensions $W = 100\mathrm{nm}$ and $L = 100\mathrm{nm}$.

a) Plot I_{DS} over V_{DS} as a function of $V_{\mathrm{GS}} = 1.2\mathrm{V}$ and $V_{\mathrm{SG}} = 0.4\mathrm{V}$, 0.8V and 1.2V for both NMOS and PMOS transistors.

b) For NMOS transistors, plot I_{DS} over V_{GS} with $V_{\mathrm{DS}} = 1.2\mathrm{V}$. Is the quadratic model still valid for 0.13μm technologies?

Task 3.4

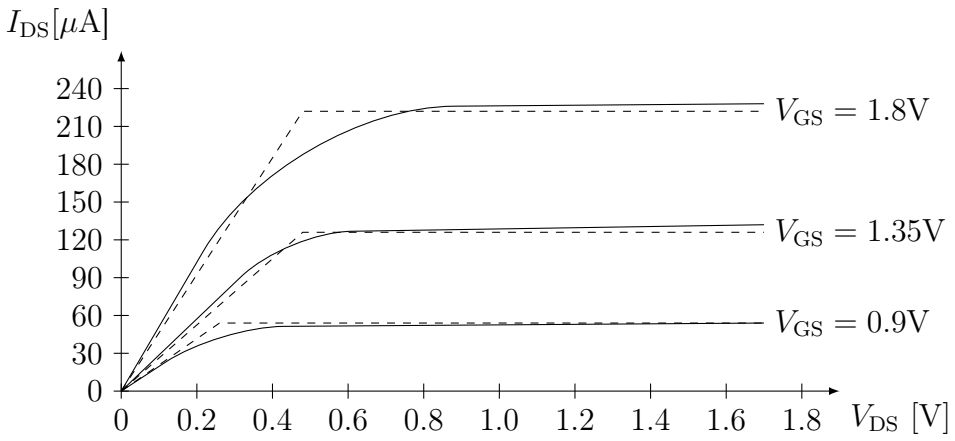

Figure 3.1: I_{DS} versus V_{DS} for NMOS

Provide the parameters (K_{s}, α) of the Alpha Power Law model (in saturation) of the NMOS transistor in Fig. 3.1. The assumption is $W/L = 1$ and $V_{\mathrm{T}} = 0.5\mathrm{V}$.

$$I_{\mathrm{DS}} = K_{\mathrm{S}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{T}})^{\alpha} \qquad \text{(Current equation in saturation range).}$$