Task 13.1 Dimensioning a Decoder

Dimension the two-stage decoder from Fig. 13.1 (FO4, $C_{\mathrm{L}} = 1$, $SE^* = 4$). The predecoder consists of 12 NANDs, the final decoder of 64 NANDs. For each level $C_{\mathrm{in}} = LE \cdot BE \cdot C_{\mathrm{out}}/SE^*$.

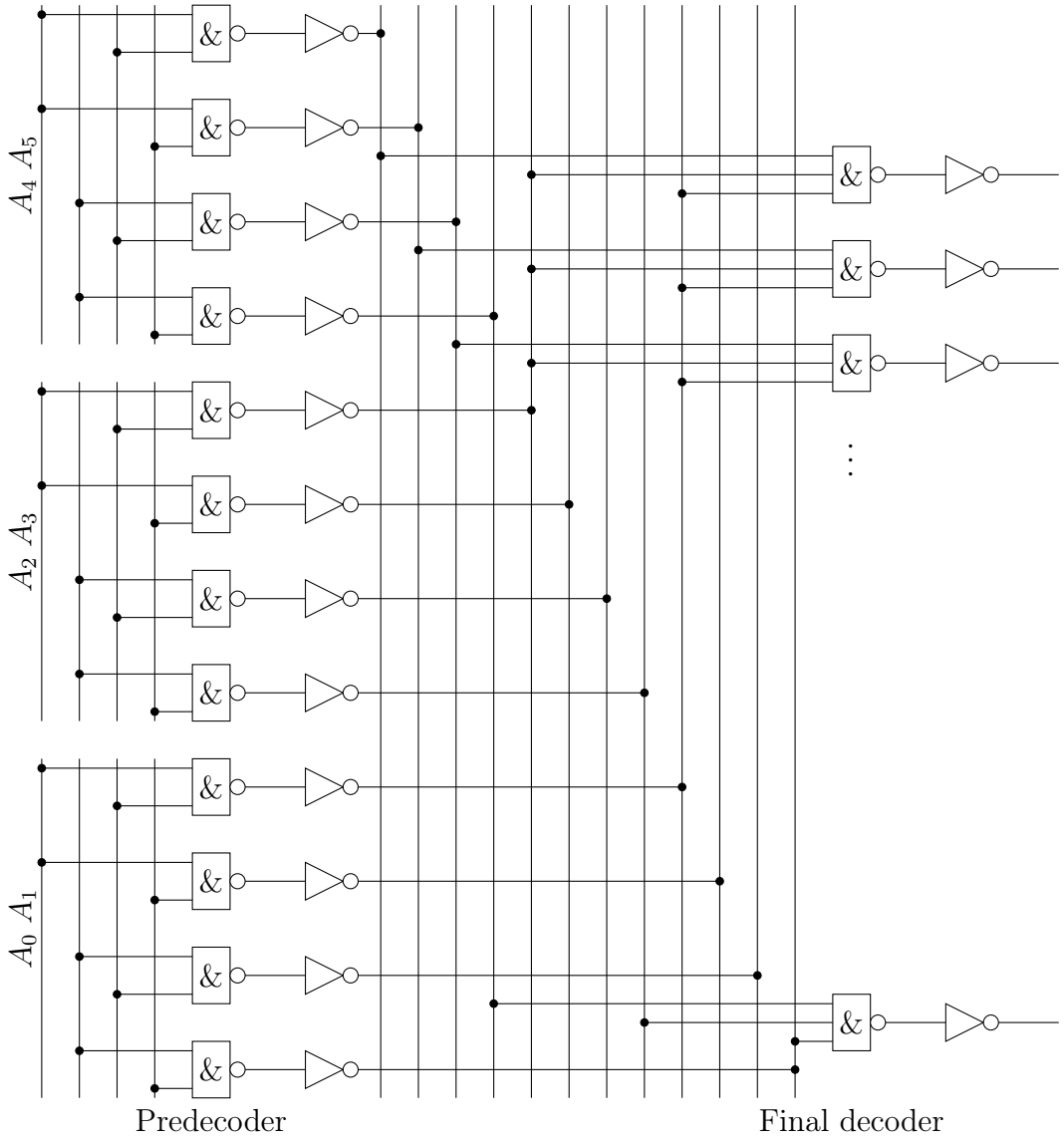

Figure 13.1: 2-stage 6-bit decoder

Task 13.2 Design Rules for a Read Cycle

Calculate the width of M1 and M3 for Read in Fig. 13.3. Tolerate a voltage increase of 0.1V in q. ($C_{\text{bit}} = 2\text{pF}$, 200mV Transition of the bitline in 2ns, 0.13μm Technologyparameter: $\mu_{\text{n}} = 270\text{cm}^2/\text{Vs}$, $C_{\text{ox}} = 1.6\mu\text{F/cm}^2$, $V_{\text{TN}} = 0.4\text{V}$, $V_{\text{DD}} = 1.2\text{V}$, $L = 100\text{nm}$, $E_{\text{CN}}L_{\text{N}} = 0.6\text{V}$, $v_{\text{sat}} = 8 \cdot 10^6\text{cm/s}$).

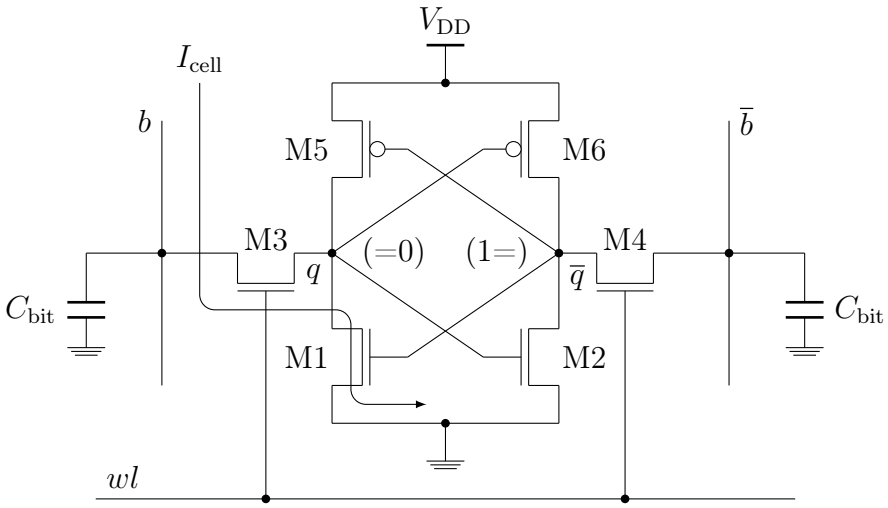

Figure 13.2: Read from a SRAM

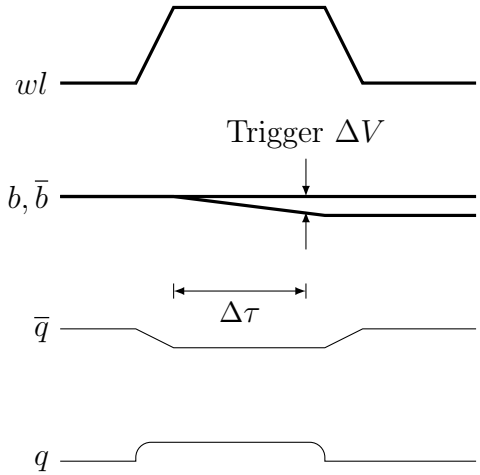

Figure 13.3: (6T) SRAM Cell (Read Operation)

Task 13.3 Word- and Bitlines

For access transistors with $W/L = 0.5\mu\text{m}/0.1\mu\text{m}$ the cell layout of a 64K SRAM is shown in Fig. 13.4. Calculate the capacities of the word lines and bitlines. The contacts on the bitlines share pairs of cells, the capacitance of a contact is 0.5fF. The line capacitance is $0.2\text{fF}/\mu\text{m}$. Use the parameters of a $0.13\mu\text{m}$ technology. The cell layout is 40λ to 30λ, ($1\mu\text{m} = 20\lambda$).

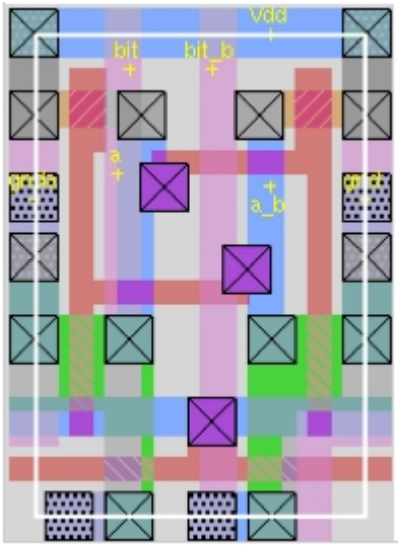

Figure 13.4: SRAM Cell Layout