Solution 9.1

It applies $t_P = R_{on}C_{load}$.

a) For the falling and rising edge follow $t_{PHL} = (12.5k\Omega)(L/W)(10.8fF) \approx 68ps$ and $t_{PLH} = (30k\Omega)(L/W)(10.8fF) \approx 81ps$. The average FO4 delay of the inverter is $t_P = (t_{PHL} + t_{PLH})/2 = 74.5ps$.

b) For the falling and rising edge follow $t_{PHL} = (12.5k\Omega)(L/W)(2.4fF + 1.2fF) = 22.5ps$ and $t_{PLH} = (30k\Omega)(L/W)(2.4fF + 1.2fF) = 27ps$. The total delay is $\tau_{total} = 2(t_{PHL} + t_{PLH}) = 99ps$.

Solution 9.2

$$\tau_{inv} = 3R_{eqn}C_gL_n = 3(12.5k\Omega)(2fF/\mu m)(0.1\mu m) = 7.5ps$$

$$\gamma_{inv} = \frac{C_{self}}{C_{in}} = \frac{C_{eff}(3W)}{C_g(3W)} = \frac{1fF/\mu m}{2fF/\mu m} = 0.5$$

Solution 9.3

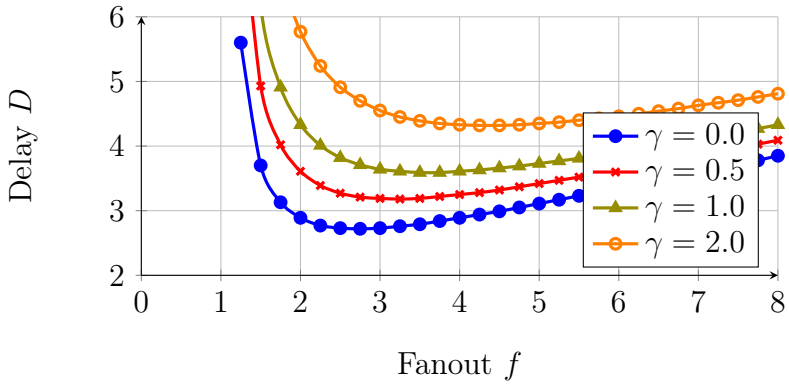

Figure 9.4: Normalized Delay D versus Fanout f

$$N \cdot \ln(f) = \ln\left(\frac{C_{load}}{C_{in}}\right) \Leftrightarrow \ln(f) = \frac{1}{3}\ln\left(\frac{200fF}{1fF}\right) \Rightarrow f = 5.84$$

The optimal fanout of three stages is 5.84. If we want to reduce the delay, we have to remove the limitation to the number of stages.
To resolve $N = \ln(C_{load}/C_{in})/ln(f)$ to N, we estimate the minimum of $\gamma = 0.5$ in Fig. 6.23 (see book), $f \approx 3.6$. With $N = \ln(200)/\ln(3.6) \approx 4\ln(f) = (1/4)\ln(200)$ and thus $f = 3.8$. It follows for 3 inverters in chain total_delay $= N \cdot \tau_{inv}(C_j/C_{j\text{-}1} + \gamma_{inv}) = 3 \cdot (7.5ps)(5.84 + 0.5) = 142.8ps$ and for 4 inverters in chain total_delay $= 4 \cdot (7.5ps)(3.8 + 0.5) = 128ps$. So the better solution are four inverters in chain, each inverter is 3.8 larger than the previous inverter.

Solution 9.4

By the fanout portion of the delay (Fanout Delay),

$$\tau_{\text{nand}}\frac{C_{\text{j+1}}}{C_{\text{in}}} = \tau_{\text{inv}}\frac{C_{\text{j+2}}}{C_{\text{j+1}}} = \tau_{\text{nor}}\frac{C_{\text{load}}}{C_{\text{j+2}}}$$

we calculate the geometric mean:

$$\begin{aligned}
\text{fanout_delay} &= \sqrt[3]{\tau_{\text{nand}}\left(\frac{C_{\text{j+1}}}{C_{\text{in}}}\right)\cdot\tau_{\text{inv}}\left(\frac{C_{\text{j+2}}}{C_{\text{j+1}}}\right)\cdot\tau_{\text{nor}}\left(\frac{C_{\text{load}}}{C_{\text{j+2}}}\right)} \\
&= \sqrt[3]{\tau_{\text{nand}}\cdot\tau_{\text{inv}}\cdot\tau_{\text{nor}}\cdot\left(\frac{C_{\text{load}}}{C_{\text{in}}}\right)} \\
&= \sqrt[3]{4\cdot 3\cdot 5\left(\frac{200\text{fF}}{2\text{fF}}\right)\cdot(R_{\text{eqn}}C_{\text{g}}L_{\text{n}})^3} \\
&= 18.2R_{\text{eqn}}C_{\text{g}}L_{\text{n}}
\end{aligned}$$

With $\tau_{\text{inv}} = 3R_{\text{eqn}}C_{\text{g}}L_{\text{n}}$, $\tau_{\text{nand}} = 4R_{\text{eqn}}C_{\text{g}}L_{\text{n}}$ and $\tau_{\text{nor}} = 5R_{\text{eqn}}C_{\text{g}}L_{\text{n}}$ then the input capacity for each gate can be calculated by setting the fanout delay:

$$\begin{aligned}
\tau_{\text{nor}}\frac{C_{\text{load}}}{C_{\text{j+2}}} = 5R_{\text{eqn}}C_{\text{g}}L_{\text{n}}\left(\frac{200\text{fF}}{C_{\text{j+2}}}\right) = 18.2R_{\text{eqn}}C_{\text{g}}L_{\text{n}} &\Rightarrow C_{\text{j+2}} = 55\text{fF} \\
\tau_{\text{inv}}\frac{C_{\text{j+2}}}{C_{\text{j+1}}} = 3R_{\text{eqn}}C_{\text{g}}L_{\text{n}}\left(\frac{55\text{fF}}{C_{\text{j+1}}}\right) = 18.2R_{\text{eqn}}C_{\text{g}}L_{\text{n}} &\Rightarrow C_{\text{j+1}} = 9.1\text{fF} \\
\tau_{\text{nand}}\left(\frac{C_{\text{j+1}}}{C_{\text{in}}}\right) = 4R_{\text{eqn}}C_{\text{g}}L_{\text{n}}\left(\frac{9.1\text{fF}}{C_{\text{in}}}\right) = 18.2R_{\text{eqn}}C_{\text{g}}L_{\text{n}} &\Rightarrow C_{\text{in}} = 2\text{fF}
\end{aligned}$$

The last line is consistent with the specified input capacity. The dimensions are then sized with the respective ratios of W_{N} to W_{P} (see Fig. 6.4 in the book). The result for the NAND gate ($C_{\text{in}} = 2\text{fF}$) is $W_{\text{P}} = W_{\text{N}} = 0.5\mu\text{m}$, for the inverter ($C_{\text{in}} = 9.1\text{fF}$) $W_{\text{P}} = 3\mu\text{m}$ and $W_{\text{N}} = 1.5\mu\text{m}$ and for the NOR gate ($C_{\text{in}} = 55\text{fF}$) $W_{\text{P}} = 22\mu\text{m}$ and $W_{\text{N}} = 5.5\mu\text{m}$.

Solution 9.5

We need to balance the LE·FO share for the delay of all gates. With Tab. 9.1 results are:

$$\begin{aligned}
\text{total_path_effort} &= LE_{\text{nand}}\cdot LE_{\text{inv}}\cdot LE_{\text{nor}}\cdot\left(\frac{C_{\text{load}}}{C_{\text{in}}}\right) = 222.2 \\
\text{stage_effort} &= \sqrt[3]{222.2} = 6
\end{aligned}$$

This is the fanout portion of the delay. The normalized path delay is then three times larger than the parasitic values P_{nand}, P_{inv} und P_{nor} from Tab. 9.2. Es ergibt sich $D = (LE_{\text{nand}}\cdot FO_1 + P_{\text{nand}}) + (LE_{\text{inv}}\cdot FO_2 + P_{\text{inv}}) + (LE_{\text{nor}}\cdot FO_3 + P_{\text{nor}}) = 3(6) + P_{\text{nand}} + P_{\text{inv}} + P_{\text{nor}} = 18 + 1 + (1/2) + (3/2) = 21$. The physical delay results from multiplication

with the reference $\tau_{\text{inv}} = 7.5\text{ps}$, min_path_delay $= \tau_{\text{inv}} \cdot D = (7.5\text{ps})(21) = 157.5\text{ps}$. Under the assumption that the delays are acceptable, we calculate the sizes sought backwards from the exit to the entrance:

$$LE_{\text{nor}}\left(\frac{C_{\text{out}}}{C_{\text{j+2}}}\right) = 6 \quad \Leftrightarrow \quad LE_{\text{nor}}\left(\frac{C_{\text{j+3}}}{6}\right) = C_{\text{j+2}} = (5/3)\left(\frac{200fF}{6}\right) = 55\text{fF}$$

$$LE_{\text{inv}}\left(\frac{C_{\text{j+2}}}{C_{\text{j+1}}}\right) = 6 \quad \Leftrightarrow \quad LE_{\text{inv}}\left(\frac{C_{\text{j+2}}}{6}\right) = C_{\text{j+1}} = (1)\left(\frac{55\text{fF}}{6}\right) = 9.1\text{fF}$$

$$LE_{\text{nand}}\left(\frac{C_{\text{j+1}}}{C_{\text{in}}}\right) = 6 \quad \Leftrightarrow \quad LE_{\text{nand}}\left(\frac{C_{\text{j+1}}}{6}\right) = C_{in} = (4/3)\left(\frac{9.1\text{fF}}{6}\right) = 2\text{fF}$$

These are the same results as in solution 9.4. The minimum delay can therefore be determined without sizing the gates. This is one of the most important advantages of LE. If the delay is not within the specification, the logic can be exchanged until a satisfactory solution is reached. Once the specification is met, the gates can be sized.

Solution 9.6

First we calculate the total_path_effort and optimal_stage_effort.

$$\text{total\_path\_effort} = \prod (LE \cdot FO) = 1\left(\frac{X}{10}\right) \cdot (\frac{5}{3})\left(\frac{Y}{X}\right) \cdot (\frac{4}{3})\left(\frac{Z}{Y}\right) \cdot 1\left(\frac{20}{Z}\right) = \frac{400}{90}$$

$$\text{stage\_effort} = \left(\frac{400}{90}\right)^{(1/4)} = 1.45$$

The normalized total path delay results in $D = 4SE^* + 2P_{\text{inv}} + P_{\text{nor}} + P_{\text{nand}} = 4(1.45) + 1.0 + 1.5 + 1.0 = 9.3$. The searched sizes are calculated again backwards from the output. With $C_{\text{in}} = LE \cdot C_{\text{out}}/SE^*$ we get $Z = (1) \cdot (20)/(1.45) = 13.8$, $Y = (4/3) \cdot (Z)/(1.45) = 12.7$, $X = (5/3) \cdot (Y)/(1.45) = 14.5$ und $C_{\text{in}} = (1) \cdot (X)/(1.45) = 10$. The input capacity $C_{\text{in}} = 10$ is confirmed again.

Solution 9.7

The self capacitances are as follows:

a) $C_{\text{self}} = (0.5 \cdot 2 + 0.5 + 0.25 \cdot 2)(2W) + (0.5 + 0.25)(3W) + (0.5 \cdot 2 + 0.25 \cdot 3)(2/3)(3W) + 0.5(5/6)(3W) = 4W + 2.25W + 3.5W + 1.25W = 11W$

b) $C_{\text{self}} = (0.5 \cdot 2 + 0.5 + 0.25 \cdot 2)(2W) + (0.5 + 0.25)(3W) + (0.5 + 0.25)(2/3)(3W) + 0.5(5/6)(3W) = 4W + 2.25W + 1.5W + 1.25W = 9W$

c) $C_{\text{self}} = (0.5 \cdot 2 + 0.5 \cdot 2 + 0.25)(2W) + (0.5 + 0.25)(3W) + (0.5 + 0.25)(2/3)(3W) + 0.5(5/6)(3W) = 4.5W + 2.25W + 1.5W + 1.25W = 9.5W$

d) $C_{\text{self}} = (0.5 \cdot 2 + 0.5 \cdot 2 + 0.25)(2W) + (0.5 + 0.5)(3W) = 4.5W + 3W = 7.5W$