Task 1.1

Provide in logic NAND gates the logic circuits called EXCLUSIVE-OR (XOR), NON-EXCLUSIVE-OR (XNOR) and 2-Input Multiplexer (MUX):

Task 1.2

Create the circuits from the expressions below using logic NAND gates:

$F_1 = AC \vee BC$
$F_2 = (A \vee B)(\overline{C} \vee B)$

Task 1.3

Calculate the complement:

a) $F = \overline{A}\,\overline{B}\,C \vee \overline{A}\,B\,\overline{C} \vee A\,B\,\overline{C}$

b) $F = A\,B\,C \vee \overline{A}\,\overline{B}\,C$

c) $F = A\,B\,C \vee A\,B\,\overline{C} \vee A\,\overline{B}$

Task 1.4

An RS latch with respect to NOR gates is given.

a) Provide the circuit structure:

b) Present the logic automaton graph:

c) Construct the reduced switching table:

Task 1.5

The JK-FF is given as a logic block.

a) Construct the switching table (excitation table):

b) Construct the reduced switching table:

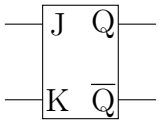

Figure 1.1: Block diagram of the JK-FF

Task 1.6

A current source I is connected to a capacitor C with an initial voltage of 0V, as shown in Fig. 1.2. The capacitor has a capacitance of 25fF. What current has I to drive for a voltage value of 0.6V to be reached in 30ps? Provide the answer in units [mA].

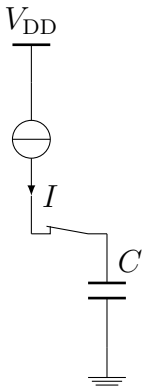

Figure 1.2: Current-driven capacitance

Task 1.7

The step $V_{in} = 1.2V$ is applied to the RC circuit in Fig. 1.3. Calculate the delay it takes to rise the voltage at the capacitor

a) to 0.6V:

b) to 1.2V:

c) from 10% to 90% of 1.2V:

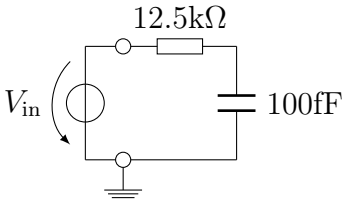

Figure 1.3: RC circuit

Task 1.8

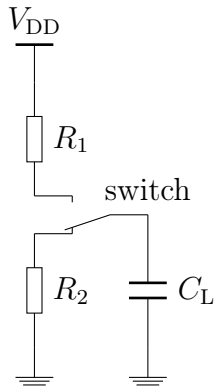

Figure 1.4: Switched RC network

A switch is used in Fig. 1.4 to connect a capacitor C_L via a resistance R_1 to V_{DD}, or via a resistance R_2 to GND. The values of the elements are $(R_1, R_2, C_L) = (30k\Omega, 12.5k\Omega, 1\mu F)$. The voltage across the capacitance is 0V.

a) The switch is now set to R_1. How long does it take the capacitance to charge to 0.6V ($V_{DD}/2$):

b) The voltage across the capacitance is 1.2V. The switch is now set to R_2. How long does it take the capacitance to discharge to 0.6V ($V_{DD}/2$):

c) Calculate the ratio of the two delays from a) and b):

Task 1.9

In 0.18μm technology a chip of the dimensions 1cm×1cm carries about 50 million transistors. According to Moor's law, how many transistors can be integrated on a chip of the same size in 0.13μm technology?

Task 1.10

A processor clocks at 2GHz ($2 \cdot 10^9$Hz). Now the processor speed doubles with each new technology. How many generations of technology will it take to reach 10GHz? How long does it take if each new technology generation lasts for 3 years?