Task 11.1

Calculate the Logical Effort (LE) of A and S in Fig. 11.1.

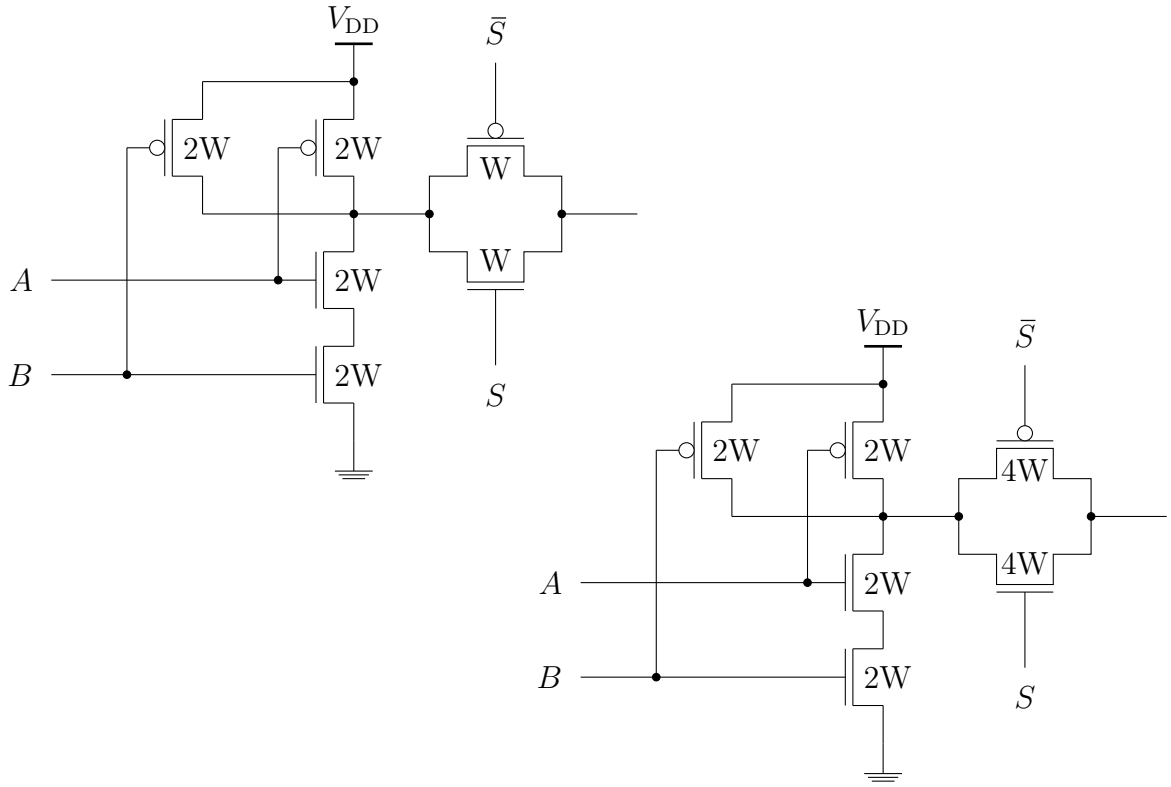

Abbildung 11.1: Logical Effort of a CMOS TG driven by a NAND

Task 11.2

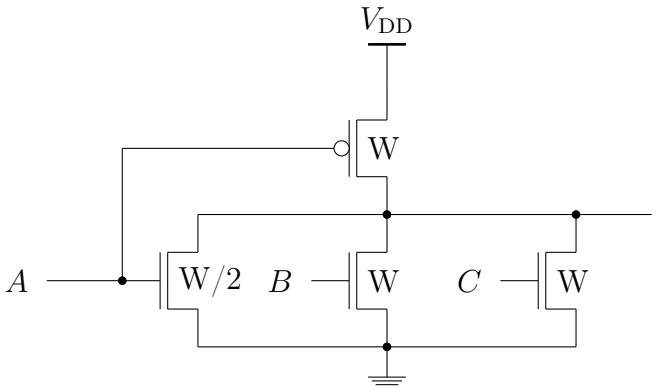

Abbildung 11.2: Special Pseudo-NMOS Gate

As shown in Fig. 11.2, there is a possibility to improve the power dissipation of a pseudo NMOS gate by linking its pull-up to an input. This also reduces the size of the corresponding pull-down to W/2. The input, here A, then behaves like a static CMOS inverter,

the other inputs, here B and C, still behave like a pseudo-NMOS inverter. The power losses for A from LOW to HIGH are less than for B and C from LOW to HIGH. Of course, this type of switching is only suitable if A - if it is switched - is switched before B and C.

a) What is the LE of input A:

b) What is the LE of the inputs B or C:

Task 11.3

Which of the multiplexers in Fig. 11.3 and Fig. 11.4 is the faster in accordance of a

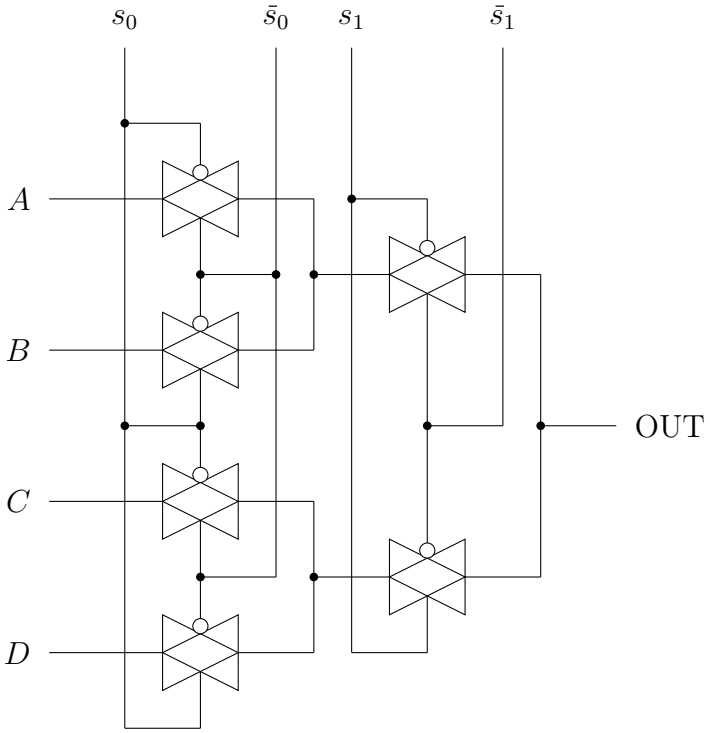

Abbildung 11.3: Two-Level Multiplexer (2MUX)

path from input to output. Each input is driven by a 1X inverter. The fanout of the multiplexer is f times larger than that of a 1X inverter.

Task 11.4

Use a NAND3 and NOR4 to show that the logical effort of a gate does not change with the pull-down and pull-up being scaled at the same time.

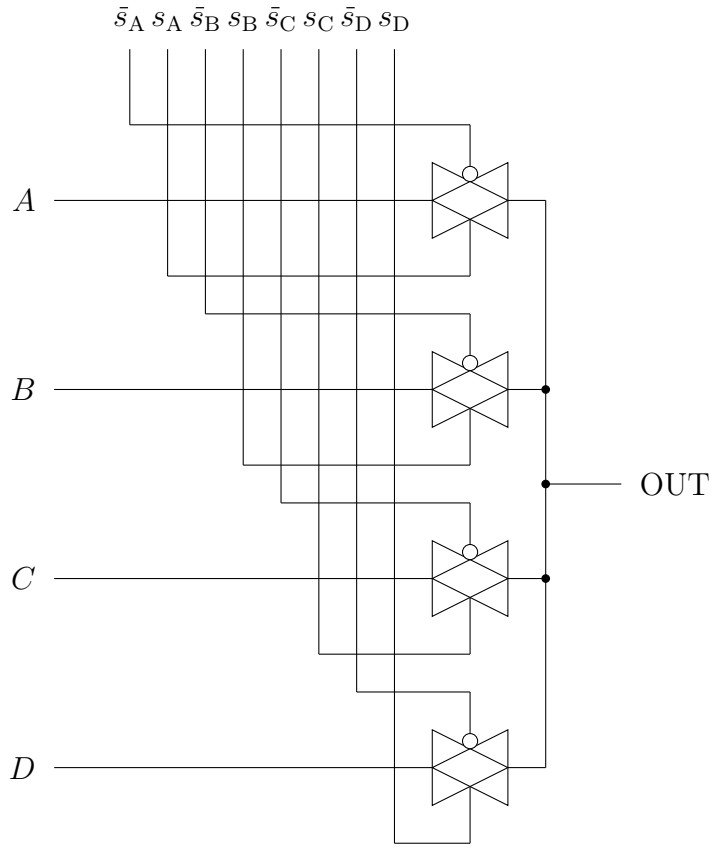

Abbildung 11.4: Single-Level Multiplexer (1MUX)

Task 11.5

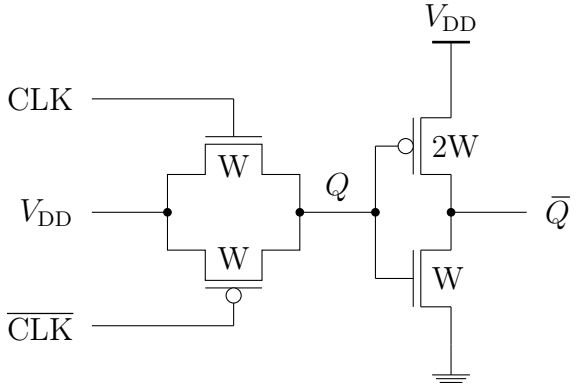

Abbildung 11.5: Dynamic D-Latch

For the dynamic D latch in Fig. 11.5 estimate the values for Q and $\overline{Q}$, for a clock from LOW to HIGH and from HIGH to LOW. Consider Clock Feedthrough. Then calculate the delay from $\overline{Q}$ (CLK from LOW to HIGH). Use the parameters of a 0.18μm CMOS technology ($W = L = 200$nm, $C_{ox} = 1\mu\text{F/cm}^2$, $V_{TN} = 0.5$V, $V_{TP} = -0.5$V, $V_{DD} = 1.8$V).