Solution 10.1

With clock feedthrough, changes in the voltage of a driven node are switched through to an isolated node proportionally to the coupling capacitance. The voltage jumps at the capacitance.
In contrast to this, charge sharing equalizes different node potentials of two isolated nodes in the event of an abrupt connection between them.

Solution 10.2

All nodes are initially set to 0V. First we calculate the input voltages for the gate nodes of the first row of the voltage field, $V_{\mathrm{DD}} - V_{\mathrm{T}}(V_{\mathrm{out}})$. The resulting source voltages of the first row are also input voltages for the gate nodes of the second row of the voltage field, $V_{\mathrm{DD}} - 2V_{\mathrm{T}}(V_{\mathrm{out2}})$.
The same applies to the gate nodes of the third line of the voltage field $V_{\mathrm{DD}} - 3V_{\mathrm{T}}(V_{\mathrm{out3}})$. However, this value is below 0V (GND).

$$\begin{aligned}
V_{\mathrm{out}} &= V_{\mathrm{DD}} - V_{\mathrm{T}} = V_{\mathrm{DD}} - V_{\mathrm{T}}(V_{\mathrm{SB}}) \\
&= V_{\mathrm{DD}} - (V_{\mathrm{T0}} + \gamma(\sqrt{V_{\mathrm{SB}} + 2|\phi_{\mathrm{F}}|} - \sqrt{2|\phi_{\mathrm{F}}|})) \\
&= 1.2\mathrm{V} - (0.4\mathrm{V} + 0.2\mathrm{V}^{1/2}(\sqrt{V_{\mathrm{out}} + 2|\text{-}0.44\mathrm{V}|} - \sqrt{2|\text{-}0.44\mathrm{V}|})) \\
&= 0.8\mathrm{V} - 0.2\mathrm{V}^{1/2}\sqrt{V_{\mathrm{out}} + 0.88\mathrm{V}} + 0.2\mathrm{V}^{1/2}\sqrt{0.88\mathrm{V}} \\
&= 0.99\mathrm{V} - 0.2\mathrm{V}^{1/2}\sqrt{V_{\mathrm{out}} + 0.88\mathrm{V}}
\end{aligned}$$

Solution by iteration, starting with the optimistic value $V_{\mathrm{out}} = 1.2\mathrm{V}$:

	${}^{\mathrm{a}}V_{\mathrm{out}}$	${}^{\mathrm{n}}V_{\mathrm{out}}$
i=1	1.20V	0.70V
i=2	0.70V	0.74V
i=3	0.74V	0.73V
	0.73V	0.73V

We also calculate V_{out2} and V_{out3}.

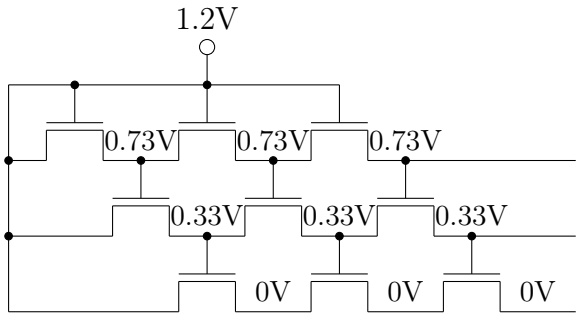

Figure 10.4: Multi-Voltage-Array

Solution 10.3

First V_Q is calculated.

$$\begin{aligned} V_\mathrm{Q} &= V_\mathrm{DD} - V_\mathrm{T} = V_\mathrm{DD} - \left(V_\mathrm{T0} + \gamma\left(\sqrt{V_\mathrm{SB} + 2|\Phi_\mathrm{F}|} - \sqrt{2|\Phi_\mathrm{F}|}\right)\right) \\ &= 1.8\mathrm{V} - \left(0.5\mathrm{V} + 0.3\mathrm{V}^{1/2}\left(\sqrt{V_\mathrm{Q} + 0.85\mathrm{V}} - \sqrt{0.85\mathrm{V}}\right)\right) = 1.15\mathrm{V} \end{aligned}$$

Since this is slightly below 1.3V (voltage at which the PMOS is switched on), it is assumed that the PMOS is „ON“. V_SG of the PMOS is relatively low and V_SD of the PMOS is relatively high. It is very likely that the transistor is in saturation. Similarly for the NMOS, its V_GS is HIGH and its V_DS is LOW. It is most likely in the linear range. Therefore $I_\mathrm{SDP}(\mathrm{sat}) = I_\mathrm{DSN}(\mathrm{lin})$:

$$\frac{W_\mathrm{P} v_\mathrm{sat} C_\mathrm{ox}(V_\mathrm{SGP} - |V_\mathrm{TP}|)^2}{V_\mathrm{SGP} - |V_\mathrm{TP}| + E_\mathrm{CP} L_\mathrm{P}} = \frac{W_\mathrm{N}\mu_\mathrm{N} C_\mathrm{ox}\left((V_\mathrm{GSN} - V_\mathrm{TN})V_\mathrm{DSN} - (V_\mathrm{DSN}^2/2)\right)}{L_\mathrm{N}(1 + V_\mathrm{DSN}/(E_\mathrm{CN} L_\mathrm{N}))}$$

$$\frac{W_\mathrm{P} v_\mathrm{sat} C_\mathrm{ox}(V_\mathrm{DD} - V_\mathrm{Q} - V_\mathrm{T})^2}{V_\mathrm{DD} - V_\mathrm{Q} - V_\mathrm{T} + E_\mathrm{CP} L_\mathrm{P}} = \frac{W_\mathrm{N}\mu_\mathrm{N} C_\mathrm{ox}\left((V_\mathrm{Q} - V_\mathrm{T})V_{\overline{\mathrm{Q}}} - (V_{\overline{\mathrm{Q}}}^2/2)\right)}{L_\mathrm{N}(1 + V_{\overline{\mathrm{Q}}}/(E_\mathrm{CN} L_\mathrm{N}))}$$

With $(1 + V_{\overline{\mathrm{Q}}}/(E_\mathrm{CN} L_\mathrm{N})) \approx 1$ and $\left(V_{\overline{\mathrm{Q}}}^2/2\right) \approx 0$ follows $V_{\overline{\mathrm{Q}}} \approx 0.0080\mathrm{V}$.

For the clock from HIGH to LOW, a feedthrough occurs at node Q. To determine it, we need all involved capacities. The capacity between clock and node Q is $C_\mathrm{GS} = C_\mathrm{OL} = (0.25\mathrm{fF}/\mu\mathrm{m})(0.2\mu\mathrm{m}) = 0.05\mathrm{fF}$, die Kapazität zwischen Knoten Q and GND is $C_\mathrm{Q} = C_\mathrm{SBN} + C_\mathrm{in,inv} = C_\mathrm{j}W + 3C_\mathrm{g}W = (0.5)(0.2)\mathrm{fF} + 3(2)(0.2)\mathrm{fF} = 1.38\mathrm{fF}$. Thus the following applies

$$\Delta V_\mathrm{Q} = \frac{C_\mathrm{GS}\Delta V_\mathrm{CLK}}{C_\mathrm{GS} + C_\mathrm{Q}} = \frac{0.05\mathrm{fF}(\text{-}1.8\mathrm{V})}{0.05\mathrm{fF} + 1.38\mathrm{fF}} = \text{-}0.06\mathrm{V}$$

and the new value $V_\mathrm{Q} := V_\mathrm{Q} + \Delta V_\mathrm{Q} = 1.15\mathrm{V} - 0.06\mathrm{V} = 1.09\mathrm{V}$. Da V_Q is above the switching voltage V_S. The circuit is stable.

$V_{\overline{\mathrm{Q}}}$ is also calculated from the current equations:

$$\begin{aligned} V_{\overline{\mathrm{Q}}} &\approx \frac{W_\mathrm{P} L_\mathrm{N} v_\mathrm{sat} C_\mathrm{ox}(V_\mathrm{DD} - V_\mathrm{Q} - V_\mathrm{T0})^2}{W_\mathrm{N}\mu_\mathrm{N} C_\mathrm{ox}(V_\mathrm{Q} - V_\mathrm{T0})(V_\mathrm{DD} - V_\mathrm{Q} - V_\mathrm{T0} + E_\mathrm{CP} L_\mathrm{P})} \\ &\approx \frac{(0.4 \times 10^{\text{-}4})(0.2)(8 \times 10^6) C_\mathrm{ox}(1.8 - 1.09 - 0.5)^2\mathrm{V}}{(0.2)(270) C_\mathrm{ox}(1.09 - 0.5)(1.8 - 1.09 - 0.5 + 4.8)} \approx 0.016\mathrm{V} \end{aligned}$$

Solution 10.4

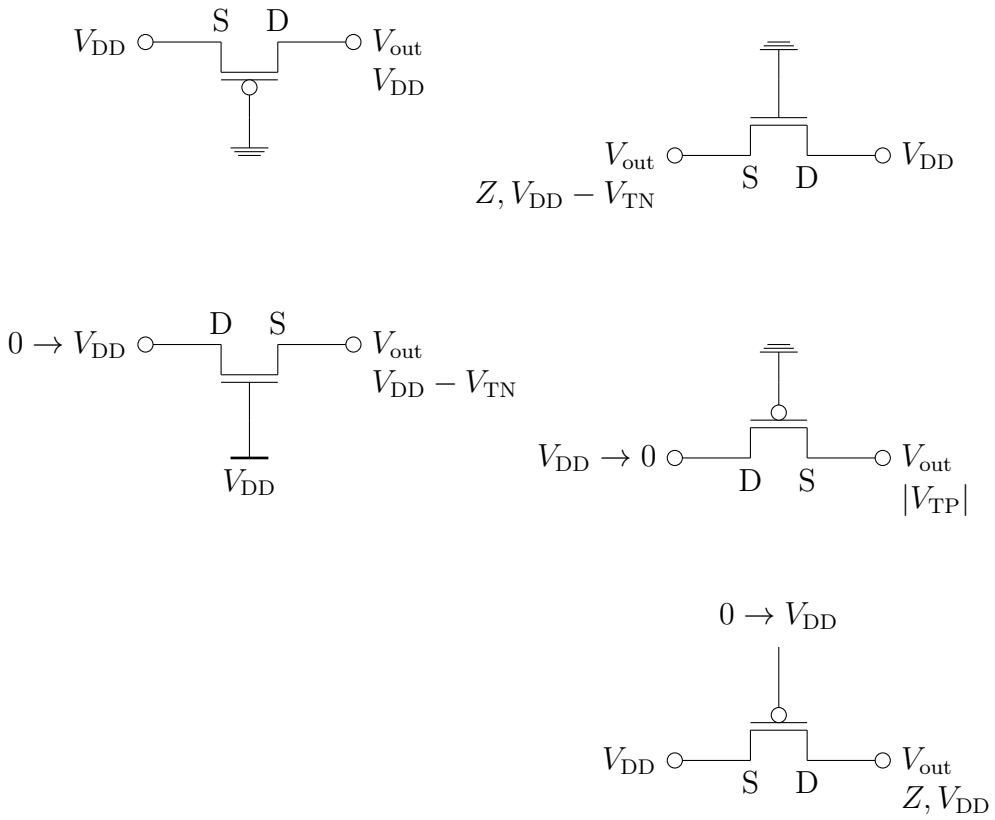

Figure 10.5: Operating States of Pass Transistors