Solution 6.1

The connection from gate to drain of the pull-up transistor results in $V_{\mathrm{GS}} = V_{\mathrm{DS}}$. Therefore, the operating point of the current voltage characteristic is in saturation range or in cutoff range (V_{DD} must be sufficiently large). The pull-up transistor is biased to V_{SB}.

$$\begin{aligned} V_{\mathrm{OH}} &= V_{\mathrm{DD}} - V_{\mathrm{TL}}(V_{\mathrm{SB}}) \\ &= V_{\mathrm{DD}} - (V_{\mathrm{T0}} + \gamma(\sqrt{V_{\mathrm{SB}} + 2|\Phi_{\mathrm{F}}|} - \sqrt{2|\Phi_{\mathrm{F}}|})) \\ &= 0.8\mathrm{V} - 0.2\mathrm{V}^{1/2}\sqrt{V_{\mathrm{OH}} + 0.88\mathrm{V}} + 0.2\mathrm{V}^{1/2}\sqrt{0.88\mathrm{V}} \\ &= 0.99\mathrm{V} - 0.2\mathrm{V}^{1/2}\sqrt{V_{\mathrm{OH}} + 0.88\mathrm{V}} \end{aligned}$$

The solution by iteration starts at the value V_{OH}=1.2V and results in V_{OH}=0.73V. Obviously a value of $V_{\mathrm{OH}} = 0.73\mathrm{V}$ of 1.2V for the supply voltage is not acceptable as input for the load (next inverter). Also note that for a different starting value the solution can be reached faster.

Solution 6.2

Equating the respective NMOS currents results in

$$\frac{W_{\mathrm{I}}}{L_{\mathrm{I}}} \frac{\mu_{\mathrm{n}}}{\left(1 + \dfrac{V_{\mathrm{OL}}}{E_{\mathrm{CN}} L_{\mathrm{I}}}\right)} \left((V_{\mathrm{DD}} - V_{\mathrm{TI}})V_{\mathrm{OL}} - \frac{V_{\mathrm{OL}}^2}{2}\right) = \frac{W_{\mathrm{L}} \nu_{\mathrm{Sat}} (V_{\mathrm{DD}} - V_{\mathrm{OL}} - V_{\mathrm{TL}})^2}{(V_{\mathrm{DD}} - V_{\mathrm{OL}} - V_{\mathrm{TL}}) + E_{\mathrm{CN}} L_{\mathrm{L}}}$$

With the biasing $V_{\mathrm{OL}} = 0.1\mathrm{V}$ the body effect is as expected low:

$$V_{\mathrm{TL}} = V_{\mathrm{T0}} + \gamma \left(\sqrt{V_{\mathrm{SB}} + 2|\Phi_{\mathrm{F}}|} - \sqrt{2|\Phi_{\mathrm{F}}|}\right) = 0.41\mathrm{V}$$

It results (z. B. $W_{\mathrm{L}} = 100\mathrm{nm}$ and $W_{\mathrm{I}} = 170\mathrm{nm}$.)

$$\frac{W_{\mathrm{I}}}{0,1 \cdot 10^{-4}\mathrm{cm}} \frac{270\mathrm{cm}^2/\mathrm{s}}{\left(1 + \dfrac{0.1}{0.6}\right)} \left(0.08 - \frac{(0.1)^2}{2}\right) = \frac{W_{\mathrm{L}} 8 \cdot 10^6 (\mathrm{cm/s})(1.1 - 0.41)^2}{(1.1 - 0.41) + 0.6}$$

$$K_{\mathrm{R}} = \frac{W_{\mathrm{I}}}{W_{\mathrm{L}}} = 1.7$$

Solution 6.3

With $x = V_{\mathrm{IL}} - V_{\mathrm{TN}}$, $y = V_{\mathrm{DD}} - V_{\mathrm{out}}$, $z = V_{\mathrm{DD}} - |V_{\mathrm{TP}}| - V_{\mathrm{TN}}$ and $a = k_{\mathrm{N}}/k_{\mathrm{P}}$ it follows from Eq. (4.17), derived from Eq. (4.16) and Eq. (6.1) in Eq. (6.2)

$$2y = z - x(1 + a) \tag{6.1}$$

$$ax^2 = y(2z - 2x - y) \tag{6.2}$$

$$2x(3+a)z = 3z^2 - x^2(a^2+2a-3) \tag{6.3}$$

Inserting the assignments $(k_N = k_P) \Leftrightarrow (a = 1)$ and $(|V_{TP}| = V_{TN}) \Leftrightarrow (z = V_{DD} - 2V_{TN})$ in Eq. (6.3) results in $x = 3z/8$ with $z = V_{DD} - 2V_{TN}$:

$$V_{IL} = \frac{1}{4}\left(\frac{3}{2}V_{DD} + V_{TN}\right) \tag{6.4}$$

From the symmetrical VTC bisecting the angle follows $V_{IL} + V_{IH} = V_{DD}$:

$$V_{IH} = \frac{1}{4}\left(\frac{5}{2}V_{DD} - V_{TN}\right) \tag{6.5}$$

Inserting of V_{IL} in Eq. (6.1) and resolving to $V_{out} = V_{OUH}$ yields

$$V_{OUH} = \frac{1}{16}V_{DD}\left(11 + \frac{3k_N}{k_P}\right) + \frac{1}{2}|V_{TP}| + \frac{1}{8}V_{TN}\left(1 - \frac{3k_N}{k_P}\right) \tag{6.6}$$

Inserting the assignments $(k_N = k_P) \Leftrightarrow (a = 1)$ and $(|V_{TP}| \neq V_{TN}) \Leftrightarrow (z = V_{DD} - |V_{TP}| - V_{TN})$ in Eq. (6.3) results in $x = 3z/8$ with $z = V_{DD} - |V_{TP}| - V_{TN}$:

$$V_{IL} = \frac{1}{8}(3V_{DD} - 3|V_{TP}| + 5V_{TN}) \tag{6.7}$$

From the skewed VTC, which is shifted in the horizontal direction to the angle bisector, follows $V_{IL} + V_{IH} = V_{DD} - |V_{TP}| + V_{TN}$:

$$V_{IH} = \frac{1}{8}(5V_{DD} - 5|V_{TP}| + 3V_{TN}) \tag{6.8}$$

Inserting of V_{IL} in Eq. (6.1) and resolving to $V_{out} = V_{OUH}$ yields

$$V_{OUH} = \frac{1}{16}V_{DD}\left(11 + \frac{3k_N}{k_P}\right) + \frac{1}{16}|V_{TP}|\left(5 - \frac{3k_N}{k_P}\right) + \frac{1}{16}V_{TN}\left(5 - \frac{3k_N}{k_P}\right) \tag{6.9}$$

Solution 6.4

With the help of SPICE you get the characteristic values $V_{OH} = 1.8\text{V}$, $V_{OL} = 0\text{V}$, $V_{IL} = 0.626\text{V}$, $V_{IH} = 0.909\text{V}$ and $V_S = 0.8\text{V}$. It follows:

$$NM_L = V_{IL} - V_{OL} = 0.626\text{V} - 0\text{V} = 0.626\text{V}$$
$$NM_H = V_{OH} - V_{IH} = 1.8\text{V} - 0.909\text{V} = 0.891\text{V}$$

From hand calculation, we already know that $V_{OH} = 1.8\text{V}$ and $V_{OL} = 0\text{V}$. The calculation of V_S can be done with $0.18\mu\text{m}$ technology parameters:

$$\chi = \sqrt{\frac{W_N E_{CP}}{W_P E_{CN}}} = \sqrt{\frac{0.4 \cdot 10^{-6}\text{m}(24 \cdot 10^4\text{V/cm})}{0.8 \cdot 10^{-6}\text{m}(6 \cdot 10^4\text{V/cm})}} = 1.41$$
$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1+\chi} = \frac{1.8\text{V} - |\text{-}0.5\text{V}| + 1.41(0.5\text{V})}{1+1.41} = 0.83\text{V}$$

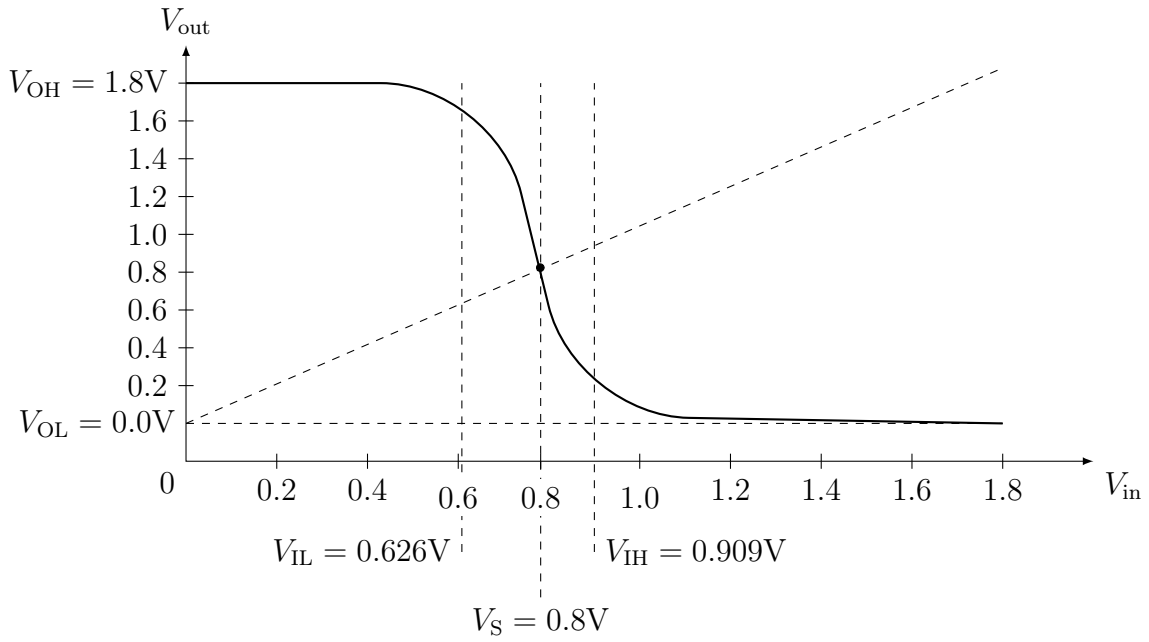

Figure 6.5: VTC of a CMOS Inverter (SPICE)

The value corresponds to the results from SPICE. The values for V_{IL} and V_{IH} require some effort, resulting in $V_{\mathrm{IL}} \approx 0.8\mathrm{V}$ and $V_{\mathrm{IH}} \approx 1.0\mathrm{V}$, $\mathrm{NM_L} = 0.8\mathrm{V}$ and $\mathrm{NM_H} = 0.8\mathrm{V}$. These values are about 15% different from the results of SPICE. But this is good enough for a manual calculation.

Solution 6.5

$W_{\mathrm{P}} \uparrow \Rightarrow \chi \downarrow \Rightarrow V_{\mathrm{S}} \uparrow$

$$\chi(W_{\mathrm{N}}, W_{\mathrm{P}}) = \sqrt{\frac{W_{\mathrm{N}} E_{\mathrm{CP}}}{W_{\mathrm{P}} E_{\mathrm{CN}}}} = \sqrt{\frac{0.1 \cdot 10^{-6}\mathrm{m}(24 \cdot 10^{4}\mathrm{V/cm})}{0.4 \cdot 10^{-6}\mathrm{m}(6 \cdot 10^{4}\mathrm{V/cm})}} = 1.0$$

$$V_{\mathrm{S}}(W_{\mathrm{N}}, W_{\mathrm{P}}) = \frac{V_{\mathrm{DD}} - |V_{\mathrm{TP}}| + \chi V_{\mathrm{TN}}}{1 + \chi} = \frac{1.2\mathrm{V} - |\text{-}0.4\mathrm{V}| + 1.0(0.4\mathrm{V})}{1 + 1.0} = 0.6\mathrm{V}$$

$$V_{\mathrm{S}}(0.1\mu\mathrm{m}, 0.1\mu\mathrm{m}) = \frac{V_{\mathrm{DD}} - |V_{\mathrm{TP}}| + \chi V_{\mathrm{TN}}}{1 + \chi} = \frac{1.2\mathrm{V} - |\text{-}0.4\mathrm{V}| + 2.0(0.4\mathrm{V})}{1 + 2.0} = 0.53\mathrm{V}$$

Solution 6.6

---

a) For high-impedance loads $I_{\mathrm{DN}}(\mathrm{sat}) = I_{\mathrm{DP}}(\mathrm{sat})$, symmetry $V_{\mathrm{GS}} = V_{\mathrm{SG}} = V_{\mathrm{DD}}/2$ and $V_{\mathrm{SB}} = 0\mathrm{V}$ applies:

$$\frac{I_{\mathrm{DN}}(\mathrm{sat})}{I_{\mathrm{DP}}(\mathrm{sat})} = \frac{W_{\mathrm{N}} \dfrac{(V_{\mathrm{DD}}/2 - V_{\mathrm{TN}})^2}{(V_{\mathrm{DD}}/2 - V_{\mathrm{TN}}) + E_{\mathrm{CN}} L N}}{W_{\mathrm{P}} \dfrac{(V_{\mathrm{DD}}/2 - |V_{\mathrm{TP}}|)^2}{(V_{\mathrm{DD}}/2 - |V_{\mathrm{TP}}|) + E_{\mathrm{CP}} L_{\mathrm{P}}}} = 1$$

With $V_{\mathrm{TN}} = |V_{\mathrm{TP}}|$, $E_{\mathrm{CN}}L_{\mathrm{N}} = 0.6\mathrm{V}$ und $E_{\mathrm{CP}}L_{\mathrm{P}} = 2.4\mathrm{V}$ follows

$$\frac{W_{\mathrm{P}}}{W_{\mathrm{N}}} = \frac{(V_{\mathrm{DD}}/2 - |V_{\mathrm{TP}}|) + E_{\mathrm{CP}}L_{\mathrm{P}}}{(V_{\mathrm{DD}}/2 - V_{\mathrm{TN}}) + E_{\mathrm{CN}}L_{\mathrm{N}}} = \frac{(0.6\mathrm{V} - 0.4\mathrm{V}) + 2.4\mathrm{V}}{(0.6\mathrm{V} - 0.4\mathrm{V}) + 0.6\mathrm{V}} = 3.25$$

b) $V_{\mathrm{T}} = V_{\mathrm{T0}} + \triangle V_{\mathrm{T}} = \left(V_{\mathrm{T0}} + \gamma\left(\sqrt{V_{\mathrm{SB}} + 2|\phi_{\mathrm{F}}|} - \sqrt{2|\phi_{\mathrm{F}}|}\right)\right)$
known is: $V_{\mathrm{TN}} = 0.4\mathrm{V}$, $|2\phi_{\mathrm{F}}| = 0.88\mathrm{V}$ und $\gamma = 0.2\mathrm{V}^{1/2}$
wanted is: V_{SB}

The NMOS operates in the saturation range, since

$$V_{\mathrm{Dsat}} = \frac{(V_{\mathrm{GS}} - V_{\mathrm{TN}})E_{\mathrm{CN}}L_{\mathrm{N}}}{(V_{\mathrm{GS}} - V_{\mathrm{TN}}) + E_{\mathrm{CN}}L_{\mathrm{N}}} = 0.34\mathrm{V} < 0.5\mathrm{V} = V_{\mathrm{DS}}$$

With $V_{\mathrm{on}} = V_{\mathrm{GS}} - V_{\mathrm{TN}} = V_{\mathrm{DD}} - (V_{\mathrm{T0}} + \triangle V_{\mathrm{T}})$ follows 50% less current

$$I_{\mathrm{DN}}(50\%) = W_{\mathrm{N}}\upsilon_{\mathrm{sat}}C_{\mathrm{ox}}\frac{V_{\mathrm{on}}^2}{V_{\mathrm{on}} + E_{\mathrm{CN}}L_{\mathrm{N}}}$$

and with $V_{\mathrm{on}} = V_{\mathrm{DD}} - V_{\mathrm{T0}}$ at $V_{\mathrm{SB}} = 0$ follows 100% current

$$I_{\mathrm{DN}}(100\%) = W_{\mathrm{N}}\upsilon_{\mathrm{sat}}C_{\mathrm{ox}}\frac{(V_{\mathrm{DD}} - V_{\mathrm{T0}})^2}{(V_{\mathrm{DD}} - V_{\mathrm{T0}}) + E_{\mathrm{CN}}L_{\mathrm{N}}} = W_{\mathrm{N}}\upsilon_{\mathrm{sat}}C_{\mathrm{ox}}a$$

The ratio K between 50% less current and 100% current is

$$K = \frac{I_{\mathrm{DN}}(50\%)}{I_{\mathrm{DN}}(100\%)} = \frac{1}{a}\frac{(V_{\mathrm{on}})^2}{(V_{\mathrm{on}}) + E_{\mathrm{CN}}L_{\mathrm{N}}} \tag{6.10}$$

The solution of the quadratic equation (6.10) yields

$$V_{\mathrm{on}} = \frac{Ka}{2}\left(1 \pm \sqrt{1 + \frac{2E_{\mathrm{CN}}L_{\mathrm{N}}}{Ka/2}}\right)$$

With $a = 0.46\mathrm{V}$, $K \approx 0.5$ and $V_{\mathrm{on}} = 0.46\mathrm{V}$ follows $\triangle V_{\mathrm{T}} = 0.34\mathrm{V}$ and $V_{\mathrm{SB}} = 6.08\mathrm{V}$.

Solution 6.7

To design the inverter in Fig. 6.7b with respect to given V_{OH}, we set $V_{\mathrm{DD}} = 1.8\mathrm{V}$. To set $V_{\mathrm{OL}} = 0.065\mathrm{V}$ over the transistor sizes we use Eq. (4.21):

$$\frac{W_{\mathrm{P}}\upsilon_{\mathrm{sat}}C_{\mathrm{ox}}(V_{\mathrm{DD}} - |V_{\mathrm{TP}}|)^2}{(V_{\mathrm{DD}} - |V_{\mathrm{TP}}|) + E_{\mathrm{CP}}L_{\mathrm{P}}} = \frac{W_{\mathrm{N}}}{L_{\mathrm{N}}}\frac{\mu_{\mathrm{n}}C_{\mathrm{ox}}}{\left(1 + \dfrac{V_{\mathrm{OL}}}{E_{\mathrm{CN}}L_{\mathrm{N}}}\right)}\left((V_{\mathrm{DD}} - V_{\mathrm{TN}})V_{\mathrm{OL}} - \frac{V_{\mathrm{OL}}^2}{2}\right)$$

$$\frac{W_{\mathrm{N}}}{W_{\mathrm{P}}} \approx 2.0$$

If you set $W_{\mathrm{P}} = 400\mathrm{nm}$ and $W_{\mathrm{N}} = 800\mathrm{nm}$ the desired voltage $V_{\mathrm{OL}} = 0.065\mathrm{V}$ should be generated.

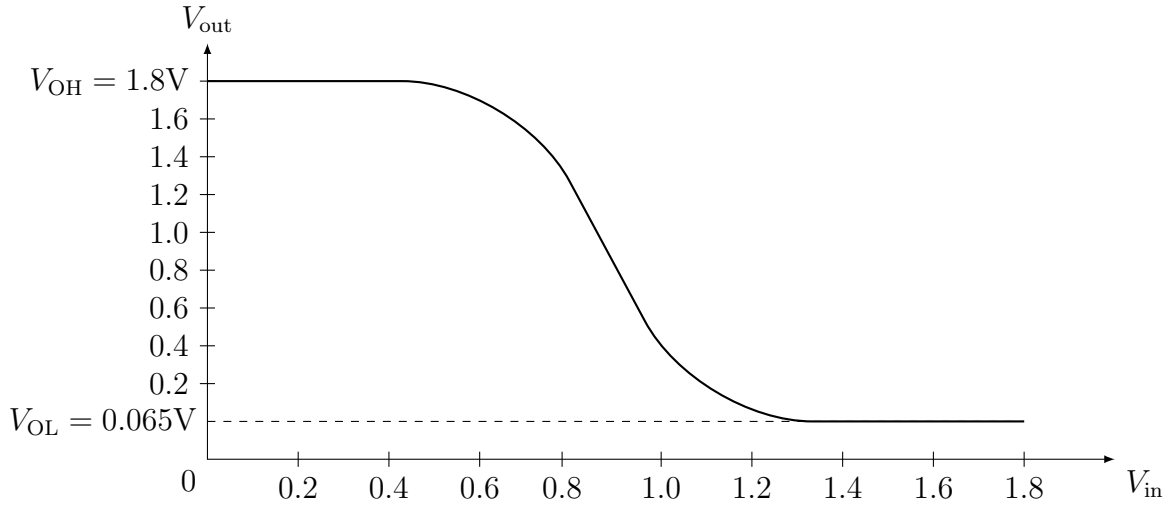

Figure 6.6: Solutions in Spice are $V_{\text{OH}} = 1.8\text{V}$ and $V_{\text{OL}} = 0.065\text{V}$

Solution 6.8

Timing has the highest priority for the CMOS inverter. The Noise Margin is set by the parameters V_{OH} and V_{OL} with $V_{\text{DD}} = 1.2\text{V}$. The current requirement is minimal because there is no cross current in the static state. The area requirement forms a tradeoff to the timing. For the calculation we use Eq. (4.22c):

$$\tau = 0.7 R_{\text{eff}} C_{\text{L}} = 50 \cdot 10^{-12}\text{s} \quad \Rightarrow \quad R_{\text{eff}} = 1.4\text{k}\Omega$$

With the help of Eq. (4.24a) we can determine the value W/L:

$$R_{\text{N}} = R_{\text{eqn}} \frac{L}{W} = (12.5\text{k}\Omega) \frac{L}{W} = 1.4\text{k}\Omega \quad \Rightarrow \quad \frac{W_{\text{N}}}{L_{\text{N}}} = 8.92$$

With the help of Eq. (4.24b) we get:

$$R_{\text{P}} = R_{\text{eqp}} \frac{L}{W} = 30k\Omega \frac{L}{W} = 1.4k\Omega \quad \Rightarrow \quad \frac{W_{\text{P}}}{L_{\text{P}}} = 21$$

With $L = 0.1\mu\text{m}$ it follows:

$$\frac{W_{\text{N}}}{L_{\text{N}}} = \frac{0.892\mu\text{m}}{0.1\mu\text{m}}, \qquad \frac{W_{\text{P}}}{L_{\text{P}}} = \frac{2.1\mu\text{m}}{0.1\mu\text{m}}$$

For the pseudo-NMOS gate we prioritize the calculation of V_{OL} (ratioed circuit). The V_{OH} requirement is satisfied by $V_{\text{DD}} = 1.2\text{V}$. The sizing of the NMOS transistor is identical with the CMOS inverter, because the time requirements are the same. We can meet the power and area requirements, but not the V_{OL} and t_{PHL} requirements.

For the PMOS transistor we get Eq. (4.21):

$$\frac{W_{\text{P}} \upsilon_{\text{sat}} C_{\text{ox}} (V_{\text{DD}} - |V_{\text{TP}}|)^2}{(V_{\text{DD}} - |V_{\text{TP}}|) + E_{\text{CP}} L_{\text{P}}} = \frac{W_{\text{N}}}{L_{\text{N}}} \frac{\mu_{\text{n}} C_{\text{ox}}}{\left(1 + \dfrac{V_{\text{OL}}}{E_{\text{CN}} L_{\text{N}}}\right)} \left((V_{\text{DD}} - V_{\text{TN}}) V_{\text{OL}} - \frac{V_{\text{OL}}^2}{2} \right)$$

$$W_\mathrm{P} = 0.963\mu\mathrm{m}$$

This gives us the dimensioning

$$\frac{W_\mathrm{N}}{L_\mathrm{N}} = \frac{0.892\mu\mathrm{m}}{0.1\mu\mathrm{m}}, \qquad \frac{W_\mathrm{P}}{L_\mathrm{P}} = \frac{0.963\mu\mathrm{m}}{0.1\mu\mathrm{m}}$$

In the case of the pseudo-NMOS inverter, pull-down and pull-up are about the same. This implies that t_PLH is well over 100ps (i.e. more than twice the size of t_PHL). This is the price for this type of charge. It also dissipates more power at low voltage level (logical zero). However, the area requirement is much smaller than for CMOS inverters and therefore better suited for circuits with high fan-in.

Solution 6.9

According to the truth table, both circuits work as tristate buffers. The right circuit, on the other hand, only has to reload smaller self-capacities.

IN	EN	OUT
0	0	Z
1	0	Z
0	1	1
1	1	0

Table 6.1: Truth Table of an inverting Tri-State Buffers

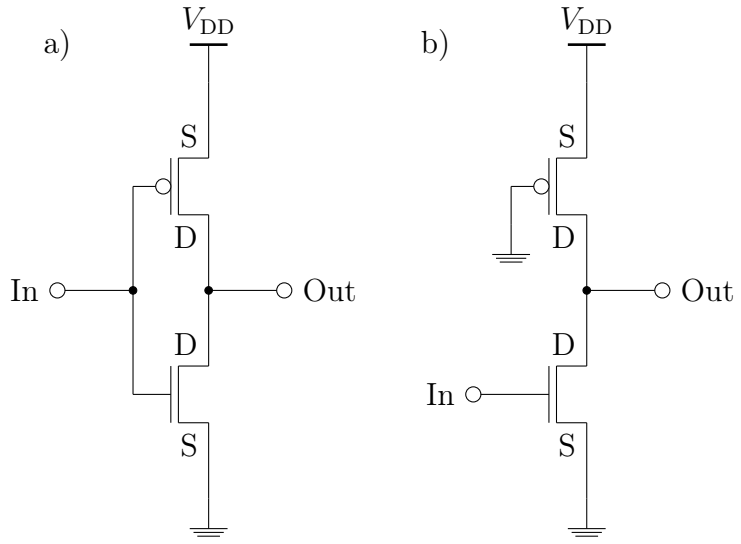

Figure 6.7: Schematic CMOS Inverter (a) and Pseudo-NMOS Inverter (b)