Solution 8.1

The cross current I_{DC} flowing through the inverter can be calculated using the current through the pull-down transistor. The pull-down transistor operates in the linear operating range.

$$I_{\mathrm{DC}} = \frac{W_{\mathrm{N}}}{L_{\mathrm{n}}} \frac{\mu_{\mathrm{n}} C_{\mathrm{ox}}}{\left(1 + \dfrac{V_{\mathrm{OL}}}{E_{\mathrm{CN}} L_{\mathrm{N}}}\right)} \left((V_{\mathrm{DD}} - V_{\mathrm{TN}}) V_{\mathrm{OL}} - \frac{V_{\mathrm{OL}}^2}{2}\right)$$

$$= 9 \frac{(270 \mathrm{cm}^2/\mathrm{Vs})(1.6 \cdot 10^{-6} \mathrm{F/cm}^2)}{\left(1 + \dfrac{0.1\mathrm{V}}{0.6\mathrm{V}}\right)} \left((1.2\mathrm{V} - 0.4\mathrm{V})0.1\mathrm{V} - \frac{(0.1\mathrm{V})^2}{2}\right) = 250\mu A$$

The consumed power is $P = I_{\mathrm{DC}} V_{\mathrm{DD}} = 250\mu\mathrm{A} \cdot 1.2\mathrm{V} = 300\mu\mathrm{W}$

Solution 8.2

i) For the specified values of #Gatter $= 10$M, $\alpha = 0.1$, $C = 20$fF, $V_{\mathrm{DD}} = 1.8$V and $f_{\mathrm{clk}} = 500$MHz it follows $P_{\mathrm{single}} = \alpha C V_{\mathrm{DD}}^2 f_{\mathrm{clk}} = 0.1(20 \cdot 10^{-15}\mathrm{F})(1.8\mathrm{V})^2(500 \cdot 10^6 \mathrm{Hz}) = 3.24\mu\mathrm{W}$ und $P_{\mathrm{gesamt}} = 10 \cdot 10^6(\mathrm{Gatter}) \cdot 3.24\mu\mathrm{W} = 32.4\mathrm{W}$.

ii) For the specified values of #Gatter $= 50$M, $\alpha = 0.05$, $C = 10$fF, $V_{\mathrm{DD}} = 1.2$V and $f_{\mathrm{clk}} = 1$GHz it follows $P_{\mathrm{single}} = \alpha C V_{\mathrm{DD}}^2 f_{\mathrm{clk}} = 0.05(10 \cdot 10^{-15}\mathrm{F})(1.2\mathrm{V})^2(1 \cdot 10^9 \mathrm{Hz}) = 0.72\mu\mathrm{W}$ und $P_{\mathrm{gesamt}} = 50 \cdot 10^6 \cdot 0.72\mu\mathrm{W} = 36\mathrm{W}$.

The performances are approximately equal, so that it seems as if both executions are equivalent.

i) With $t_{\mathrm{P}} = 1/(2f) = 1/(2 \cdot 500 \cdot 10^6 \mathrm{Hz}) = 1$ns results an energy delay product of EDP $= P \cdot t_{\mathrm{P}}^2 = 32.4\mathrm{W} \cdot (1\mathrm{ns})^2 = 32.4 \cdot 10^{-18}\mathrm{Js}$.

i) With $t_{\mathrm{P}} = 1/(2f) = 1/(2 \cdot 1 \cdot 10^9 \mathrm{Hz}) = 0.5$ns results an energy delay product of EDP $= P \cdot t_{\mathrm{P}}^2 = 36\mathrm{W} \cdot (0.5\mathrm{ns})^2 = 9 \cdot 10^{-18}\mathrm{Js}$.

The second design has a smaller energy delay product and is therefore cheaper.

Solution 8.3

All the work performed on an RC circuit is composed of the dissipated energy at the resistor and the stored energy at the capacitor.

- Time course of the electrical energy that is converted into heat or emitted as heat at the ohmic resistor during the charging process:

$$E_{\mathrm{R}}(t) = \int_0^t \mathrm{d}E_{\mathrm{R}}(t) = \int_0^t P_{\mathrm{R}}(t)\, \mathrm{d}t = \int_0^t i_{\mathrm{c}}(t) V_{\mathrm{R}}(t)\, \mathrm{d}t$$

$$E_{\mathrm{R}}(t = \infty) = \int_0^\infty C \cdot \frac{\mathrm{d}V_{\mathrm{out}}(t)}{\mathrm{d}t}(V_{\mathrm{in}}(t) - V_{\mathrm{out}}(t))\, \mathrm{d}t = C \int_0^{V_{\mathrm{DD}}}(V_{\mathrm{DD}} - V_{\mathrm{out}})\, \mathrm{d}V_{\mathrm{out}}$$

$$= \frac{1}{2} C V_{\mathrm{DD}}^2$$

- Time course of the electrical energy that is stored as potential energy at the capacitor during the charging process:

$$E_{\mathrm{C}}(t) = \int_0^t \mathrm{d}E_{\mathrm{C}}(t) = \int_0^t P_{\mathrm{C}}(t)\,\mathrm{d}t = \int_0^t i_{\mathrm{c}}(t)V_{\mathrm{C}}(t)\,\mathrm{d}t$$

$$E_{\mathrm{C}}(t = \infty) = \int_0^\infty C \cdot \frac{\mathrm{d}V_{\mathrm{out}}(t)}{\mathrm{d}t}V_{\mathrm{out}}(t)\,\mathrm{d}t = C\int_0^{V_{\mathrm{DD}}} V_{\mathrm{out}}\,\mathrm{d}V_{\mathrm{out}}$$

$$= \frac{1}{2}CV_{\mathrm{DD}}^2$$

Solution 8.4

This applies to NMOS and PMOS:

$$(I_{\mathrm{Dsat}})_{\mathrm{N}} = W_{\mathrm{n}}v_{\mathrm{sat}}C_{\mathrm{ox}}\frac{(V_{\mathrm{DD}} - V_{\mathrm{TN}})^2}{(V_{\mathrm{DD}} - V_{\mathrm{TN}}) + E_{\mathrm{CN}}L_{\mathrm{N}}}$$

$$= (0.1 \cdot 10^{-4}\mathrm{cm})(8 \cdot 10^6\mathrm{cms}^{-1})(1.6 \cdot 10^{-6}\mathrm{Fcm}^{-2})\frac{(1.2\mathrm{V} - 0.4\mathrm{V})^2}{(1.2\mathrm{V} - 0.4\mathrm{V}) + 0.6\mathrm{V}}$$

$$\approx 60\mu\mathrm{A}$$

$$R_{\mathrm{N}} = \frac{V_{\mathrm{DD}}/2}{0.7(I_{\mathrm{Dsat}})_{\mathrm{N}}} = \frac{1.2\mathrm{V}/2}{0.7(60\mu\mathrm{A})} = 14.5\mathrm{k}\Omega$$

$$(I_{\mathrm{Dsat}})_{\mathrm{P}} = W_{\mathrm{p}}v_{\mathrm{sat}}C_{\mathrm{ox}}\frac{(V_{\mathrm{DD}} - |V_{\mathrm{TP}}|)^2}{(V_{\mathrm{DD}} - |V_{\mathrm{TP}}|) + E_{\mathrm{CP}}L_{\mathrm{P}}}$$

$$= (0.1 \cdot 10^{-4}\mathrm{cm})(8 \cdot 10^6\mathrm{cms}^{-1})(1.6 \cdot 10^{-6}\mathrm{Fcm}^{-2})\frac{(1.2\mathrm{V} - 0.4\mathrm{V})^2}{(1.2\mathrm{V} - 0.4\mathrm{V}) + 2.4\mathrm{V}}$$

$$\approx 25\mu\mathrm{A}$$

$$R_{\mathrm{P}} = \frac{V_{\mathrm{DD}}/2}{0.7(I_{\mathrm{Dsat}})_{\mathrm{P}}} = \frac{1.2\mathrm{V}/2}{0.7(25\mu\mathrm{A})} = 33.5\mathrm{k}\Omega$$

Solution 8.5

The input capacity is $C_{\mathrm{G}} = C_{\mathrm{g}}(W_{\mathrm{N}} + W_{\mathrm{P}}) = C_{\mathrm{g}}(3W + 2W) = C_{\mathrm{g}}(5W)$.

The intrinsic capacity is $C_{\mathrm{self}} = C_{\mathrm{eff}}(W_{\mathrm{N}}+W_{\mathrm{P}})$, $C_{\mathrm{self}}/(1\mu\mathrm{F}) = (0.5 \cdot 2+0.25 \cdot 2+0.5)(2W)+ (0.5 + 0.25)(3W) + (0.5 \cdot 2 + 0.25 \cdot 3)(3W)((V_{\mathrm{DD}} - V_{\mathrm{TN}})/V_{\mathrm{DD}}) + (0.25)(3W) ((2V_{\mathrm{DD}} - V_{\mathrm{TN}})/V_{\mathrm{DD}}) = 4W + 2.25W + 5.25W + 1.5W - 6W(V_{\mathrm{TN}}/V_{\mathrm{DD}}) = 13W - 6W(V_{\mathrm{TN}}/V_{\mathrm{DD}})$.

The NMOS transistors share the source/drain areas. Two PMOS transistors share their drain areas.
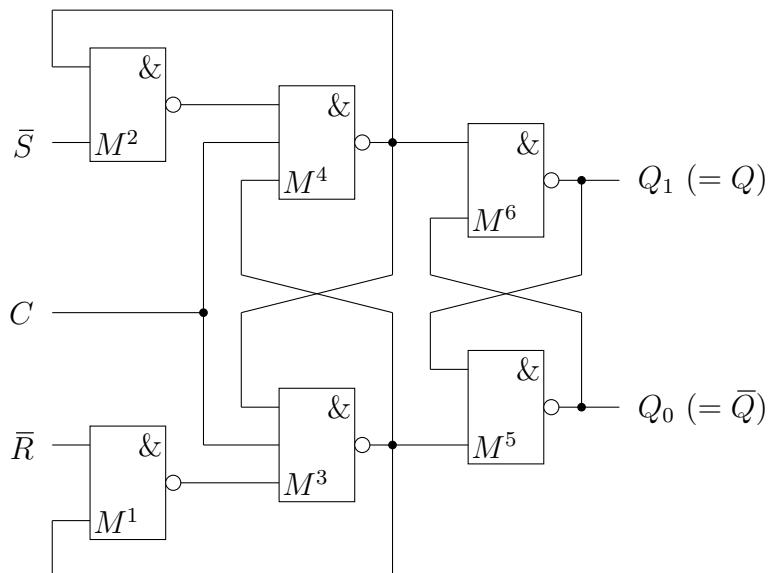
Solution 8.6

C_g and C_{eff} are for an inverter in 0.13μm or 0.18μm the same, $C_g = C_{\text{ox}}L + 2C_{\text{ol}} = 1.6\text{fF}/\mu\text{m} + 2(0.25\text{fF}/\mu\text{m}) \approx 2\text{fF}/\mu\text{m}$ und $C_{\text{eff}} = C_j + 2C_{\text{ol}} = 0.5\text{fF}/\mu\text{m} + 2(0.25\text{fF}/\mu\text{m}) \approx 1\text{fF}/\mu\text{m}$. This results for its capacities:

$$C_{\text{fanout}} = 4C_g(W_n + W_p) = 4(2\text{fF}/\mu\text{m})(4\lambda + 8\lambda) = 96\lambda\text{fF}$$
$$C_{\text{self}} = C_{\text{eff}}(W_n + W_p) = (1\text{fF}/\mu\text{m})(4\lambda + 8\lambda) = 12\lambda\text{fF}$$
$$C_{\text{load}} = C_{\text{fanout}} + C_{\text{self}} + C_{\text{wire}} = 96\lambda\text{fF} + 12\lambda\text{fF} + 0 = 108\lambda\text{fF}$$
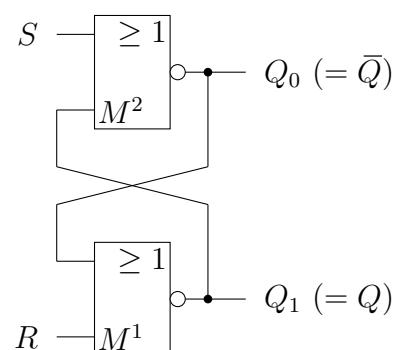
Solution 8.7

Figure 8.3: Positive edge triggered RS-FF (low-active)

S	R	Q_1	Q_0	Comment
0	0	$\overline{Q}_0$	$\overline{Q}_1$	hold ($\overline{Q}_0 = Q_1$)
0	1	0	1	reset
1	0	1	0	set
1	1	0	0	don't care

Figure 8.4: RS Latch realized by NOR Gates (high-active)
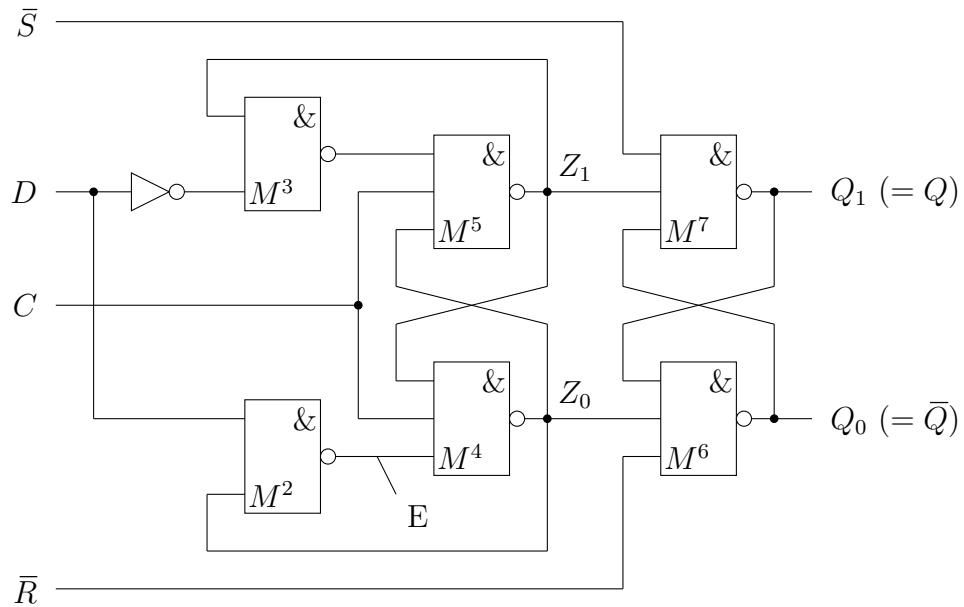
C	Z_1	Z_0	S	R	Z_1	Z_0	Q_1 Q_0
1	0	0	0	0	$*$	$*$	undef
1	0	0	0	1	$*$	$*$	undef
1	0	0	1	0	$*$	$*$	undef
1	0	0	1	1	$*$	$*$	undef
1	0	1	0	0	0	1	stable
1	0	1	0	1	0	1	stable
1	0	1	1	0	0	1	stable
1	0	1	1	1	0	1	stable
1	1	0	0	0	1	0	stable
1	1	0	0	1	1	0	stable
1	1	0	1	0	1	0	stable
1	1	0	1	1	1	0	stable
1	1	1	0	0	1	1	stable
1	1	1	0	1	1	0	reset
1	1	1	1	0	0	1	set
1	1	1	1	1	$*$	$*$	undef
0	$-$	$-$	$-$	$-$	1	1	stable
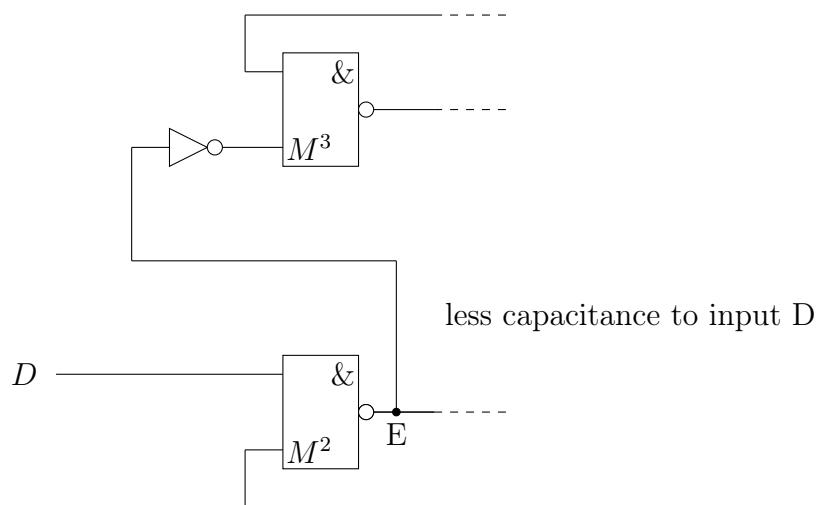
Z_1	Z_0	Q_1	Q_0	Comment
0	0	1	1	dont care
0	1	1	0	set
1	0	0	1	reset
1	1	$\overline{Q}_0$	$\overline{Q}_1$	hold ($\overline{Q}_0 = Q_1$)

Table 8.1: Switching sequence tables

With $\overline{R} = D$ and $\overline{S} = \overline{D}$ it becomes a positive edge-controlled D-FF. With the new

Figure 8.5: Positive edge triggered D-FF (high-active)

lines (S, R) the D-FF can be initialized to $(Q_1, Q_0) \in \{[01], [10], [11]\}$.

Figure 8.6: Contributions to the input capacity of D are only the input of M^2

C	Z_1	Z_0	D	Z_1	Z_0	Q_1	Q_0	E	Comment
1	0	0	1	$*$	$*$	$*$		$*$	undef
1	0	0	0	$*$	$*$	$*$		1	undef
1	0	1	1	0	1	set		0	stable
1	0	1	0	0	1	set		1	stable
1	1	0	1	1	0	reset		1	stable
1	1	0	0	1	0	reset		1	stable
1	1	1	1	0	1	set		0	stable
1	1	1	0	1	0	reset		1	stable
0	$-$	$-$	$-$	1	1	hold			

Table 8.2: Switching sequence table