
Solution 2.1

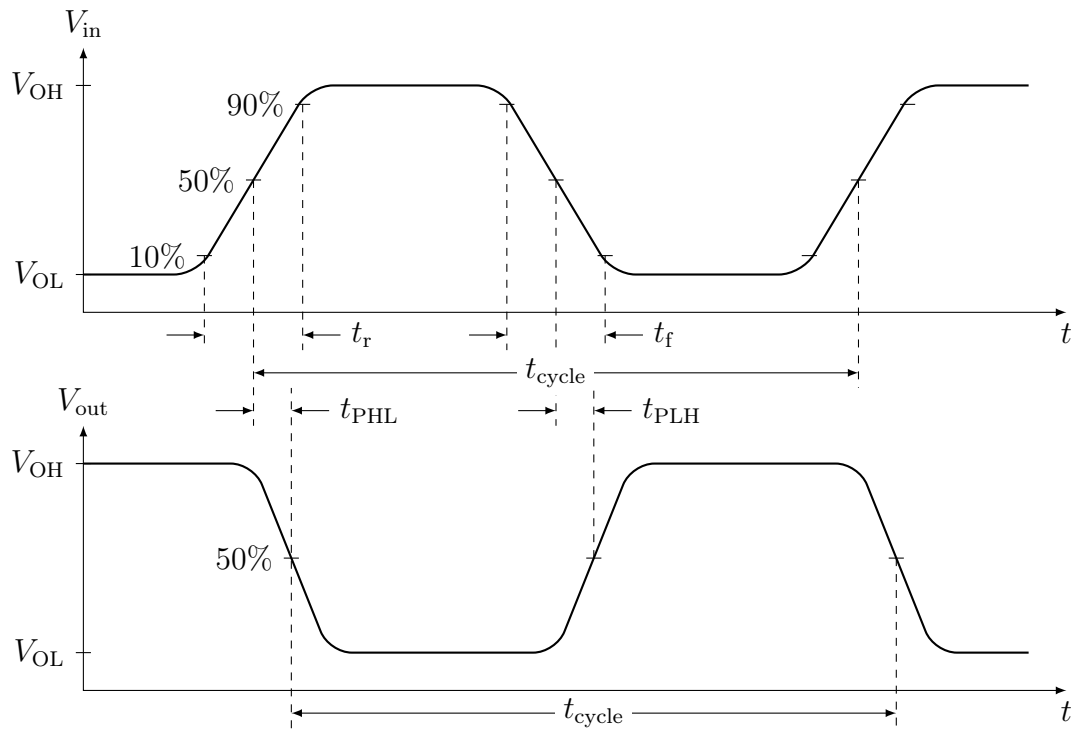


Figure 2.2: Definition of inverter delay

The time interval between the 50% values of successive voltages results in the delay t_{PHL} and t_{PLH} at the output of the inverter for rising and falling edges at the input of the inverter respectively. The average delay time is $t_P = (t_{PHL} + t_{PLH})/2$. For symmetrical inverters $t_{PHL} = t_{PLH}$ applies. Each inverter delays a signal by t_P .

a) Delay from A to B :

$$t_P = n \cdot t_0 = 5 \cdot 2\text{ns} = 10\text{ns}$$

b) Period of the ring oscillator:

$$T = 2 \cdot n \cdot t_0 = 2 \cdot 5 \cdot 2\text{ns} = 20\text{ns}$$

Frequency of the ring oscillator:

$$f = 1/T = 1/20\text{ns} = 50\text{MHz}$$

Solution 2.2

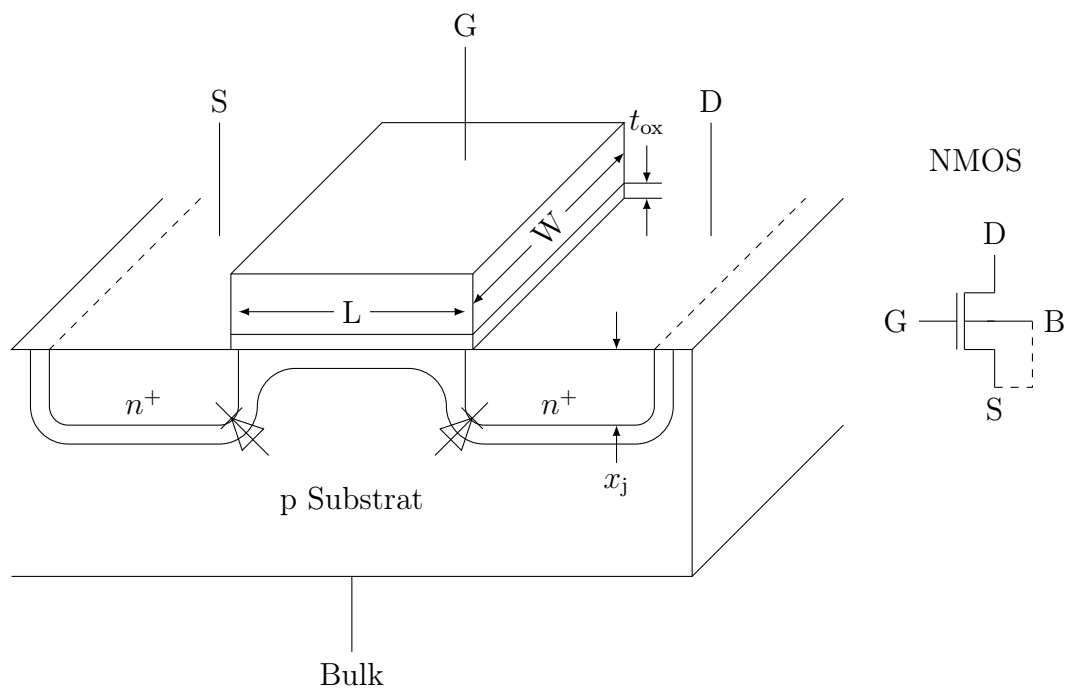


Figure 2.3: NMOS transistor structure and symbol

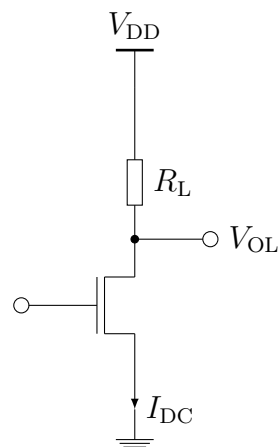


Figure 2.4: Cross current $I_{DC} = (V_{DD} - V_{OL})/R_L$

Solution 2.3

a) Φ_F : < 0 for p-type semiconductor, > 0 for n-type semiconductor:

$$2|\Phi_{Fp}| = \frac{2kT}{q} \left| \ln \frac{n_i}{p} \right| = 2(0.026V) \left| \ln \frac{1.45 \cdot 10^{10} \text{cm}^{-3}}{3 \cdot 10^{17} \text{cm}^{-3}} \right| = 0.88V$$

b) Width X_d and negative charge Q_{B0} of the space charge region:

$$X_d = \left(\frac{2\epsilon_{si}|\Phi_s - \Phi_F|}{qN_A} \right)^{1/2} = \sqrt{\frac{2(11.7)8.85 \cdot 10^{-14} \text{AsV}^{-1} \text{cm}^{-1}(0.88V)}{(1.6 \cdot 10^{-19} \text{As})(3 \cdot 10^{17} \text{cm}^{-3})}} = 60 \text{nm}$$

$$\begin{aligned} Q_{B0} &= -\sqrt{(2qN_A\epsilon_{si})| - 2\Phi_F|} \\ &= -\sqrt{2(1.6 \cdot 10^{-19} \text{As})(3 \cdot 10^{17} \text{cm}^{-3})(1.0 \cdot 10^{-12} \text{AsV}^{-1} \text{cm}^{-1})| - 0.88V|} \\ &\approx -3 \cdot 10^{-7} \text{C/cm}^2 \end{aligned}$$

c) Oxide capacity C_{ox} and body factor γ :

$$\begin{aligned} C_{ox} &= \frac{4\epsilon_o}{t_{ox}} = \frac{4(8.85 \cdot 10^{-14} \text{AsV}^{-1} \text{cm}^{-1})}{22\text{\AA}} = 1.6 \cdot 10^{-6} \text{F/cm}^2 \\ \gamma &= \frac{1}{C_{ox}} \sqrt{2q\epsilon_{si}N_A} \\ &= \frac{\sqrt{2(1.6 \cdot 10^{-19} \text{As})11.7(8.85 \cdot 10^{-14} \text{AsV}^{-1} \text{cm}^{-1})(3 \cdot 10^{17} \text{cm}^{-3})}}{1.6 \cdot 10^{-6} \text{F/cm}^2} \\ &\approx 0.2V^{1/2} \end{aligned}$$

d) Threshold voltage V_{T0} :

$$\Phi_{GC} = \Phi_{Fp} - \Phi_{G(\text{Gate})} = -0.44V - 0.55V = -0.99V$$

$$\frac{Q_{B0}}{C_{ox}} = \frac{-3 \cdot 10^{-7} \text{C/cm}^2}{1.6 \cdot 10^{-6} \text{F/cm}^2} = -0.188V$$

$$\frac{Q_{ox}}{C_{ox}} = \frac{(2 \cdot 10^{10} \text{cm}^{-2})(1.6 \cdot 10^{-19} \text{As})}{1.6 \cdot 10^{-6} \text{F/cm}^2} = 0.002V$$

$$\begin{aligned} V_{T0} &= \Phi_{GC} - 2\Phi_{FP} - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \\ &= -0.99V - (-0.88V) - (-0.188V) - 0.002V \\ &= 0.08V \end{aligned}$$

In the above solution we assume that the n^+ gate doping is so high that the Fermi level in the gate coincides with the conduction band. An electrostatic potential of $\Phi_{G(\text{Gate})} = 0.55\text{V}$ is implied. If the gate were p^+ -doped, the value of V_{T0} would be 1.18V . Unfortunately, this value is above the desired target level. Therefore, the doping of the poly-gate must be n^+ to keep the value below the target level. For the same reason the poly-gate of p-channel transistors is doped with p^+ . Of course, the above calculated values are not really applicable for NMOS devices, but only an approximation model, which should represent the trend. We need a value closer to $V_{T0} = 0.4\text{V}$.

e) V_T is shifted by $\frac{Q_I}{C_{\text{ox}}} = \frac{qN_I}{C_{\text{ox}}}$.

$$N_I = \frac{Q_I}{q} = \frac{C_{\text{ox}}\Delta V}{q} = \frac{1.6 \cdot 10^{-6}\text{F/cm}^2(0.4\text{V} - (0.08\text{V}))}{1.6 \cdot 10^{-19}\text{As}} = 3.2 \cdot 10^{12} \frac{\text{ions}}{\text{cm}^2}$$