Task 10.1

Explain the difference between clock feedthrough and charge sharing.

Task 10.2

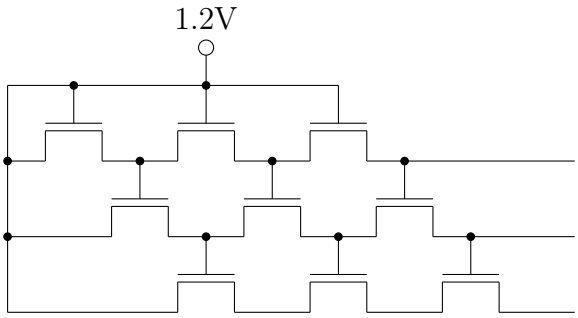

Figure 10.1: Multi-Voltage-Array

Calculate the Voltage at all nodes of the Multi-Voltage-Array in Figure 10.1 taking into account the body effect. All nodes are at 0V at the beginning. Use the values of a 0.13μm technology ($2|\Phi_F| = 0.\ 88$V, $\gamma = 0.2\text{V}^{1/2}$, $V_T = 0.4$V, $V_{DD} = 1.2$V).

Task 10.3

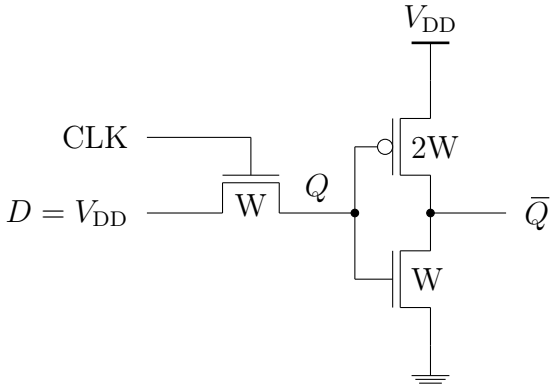

Figure 10.2: Dynamic (Positive Edge Controlled) D-Latch

For the dynamic D latch in Fig. 10.2, estimate the output voltages for Q and $\overline{Q}$, for the clock (CLK) at the input from LOW (GND) to HIGH (V_{DD}) and HIGH (V_{DD}) to LOW (GND). Consider Clock Feedthrough. Use the parameters of a 0.18μm CMOS technology. ($W = 200$nm, $\mu_n = 270\text{cm}^2/\text{Vs}$, $\mu_p = 70\text{cm}^2/\text{Vs}$, $C_{ox} = 1\mu\text{F/cm}^2$, $V_{TN} = 0.5$V, $V_{TP} = $ -0.5V, $V_{DD} = 1.8$V, $L = 200$nm, $E_{CN}L = 1.2$V, $E_{CP}L = 4.8$V, $\upsilon_{sat} = 8 \cdot 10^6\text{cm/s}$)

Task 10.4

Add Source (S), Drain (D) and the value of V_{out} to the pass transistors.

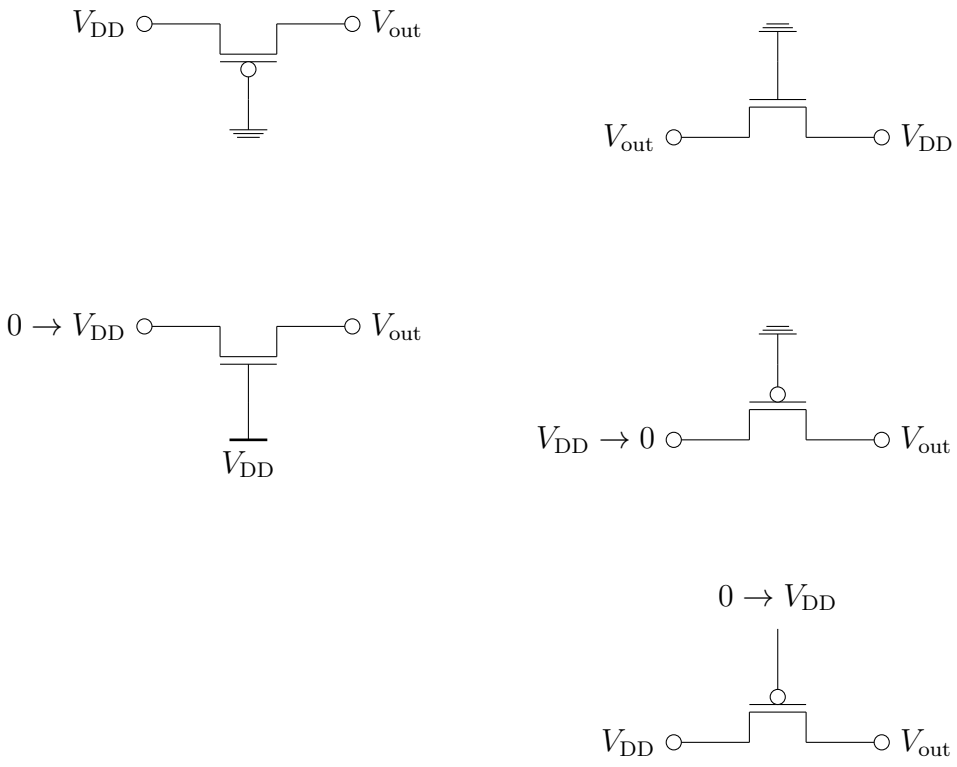

Figure 10.3: Operating States of Pass Transistors