## Solution 5.1

The voltage transfer characteristic is shown in Fig. 5.3. In the non-inverting case, the logic output value is equal to the logic input value. The transfer characteristic of the buffer is the transfer characteristic of the inverter mirrored at the bisecting line. Each curve point of unit gain, $(V_{\mathrm{IL}}, V_{\mathrm{OUL}})$ and $(V_{\mathrm{IH}}, V_{\mathrm{OUH}})$, has a positive slope of $+1$. Along the $V_{\mathrm{out}}$ axis the bands of tolerance are the noise levels $\mathrm{SSNM_L}$ and $\mathrm{SSNM_H}$ plotted. Along the $V_{\mathrm{in}}$ axis the limits of the noise levels $\mathrm{NM_L}$ and $\mathrm{NM_H}$ are plotted.
The output ranges remain approximately constant accross the respective input ranges $V_{\mathrm{OL}}$ to $V_{\mathrm{IL}}$ and $V_{\mathrm{IH}}$ to $V_{\mathrm{OH}}$. Outside these ranges, the output voltage is in the range of high gain and is amplified.

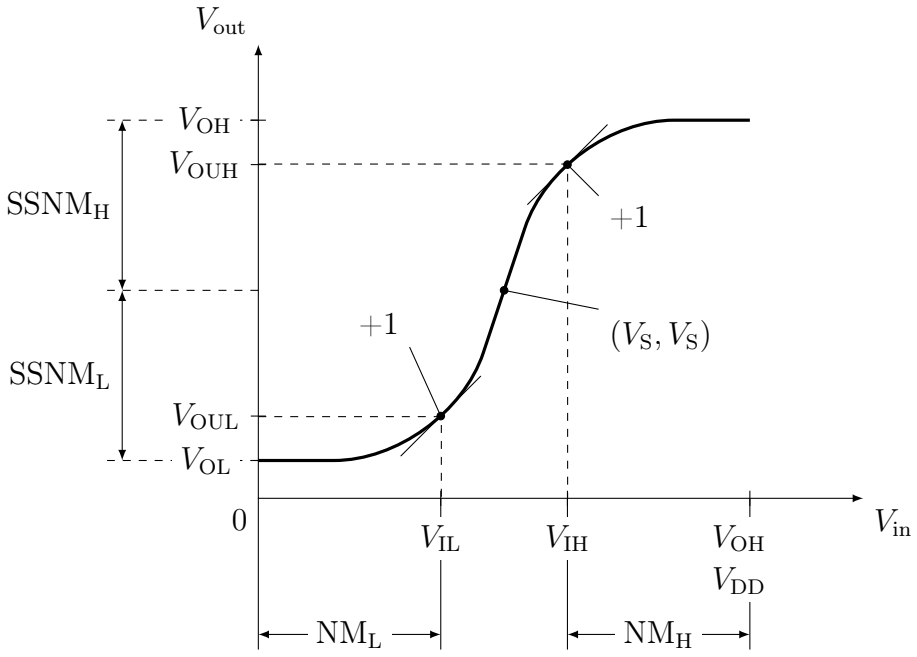


**Figure 5.3:** VTC of a Buffer

## Solution 5.2

Deriving $V_{\mathrm{OUL}}$:

$$V_{\mathrm{IH}} = V_{\mathrm{T}} + 2V_{\mathrm{out}} - \frac{1}{kR_{\mathrm{L}}} \tag{4.8d}$$

$$\frac{k}{2}\left(2(V_{\mathrm{IH}} - V_{\mathrm{T}})V_{\mathrm{out}} - V_{\mathrm{out}}^2\right) = \frac{V_{\mathrm{DD}} - V_{\mathrm{out}}}{R_{\mathrm{L}}} \tag{4.8e}$$

By substituting (4.8d) for (4.8e) and resolving to $V_{\mathrm{out}}$:

$$\frac{V_{\mathrm{DD}} - V_{\mathrm{out}}}{R_{\mathrm{L}}} = \frac{k}{2}\left(2(2V_{\mathrm{out}} - \frac{1}{kR_{\mathrm{L}}} + V_{\mathrm{T}} - V_{\mathrm{T}})V_{\mathrm{out}} - V_{\mathrm{out}}^2\right)$$

$$= \frac{k}{2}\left(3V_{\text{out}}^2 - \frac{2V_{\text{out}}}{kR_{\text{L}}}\right)$$

$$V_{\text{out}} = \overset{+}{(-)}\sqrt{\frac{2V_{\text{DD}}}{3kR_{\text{L}}}}$$

Deriving $V_{\text{S}}$:

$$\frac{W\nu_{\text{sat}}C_{\text{ox}}(V_{\text{S}} - V_{\text{T}})^2}{(V_{\text{S}} - V_{\text{T}}) + E_{\text{c}}L} = \frac{V_{\text{DD}} - V_{\text{S}}}{R_{\text{L}}}$$

with $\nu_{\text{sat}} = \mu E_{\text{c}}/2$ and $k = (W/L)\mu_{\text{n}}C_{\text{ox}}$ follows:

$$V_{\text{S}} = V_{\text{T}} + \frac{V_{\text{DD}} - V_{\text{T}} - E_{\text{c}}L}{2 + kR_{\text{L}}E_{\text{c}}L} + \sqrt{\frac{2(V_{\text{DD}} - V_{\text{T}})E_{\text{c}}L}{2 + kR_{\text{L}}E_{\text{c}}L}}$$

for $E_{\text{c}}L \gg 1$ (long channel devices) follows:

$$V_{\text{S}} = V_{\text{T}} + \frac{1}{kR_{\text{L}}} + \sqrt{\frac{2(V_{\text{DD}} - V_{\text{T}})}{kR_{\text{L}}}}$$

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**Solution 5.3**

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$$V_{\text{OH}} = V_{\text{DD}} = 1.2\text{V}$$

$$k = k'(W/L) = 430\frac{\mu\text{A}}{\text{V}^2} \cdot 2.0$$

Assumption: Transistor is in the linear range:

$$V_{\text{OL}} \approx \frac{V_{\text{DD}}}{1 + kR_{\text{L}}(V_{\text{DD}} - V_{\text{T}})} = \frac{1.2\text{V}}{1 + (430 \cdot 10^{-6}\text{AV}^{-2})(2)(20 \cdot 10^{3}\Omega)(1.2\text{V} - 0.4\text{V})} \approx 0.08\text{V}$$

Assumption: Transistor is in the saturation range:

$$V_{\text{IL}} = \frac{1}{kR_{\text{L}}} + V_{\text{T}} = \frac{1}{(430 \cdot 10^{-6}\text{AV}^{-2})(2)(20 \cdot 10^{3}\Omega)} + 0.4\text{V} = 0.46\text{V}$$

Assumption: Transistor is in the linear range:

$$V_{\text{IH}} = V_{\text{T}} + \sqrt{\frac{8V_{\text{DD}}}{3kR_{\text{L}}}} - \frac{1}{kR_{\text{L}}}$$

$$= 0.4\text{V} + \sqrt{\frac{8}{3}\frac{1.2\text{V}}{(2)(430 \cdot 10^{-6}\text{AV}^{-2})(20 \cdot 10^{3}\Omega)}} - \frac{1}{(2)(430 \cdot 10^{-6}\text{AV}^{-2})(20 \cdot 10^{3}\Omega)} \approx 0.77\text{V}$$

Solution:

$$\mathrm{NM_L} = V_{\mathrm{IL}} - V_{\mathrm{OL}} = 0.46\mathrm{V} - 0.08\mathrm{V} = 0.38\mathrm{V}$$
$$\mathrm{NM_H} = V_{\mathrm{OH}} - V_{\mathrm{IH}} = 1.2\mathrm{V} - 0.77\mathrm{V} = 0.43\mathrm{V}$$

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**Solution 5.4**

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Resolving from SPICE:

$$\mathrm{NM_L} = V_{\mathrm{IL}} - V_{\mathrm{OL}} = 0.558\mathrm{V} - 0.085\mathrm{V} = 0.473\mathrm{V}$$
$$\mathrm{NM_H} = V_{\mathrm{OH}} - V_{\mathrm{IH}} = 1.8\mathrm{V} - 0.972\mathrm{V} = 0.828\mathrm{V}$$
$$V_{\mathrm{S}} = 0.78\mathrm{V}$$

Hand calculation:

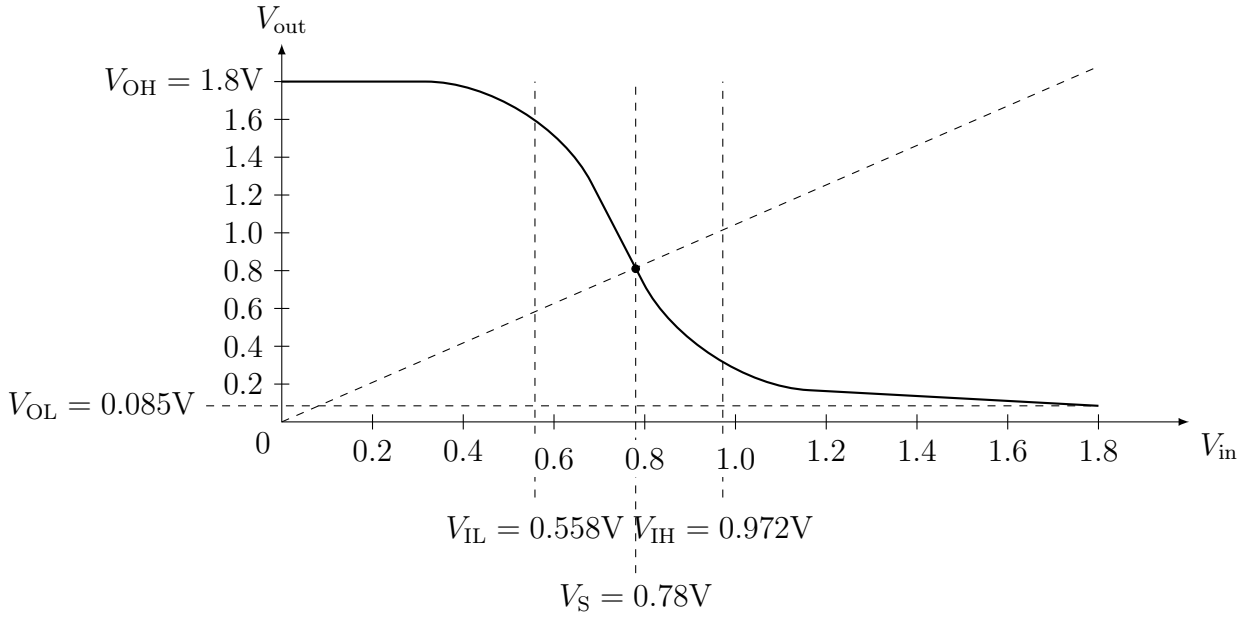


**Figure 5.4:** VTC: Solution resolved from SPICE

$$V_{\mathrm{OL}} \approx \frac{V_{\mathrm{DD}}}{1 + kR_{\mathrm{L}}(V_{\mathrm{DD}} - V_{\mathrm{T}})} = \frac{1.8\mathrm{V}}{1 + (2)\left(270\frac{\mu\mathrm{A}}{\mathrm{V}^2}\right)(30k\Omega)(1.8\mathrm{V} - 0.5\mathrm{V})} \approx 0.082\mathrm{V}$$
$$V_{\mathrm{IL}} = \frac{1}{kR_{\mathrm{L}}} + V_{\mathrm{T}} = 0.06\mathrm{V} + 0.5\mathrm{V} = 0.56\mathrm{V}$$
$$V_{\mathrm{IH}} = V_{\mathrm{T}} + \sqrt{\frac{8V_{\mathrm{DD}}}{3kR_{\mathrm{L}}}} - \frac{1}{kR_{\mathrm{L}}} = 0.5\mathrm{V} + 0.54\mathrm{V} - 0.06\mathrm{V} = 0.98\mathrm{V}$$

$$\mathrm{NM_L} = V_{\mathrm{IL}} - V_{\mathrm{OL}} = 0.478\mathrm{V}$$

$$\mathrm{NM_H} = V_{\mathrm{OH}} - V_{\mathrm{IH}} = 0.817\mathrm{V}$$

$$\frac{W\nu_{\mathrm{sat}}C_{\mathrm{ox}}(V_{\mathrm{S}} - V_{\mathrm{T}})^2}{(V_{\mathrm{S}} - V_{\mathrm{T}}) + E_{\mathrm{c}}L} = \frac{V_{\mathrm{DD}} - V_{\mathrm{S}}}{R_{\mathrm{L}}}$$

$$\frac{(0.4 \cdot 10^{-4}\mathrm{cm})(8 \cdot 10^{6}\mathrm{cms}^{-1})(10^{-6}\mathrm{Fcm}^{-2})(V_{\mathrm{S}} - 0.5\mathrm{V})^2}{(V_{\mathrm{S}} - 0.5\mathrm{V}) + 1.2\mathrm{V}} = \frac{1.8\mathrm{V} - V_{\mathrm{S}}}{30k\Omega}$$

$$V_{\mathrm{S}} = 0.89\mathrm{V}$$

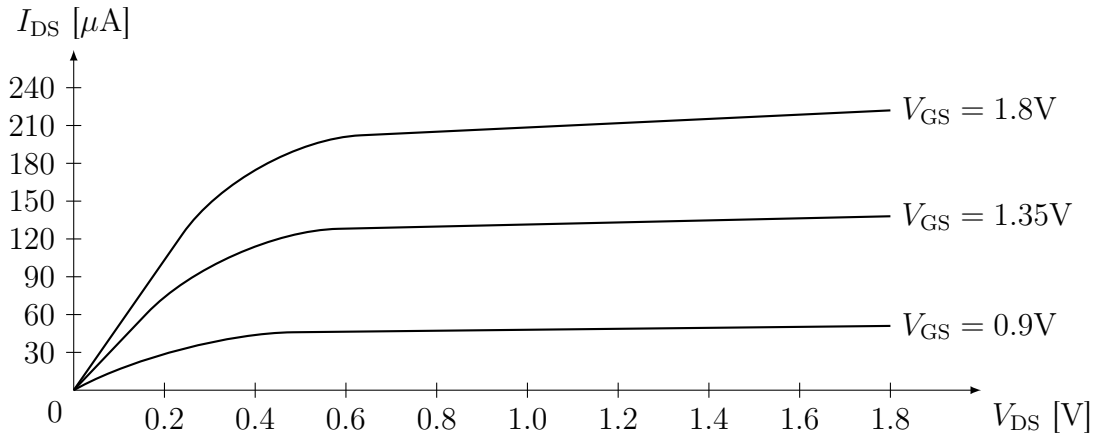


**Figure 5.5:** $I_{\mathrm{DS}}$ versus $V_{\mathrm{DS}}$ for NMOS($W/L = 2$)

However, this value is about 15% larger than the result from SPICE. The reason for this is that the channel length modulation has been neglected in the calculation. It should be remembered that the transistor was in the saturation range when $V_{\mathrm{S}}$ was calculated. The analysis of the curves in SPICE below $V_{\mathrm{GS}} = 0.9\mathrm{V}$ shows that due to channel length modulation and DIBL (Drain Induced Barrier Lowering) there is a noticeable increase in current in the saturation range. The term ($1+\lambda\ V_{\mathrm{S}}$) of the current equation and a lower $V_{\mathrm{T}}$ due to the DIBL increase the actual saturation current. It reduces $V_{\mathrm{S}}$ to 0.78V instead of the hand calculated value of 0.89V.

**Solution 5.5**

a) i) ($V_{\text{in}} = \text{H}$) $\Rightarrow$ The NMOS is conducting, there's a crossflow from $V_{\text{DD}}$ to GND.

ii) The upper NMOS (load) is conductive for $V_{\text{in}} = \text{H}$. The lower NMOS is conductive for $V_{\text{in}} = \text{H}$. A cross current flows. Power is consumed.

iii) like ii).

iv) ($V_{\text{in}} = \text{H}$) $\Rightarrow$ "Both transistors are conducting." $\Rightarrow$ "There's a crossflow from $V_{\text{DD}}$ to GND."

b) i) ($V_{\text{in}} = \text{L}$) $\Rightarrow$ "The lower NMOS is not conducting, there is no cross flow from $V_{\text{DD}}$ to GND."

ii) The upper NMOS (load) is non-conductive for $V_{\text{in}} = \text{L}$. The lower NMOS is not conductive for $V_{\text{in}} = \text{L}$. There is no cross flow. No power is consumed.

iii) The upper NMOS (load) is conducting for $V_{\text{in}} = \text{L}$. The lower NMOS is not conductive for $V_{\text{in}} = \text{L}$. There is no cross flow. No power is consumed.

iv) ($V_{\text{in}} = \text{L}$) $\Rightarrow$ "Both transistors are non-conducting." $\Rightarrow$ "There's no crossflow from $V_{\text{DD}}$ to GND."

c) For $V_{\text{in}} = \text{L}$ follows at circuits i) and iii) $V_{\text{OH}} = V_{\text{DD}} = 1.2\text{V}$.

d) For $V_{\text{in}} = \text{H}$ $V_{\text{OH}} > 0\text{V}$ follows for all circuits.

e) For circuit ii), iii) and iv), the transfer characteristic depends on the sizing of the two NMOS. In circuit ii), the lower NMOS must have a higher driver capability to produce a valid Low (L) at the output. In circuit iv), the expected value Low (L) depends on the ratio of the two NMOS, $V_{\text{OL}}$ is slightly higher than $V_{\text{DD}}/2$.