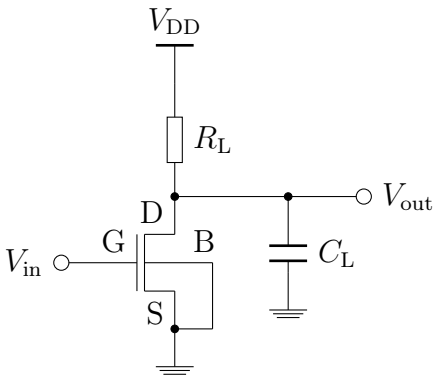

Figure 5.1: Inverter (W/L) with resistive load R_L

Task 5.1

Draw the voltage transfer characteristic (VTC) of a (non-inverting) buffer. Determine the bands of noise (Noise Margins) as well as the voltage transfer characteristic (VTC) by designating important points of the curve.

Task 5.2

For a resistive load inverter (R_L), derive the formulas for V_{OUL} and V_S. What values do you expect for Long Channel Devices?

Task 5.3

The following data is given for the inverter in Fig. 5.1. Specify the signal amplitudes permitted for multiple noise sources (MSNM).

$$k' = \mu_n C_{ox} = 430\mu A/V^2, \quad V_T = 0.4V,$$
$$V_{DD} = 1.2V, \quad R_L = 20k\Omega, \quad W/L = 2.0$$

Task 5.4

Compare the voltage transfer characteristic of a SPICE simulation with the results of a hand calculation for a resistive NMOS inverter with $R_L = 30k\Omega$, $W = 400nm$ and $L = 200nm$. Calculate V_{OH}, V_{OL}, V_{IH}, V_{IL}, and V_S. Use the following parameters of a $0.18\mu m$ CMOS technology:

$$k' = \mu_n C_{ox} = 270\mu A/V^2, \quad C_{ox} = 1\mu F/cm^2, \quad V_T = 0.5V$$
$$E_c L = 1.2V, \quad V_{DD} = 1.8V, \quad v_{sat} = 8 \cdot 10^6 cm/s$$

Task 5.5

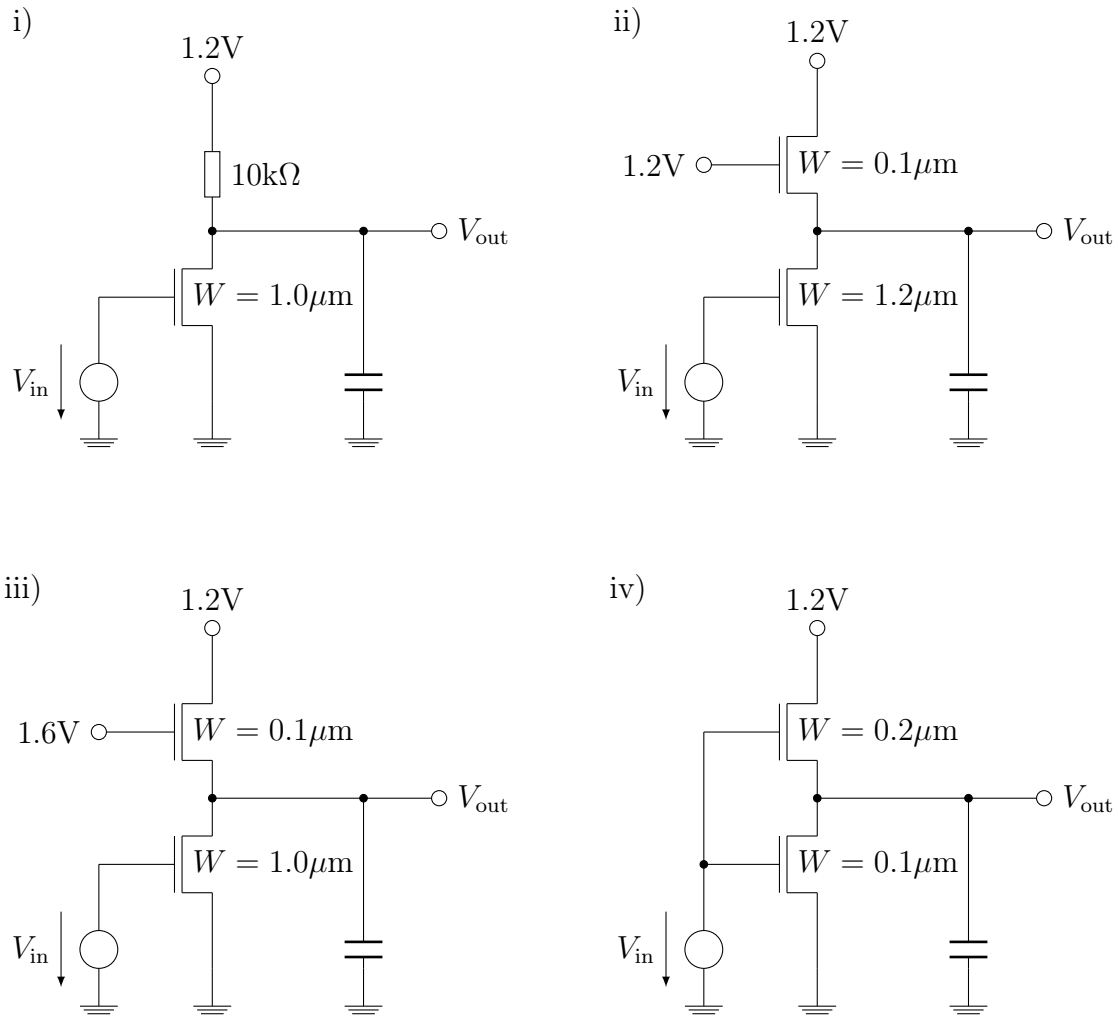

Figure 5.2: Different loads of an inverter ($L = 0.1\mu$m)

The circuits in Fig. 5.2 show different implementations of an inverter whose output is connected to a capacitor. Use the parameters of a 0.13μm technology:

$V_{T0} = 0.4\text{V}, \quad V_{DD} = 1.2\text{V}$

a) Which circuit consumes power at V_{in} = H:

b) Which circuit consumes power at V_{in} = L:

c) Which circuit exhibits $V_{OH} = 1.2\text{V}$:

d) Which circuit exhibits $V_{OL} = 0.0\text{V}$:

e) In which circuit does the function depend on sizing: