

INTERNATIONAL EDITION

David A. Hodges
Horace G. Jackson
Resve A. Saleh

Third Edition

Analysis and Design of Digital Integrated Circuits

In Deep Submicron Technology

Contents

Preface to Third Edition	xiii
1 Deep Submicron Digital IC Design	1
1.1 Introduction	1
1.2 Brief History of IC Industry	3
1.3 Review of Digital Logic Gate Design	6
1.3.1 Basic Logic Functions	6
1.3.2 Implementation of Logic Circuits	9
1.3.3 Definition of Noise Margin	11
1.3.4 Definition of Transient Characteristics	12
1.3.5 Power Estimation	14
1.4 Digital Integrated Circuit Design	15
1.4.1 MOS Transistor Structure and Operation	16
1.4.2 CMOS Versus NMOS	17
1.4.3 Deep Submicron Interconnect	19
1.5 Computer-Aided Design of Digital Circuits	24
1.5.1 Circuit Simulation and Analysis	24
*1.6 The Challenges Ahead	26
1.7 Summary	31
2 MOS Transistors	35
2.1 Introduction	35
2.2 Structure and Operation of the MOS Transistor	37
2.3 Threshold Voltage of the MOS Transistor	41
2.4 First-Order Current-Voltage Characteristics	52
2.5 Derivation of Velocity-Saturated Current Equations	57
2.5.1 Effect of High Fields	57
2.5.2 Current Equations for Velocity-Saturated Devices	61
*2.6 Alpha-Power Law Model	66
2.7 Subthreshold Conduction	68

2.8	Capacitances of the MOS Transistor	70
2.8.1	Thin-Oxide Capacitance	71
2.8.2	pn Junction Capacitance	73
2.8.3	Overlap Capacitance	79
2.9	Summary	81
3	Fabrication, Layout, and Simulation	89
3.1	Introduction	89
3.2	IC Fabrication Technology	90
3.2.1	Overview of IC Fabrication Process	90
3.2.2	IC Photolithographic Process	92
3.2.3	Making Transistors	93
3.2.4	Making Wires	97
3.2.5	Wire Capacitance and Resistance	100
3.3	Layout Basics	104
3.4	Modeling the MOS Transistor for Circuit Simulation	107
3.4.1	MOS Models in SPICE	107
3.4.2	Specifying MOS Transistors	108
3.5	SPICE MOS LEVEL 1 Device Model	111
3.5.1	Extraction of Parameters for MOS LEVEL 1	113
*3.6	BSIM3 Model	115
3.6.1	Binning Process in BSIM3	115
3.6.2	Short-Channel Threshold Voltage	116
3.6.3	Mobility Model	119
3.6.4	Linear and Saturation Regions	120
3.6.5	Subthreshold Current	122
3.6.6	Capacitance Models	123
3.6.7	Source/Drain Resistance	124
*3.7	Additional Effects in MOS Transistors	125
3.7.1	Parameter Variations in Production	125
3.7.2	Temperature Effects	125
3.7.3	Supply Variations	127
3.7.4	Voltage Limitations	128
3.7.5	CMOS Latch-up	128
*3.8	Silicon-on-Insulator (SOI) Technology	130
*3.9	SPICE Model Summary	132
4	MOS Inverter Circuits	143
4.1	Introduction	143
4.2	Voltage Transfer Characteristics	144
4.3	Noise Margin Definitions	147
4.3.1	Single-Source Noise Margin (SSNM)	148
4.3.2	Multiple-Source Noise Margin (MSNM)	150
4.4	Resistive-Load Inverter Design	153

4.5	NMOS Transistors as Load Devices	162
4.5.1	Saturated Enhancement Load	162
4.5.2	Linear Enhancement Load	166
4.6	Complementary MOS (CMOS) Inverters	168
4.6.1	DC Analysis of CMOS Inverter	168
4.6.2	Layout Design of CMOS Inverter	176
4.7	Pseudo-NMOS Inverters	178
4.8	Sizing Inverters	181
4.9	Tristate Inverters	184
4.10	Summary	185
5	Static MOS Gate Circuits	195
5.1	Introduction	195
5.2	CMOS Gate Circuits	197
5.2.1	Basic CMOS Gate Sizing	198
5.2.2	Fanin and Fanout Considerations	202
5.2.3	Voltage Transfer Characteristics (VTC) of CMOS Gates	205
5.3	Complex CMOS Gates	209
5.4	XOR and XNOR Gates	212
5.5	Multiplexer Circuits	214
5.6	Flip-Flops and Latches	214
5.6.1	Basic Bistable Circuit	215
5.6.2	SR Latch	216
5.6.3	JK Flip-Flop	220
5.6.4	JK Master-Slave Flip-Flop	221
5.6.5	JK Edge-Triggered Flip-Flop	222
5.7	D Flip-Flops and Latches	223
5.8	Power Dissipation in CMOS Gates	227
5.8.1	Dynamic (Switching) Power	228
5.8.2	Static (Standby) Power	235
5.8.3	Complete Power Equation	237
5.9	Power and Delay Tradeoffs	238
5.10	Summary	241
6	High-Speed CMOS Logic Design	249
6.1	Introduction	249
6.2	Switching Time Analysis	251
6.2.1	Gate Sizing Revisited—Velocity Saturation Effects	255
6.3	Detailed Load Capacitance Calculation	257
6.3.1	Fanout Gate Capacitance	258
6.3.2	Self-Capacitance Calculation	260
6.3.3	Wire Capacitance	267

6.4	Improving Delay Calculation with Input Slope	267
6.5	Gate Sizing for Optimal Path Delay	276
6.5.1	Optimal Delay Problem	276
6.5.2	Inverter Chain Delay Optimization—FO4 Delay	277
6.5.3	Optimizing Paths with NANDs and NORs	283
6.6	Optimizing Paths with Logical Effort	286
6.6.1	Derivation of Logical Effort	286
6.6.2	Understanding Logical Effort	292
6.6.3	Branching Effort and Sideloads	297
6.7	Summary	301
7	Transfer Gate and Dynamic Logic Design	309
7.1	Introduction	309
7.2	Basic Concepts	310
7.2.1	Pass Transistors	310
7.2.2	Capacitive Feedthrough	313
7.2.3	Charge Sharing	316
7.2.4	Other Sources of Charge Loss	318
7.3	CMOS Transmission Gate Logic	318
7.3.1	Multiplexers Using CMOS Transfer Gates	320
7.3.2	CMOS Transmission Gate Delays	325
7.3.3	Logical Effort with CMOS Transmission Gates	331
7.4	Dynamic D-Latches and D Flip-Flops	333
7.5	Domino Logic	336
7.5.1	Logical Effort for Domino Gates	342
7.5.2	Limitations of Domino Logic	343
7.5.3	Dual-Rail (Differential) Domino Logic	346
7.5.4	Self-Resetting Circuits	349
7.6	Summary	349
8	Semiconductor Memory Design	359
8.1	Introduction	359
8.1.1	Memory Organization	360
8.1.2	Types of Memory	362
8.1.3	Memory Timing Parameters	363
8.2	MOS Decoders	364
8.3	Static RAM Cell Design	368
8.3.1	Static Memory Operation	368
8.3.2	Read Operation	371
8.3.3	Write Operation	374
8.3.4	SRAM Cell Layout	376
8.4	SRAM Column I/O Circuitry	377
8.4.1	Column Pull-Ups	378

8.4.2	Column Selection	380
8.4.3	Write Circuitry	382
8.4.4	Read Circuitry	382
8.5	Memory Architecture	390
8.6	Summary	393
9	Additional Topics in Memory Design	399
9.1	Introduction	399
*9.2	Content-Addressable Memories (CAMs)	400
*9.3	Field-Programmable Gate Array	407
9.4	Dynamic Read-Write Memories	413
9.4.1	Three-Transistor Dynamic Cell	414
9.4.2	One-Transistor Dynamic Cell	415
9.4.3	External Characteristics of Dynamic RAMs	419
9.5	Read-Only Memories	421
9.5.1	MOS ROM Cell Arrays	421
9.6	EPROMs and E ² PROMs	425
*9.7	Flash Memory	432
*9.8	FRAMs	435
9.9	Summary	436
10	Interconnect Design	441
10.1	Introduction	441
10.2	Interconnect RC Delays	444
10.2.1	Wire Resistance	444
10.2.2	Elmore Delay Calculation	446
10.2.3	RC Delay in Long Wires	449
10.3	Buffer Insertion for Very Long Wires	453
10.4	Interconnect Coupling Capacitance	457
10.4.1	Components of Coupling Capacitance	457
10.4.2	Coupling Effects on Delay	463
10.4.3	Capacitive Noise or Crosstalk	467
*10.5	Interconnect Inductance	468
*10.6	Antenna Effects	473
10.7	Summary	477
11	Power Grid and Clock Design	483
11.1	Introduction	483
11.2	Power Distribution Design	484
11.2.1	IR Drop and Ldi/dt	485
11.2.2	Electromigration	488
11.2.3	Power Routing Considerations	491

11.2.4	Decoupling Capacitance Design	493
11.2.5	Power Distribution Design Example	495
11.3	Clocking and Timing Issues	499
11.3.1	Clock Definitions and Metrics	499
11.3.2	Clock Skew	501
11.3.3	Effect of Noise on Clocks and FFs	504
11.3.4	Power Dissipation in Clocks	506
11.3.5	Clock Generation	507
11.3.6	Clock Distribution for High-Performance Designs	509
11.3.7	Example of a Clock Distribution Network	511
11.4	Phase-Locked Loops/Delay-Locked Loops	514
11.4.1	PLL Design Considerations	516
11.4.2	Clock Distribution Summary	522
Appendix A A Brief Introduction to SPICE		529
A.1	Introduction	529
A.2	Design Flow	530
A.3	Syntax	531
A.3.1	Title	532
A.3.2	Settings of Various Global Parameters	532
A.3.3	Listing of Sources and Active and Passive Elements	534
A.3.4	Analysis Statements	541
A.4	Complete SPICE Examples	545
Appendix B Bipolar Transistors and Circuits		547
B.1	The Bipolar Junction Transistor	547
B.2	The Schottky-Barrier Diode	550
B.3	BJT Model for Circuit Simulation	552
B.4	Bipolar Transistor Inverter	553
B.5	Voltage Transfer Characteristics	554
B.6	Schottky-Clamped Inverter	556
B.7	BJT Inverter Switching Times	557
B.8	Bipolar Digital Gate Circuits	558
B.9	Voltage Transfer Characteristics	558
B.10	Propagation Delay Time	561
B.11	Input Clamp Diodes	561
Index		563

Chapter 1**Deep Submicron Digital IC Design**

In the first chapter, we provide a perspective on digital design in the deep submicron era and motivate the topics in the rest of the book. We briefly review important concepts of logic gates primarily to provide notational context for the book, including the ideal logic element, static input-output characteristics, noise margin, and propagation delay time. Then we elaborate on the key issues in deep submicron such as power dissipation, velocity saturated transistors, interconnect resistance, coupling capacitance, and inductance. The role of computer-aided design tools such as SPICE is described. The chapter concludes with the challenges ahead as described in the technology roadmap.

Chapter 2**MOS Transistors**

The short-channel device models to be used in the rest of this book are described in this chapter. To begin the treatment, rudimentary device physics concepts are covered to explain the threshold voltage equation and the transistor current equations. Both long- and short-channel models are derived. Then the oxide and junction capacitance models are described to complete the chapter.

Chapter 3**Fabrication, Layout, and Simulation**

This chapter describes the relationship between fabrication, layout, and simulation in the integrated circuit design process. The topics of fabrication and layout are important to IC designers and should be well-understood. However, for this course, it serves more as a background for the rest of the text. The more important subject is simulation with SPICE. The model parameters for SPICE are detailed in this chapter. A brief user manual is provided in Appendix A for those unfamiliar with the basics of SPICE. We also provide some advanced material on MOS transistors and fabrication technologies of the future.

Chapter 4**MOS Inverter Circuits**

This is a core chapter on MOS digital inverters and introduces concepts of voltage transfer characteristics, noise margins, inverter configurations, and simple timing and power calculations. Analytical equations are derived for noise margin parameters and switching thresholds of inverters for a number of MOS inverters.

Chapter 5**Static MOS Gate Circuits**

This is another core chapter of the book. It examines the static design issues for NANDs, NORs, and complex gates. It develops extensions to inverter design to size the transistors in CMOS gates. Sequential elements, such as flip-flops and latches, are described in this chapter. The chapter concludes with a detailed treatment of the various components of power dissipation in logic gates.

Chapter 6

High-Speed CMOS Logic Design

This chapter describes the issues involved in high-speed logic design. It develops useful equations for switching delay calculation for step and ramp inputs. This involves the use of the large-signal on-resistance of gates, and the calculation of the loading capacitance, both of which are detailed. The total capacitance can be computed using two key parameters for input and output capacitance. Gate sizing for equal delay and minimal delay are described. The thrust of the latter half of this chapter is high-speed logic optimization using logical effort.

Chapter 7

Transfer Gate and Dynamic Logic Design

In this chapter, we explore dynamic design techniques using transmission gates and precharged logic. The important concepts of charge-sharing, bootstrapping, feedthrough, and charge leakage are elaborated in this chapter. Domino logic is described in detail as it is the most common form of dynamic logic in use today. These concepts lay the groundwork for the operation of many of the memory circuits discussed in the next two chapters.

Chapter 8

Semiconductor Memory Design

This chapter addresses the analysis and design of VLSI memories, commonly known as semiconductor memories. In this chapter, we classify the different types of memory, examine the major subsystems, and then focus on the static RAM (SRAM) design issues. This topic is particularly suitable for our study of CMOS digital design as it allows us to apply many of the basic concepts presented in earlier chapters. The entire design process for static RAMs is described in detail.

Chapter 9

Additional Topics in Memory Design

This chapter explores a variety of other semiconductor memories, their architectures, access mechanisms, and cell configurations. We begin by examining content-addressable memories, since they are a derivative of the SRAM architecture. We also cover an important application of SRAM cells in the growing market segment of programmable logic called field-programmable gate-arrays (FPGAs). The chapter sequences through dynamic RAMs, mask-programmable ROMs, erasable programmable ROMs, electrically-erasable ROMs and Flash memories, and concludes with a look at memory cells based on ferroelectric materials called FRAMs.

Chapter 10

Interconnect Design

This chapter is devoted to the study of interconnect issues that the IC designer faces when designing in deep submicron technologies. It addresses the issues associated with *RLC* aspects of wires in detail. We begin by re-examining the *RC* delay calculation using the Elmore delay, and address the issue of buffer insertion in long wires.

USEFUL DESIGN PARAMETERS (simplified)

Name	Symbol	0.18 μm		0.13 μm		Units
		NMOS	PMOS	NMOS	PMOS	
Channel Length (rounded for convenience)	L	200	200	100	100	nm
Supply Voltage	V_{DD}	1.8	1.8	1.2	1.2	V
Oxide Thickness	t_{ox}	35	35	22	22	Å
Oxide Capacitance	C_{ox}	1.0	1.0	1.6	1.6	$\mu\text{F}/\text{cm}^2$
Threshold Voltage	V_{T0}	0.5	-0.5	0.4	-0.4	V
Body-Effect Term	γ	0.3	0.3	0.2	0.2	$\text{V}^{1/2}$
Fermi Potential	$2 \phi_F $	0.84	0.84	0.88	0.88	V
Junction Capacitance Coefficient	C_{j0}	1.6	1.6	1.6	1.6	$\text{fF}/\mu\text{m}^2$
Built-In Junction Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Grading Coefficient	m	0.5	0.5	0.5	0.5	—
Nominal Mobility (low vertical field)	μ_0	540	180	540	180	$\text{cm}^2/\text{V}\cdot\text{s}$
Effective Mobility (high vertical field)	μ_e	270	70	270	70	$\text{cm}^2/\text{V}\cdot\text{s}$
Critical Field	E_c	6×10^4	24×10^4	6×10^4	24×10^4	V/cm
Critical Field $\times L$	$E_c L$	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eff}	12.5	30	12.5	30	$\text{k}\Omega/\square$

Name	Symbol	Value	Units
Gate Capacitance Coefficient	C_g	2	$\text{fF}/\mu\text{m}$
Self Capacitance Coefficient	C_{eff}	1	$\text{fF}/\mu\text{m}$
Wire Capacitance Coefficient	C_w	0.1–0.25	$\text{fF}/\mu\text{m}$
Al Wire Resistance	R_{\square}	25–60	$\text{m}\Omega/\square$
Cu Wire Resistance	R_{\square}	20–40	$\text{m}\Omega/\square$
Wire Inductance	L_{eff}	40–50	$\text{pH}/\mu\text{m}$

USEFUL PHYSICAL AND MATERIAL CONSTANTS

Name	Symbol	Value	Units
Electron Charge	q	1.6×10^{-19}	C
Boltzmann's Constant	k	1.38×10^{-23}	J/°K
Room Temperature	T	300	°K (27°C)
Thermal Voltage	$V_{th} = kT/q$	26	mV (at 27°C)
Dielectric Constant of Vacuum	ϵ_0	8.85×10^{-14}	F/cm
Dielectric Constant of Silicon	ϵ_{si}	$11.7 \epsilon_0$	F/cm
Dielectric Constant of SiO ₂	ϵ_{ox}	$3.97 \epsilon_0$	F/cm
Intrinsic Carrier Concentration	n_i	1.45×10^{10}	cm ⁻³ (at 27°C)
Carrier Saturation Velocity In Silicon	v_{sat}	8×10^6	cm/s
Aluminum Resistivity	ρ_{Al}	2.7	$\mu\Omega$ -cm
Copper Resistivity	ρ_{Cu}	1.7	$\mu\Omega$ -cm
Tungsten Resistivity	ρ_W	5.5	$\mu\Omega$ -cm

ENGINEERING SCALE FACTORS

G	giga	10^9
M	mega	10^6
k	kilo	10^3
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

METER CONVERSION FACTORS

$1 \mu\text{m} = 10^{-4} \text{cm} = 10^{-6} \text{m}$
 $1 \text{m} = 10^2 \text{cm} = 10^6 \mu\text{m}$
 $0.1 \mu\text{m} = 100 \text{nm}$
 $1 \text{\AA} = 10^{-8} \text{cm} = 10^{-10} \text{m}$