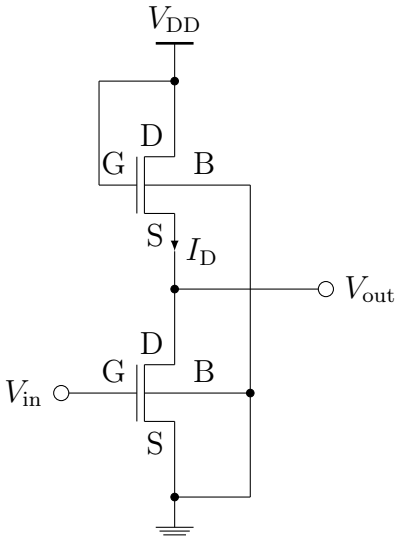

Figure 6.1: NMOS Inverter

Task 6.1

Fig. 6.1 shows a pull-up transistor. Specify whether the transistor is operating in the saturation or cut-off range during operation and calculate the output voltage high (V_{OH}). Use the values of a 0.13μm technology ($2|\Phi_F| = 0.88$V, $\gamma = 0.2\text{V}^{1/2}$).

Task 6.2

Design an inverter with a NMOS load. For the input voltage $V_{in} = V_{DD}$ an output level $V_{OL} = 0.1$V is required. Use the values of a 0.13μm technology ($\mu_n = 270\text{cm}^2/\text{Vs}$, $E_{CN}L = 0.6$V, $v_{sat} = 8 \cdot 10^6\text{cm/s}$).

Task 6.3

Derive the general formulas V_{IL}, V_{IH} and V_{OUH} for the CMOS inverter in Fig. 6.2. The NMOS transistor is in saturation range, the PMOS transistor in linear range.

Task 6.4

Compare the voltage transfer characteristic from a SPICE calculation with the results of a manual calculation for a CMOS inverter (Fig. 6.2) with $W_N = 400$nm and $W_p = 800$nm. Use the values of a 0.18μm CMOS technology ($\mu_n = 270\text{cm}^2/\text{Vs}$, $\mu_p = 70\text{cm}^2/\text{Vs}$, $C_{ox} = 1\mu\text{F/cm}^2$, $V_{TN} = 0.5$V, $V_{TP} = -0.5$V, $V_{DD} = 1.8$V, $L = 200$nm, $E_{CN}L = 1.2$V, $E_{CP}L = 4.8$V, $v_{sat} = 8 \cdot 10^6\text{cm/s}$).

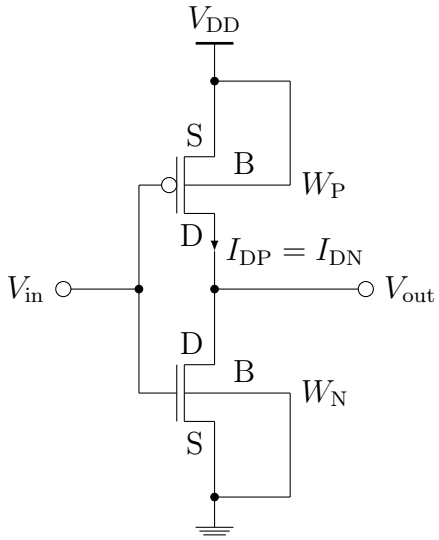

Figure 6.2: CMOS Inverter

Task 6.5

Calculate the switching point V_S of a CMOS inverter with $W_P = 400$nm and $W_P = 100$nm. In both cases $W_N = 100$nm applies. How do changes from W_P affect V_S? Use the values of a 0.13μm technology ($E_{CP} = 4E_{CN}$).

Task 6.6

Calculate drain currents and threshold voltages of the CMOS Inverter.

a) How large must the ratio W_P/W_N be for the inverter in Fig. 6.2 to have symmetrical pull-up and pull-down behavior ($I_{DN}(\text{sat}) = I_{DP}(\text{sat})$).

b) In standby mode, the NMOS should draw 50% less power. In this mode, $V_{in} = V_{DD}$ and $V_{out} = 0.5$V. Which voltage must be V_{SB}?

Use the values of a 0.13μm technology.

Task 6.7

Design a pseudo-NMOS inverter as shown in Fig. 6.3b with $V_{OH} = V_{DD} = 1.8$V and $V_{OL} = 0.065$V. Compare the voltage transfer characteristic (VTC) from a SPICE calculation with the results of a manual calculation. Use the values of a 0.18μm technology.

Task 6.8

Given are the CMOS and the pseudo-NMOS inverter in Fig. 6.3. Size the two inverters according to the following specification assuming that the load is 50fF: CMOS Inverter - $t_{PHL} = t_{PLH} < 50$ps, $V_{OH} = 1.2$V, $V_{OL} = 0$V, low power consumption and minimum area; pseudo-NMOS Inverter - $t_{PHL} < 50$ps, $V_{OH} = 1.2$V, $V_{OL} = 0.1$V, low power consumption

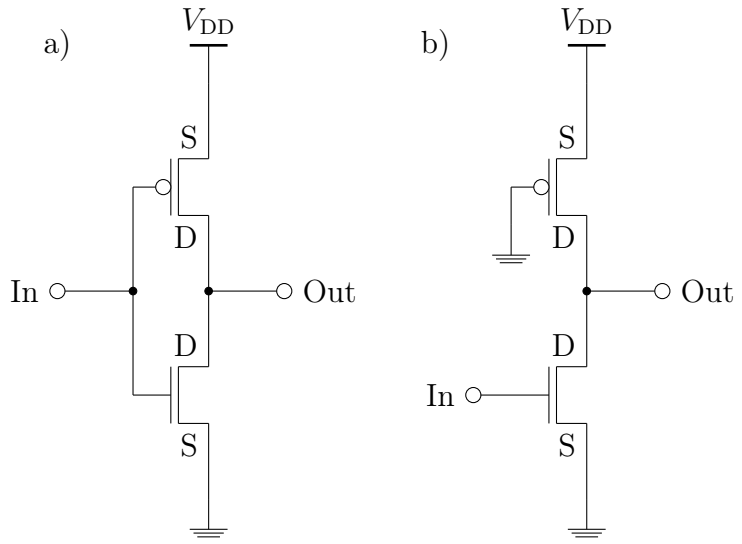

Figure 6.3: Schematic CMOS Inverter (a) and Pseudo-NMOS Inverter (b)

and minimum area. $V_{PHL} = 0.2$V, pseudo-NMOS Inverter - $t_{PHL} < 50$ps, $V_{OH} = 1.1$V, $V_{OL} = 0.1$V, low power consumption and minimum area.

Task 6.9

The two CMOS circuits in Fig. 6.4 are considered as tristate buffers. Discuss how these two circuits work as tristate buffers and which one is more suitable as a tristate buffer.

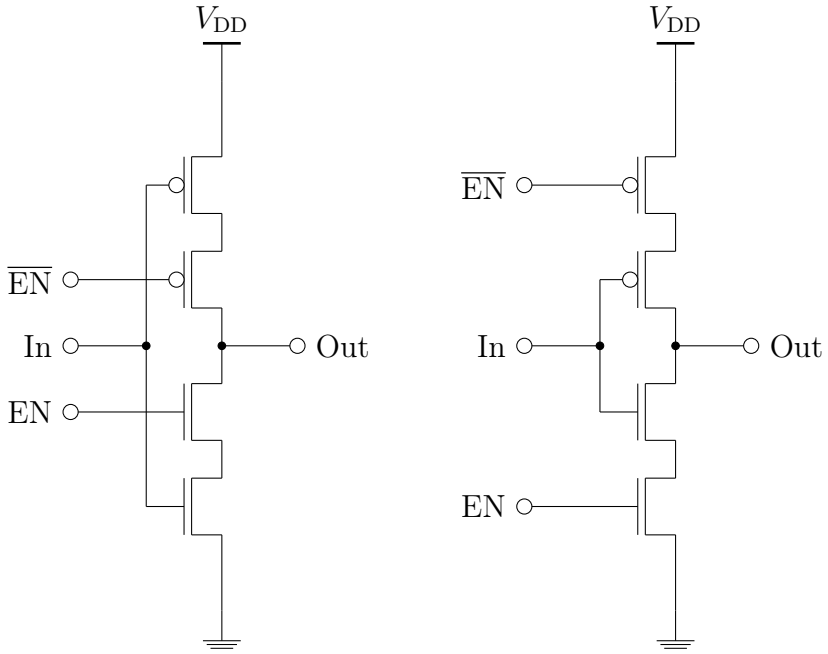

Figure 6.4: Tri-State Inverter