Solution 11.1

a) $LE(A) = \frac{(C_{\text{in}}R_{\text{on}})_{\text{gate}}}{(C_{\text{in}}R_{\text{on}})_{\text{inv}}} = \frac{4W(2R)}{3W(R)} = \frac{8}{3}$

$LE(S) = \frac{(C_{\text{in}}R_{\text{on}})_{\text{gate}}}{(C_{\text{in}}R_{\text{on}})_{\text{inv}}} = \frac{W(2R)}{3W(R)} = \frac{2}{3}$

b) $LE(A) = \frac{(C_{\text{in}}R_{\text{on}})_{\text{gate}}}{(C_{\text{in}}R_{\text{on}})_{\text{inv}}} = \frac{4W(5R/4)}{3W(R)} = \frac{5}{3}$

$LE(S) = \frac{(C_{\text{in}}R_{\text{on}})_{\text{gate}}}{(C_{\text{in}}R_{\text{on}})_{\text{inv}}} = \frac{4W(5R/4)}{3W(R)} = \frac{5}{3}$

Solution 11.2

a) For equal rise and fall times we double the size of the transistors:

$$LE(A) = \frac{(C_{\text{in}}R_{\text{on}})_{\text{gate}}}{(C_{\text{in}}R_{\text{on}})_{\text{inv}}} = \frac{C_{\text{g}} \cdot 3W \cdot R_{\text{eqn}}}{C_{\text{g}} \cdot 3W \cdot R_{\text{eqn}}} = 1$$

b) For the pseudo-NMOS we first have to calculate the ratio of the currents, since these are different for the PMOS and NMOS. In case of the pull-up the PMOS charges the output, so for the same delay the output is doubled:

$$LE(B) = \frac{(C_{\text{in}}R_{\text{on}})_{\text{gate}}}{(C_{\text{in}}R_{\text{on}})_{\text{inv}}} = \frac{C_{\text{g}} \cdot 2W \cdot R_{\text{eqn}}}{C_{\text{g}} \cdot 3W \cdot R_{\text{eqn}}} = \frac{2}{3}$$

Solution 11.3

The results for a two-stage multiplexer ($R_{\text{inv}} = R$, $R_{\text{TG}} = R$) are

$$\begin{aligned}
C_1 &= C_{\text{in,TG,on}} + C_{\text{self,inv}} \\
&= (C_{\text{eff}}2W + C_{\text{g}}W) + C_{\text{eff}}3W \\
&= C_{\text{eff}}5W + C_{\text{g}}W \\
C_2 &= C_{\text{out,TG,on}} + C_{\text{out,TG,off}} + C_{\text{in,TG,on}} \\
&= (C_{\text{eff}}2W + C_{\text{g}}W) + C_{\text{eff}}2W + (C_{\text{eff}}2W + C_{\text{g}}W) \\
&= C_{\text{eff}}6W + C_{\text{g}}2W \\
C_3 &= C_{\text{out,TG,on}} + C_{\text{out,TG,off}} + C_{\text{in,inv}} \\
&= (C_{\text{eff}}2W + C_{\text{g}}W) + C_{\text{eff}}2W + C_{\text{g}}\text{f}3W \\
&= C_{\text{eff}}4W + C_{\text{g}}(1 + 3\text{f})W
\end{aligned}$$

$$t_{\text{Elmore,2MUX}} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3$$

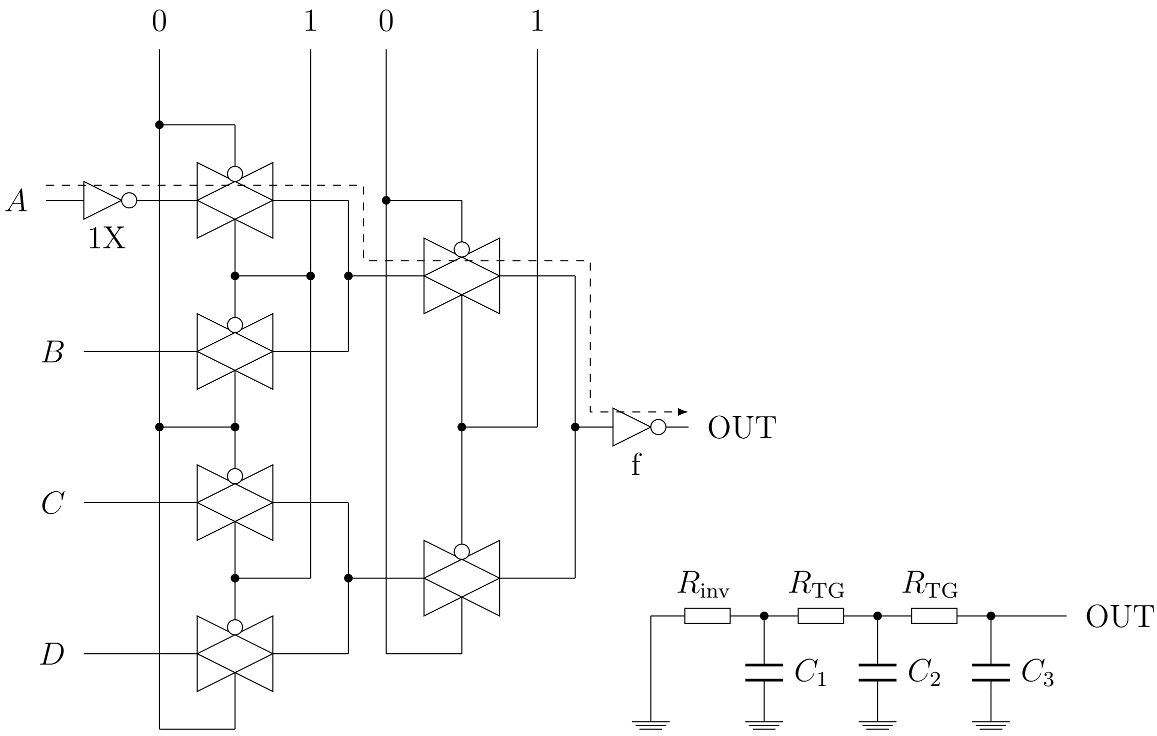


Figure 11.6: Two-Stage Multiplexer (2MUX)

$$
\begin{aligned}
&= R_{\text{inv}}C_1 + (R_{\text{inv}} + R_{\text{TG}})C_2 + (R_{\text{inv}} + 2R_{\text{TG}})C_3 \\
&= R(29C_{\text{eff}} + 8C_{\text{g}} + 9\text{f}C_{\text{g}})W
\end{aligned}
$$

and for a single-stage multiplexer ($R_{\text{inv}} = R$, $R_{\text{TG}} = R$)

$$
\begin{aligned}
C_4 &= C_{\text{in,TG,on}} + C_{\text{self,inv}} \\
&= (C_{\text{eff}}2W + C_{\text{g}}W) + C_{\text{eff}}3W \\
&= C_{\text{eff}}5W + C_{\text{g}}W \\
C_5 &= C_{\text{TG,on}} + 3C_{\text{TG,off}} + C_{\text{in,inv}} \\
&= C_{\text{eff}}2W + C_{\text{g}}W + 3C_{\text{eff}}2W + C_{\text{g}}\text{f}3W \\
&= C_{\text{eff}}8W + C_{\text{g}}(1 + 3\text{f})W
\end{aligned}
$$

$$
\begin{aligned}
t_{\text{Elmore,1MUX}} &= R_4C_4 + (R_4 + R_5)C_5 \\
&= RC_{\text{eff}}21W + RC_{\text{g}}(3 + 6\text{f})W \\
&= R(21C_{\text{eff}} + 3C_{\text{g}} + 6\text{f}C_{\text{g}})W
\end{aligned}
$$

Comparing the two cases, 2MUX is slower than 1MUX. However, 1MUX requires more routing resources.

Many transfer gates without buffering quickly increase the delay. For driving a large load, TGs do not have the necessary driver capability.

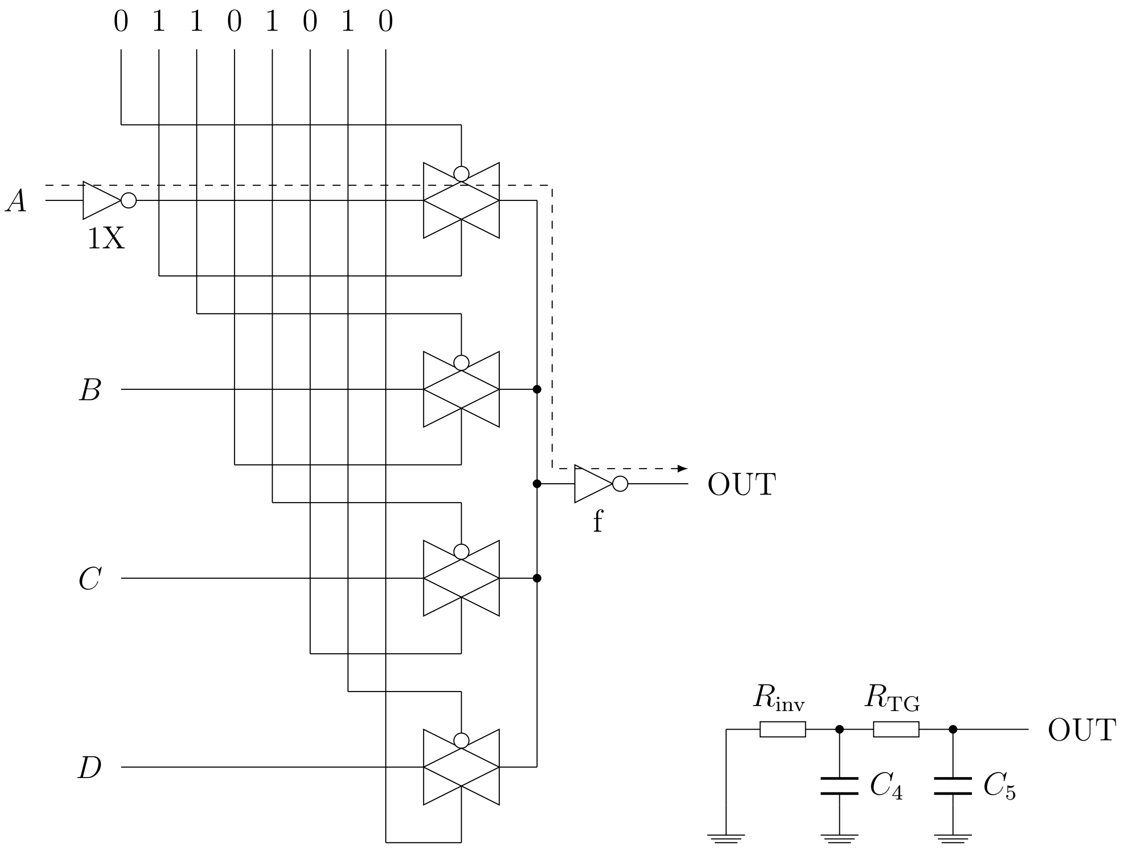
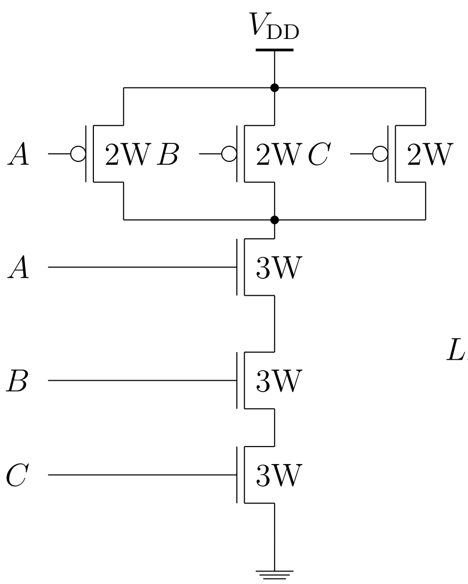


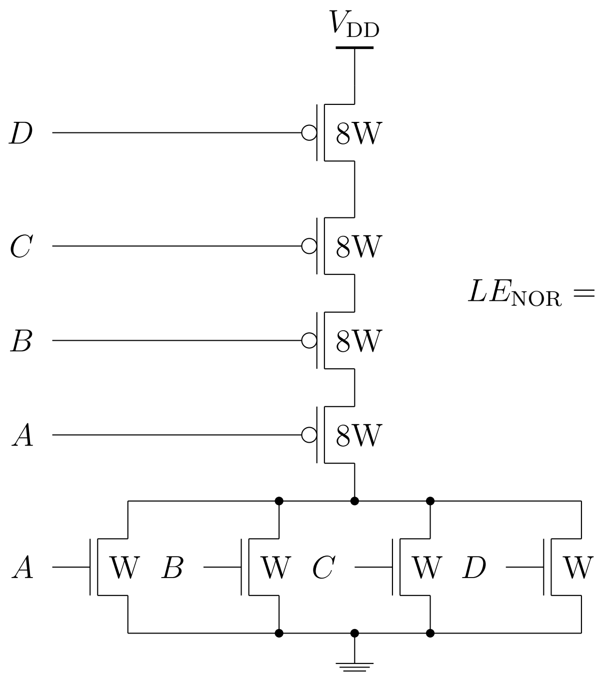
Figure 11.7: One-stage Multiplexer (1MUX)

Solution 11.4



$$LE_{\text{NAND}} = \frac{\tau_{\text{NAND}}}{\tau_{\text{INV}}} = \frac{n \cdot (2W + 3W) \cdot R/n}{(2W + 1W) \cdot R} = \frac{5}{3}$$

Figure 11.8: NAND3



$$LE_{\mathrm{NOR}} = \frac{\tau_{\mathrm{NOR}}}{\tau_{\mathrm{INV}}} = \frac{n \cdot (8W + 1W) \cdot R/n}{(2W + 1W) \cdot R} = \frac{9}{3}$$

Figure 11.9: NOR4

Solution 11.5

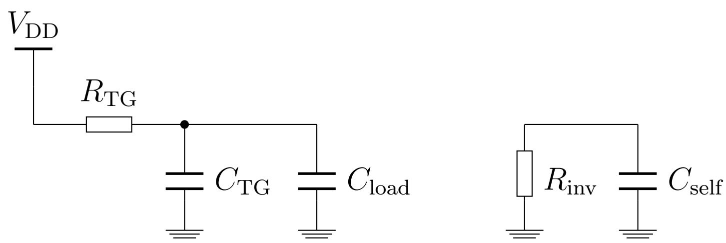


Figure 11.10: Equivalent Circuit Diagram

$V_{\mathrm{Q}} = V_{\mathrm{DD}} = 1,8\mathrm{V}$ and $V_{\overline{\mathrm{Q}}} = 0\mathrm{V}$. The clock feedthrough has no effect, because PMOS dominates. For a CLK of $0 \rightarrow 1$ the TG is in the ON state.

For the CLK (A is already switched) dependent delay of $\overline{Q}$ follows

$$\begin{aligned} t_{\mathrm{PHL}} &= R_{\mathrm{TG}}(C_{\mathrm{TG}} + C_{\mathrm{load}}) + R_{\mathrm{inv}}C_{\mathrm{self}} \\ &= R_{\mathrm{eqn}}(C_{\mathrm{g}} + 2C_{\mathrm{eff}} + 3C_{\mathrm{g}} + 3C_{\mathrm{eff}})W \\ &= (12.5 \cdot 10^3\Omega)(2 + 2 \cdot 1 + 3 \cdot 2 + 3 \cdot 1)(10^{-15}\mathrm{F})(0.2) \\ &= 25\mathrm{ps} + 7.5\mathrm{ps} \\ &= 32.5\mathrm{ps} \end{aligned}$$