Task 7.1

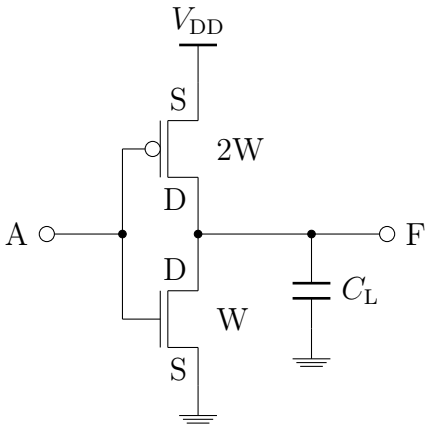

Figure 7.1: Sizing a CMOS Inverter

Design a NAND3 and NOR3 gate in CMOS. It is assumed that all transitions are to be sized according to the inverter in Fig. 7.1.

Task 7.2

Provide two additional multi-level implementions of an AND8 gate.

Task 7.3

a) Calculate the switching voltage V_S of a NAND2 (Fig. 7.2). Boundary conditions are:

   i) exactly one input is connected to V_{DD}, the other input performs a transition from 0 to V_{DD};

   ii) both inputs are connected to each other.

   Assumption: 0.18 μm technology parameter, $W_N = W_P = 400$nm.

b) Use SPICE to compare the voltage transfer characteristics (V_S) of the two above cases of a NAND2. Also, assume that the A and B inputs each switch independently. Why are the results different?

Task 7.4

Given is the expression

$F = \overline{AB + CD}$.

Implement it as single-level CMOS complex as well as pseudo-NMOS.

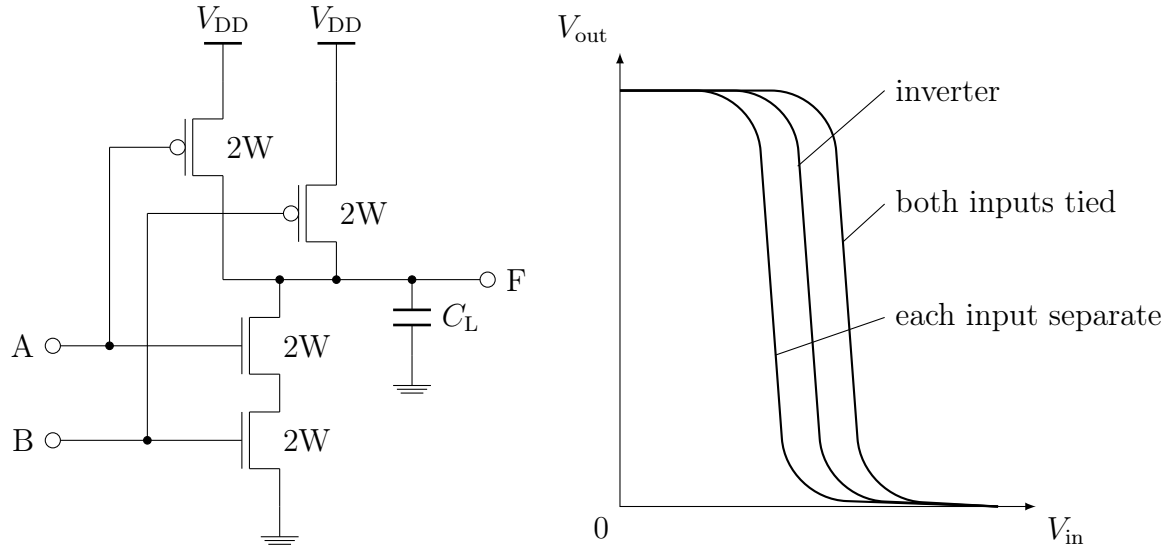

Figure 7.2: Voltage Transmission Characteristics (VTC) of NAND2

Task 7.5

Design the logical function for the circuit in Fig. 7.3. What is the worst case for the voltages V_{OH} and V_{OL}? Assume a load capacitance of 100fF at the output. What does this influence the logical values High (H) and Low (L)?

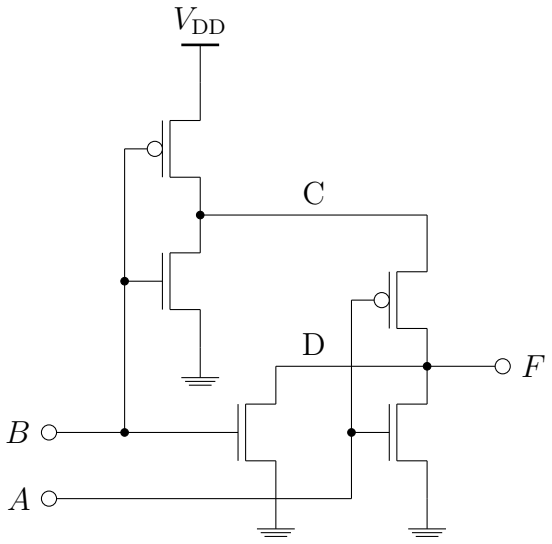

Figure 7.3: Schematic of a digital circuit

Task 7.6

Design a RS Latch in 0.13μm CMOS technology($\mu_\mathrm{n} = 270\mathrm{cm}^2/\mathrm{Vs}$, $C_\mathrm{ox} = 1.6\mu\mathrm{F}/\mathrm{cm}^2$, $V_\mathrm{TN} = 0.4\mathrm{V}$, $V_\mathrm{TP} = -0.4\mathrm{V}$, $V_\mathrm{DD} = 1.2\mathrm{V}$, $E_\mathrm{CN} = 6 \cdot 10^4\mathrm{V}/\mathrm{cm}$, $E_\mathrm{CP} = 4E_\mathrm{CN}$, $L = 100\mathrm{nm}$, $\upsilon_\mathrm{sat} = 8 \cdot 10^6\mathrm{cm}/\mathrm{s}$, $E_\mathrm{CN}L = 0.6\mathrm{V}$, $|2\phi_\mathrm{F}| = 0.88\mathrm{V}$, $\gamma = 0.2\mathrm{V}^{1/2}$, $R_\mathrm{L} = 20\mathrm{k}\Omega$) Use NOR gates with a delay of 400ps. The load driven by Q or $\overline{Q}$ is 100fF.

Task 7.7

The circuit in Fig. 7.4 is a saturated-enhancement load NMOS NOR. Calculate V_OL and V_OH, I_DC and power P_DC for the output to logical zero. All transistors should be $2\lambda/2\lambda$ circuits. Use a 0.13μm technology.

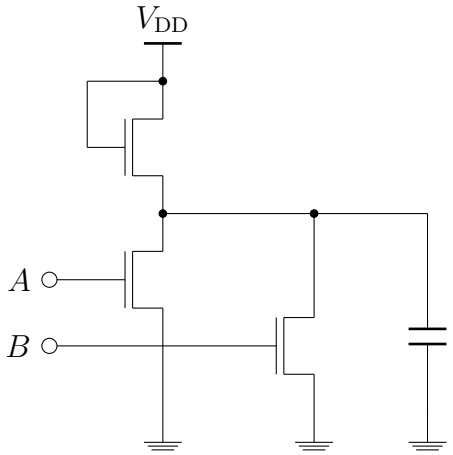

Figure 7.4: Saturated-Enhancement Load NMOS NOR