Solution 13.1 Dimensioning a Decoder

We work our way from the exit to the entrance, taking into account the LE and BE: $C_{\text{out}} = 1$, $C_{\text{inv1}} = (1 \cdot 1 \cdot C_{\text{out}})/4$, $C_{\text{nand3}} = (5/3 \cdot 1 \cdot C_{\text{inv1}})/4$, $C_{\text{inv2}} = (1 \cdot 16 \cdot C_{\text{nand3}})/4$, $C_{\text{nand2}} = (4/3 \cdot 1 \cdot C_{\text{inv2}})/4$.

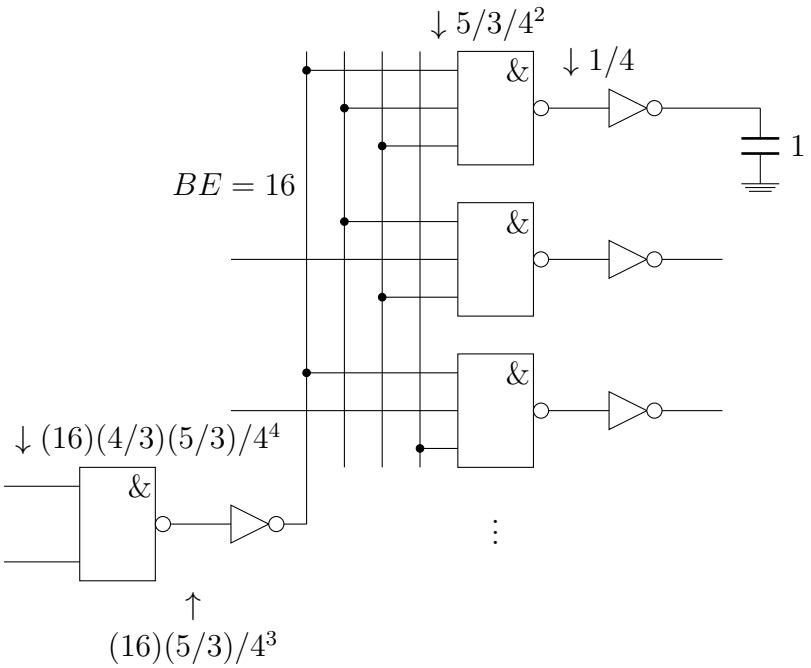

Figure 13.3: Dimensioning a Path with LE

Solution 13.2 Design Rules for a Read Cycle

For wl =H M3 behaves like a saturated-enhancement-load for M1. The driver M1 is located in the linear range:

$$\frac{W_1}{L_1}\frac{\mu_\mathrm{n}C_\mathrm{ox}}{\left(1+\frac{V_\mathrm{q}}{E_\mathrm{CN}L_1}\right)}\left[(V_\mathrm{DD}-V_\mathrm{T1})V_\mathrm{q}-\frac{V_\mathrm{q}^2}{2}\right]=\frac{W_3 v_\mathrm{sat}C_\mathrm{ox}(V_\mathrm{DD}-V_\mathrm{q}-V_\mathrm{T3})^2}{(V_\mathrm{DD}-V_\mathrm{q}-V_\mathrm{T3})+E_\mathrm{CN}L_3}$$

Eleminate C_ox, insert $V_\mathrm{q}=0.1\mathrm{V}$ and ignore the body effect, resulting in

$$\frac{W_1}{0.1\cdot^{-4}\,\mathrm{cm}}\frac{\left(270\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right)}{\left(1+\frac{0.1}{0.6}\right)}\left[(1.2-0.4)0.1-\frac{0.1^2}{2}\right]=\frac{W_3(8\cdot10^6\mathrm{cm/s})(1.2-0.1-0.4)^2}{(1.2-0.1-0.4)+0.6}$$

$$\therefore\frac{W_1}{W_3}\approx 1.7$$

With body effect this ratio would be lower. The actual values of the transistor widths then depend on the desired rate of change of the bit line voltage, the specified delay and the discharge current. For a transition of 200mV in 2ns for a total bit line capacity of 2pF, the average current through M1 and M3 is

$$I_\mathrm{cell}=C_\mathrm{bit}\cdot\frac{\Delta V}{\Delta\tau}=2\mathrm{pF}\cdot\frac{200\mathrm{mV}}{2\mathrm{ns}}=200\mu\mathrm{A}$$

For the switched on access transistor we can calculate its width:

$$I_\mathrm{cell}\approx\frac{W_3(8\cdot10^6\mathrm{cm/s})(1.6\mu\mathrm{F/cm}^2)(1.2-0.1-0.4)^2}{(1.2-0.1-0.4)+0.6}=200\mu\mathrm{A}$$

$$\therefore W_3=0.4\mu\mathrm{m}$$

That makes $W_1=0.7\mu\mathrm{m}$. Both sizes are too large for a 1MBit SRAM.

Solution 13.3 Word and Bit Lines

If we design a 64K SRAM, it would contain a core range of 256×256 cells. We now ignore the resistance. The total column capacitance (bitlines) would be due to the gate capacitance of 512 access transistors and the line capacitance of 256 cells:

$$C_{\text{word}} = 512 \times 2\text{fF}/\mu\text{m} \times 0.5\mu\text{m} + 256 \times 30\lambda \times 0.2\text{fF}/\mu\text{m} \times 1\mu\text{m}/20\lambda = 589\text{fF}$$

The bit capacitance per cell due to the S/D capacitance of the access transistors is less than usual, because the voltage drop over the transition is near V_{DD}. In addition, there is a line capacitance and half a contact capacitance per cell:

$$C_{\text{bit}} = 256\times0.5\text{fF}/\mu\text{m}\times0.5\mu\text{m}+256\times40\lambda\times0.2\text{fF}/\mu\text{m}\times0.1\mu\text{m}/2\lambda+128\times0.5\text{fF} = 230\text{fF}$$