APPENDIX
B

Bipolar Transistors and Circuits

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B.1 The Bipolar Junction Transistor

Before manufacturable MOS technologies were developed, digital integrated circuits were based upon bipolar junction transistors (BJTs) and Schottky-barrier (metal-semiconductor) diodes (SBDs). The word *bipolar* refers to the fact that both electrons and holes are required for normal operation of the BJT. For MOS transistors (sometimes termed *unipolar*), only one type of mobile carrier is required for normal operation.

This Appendix provides a brief summary of the structure and operation of BJTs and SBDs, and an introduction to the most widely used digital circuits based upon them. A short summary of the model representations for BJTs and SBDs in the SPICE circuit simulation program is also included in this Appendix.

An *npn* bipolar junction transistor is made by forming two *pn* junctions in a single silicon crystal, such that the *p* region is common and very narrow ($\leq 0.5\ \mu$m). This is shown in cross section in Figure B.1a, where the two *n* regions, the emitter *E*

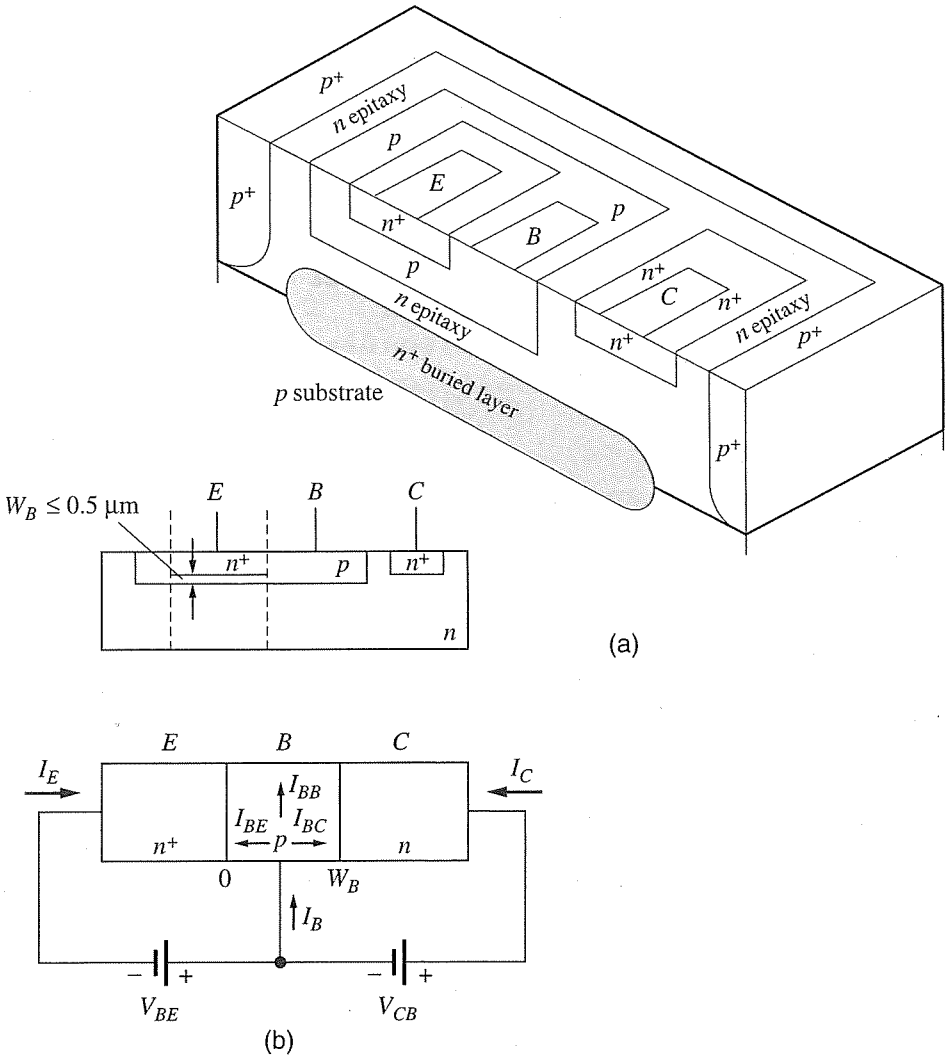


Figure B.1

(a) Cross section of *npn* bipolar junction transistor. (b) *npn* transistor structure biased in the forward active mode.

and the collector *C*, sandwich the *p* region, the base *B*. The analysis that follows is idealized in that a one-dimensional structure is assumed. The dashed lines in Figure B.1a show where such a region may be assumed to exist.

The biasing batteries as shown in Figure B.1b cause the transistor to operate in the forward active mode. That is, the base-emitter junction is forward-biased by V_{BE} being positive at the base, and the base-collector junction is reverse-biased by V_{CB} being positive at the collector. The emitter must be much more heavily doped (*n-type*) than the base (*p-type*) to achieve effective operation.

As we forward-bias the emitter junction, electrons (the majority carriers in the emitter of this *npn* example) are thus injected (emitted) into the base, where they become minority carriers since the base is a *p* region. At the reverse-biased collector

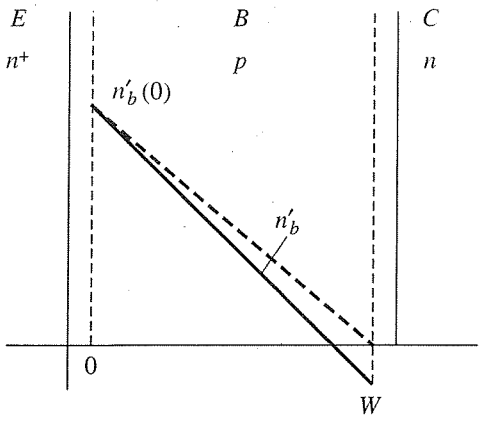


Figure B.2
Excess minority carrier concentration in neutral base region; *npn* transistor biased in forward active mode.

junction, electrons are swept out (collected) by the positive collector and are seen as collector current, I_C.

The steady-state distribution of injected electrons across the base is shown in Figure B.2. During transit, a small fraction of the electrons in transit (typically less than 1%) are lost to recombination and are seen as current at the base, I_B. The injected electron current, the emitter current I_E, crosses the base region primarily by *diffusion* driven by the electron concentration gradient from left to right. The ratio of I_C/I_B is the dc common emitter forward current gain, β_F. A typical value is $\beta_F = 100$. The ratio of I_C/I_E is the dc forward current gain; $\alpha_F \approx 0.99$ is typical.

Because the emitter-base junction is a normal *pn* junction, we can relate the emitter current I_E to the base-emitter voltage V_{BE} using

$$I_E = I_S(e^{V_{BE}/V_T} - 1) \tag{B.1}$$

where I_S the reverse saturation current of the emitter-base diode, and V_T is the thermal voltage given by kT/q. (Note: this is not the threshold voltage of the MOS device.) A typical value for an integrated circuit transistor is $I_S = 10^{-16}$ A.

Below, when we discuss the dynamic properties of the junction transistor, we will make use of the charge-control expressions. This will require a knowledge of the *excess minority carrier charge* Q_F stored in the neutral base region. Consider a steady-state condition and neglect the small loss due to recombination. The integral of the triangular area under the charge distribution shown in Figure B.2 can be interpreted as being proportional to Q_F. The slope of the distribution can be interpreted as being proportional to flux of charge, or current I_C. For a fixed base width W, current I_C and charge Q_F must be in direct proportion, with a constant of proportionality having dimensions of time. Thus we define the relationship:

$$Q_F = \tau_F I_C \tag{B.2}$$

We term the constant τ_F as the *mean forward transit time* of the minority carriers in the base. It is the mean time for the minority carriers to diffuse across the neutral base region from the emitter to the collector.

Simply considering the geometry in Figure B.2, it is clear that if the current (slope) is held constant while base width W is increased, the charge (area) must increase in proportion to W^2. To achieve fast switching in digital circuits, the charge to be moved should be minimized. Thus, minimizing W is important.

If the emitter and collector connections in Figure B.1b are reversed, the transistor would be operating in the reverse active mode. Due to the extremely asymmetric geometry of emitter and collector in the physical structure of Figure. B.1a, the inverse current gain β_R is very low and the reverse transit time τ_R is much larger than for forward active operation. The fact that the collector is more lightly doped than the base means that more minority carriers would be injected from the base to the (much larger) collector than vice versa. Removing such carriers to turn off a conducting reverse transistor is a relatively slow process. Reverse operation of integrated circuit BJTs must be avoided in digital circuits having any speed requirement.

Bipolar transistors have *pn* junction capacitances that are derived in the same way as for MOS transistors (see Section 2.8.2). BJTs also have (undesired) small resistances in series with all electrode connections.

B.2 The Schottky-Barrier Diode

Very useful diodes can be made by forming a microscopically clean contact between certain metals and a lightly doped ($N_D \leq 10^{16}$ cm^{-3}) *n*-type semiconductor, as illustrated in Figure B.3. Because practical means of forming the necessary clean interface were not developed until about 1970, Schottky-barrier diodes[1] were not used in

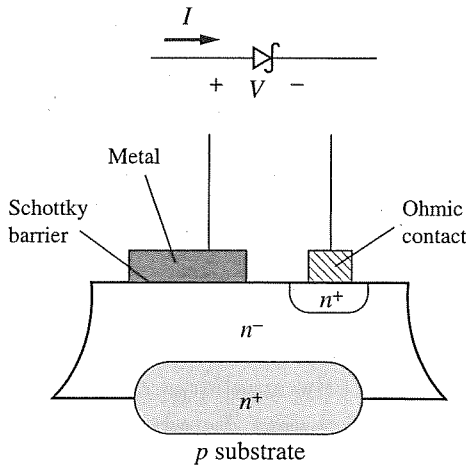


Figure B.3
Cross section of Schottky-barrier diode.

[1] Named for W. Schottky, a pioneer in the study of metal-semicondutor interfaces.

early integrated circuits. Included in Figure B.3 is the circuit symbol for a Schottky diode.

The principal advantage of Schottky diodes is that all conduction is via electrons flowing in metal or n-type silicon. That is, only majority carriers contribute to current flow. Hence there are no minority carrier storage effects, and their limitations on diode switching speed are completely eliminated.

A detailed understanding of the Schottky diode generally involves energy-band theory, which is beyond the scope of this section. For every metal-semiconductor contact there is a characteristic potential barrier ϕ_B which depends only on the two materials. This is the *Schottky barrier.* It is not a function of semiconductor doping and is only a weak function of temperature. The barrier potential blocks the flow of electrons from the metal toward the semiconductor.

In the neutral semiconductor, far from the barrier, and with no externally applied potentials, the electron potential energy in the semiconductor is $\phi_n = V_T \ln (N_D/n_i)$. The potential difference $\phi_B - \phi_n = \phi_0$ is simply the equilibrium difference in energy for electrons in the metal compared to electrons in the semiconductor. It is analogous to the built-in junction potential for the pn junction diode. Externally applied reverse bias adds to ϕ_0 and increases the width of the depletion region, which extends entirely into the semiconductor. Depletion layer width, capacitance, etc., are identical to those for an abrupt p^+n junction diode.

Forward bias subtracts from ϕ_0, allowing electrons to flow from the n-type semiconductor into the metal. Although holes do not take part in forward conduction, the roles of electrons, ϕ_0 and V, are identical to the case of the pn junction diode. Hence it is not surprising that detailed analysis, omitted here, yields

$$I = I_0(e^{V/V_T} - 1) \tag{B.3}$$

A typical approximate value for the saturation current of a 20 μm^2 titanium silicide-n^- silicon barrier as often used in BJT integrated circuits is 10^{-10} A. A corresponding typical value for pn junction diodes of the same area is 2×10^{-17} A. The larger values of I_0 for Schottky diodes result in smaller forward voltage drops at any fixed current density. From the diode Equation (B.3) we have the useful rule of thumb that forward voltage drop for a fixed current at room temperature decreases by 60 mV for each factor of 10 increase of I_S or I_0. Thus for these typical values of saturation current, the difference in forward voltage between Schottky and pn junction diodes at the same forward current is about 0.4 V.

Not all metal-semiconductor contacts have diode characteristics. When the semiconductor is heavily doped (N_A or $N_D > 10^{18}$ cm^{-3}), the depletion layer becomes so narrow that carriers can travel in either direction through the potential barrier by a quantum-mechanical carrier transport mechanism known as *tunneling.* Under these conditions, current flows equally well in either direction, resulting in what is usually described as an *ohmic contact.* In fact, this is the physical explanation for most all ohmic contacts to semiconductor devices.

The diode model used in SPICE applies just as well for the Schottky-barrier diode, but with $I_0 = I_S$, and $\tau_T = 0$. SBDs and junction diodes have depletion layer capacitance represented by the same equations.

B.3 BJT Model for Circuit Simulation

As with the MOS transistor, accurate simulation of circuits using BJTs and SBDs requires that the devices be modeled in mathematical terms. The dc characteristics of the intrinsic BJT are modeled by nonlinear current sources I_C and I_E as shown in Equations B.4.1a, B.4.1.b, and B.4.2. (Terms for both forward and reverse operation are included for completeness.) The equations used in SPICE may be simplified to yield the classic Ebers-Moll equations

$$I_E = \frac{I_S}{\alpha_F}(e^{V_{BE}/V_T} - 1) - I_S(e^{V_{BC}/V_T} - 1) \tag{B.4.1a}$$

$$I_C = I_S(e^{V_{BE}/V_T} - 1) - \frac{I_S}{\alpha_r}(e^{V_{BC}/V_T} - 1) \tag{B.4.1b}$$

$$I_S = \alpha_F I_{ES} = \alpha_R I_{CS} \tag{B.4.2}$$

The ohmic resistances of the neutral base, collector, and emitter regions of the BJT are modeled by linear resistors r_b, r_c, and r_e.

Charge storage in the BJT is modeled by the two nonlinear charge storage elements Q_{BE} and Q_{BC}, which are determined by the equations

$$Q_{BE} = \tau_F I_S(e^{V_{BE}/V_T} - 1) + C_{je0}\int_0^{V_{BE}}\left(1 - \frac{V}{\phi_e}\right)^{-m_e} dV \tag{B.4.3a}$$

$$Q_{BC} = \tau_R I_S(e^{V_{BC}/V_T} - 1) + C_{jc0}\int_0^{V_{BC}}\left(1 - \frac{V}{\phi_c}\right)^{-m_c} dV \tag{B.4.3b}$$

Equivalently, these elements can be represented by voltage-dependent capacitors, since

$$C_{BE} = \frac{dQ_{BE}}{dV_{BE}} = \frac{\tau_F I_S}{V_T} e^{V_{BE}/V_T} + \frac{C_{je0}}{[1 - (V_{BE}/\phi_e)]^{m_e}} \tag{B.4.4a}$$

$$C_{BC} = \frac{dQ_{BC}}{dV_{BC}} = \frac{\tau_R I_S}{V_T} e^{V_{BC}/V_T} + \frac{C_{jc0}}{[1 - (V_{BC}/\phi_c)]^{m_c}} \tag{B.4.4b}$$

The charge storage elements Q_{BE} and Q_{BC} model the charge stored in the neutral base region Q_F and Q_R as well as the charge stored in the depletion regions Q_{je} and Q_{jc}.

Charge storage in the depletion regions is represented by V_{BE} and the model parameters C_{je0}, ϕ_e, and m_e for the emitter junction and V_{BC}, C_{jc0}, ϕ_c, and m_c for the collector junction.

Charge storage due to minority carrier injection across the junctions is described by the exponential terms in Equations B.4.3a and B.4.3b. The effect is modeled by the transit time parameters τ_F for the emitter junction and τ_R for the collector junction.

The model equations are complete for a discrete BJT. For an integrated circuit transistor we must add one more component. As illustrated in Figure B.1a, isolation of transistor collectors from each other and from the substrate is achieved using a reverse-biased diode. Assuming it remains reverse-biased, we find that this diode may be modeled by a current source (representing the diode leakage current) in parallel with a voltage-dependent depletion-layer capacitance.

For an integrated circuit *npn* transistor, this isolation diode is effectively connected between the collector and substrate. The substrate is common to all the components in the integrated circuit. This diode is modeled as a capacitance between the collector and substrate (C_{CS}) and is added to the basic model for the transistor in the forward active mode, as follows

$$C_{CS} = \frac{C_{js0}}{[1 - (V_{SC}/\phi_s)]^{m_s}} \tag{B.4.5}$$

B.4 Bipolar Transistor Inverter

Bipolar transistor technology has been succeeded by MOS technology for virtually all new designs of digital circuits and systems. However, discrete bipolar transistors, or combinations of a very few BJTs, still are used in digital systems. Examples include applications with external loads requiring drive current more than 0.1 A or load voltages more than 10 V. Bipolar devices driven by a MOS integrated circuit often are employed in such cases. Bipolar devices are readily available for switching up to 100 A or 1000 V. The elementary building block in such situations is a bipolar transistor logic inverter.

The discussion below also supports a subsequent description of historical TTL bipolar logic configuration, so the examples typically refer to 5 V operation with milliampere currents. Bear in mind that operation at higher voltages and currents is entirely feasible.

A simple but practical configuration of a bipolar transistor logic inverter is shown in Figure B.4. Listed are some typical data for the transistor in this circuit.

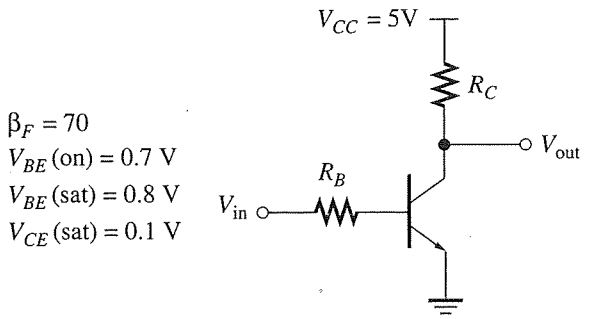


Figure B.4
Bipolar transistor inverter.

We assume that these data are independent of collector current, but with $I_C = 0.01\ I_{C\,(EOS)}$, and $V_{in} = V_{BE(on)}$, where (EOS) stands for edge of saturation. It can be seen from the circuit that, with the input voltage V_{in} less than the turn-on voltage $V_{BE(on)}$ for the transistor, the collector current will essentially be zero and the output voltage V_{out} will be equal to V_{CC}; that is, the transistor will be cut off.

When the input voltage is increased above $V_{BE(on)}$, the transistor turns on and enters the forward active region, where the collector current is related to the base current as $I_C = \beta_F I_B$. Now $V_{out} = V_{CC} - I_C R_C$. Therefore as the input voltage increases, the output voltage decreases; the direction of the voltage change is inverted. With sufficient input voltage, when the output voltage (which is in fact V_{CE} of the transistor) has fallen sufficiently, the transistor enters the saturation region. In the saturation region the output voltage shows little, if any, change as the input voltage is further increased.

Confusion arises from the different uses of the word *saturation* in MOS and bipolar circuit contexts. In the bipolar case, a transistor is said to be operating in saturation when the collector-emitter voltage is near zero, almost independent of output current. (In the MOS case, the transistor is in saturation when the output current is constant, nearly independent of the output voltage.)

B.5 Voltage Transfer Characteristics

The *voltage transfer characteristic* for the transistor inverter is shown in Figure B.5, where straight-line asymptotes are used to join the two main breakpoints of the characteristic. At BP1, the input voltage is just at the point of turning the transistor on, but the output voltage is still very close to the cutoff value; that is, the collector current is very small. At BP2, the input voltage is now great enough to bring the

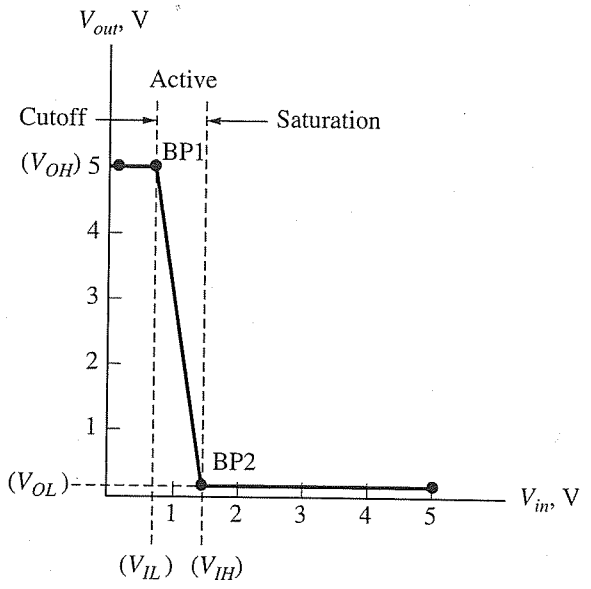


Figure B.5
Voltage transfer characteristic.

transistor to the edge of the saturation region. The collector current is now at, or very nearly at, its maximum value, since any further increase in the input voltage results in hardly any change in the output voltage. Observe that the two breakpoints separate the following three regions of operation for the transistor:

1. Cutoff
2. Active
3. Saturation

The coordinates of BP1 are V_{IL} and V_{OH}, and for BP2 they are V_{IH} and V_{OL}, where these quantities have the same definitions as in Chapter 4, Section 4.2. Determining values for these quantities in a bipolar inverter is easy, as follows. From the circuit of Figure B.4:

1. V_{OH}, which is equivalent to V_{CE} with the transistor at the edge of the cutoff region, that is, V_{CC}. For the given example it is 5 V. Hence,

$$V_{OH} = V_{CC}$$

   However, V_{OH} is usually measured with $V_{\text{in}} = V_{OL}$

2. V_{OL}, which is equivalent to V_{CE} with the transistor at the edge of the saturation region, that is, $V_{CE\,(\text{sat})}$. In the example it is 0.1 V. Thus,

$$V_{OL} = V_{CE(\text{sat})}$$

   V_{OL} is commonly measured with $V_{\text{in}} = V_{OH}$

3. V_{IL}, which is the input voltage just sufficient to turn the transistor on. In this example it is $V_{BE(\text{on})}$, which is given as 0.7 V. Therefore,

$$V_{IL} = V_{BE(\text{on})}$$

4. V_{IH}, which is the input voltage just sufficient to saturate the transistor. Now with the transistor just at the edge of saturation, $I_C = I_{C\,(\text{EOS})}$, where

$$I_{C(\text{EOS})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \tag{B.5.1}$$

But since the transistor is also at the edge of the forward active region,

$$I_{C(\text{EOS})} = \beta_F I_{B(\text{EOS})} \tag{B.5.2}$$

where, with the input at V_{IH},

$$I_{B(\text{EOS})} = V_{IH} - \frac{V_{BE(\text{sat})}}{R_B} \tag{B.5.3}$$

Therefore, solving for V_{IH} using Equations (B.5.2) and (B.5.1),

$$\text{V}_{IH} = \text{V}_{BE(\text{sat})} + \frac{R_B}{R_C}\frac{V_{CC} - VC_{CE(\text{sat})}}{\beta_F} \tag{B.5.4}$$

Using the numeric values,

$$V_{IH} = 0.8 + 10\,\text{k}\Omega/1\,\text{k}\Omega\,5 - 0.1/70 = 1.5\,\text{V}$$

Hence the coordinates of BP1 are $V_{\text{in}} = 0.7$ V and $V_{\text{out}} = 5.0$ V; for BP2 they are $V_{\text{in}} = 1.5$ V and $V_{\text{out}} = 0.1$ V.

Note that the slope of the characteristic in Figure B.5 relates to the voltage gain of the transistor inverter, since the voltage gain is given as

$$a_v = \Delta V_{\text{out}}/\Delta V_{\text{in}} \tag{B.5.5}$$

In the cutoff and saturation regions the slope is zero as is, of course, the voltage gain. But in the active region the slope directly indicates the voltage gain. Now straight-line asymptotes have been used in the voltage transfer characteristic to uniquely identify the breakpoints. More accurately, these breakpoints define the points on the characteristic curve where the small-signal voltage gain is 1.0; they are then identified as the *unity-gain points*. In particular, we note from Figure B.5 that to the left of BP1 and to the right of BP2 the voltage gain is <1.0, but to the right of BP1 and to the left of BP2, that is, in the active region, the voltage gain is >1.0.

B.6 Schottky-Clamped Inverter

As mentioned earlier, to minimize switching delays bipolar integrated circuits must be designed to prevent the collector-base junction from ever becoming appreciably forward biased. A Schottky-barrier diode (SBD) connected between the base and the collector of the inverter transistor, as in Figure B.6, is an effective solution. By extending the base metal to contact the more lightly doped collector region, this extra diode is included by a simple addition to the fabrication procedure.

The Schottky clamp effectively prevents the transistor from saturating; hence there is no saturation delay time for the inverter circuit. When the transistor approaches saturation, because of a high voltage level at the input, any base current in excess of $\beta_F I_B$ is diverted from the base through the Schottky diode and then into the collector of the transistor. The forward voltage drop of the Schottky diode is less than the voltage drop of the base-collector junction diode of the transistor. At room temperature the forward voltage drop of a titanium silicide to n-type silicon Schottky diode is about 0.3 V. Thus for a clamped inverter circuit, and a transistor with $V_{BE(\text{on})} = 0.7$ V, with the SBD conducting the voltage between collector and emitter, $V_{CE} = 0.7 - 0.3 = 0.4$ V. This is to be compared with $V_{CE(\text{sat})} = 0.1$ V for the transistor without a Schottky diode. In the saturation mode, both junctions of the transistor are forward-biased. Hence, with $V_{BE(\text{sat})} = 0.8$ V and $V_{CE(\text{sat})} = 0.1$ V, $V_{BC(\text{sat})} = 0.7$ V.

The Schottky diode effectively limits the minimum base-collector voltage to 0.4 V; therefore, although the base-collector junction is forward-biased (by 0.4 V), it is conducting little current. The Schottky diode is forward-biased, but as noted above there is no minority carrier charge storage in a SBD. Despite the fact that the

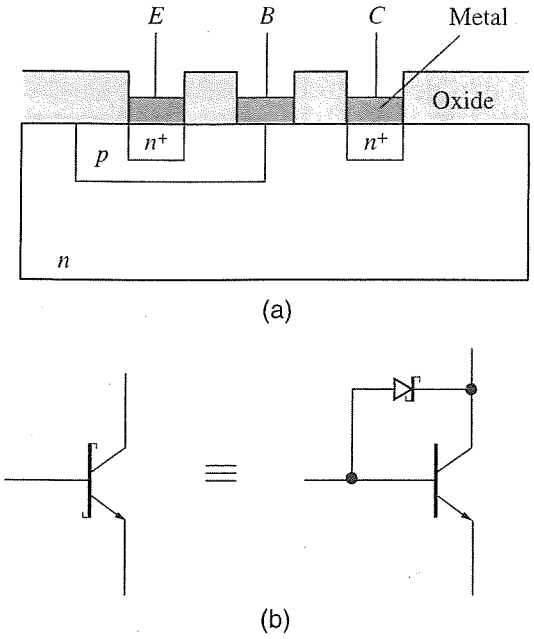


Figure B.6
(a) Cross section of Schottky-clamped transistor. (b) Circuit symbol for Schottky-clamped transistor.

collector-base junction itself is not conducting significantly, this operating point still may be referred to as "saturation".

While the inclusion of the Schottky diode has improved the transient characteristics of the bipolar transistor inverter, unfortunately it has an opposite effect on the static characteristics. In particular, the low noise margin NM_L has been made worse because V_{OL} is increased from 0.1 to 0.4 V. Hence, NM_L has been decreased by the same amount. The Schottky diode has a minimal effect on the high noise margin NM_H.

B.7 BJT Inverter Switching Times

The transient behavior of a bipolar transistor inverter is limited by charge storage in depletion layer capacitances of the base-emitter, base-collector, and collector-substrate junctions. When a Schottky-barrier clamp is included, its depletion layer capacitance adds in parallel with the collector-base *pn* junction capacitance. All these depletion layer capacitances are modeled in the same way as the *pn* junction depletion layer capacitances of the MOS transistor, as described previously in Chapter 2.

In addition, there is charge stored in the base of the BJT, denoted as $Q_F = \tau_F I_C$, as explained earlier in this Appendix. This charge must be delivered to turn on the transistor and removed to turn it off. The base-emitter and base-collector depletion layer charges and Q_F all must be delivered to and removed from the base terminal. The base-emitter voltage change during switching usually is only a few tenths of a

volt. Therefore, it is straightforward to make simple hand estimates of switching time by adding up the necessary changes in charge, and dividing the sum by the current the external circuit can deliver to the base node.

SPICE or another circuit simulator is an essential tool for accurately computing the transient performance of more complex circuits such as transistor-transistor logic (TTL) and emitter-coupled logic (ECL).

B.8 Bipolar Digital Gate Circuits

Bipolar digital gate circuits no longer are used in new designs. As a matter of technical and historical interest, here we briefly describe the first member of the *transistor-transistor logic (TTL)* series that was widely used in minicomputers and other digital systems from 1970 to 1985. TTL displaced earlier bipolar logic families such as *resistor-transistor logic (RTL)* and *diode-transistor logic (DTL)* because it provided better load driving capability and shorter propagation delays for the same power consumption. Another family, *emitter-coupled logic (ECL)*, was used in a few systems where its shorter propagation delays offset its higher cost.

The schematic diagram and IC layout for an early commercial *transistor-transistor logic (TTL)* circuit are shown in Figure B.7. This was known as the Series 74, exemplified here as a 2-input NAND gate, where $F = \overline{AB}$. Schottky clamps had not yet been developed. The input terminals of the TTL gate are connected to separate emitters of transistor Q_1, performing the AND function immediately in a relatively small area. Q_1 violates the rule that base-collector junctions never should be forward-biased, but detailed analysis shows that in this particular case the reverse stored charge in Q_1 speeds turn-off of Q_2. Transistor Q_2 provides voltage of opposite phase to the bases of output transistors Q_3 and Q_4 so that only one of these is turned *on* in each of the two logic states. Diode D_1 provides additional voltage drop to minimize the current spike from supply to ground during switching between states. Resistor R_2 is the path for current to turn off Q_3.

The active pull-down (Q_3) and pull-up circuits (Q_4), familiarly known as a *totem-pole* output circuit, provide more current to discharge and charge parasitic capacitance associated with the load, thus decreasing the transition times at the turn-on and turn-off of these digital gates. The layout of Figure B.7(b) shows a dual 4-input TTL NAND gate.

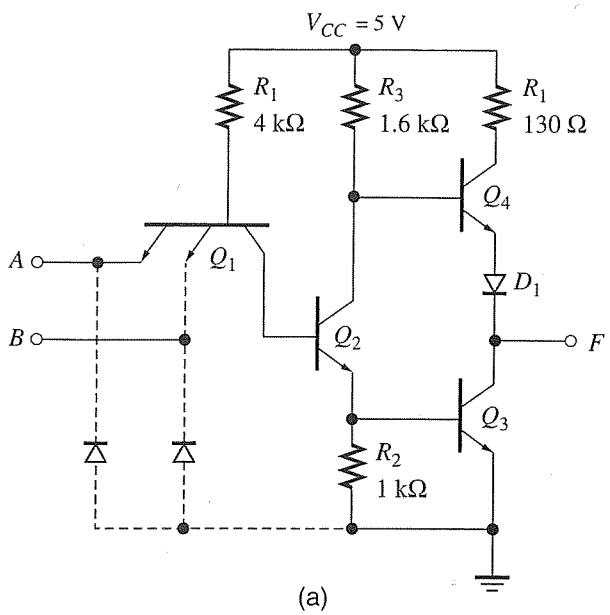
B.9 Voltage Transfer Characteristics

The voltage transfer characteristic of the standard TTL NAND gate is displayed in Figure B.8. In describing the characteristic we assume the usual typical values, that is

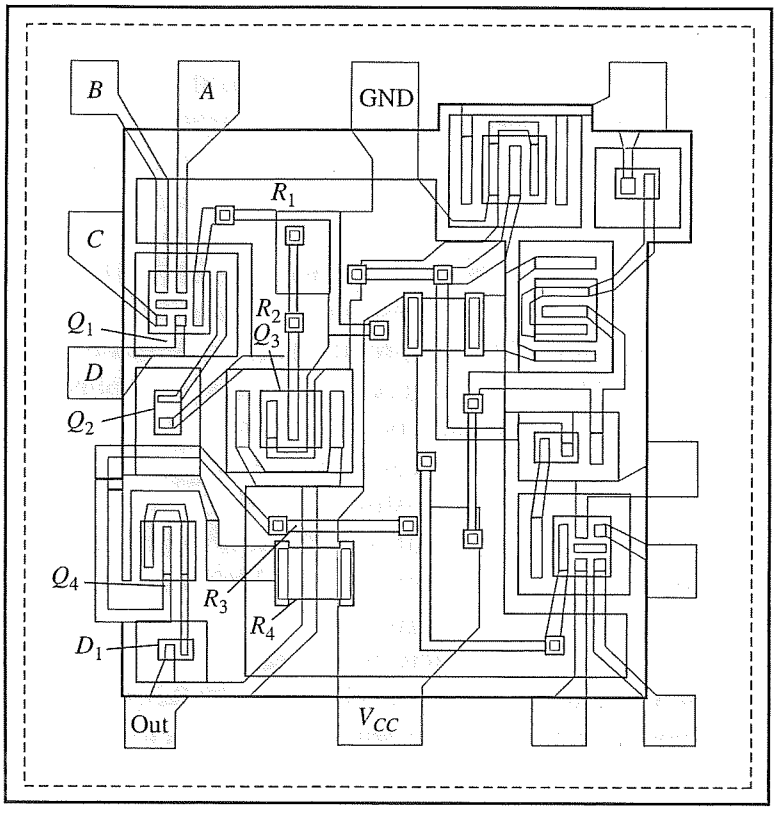
$$V_{BE(on)} = 0.7\ V$$

$$V_{BE(\text{sat})} = 0.8\text{V}$$

$$V_{CE(\text{sat})} = 0.1\text{V}$$



(a)



(b)

Figure B.7
(a) Standard 2-input TTL NAND gate circuit. (b) Layout of a dual 4-input TTL NAND gate.

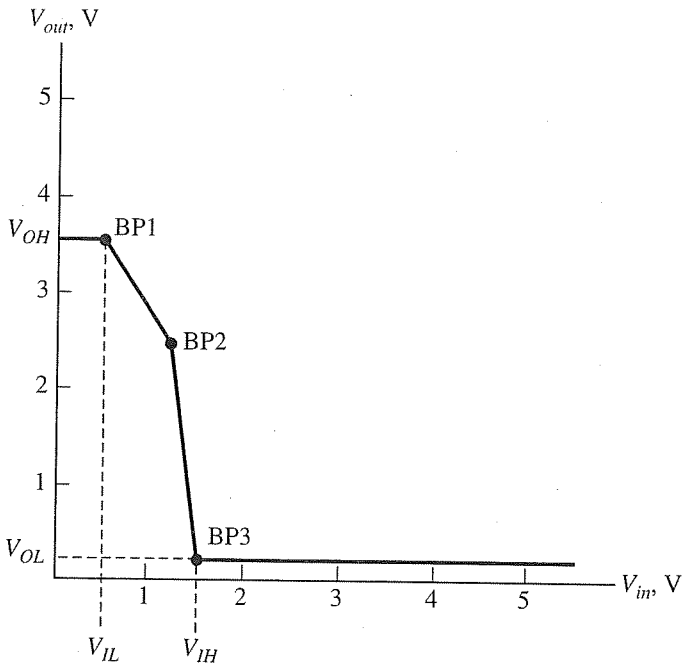


Figure B.8
Voltage transfer characteristic of the standard TTL circuit.

First note, with either input (A or B) low (that is, $V_{in} = 0.1$ V), transistor Q_1 is operating in the saturated mode. This is because with the base-emitter junction forward-biased, the base current of Q_1 will be approximately 1 mA. But the collector current of Q_1 is limited to the reverse, or leakage, current across the collector-base junction of transistor Q_2, and this will typically be approximately 1 nA. With $I_{C1} \ll \beta_F I_{B1}$, transistor Q_1 must be saturated. As a consequence, $V_{CE1} = V_{CE(sat)} = 0.1$ V, and so $V_{C1} = 0.2$ V. But $V_{C1} = V_{B2}$; both transistors Q_2 and Q_3 must therefore be cut off. Hence, with either input low, the output is high. Now to provide even leakage current to the output node, transistor Q_4 must be on. Therefore, with $V_{BE4(on)} = V_{D1(on)} = 0.7$ V, we have that $V_{OH} = V_{CC} - 2V_{BE(on)} = 3.6$ V.

The first breakpoint in the characteristic occurs when transistor Q_2 turns on. That is, with $V_{C1} = V_{B2} = 0.7$ V and $V_{E2} = 0$ V, $V_{BE2} = 0.7$ V but $V_{BE3} = 0$ V. Base current to Q_2 is provided by the forward-biased base-collector junction of Q_1. Recall that in saturation, both junctions of the transistor are forward-biased. Hence with $V_{C1} = 0.7$ V and $V_{CE1(sat)} = 0.1$ V, $V_{E1} = V_{in} = 0.6$ V. Thus at the first breakpoint, $V_{IL} = 0.6$ V and $V_{OH} = 3.6$ V.

The second breakpoint occurs when transistor Q_3 turns on. But $V_{BE3} = V_{R2}$, and therefore $I_{E2} = V_{R2}/R_2$. Consequently, for $V_{BE3} = V_{BE(on)} = 0.7$ V, $I_{C2} = I_{E2} = 0.7$ V/1 kΩ = 0.7 mA. The voltage at the collector of Q_2 is $V_{C2} = V_{CC} - I_{C2}R_3 = 5 - (0.7)(1.6) = 3.9$ V. Note that with $V_{CE2} = V_{C2} - V_{E2} = 3.9 - 0.7 = 3.2$ V, Q_2 is operating in the forward-active mode. The gate output voltage is $2V_{BE(on)}$ below V_{C2}; therefore $V_{out} = 2.5$ V. To determine the input voltage, transistor Q_1 is still in the saturation mode,

and $V_{C1} = V_{BE2} + V_{BE3}$; that is, $2V_{BE(on)} = 1.4$ V. Hence, $V_{in} = 1.3$ V. The coordinates of the second breakpoint are $V_{in} = 1.3$ V and $V_{out} = 2.5$ V.

The third, and final, breakpoint occurs when Q_3 saturates. The gate output voltage is then $V_{CE(sat)} = 0.1$ V. With transistor Q_2 also saturated, $V_{C1} = 2V_{BE(sat)} = 1.6$ V. Transistor Q_1 is still saturated, so that $V_{in} = 1.6 - 0.1 = 1.5$ V. The coordinates are $V_{in} = 1.5$ V and $V_{out} = 0.1$ V.

B.10 Propagation Delay Time

The use of a transistor at the input of the TTL circuit improves the propagation delay time, in particular t_{PLH}. Refer to Figure B.7a. For the output to go high, it is necessary to turn off base current to transistor Q_3. Therefore, we must quickly turn off transistor Q_2. Prior to the transition the input is at a high level and both transistors Q_2 and Q_3 are saturated, and $V_{C1} = 1.6$ V. With a high-to-low transition at the input, $V_{E1} = 0.1$ V. Therefore initially, $V_{CE1} = 1.5$ V and transistor Q_1 operates in the forward active mode. That is, until Q_1 saturates, the collector current is $I_{C1} = \beta_F I_{B1}$. This current, which can be appreciable, is the turn-off base current for transistor Q_2. Note that it is not until after Q_2 turns off that Q_1 saturates. Hence, because of the forward current gain β_F of transistor Q_1, transistor Q_2 quickly turns off. With Q_2 off, transistor Q_4 becomes a source of current to the output, causing the gate output to go high, provided that Q_3 is off. The turn-off base current for Q_3 is through R_2. The turn-off time for Q_3 is usually longer than that of Q_2. But transistor Q_1 does serve to decrease the propagation delay time t_{PLH}.

Later versions of TTL incorporated Schottky clamps to reduce propagation delays and additional devices to "square up" the voltage transfer characteristic by eliminating BP2 and moving BP1 to the right. They were known as Series 74S, 74LS, 74ALS, etc. For details on these circuits and on ECL, see the earlier edition of this text.

B.11 Input Clamp Diodes

Finally, in the description of the TTL circuit of Figure B.7, the clamp diode from each input to ground should be noted. For the static conditions of a high or low level at the input, they are reverse-biased and play no part in the circuit. However, as the output changes state, the switching transition times of these circuits are very short. Any inductance associated with the load or power supply lines causes high-frequency oscillations ("ringing") to appear on the output lines. Hence the input to a gate can be greater than 5 V on the positive swing and less than 0 V on the negative swing. The positive swing reverse-biases the emitter-base junction of the input transistor, but the base resistor R_1 limits the current and no harm is done. On the negative swing, with transistor Q_1 saturated, the voltage at the collector will only be 0.1 V more positive than the emitter voltage. The result is that the collector-substrate isolation diode of Q_1 can be forward-biased. This can lead to undesired voltage spikes at other nodes in the circuit or possible fatal damage to the IC. The diodes at the input "clamp" the input voltage so that it cannot swing more negative

Table B.1
Standard transistor-transistor logic (54/74 TTL): typical electrical characteristics at $T_A = 25°C$

V_{OH}/V_{OL}	3.5 V/0.2 V	Fan-out	10
V_{IH}/V_{IL}	1.5 V/0.5 V	Supply volts	+ 5.0 V
NM_H/V_L	2.0 V/0.3 V	Power dissipation per gate	10 mW
Logic swing	3.3 V	Propagation delay time	10 ns

than about -0.7 V. Later versions of TTL use Schottky diodes in the input clamp position.

The electrical characteristics for this standard TTL gate circuit are shown in Table B.1. Note that the power-delay product, 100 pJ, of the original TTL circuit is much larger than that today's CMOS logic circuits. The most advanced TTL family, 74ALS, has typical propagation delay of 4 ns and typical power consumption of 1 mW, still far greater than for today's CMOS.

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