ememory

EG001K32GK05DLB03

SMIC 55nm 1.2V/2.5V LL Process

1K x 32 bits One Time Programmable Device

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Preliminary version may change spec after proven on silicon.

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1K x 32-bits One Time Programmable

eMemory's 55nm OTP device (NeoFuse®) is adopted in SMIC 55nm single poly baseline ULP process. NeoFuse® is an antifuse based technology, which is capable for security code storage. This IP programming voltage is generated from an internal charge pump.

Features

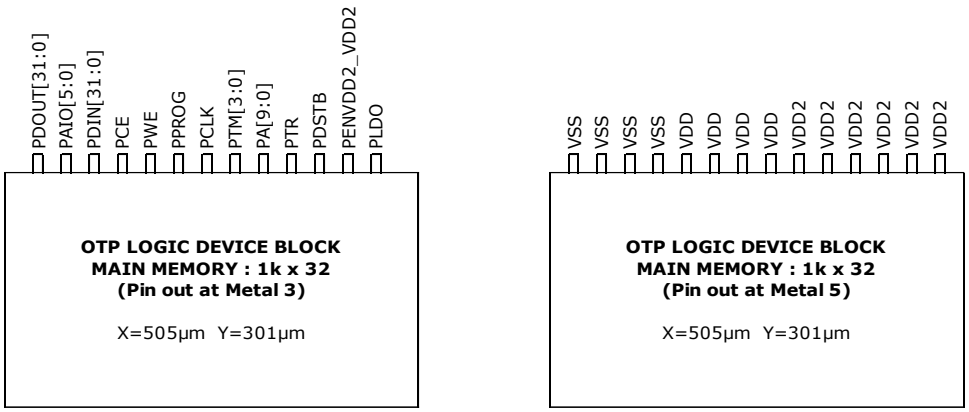
- SMIC 1.2V/2.5V LL Process
  - 1P5M IP Design(M1, M2~M5 follow inter metal rule).
  - Capable of using on 1P5M/1P6M/ 1P7M/1P8M/1P9M/1P10M process
  - Use1.2V SVT N/PMOS, 1.2V HVT NMOS and 2.5V N/P MOS
- VDD and VDD2 Power Supply
  - 0.81V~1.32V VDD, 2.25V~3.63V VDD2 for Read
  - 0.81V~1.32V VDD, 2.25V~3.63V VDD2 for Program
- Memory Organization 1K x 32-bits
- 1-Bits Program Operation
- Built-in 1bit Charge Pump
- Built-in ECC scheme
- Junction Temperature T_J **:**
  - Read Mode:-40°C ~ 125°C
  - Program Mode: -40°C ~ 125°C
- Data Retention**:** >10 Years
- Special Boolean operation is required, please refer to Special Note of Release Note document.
- **NeoFuse Cell :**1.2V device
- **IP Size :**0.152 mm^2 (505 um x 301um)
  On silicon size: 0.123 mm^2
- **Access Time :**
  - 50ns(max) at 0.9V~1.32V VDD
  - 60ns(max) at 0.81V~0.9V VDD
- **Bit Program Time :**
  - 10μ s (min)
- Operating Current @ 20MHz:
  - I_{VDD_R} :0.7mA/2.1mA (typ./max.)
  - I_{VDD2_R} :1.5mA/2.2mA (typ./max.)
- Deep Standby Current:
  - I_{VDD_DSB} : 0.02uA/6.5uA (typ./max.)
  - I_{VDD2_DSB}: 0.01uA/1uA (typ./max.)

General Description

EG001K32GK05DLB03 is a CMOS 1K x 32-bits One Time Programmable device. The main memory is organized as 1,024 by 32 bits. The OTP cell design will provide a low cost logic process OTP approach compared with alternative approaches. The EG001K32GK05DLB03 is programmed by 1.2V, 3.3V power supply.

PGM is the abbreviation for program and $\mathbf{T_J}$ stands for junction temperature.

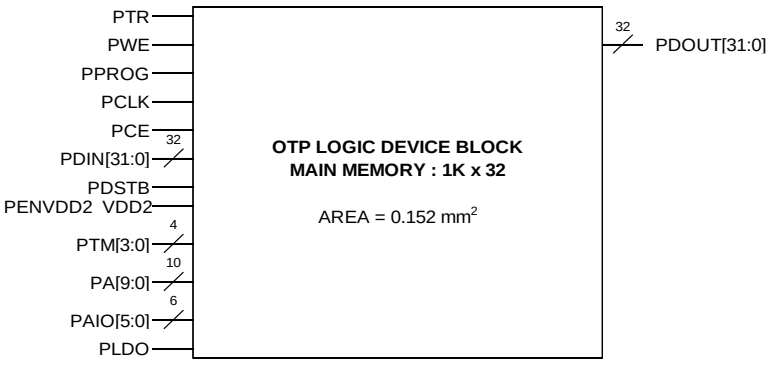
Pin Assignments



Power Connection Requirement

- Power/Ground bouncing beyond DC specifications is not allowed.
- It is necessary to connect at least two power sets of VDD/VDD2/VSS, and metal width should be at least same as VDD/VDD2/VSS pin width.

Symbol



Pin Description

Pin Name	Direction	Description
PA[9:0]	I	Address input for Read operation
PAIO[5:0]	I	Address input for programming operation
PDIN[31:0]	I	Data input
PDOUT[31:0]	O	Data output
PTM[3:0]	I	Pins for Test mode enabling
PWE	I	Pin to Define program cycle
PPROG	I	Pin to Program mode enabling
PCLK	I	Pin for Clock input
PCE	I	Pin for IP enabling
PTR	I	Test row enable
PDSTB	I	Pin for Deep standby mode enabling (low active)
PLDO	I	Enable LDO to generate for 2.5V power
VDD	I	1.1V Power supply
VDD2	I	3.3V Power supply
VSS	I	Ground
PENVDD2_VDD2	I	VDD2 Enable Pin (VDD2 domaim)

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Notes

1. No glitch immunity on these signals. Users should provide the non-glitch signals to all pins.

Operation Mode Truth Table

Truth Table

Mode	Type	PTM[3:0]	PCLK	PCE	PWE	PPROG	PTR	PDSTB	PLDO	PENVDD2_VDD2
User Mode	Stand-by	LLLL	H or L	L	L	L	L	H	H	H
	Deep Stand-by	LLLL	H or L	L	L	L	L	L	L	H
	Read Access	LLLL	↗	H	L	L	H or L	H	H	H
	Program Entry	LLHL	×	H	L	L	H or L	H	H	H
	Program Access	LLHL	×	H	H	H	H or L	H	H	H
Test Mode	Room Temp. initial Margin Read Mode	LLLH	↗	H	L	L	H or L	H	H	H
	Room Temp. PGM Margin Read Mode	LHLL	↗	H	L	L	H or L	H	H	H
	High Temp. initial Margin Read Mode	HLLH	↗	H	L	L	H or L	H	H	H
	High Temp. PGM Margin Read Mode	HHLL	↗	H	L	L	H or L	H	H	H

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Notes

1. H stands for logic High level. L stands for logic Low level.
2. PCE pin is not latched by PCLK during read access. The timing dependency is only enable/disable time basically, not setup/hold time.
3. Initial Margin Read Mode provides initial state check to filter out defect bit in the testing flow.
4. PGM Margin Read Mode is a test mode for CP sorting and provides a critical read condition to filter out “weak programmed” bits in the testing flow. To ensure programming success, customer should implement this mode.
5. High temperature (>85C) Initial Margin Read Mode provides initial state check to filter out defect bit in high temperature (>85C) in the testing flow.
6. High temperature (>85C) PGM Margin Read Mode is a test mode for CP sorting and provides a critical read condition to filter out “weak programmed” bits in high temperature in the testing flow. To ensure programming success, customer should implement this mode.

Write/Read Truth Table

Cell State	PDIN Write	PDOUT Read
Programmed	L	L
Un-programmed(Initial)	H	H

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Program Selection Table

PA	Bit Selection For Write Data Input	Data Readout
Select 1K32	PAIO[5:0]=000000	PDOUT[0]
	PAIO[5:0]=000001	PDOUT[1]
	PAIO[5:0]=000010	PDOUT[2]
	.....	.....
	PAIO[5:0]=011111	PDOUT[31]

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Address/PDOUT Description Table

Mode	Type	PA[9:0]	PAS	PAIO[5:0]	PDOUT
User Mode	Stand-by	-	-	-	-
	Read Access	Address-in	-	-	PDOUT[31:0]
	Program Access	Address-in	Address-in	Address-in	-
Test Mode	PGM Margin Read Mode	Address-in	-	-	PDOUT[31:0]
	Initial Margin Read Mode	Address-in	-	-	PDOUT[31:0]

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DC Specifications

Recommended DC Operating Conditions

Operating Mode	Power Pin	Min	Typ	Max	Unit
Read Mode	V_{DD}	0.81	1.2	1.32	V
	V_{DD2}	2.25	3.3	3.63	V
	V_{SS}		0		V
PGM Mode	V_{DD}	0.81	1.2	1.32	V
	V_{DD2}	2.25	3.3	3.63	V
	V_{SS}		0		V

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Notes

1. **Power supply voltage beyond DC operating range is not guaranteed.**
2. **Power/Ground bouncing beyond DC operating range might cause invalid data output. It's not guaranteed by eMemory and customers must take care of power stability on their own.**
3. **Normally, operating junction temperature is from -40°C to 125°C, and Program operation should be at junction temperature -40°C ~ 125°C.**

DC Electrical Characteristics

Parameter	Power Pin	Typ	Max	Unit	Test Condition
Read Current @20MHz	IVDD_R	700	2100	µA	VDD=VDDMAX, VDD2=VDD2MAX, PTM[3:0]=0, PA[9:0]=0/VDD, PCE=VDD, PDIN[31:0]=0/VDD, PPROG=PWE=0, PDSTB=PLDO=VDD PENVDD2_VDD2=VDD2
	IVDD2_R	1500	2200	µA	
Read Current II @1MHz	IVDD_R	200	1200	µA	VDD=VDDMAX, VDD2=VDD2MAX, PTM[3:0]=0, PA[9:0]=0/VDD, PCE=VDD, PDIN[31:0]=0/VDD, PPROG=PWE=0, PDSTB=PLDO=VDD PENVDD2_VDD2=VDD2
	IVDD2_R	1200	2000	µA	
Normal Program Current	IVDD_P	110	1000	µA	VDD=VDDMAX, VDD2=VDD2MAX, PDSTB=VDD, PTM[3:0]=2, PDIN[31:0]=0 ,PPROG=PCE=PWE= PLDO=VDD PENVDD2_VDD2=VDD2
	IVDD2_P	4	5	mA	
Standby Current	IVDD_SB	1	600	µA	VDD=VDDMAX, VDD2=VDD2MAX, PTM[3:0]=0, PA[9:0]=0/VDD, PCLK=PDIN[31:0]=0/VDD, PDSTB=PLDO=VDD, PPROG=PCE=PWE=0, PENVDD2_VDD2=VDD2
	IVDD2_SB	800	1100	µA	
Deep Standby Current	IVDD_DSB	0.02	6.5	µA	VDD=VDDMAX, VDD2=VDD2MAX, PTM[3:0]=0, PA[9:0]=0/VDD, PCLK=PDIN[31:0]=0/VDD, PDSTB=PLDO= PPROG=PCE=PWE=0 PENVDD2_VDD2=VDD2
	IVDD2_DSB	0.01	1	µA	

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Notes

1. **All electrical parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.**
2. **Capacitive loading should less than 0.1pF same as simulation conditions.**
3. **No active current at standby mode, thus I_{SB} is dependent on device leakage current.**
4. **Typical DC SPEC is defined at typical operation voltage and room temperature.**
5. **Normally, operating junction temperature is from -40°C to 125°C, and Program operation should be at junction temperature -40°C ~ 125°C.**

Timing

Timing Parameters (C_{LOAD}=0.1pF)

Parameter	Symbol	Min	Max	Unit
Rising Time	T_r	-	1	ns
Falling Time	T_f	-	1	ns
Read Data Access Time @VDD=0.9V~1.32V	T_{cd}	-	50	ns
Clock Cycle Time @VDD=0.9V~1.32V	T_{cyc}	50	-	ns
Clock Pulse High Time	T_{kh}	20	-	ns
Clock Pulse Low Time	T_{kl}	20	-	ns
Address Setup Time	T_{as}	1	-	ns
Address Hold Time	T_{ah}	15	-	ns
IP Enable Time	T_{cs}	10	-	µs
PCE Disable Time	T_{ch}	0	-	ns
Output Data Hold Time	T_{oh}	0.1	-	ns
Program Pulse Width Time	T_{pw}	10	20	µs
Program Pulse Interval Time	T_{pwi}	1	5	µs
Control Signal Enable Time	T_{vds_VDD}	1	-	µs
Program Address Setup Time	T_{asp}	1	-	ns
Program Address Hold Time	T_{ahp}	2	-	ns
Program Data Setup Time	T_{dsp}	1	-	ns
Program Data Hold Time	T_{dhp}	2	-	ns
Read Data Access Time-2 @VDD=0.81V~0.9V	T_{cd}	-	60	ns
Clock Cycle Time-2 @VDD=0.81V~0.9V	T_{cyc}	60	-	ns
Program Mode Recovery Time	T_{ppr}	5	100	µs
Program Mode Setup Time	T_{pps}	5	20	µs
Program Mode Hold Time	T_{pph}	5	20	µs
Active Mode to Deep Standby Hold Time	T_{ash}	10	-	ns
Deep Standby to Active Mode Setup Time	T_{sas}	2	-	µs
PTM Mode Setup Time	T_{ms}	1	-	ns
PTM Mode Hold Time	T_{mh}	1	-	ns
IP Enable Time in Program	T_{csp}	10	100	µs
LDO Setup Time	T_{pls}	10	-	µs

Parameter	Symbol	Min	Max	Unit
LDO Hold Time	T_{plh}	0	-	ns
VDD2 Power Up Setup Time	T_{vd2us}	1	-	µs
VDD Power Up Setup Time	T_{vdus}	1	-	µs
VDD2 Power Enable Setup Time	T_{vd2ens}	0	-	ns
VDD Power Enable Setup Time	T_{vdens}	0	-	ns
Power Enable Setup Time	T_{pens}	1	-	µs
Power Enable Hold Time	T_{penh}	0	-	ns
VDD2 Power Down Hold Time	T_{vd2dh}	0	-	ns
VDD Power Down Hold Time	T_{vddh}	0	-	ns

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Notes

1. **All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.**
2. **Capacitive loading should less than 0.1pF same as simulation conditions.**
3. **T_{pw} have maximum value limitation, which is reliability concern to avoid long HV stress time.**
4. **Tsas and Tash values are the simulation results based on VDD2 current = 100mA (max)**
5. **Normally, operating junction temperature is from -40°C to 125°C, and Program operation should be**
6. **At junction temperature -40°C ~125°C.**

Input Capacitance

Parameter	Symbol	Min	Max	Unit	Test Condition
Control Input	C_{CON}	-	0.02	pF	VIN=0 at f=1 MHz
Address Input	C_{ADD}	-	0.02	pF	VIN=0 at f=1 MHz
Data Input	C_{DIN}	-	0.02	pF	VIN=0 at f=1 MHz

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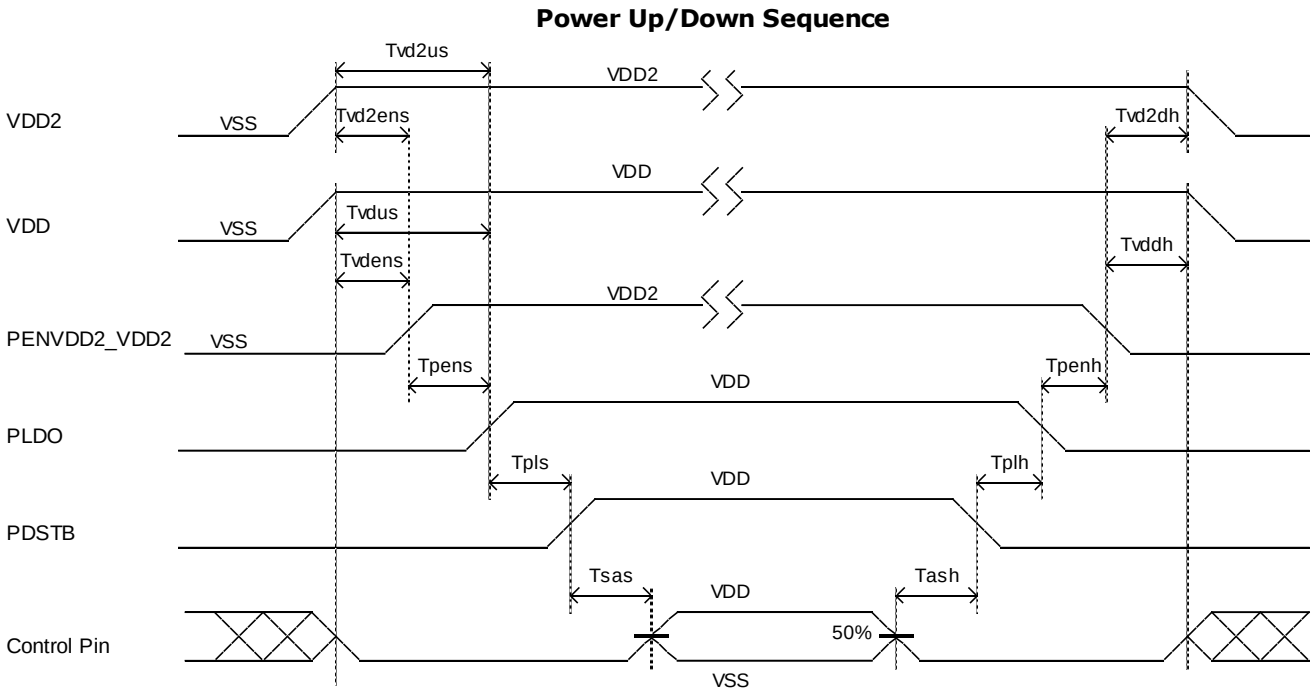
Timing Waveforms

Timing Definition

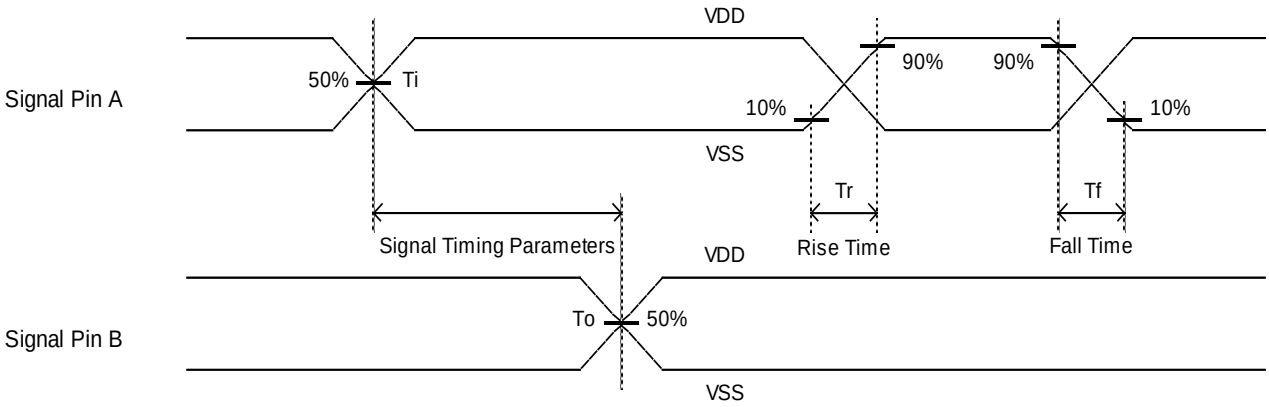


- VDD/VDD2/VSS level is specified in each timing waveform.
- Power up sequence timing is based on power measuring point while VDD/VDD2 is stable as waveform indicated.
- Signal to signal timing is measured from T_i to T_o of input/output signal at 50% VDD/VDD2 level based on VSS=0V.
- Signal rise time T_r (fall time T_f) is defined from 10% => 90% (10% <= 90%) of VDD/VDD2 level based on VSS=0V.

Timing Waveforms

Timing Definition

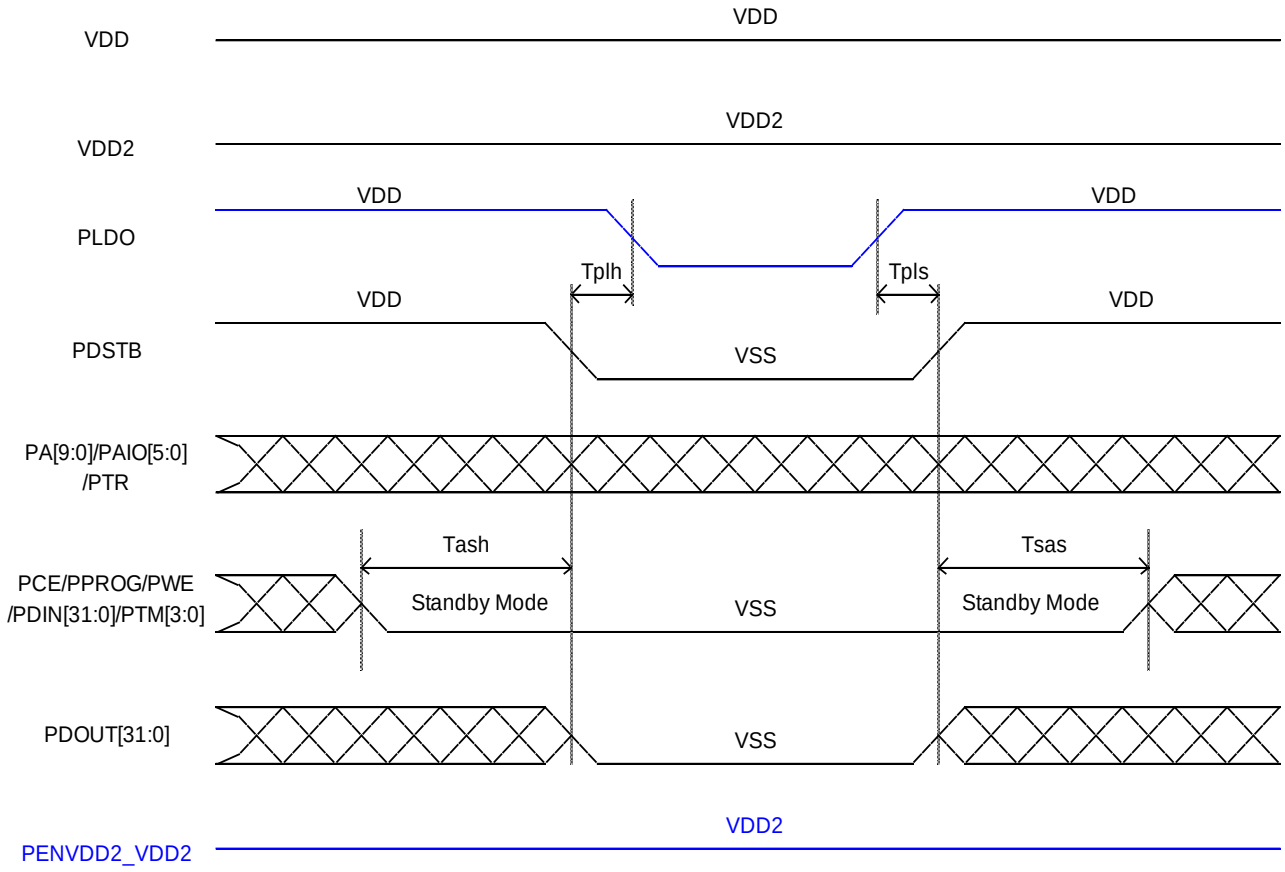
Signal Pin Timing Definition



- VDD/VDD2/VSS level is specified in each timing waveform.
- Power up sequence timing is based on power measuring point while VDD/VDD2 is stable as waveform indicated.
- Signal to signal timing is measured from T_i to T_o of input/output signal at 50% VDD/VDD2 level based on VSS=0V.
- Signal rise time T_r (fall time T_f) is defined from 10% => 90% (10% <= 90%) of VDD/VDD2 level based on VSS=0V.

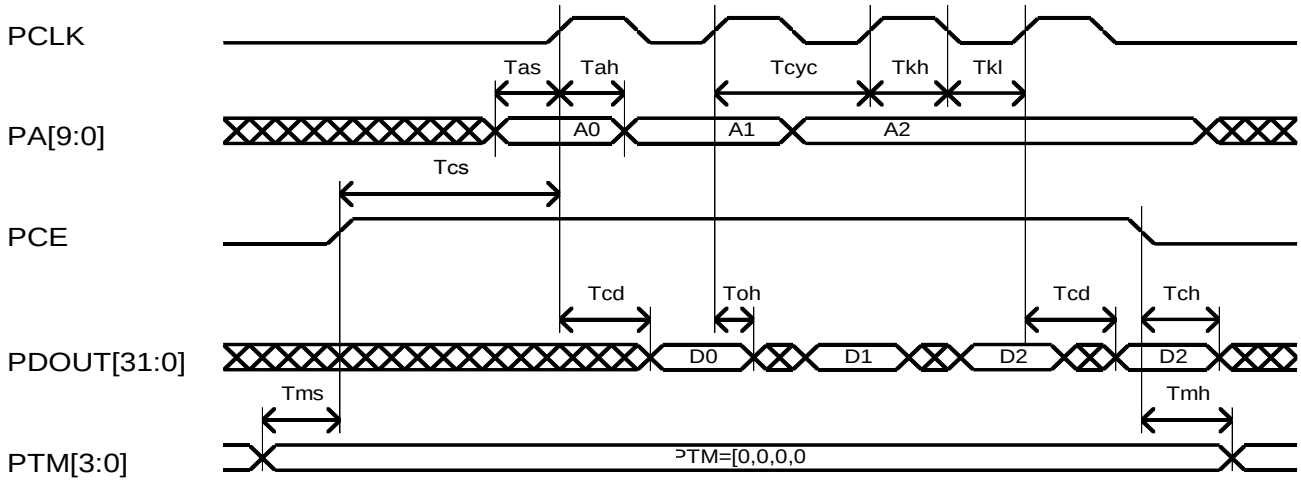
Timing Definition

Deep Standby Mode Timing Definition



User Mode

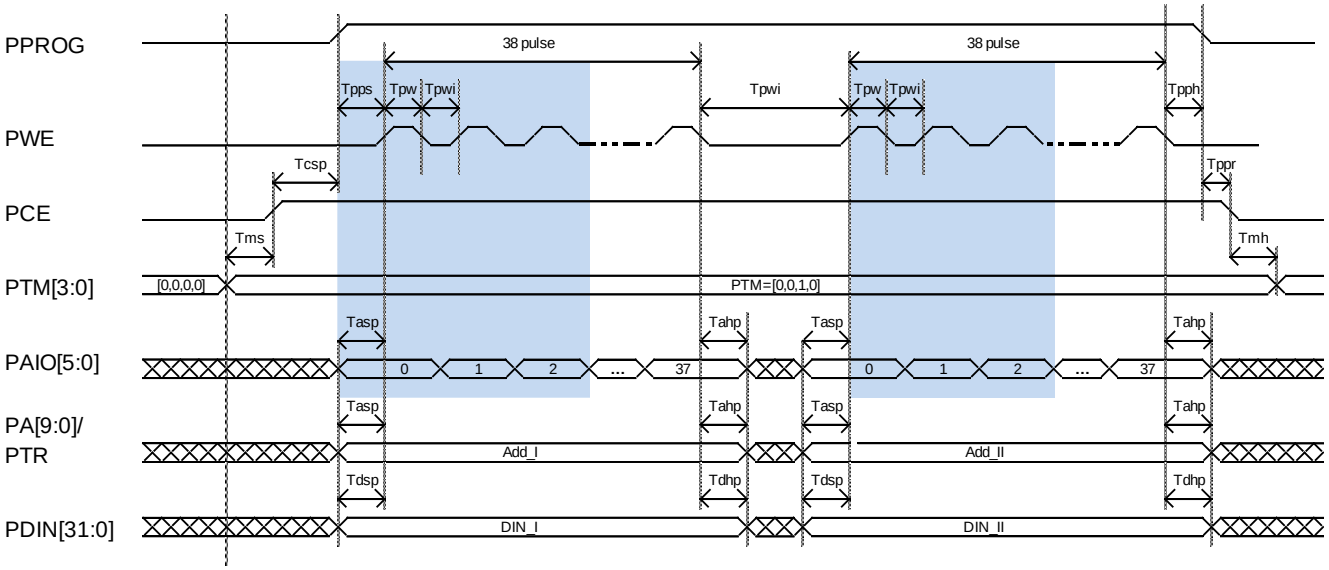
Read Cycle



PTR=H/L, PPROG=PWE=0, PDSTB=V_{DD}, PDIN[31:0]=H/L, PLDO=H

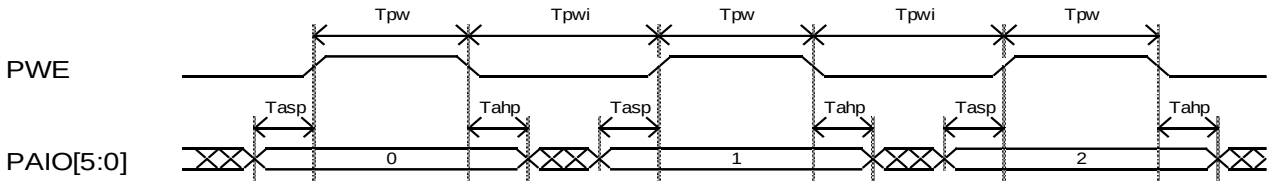
PENVDD2_VDD2=VDD2,VDD=0.81V~1.32V, VDD2=2.25V~3.63V, VSS=0V,

Program Cycle



PTR=H/L, PDSTB=V_{DD}, VDD=0.81V~1.32V, VDD2=2.25V~3.63V, VSS=0V, PENVDD2_VDD2=VDD2 , PLDO=H

Zoom In

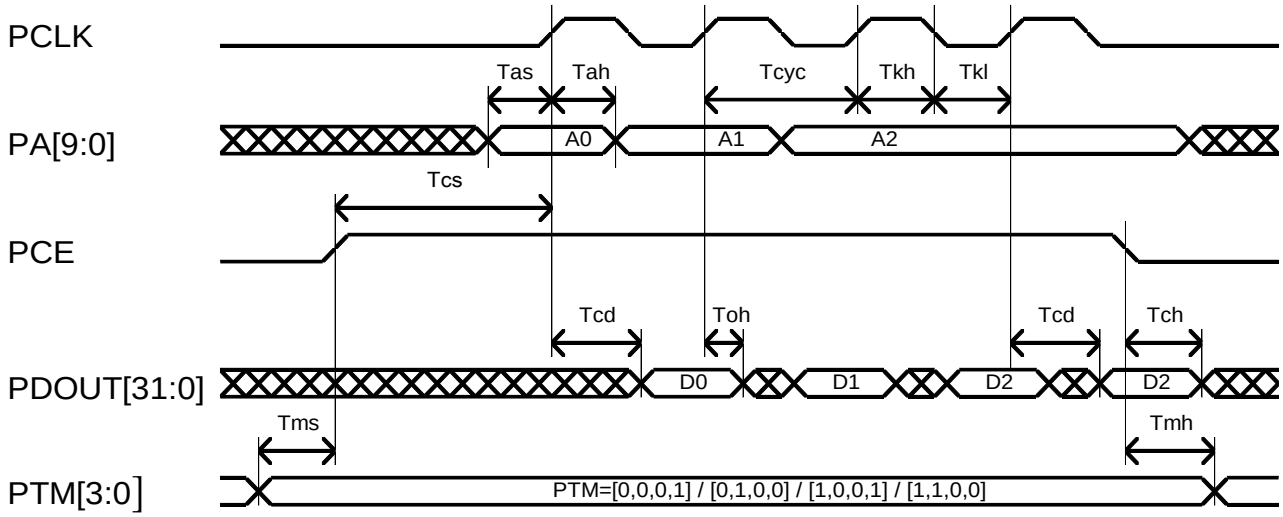


Notes

1. **PWE needs to be toggled for specific PAIO (PAIO=0~31) that PDIN data is "0". When PDIN data is "1", PWE doesn't have to be toggled.**
2. **PWE needs to be toggled for PAIO=32~37 (last 6 PAIO).**
3. **This NeoFuse IP with ECC functionality (Error-Correcting Code) needs customer's special attention: not only 32 data bits but also 6 ECC bits need to be programmed for one address at the same time. It means the minimum data string is 32 bits for each write operation and only can be programmed one time in each address.**

Test Mode

Margin Read Cycle



PTR=H/L, PPROG=PWE=0, PDSTB=V_{DD}, PDIN[31:0]=H/L, VDD=1.2V, VDD2=3.3V, VSS=0V, PENVDD2_VDD2=VDD2, PLDO=H

PTM[3:0]=[0,0,0,1] for initial Margin Read,PTM[3:0]=[0,1,0,0] for PGM Margin Read,

PTM[3:0]=[1,0,0,1] for HT initial Margin Read,PTM[3:0]=[1,1,0,0] for HT PGM Margin Read,

Notes

1. VDD/VDD2 needs to use typical value 1.2V/3.3V when doing Margin Read Mode.

Test Row Select

Test Row Address/PDOUT Description Table

Mode	Type	PA[3:0]	PA[9:4]	PAS	PAIO[5:0]	PDOUT
User Mode	Stand-by	-	-	-	-	-
	Read Access	Address-in	Must=0	-	-	PDOUT[31:0]
	Program Access	Address-in	Must=0	Address-in	Address-in	-
Test Mode	PGM Margin Read Mode	Address-in	Must=0	-	-	PDOUT[31:0]
	Initial Margin Read Mode	Address-in	Must=0	-	-	PDOUT[31:0]
	HT PGM Margin Read Mode	Address-in	Must=0			PDOUT[31:0]
	HT Initial Margin Read Mode	Address-in	Must=0			PDOUT[31:0]

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Notes

1. **PTR=H with PA valid address specified in the figure to select test row.**
2. **Test Row is individual memory block for testing, it does not include in main array size.**