DLIN

LIN Bus Controller

TEST PLAN

ver. 1.05.BS

Contents

1. OVERVIEW

The document describes all stimulation tests used to verify functionality of the DCD DLIN Core. Each test is composed from the CPUSTIM.TXT file containing a stimulus vectors used by CPUSTIM.V(HD) module and NODESTIM.TXT file which is used by NODESTIM.V(HD) module. Each module creates it own log file with description of detected errors. Each test is composed of three files:

CPUSTIM.TXT : *CPU stimulation vectors and reference*
NODESTIM.TXT : *NODE stimulation vectors and reference*
CPULOG.TXT : *CPUSTIM log file*
NODELOG.TXT : *NODESTIM log file*
RESULT.TXT : *Summary of test execution*

2. DLIN TESTS

Operation	Test name
DLIN bit error detects	BIT_ERROR
DLIN checkesum error detects	CHECKSUM_ERROR
DLIN framming error detects	FRAMMING_ERROR
Header Delay counter feature enabled	HEADER_DELAY
Header Delay counter with ABORT command	HEADER_DELAY_ABORT
Header send with max. header delay value	HEADER_DELAY_MAX_DELAY
Header Delay set on 15 and prescaler set on 0	HEADER_DELAY_PRE_0_DLY_15
Header Delay set on 0 and prescaler set on 15	HEADER_DELAY_PRE_15_DLY_0
Two transmission with Header Delay	HEADER_DELAY_TWO_TRANS
DLIN header detects	HEADER_DETECT
DLIN receive one header sequence after another	HEADER_HEADER
DLIN master expecte send response, slave transmit receive response	HEADER_RX_RESPONSE_HEADER
DLIN master expecte receive response, slave transmit send response	HEADER_TX_RESPONSE_HEADER
DLIN master get abort command durring sending break signal	MASTER_ABORT_IN_BREAK
DLIN master get abort command durring sending SYNC field	MASTER_ABORT_IN_SYNC
DLIN master get abort command durring sending PID field	MASTER_ABORT_IN_PID
DLIN master get abort command durring sending TX response	MASTER_ABORT_IN_TX_RESPONSE
DLIN master get abort command durring RX response	MASTER_ABORT_IN_RX_RESPONSE
DLIN slave abort current command	SLAVE_ABORT_COMMAND
DLIN master detects overrun error	MASTER_OVERRUN_ERROR
DLIN slave detects overrun error	SLAVE_OVERRUN_ERROR
Break sequence has been detected inside another break sequence	SLAVE_BREAK_IN_BREAK
Break sequence has been detected inside PID sequence	SLAVE_BREAK_IN_PID
Break sequence has been detected inside synchronization	SLAVE_BREAK_IN_SYNC
Slave receive 2 bytes in LIN1.3 mode	SLAVE_LIN13_RX_RESPONSE_2B
Slave receive 4 bytes in LIN1.3 mode	SLAVE_LIN13_RX_RESPONSE_4B
Slave receive 8 bytes in LIN1.3 mode	SLAVE_LIN13_RX_RESPONSE_8B
Slave transmit 2 bytes in LIN1.3 mode	SLAVE_LIN13_TX_RESPONSE_2B
Slave transmit 2 bytes in LIN1.3 mode	SLAVE_LIN13_TX_RESPONSE_2B_9600
Slave transmit 2 bytes in LIN1.3 mode	SLAVE_LIN13_TX_RESPONSE_2B_2400
Slave transmit 2 bytes in LIN1.3 mode	SLAVE_LIN13_TX_RESPONSE_2B_1200
Slave transmit 4 bytes in LIN1.3 mode	SLAVE_LIN13_TX_RESPONSE_4B
Slave transmit 8 bytes in LIN 1.3 mode	SLAVE_LIN13_TX_RESPONSE_8B
Slave receive 0 byte in LIN2.1 mode	SLAVE_LIN21_RX_RESPONSE_0B
Slave receive 1 byte in LIN2.1. mdoe	SLAVE_LIN21_RX_RESPONSE_1B
Slave receive 2 bytes in LIN2.1 mode	SLAVE_LIN21_RX_RESPONSE_2B
Slave receive 3 bytes in LIN2.1 mode	SLAVE_LIN21_RX_RESPONSE_3B
Slave receive 4 bytes in LIN2.1 mdoe	SLAVE_LIN21_RX_RESPONSE_4B
Slave receive 5 bytes in LIN2.1 mdoe	SLAVE_LIN21_RX_RESPONSE_5B
Slave receive 6 bytes in LIN2.1 mdoe	SLAVE_LIN21_RX_RESPONSE_6B
Slave receive 7 bytes in LIN2.1 mdoe	SLAVE_LIN21_RX_RESPONSE_7B
Slave receive 8 bytes in LIN2.1 mode	SLAVE_LIN21_RX_RESPONSE_8B
Slave transmit 0 byte in LIN2.1 mode	SLAVE_LIN21_TX_RESPONSE_0B
Slave transmit 1 byte in LIN2.1. mdoe	SLAVE_LIN21_TX_RESPONSE_1B
Slave transmit 2 bytes in LIN2.1 mode	SLAVE_LIN21_TX_RESPONSE_2B
Slave transmit 3 bytes in LIN2.1 mode	SLAVE_LIN21_TX_RESPONSE_3B
Slave transmit 4 bytes in LIN2.1 mdoe	SLAVE_LIN21_TX_RESPONSE_4B
Slave transmit 5 bytes in LIN2.1 mdoe	SLAVE_LIN21_TX_RESPONSE_5B
Slave transmit 6 bytes in LIN2.1 mdoe	SLAVE_LIN21_TX_RESPONSE_6B
Slave transmit 7 bytes in LIN2.1 mdoe	SLAVE_LIN21_TX_RESPONSE_7B
Slave transmit 8 bytes in LIN2.1 mode	SLAVE_LIN21_TX_RESPONSE_8B
Slave TX responses	SLAVE_SHORT_TX_RESPONSE
Slave detected synchronization error	SLAVE_SYNC_ERROR
Slave synchronization test	SLAVE_SYNCHRONIZATION
Slave synchronization test wit Delay	SLAVE_SYNCH_WITH_DELAY
Slave waits on 1 byte, detects timeout error	TIMEOUT_ERROR_WAIT_1_BYTE

Slave waits on 2 bytes, detets timeout error	TIMEOUT_ERROR_WAIT_2_BYTES
Slave waits on 4 bytes, detets timeout error	TIMEOUT_ERROR_WAIT_4_BYTES
Slave waits on 8 bytes, detets timeout error	TIMEOUT_ERROR_WAIT_8_BYTES
Checksum calculation in LIN1.3 mode	LIN13_CHECKSUM
Checksum caltulation errors detect	LIN13_CHECKSUM_ERROR
Variable frame length mode	LIN13_VAR_SIZE
Checksum error detects in variable frame length mode	LIN13_VAR_SIZE_PER
Frame timeout error detects in variable frame length mode	LIN13_VAR_SIZE_TOER
Checksum calculation in LIN21 mode	LIN21_CHECKSUM
Checksum calculation errors detect	LIN21_CHECKSUM_ERROR
DLIN Divisor test 1	DIVISOR_1
DLIN Divisor Test 2	DIVISOR_2
LOG MODE Test	LOG_MODE
LOG Mode before header	LOG_MODE_BEFORE_HEADER
LOG Mode switch test	LOG_MODE_SWITCH
Master node receive 0 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_0B
Master node receive 1 byte response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_1B
Master node receive 2 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_2B
Master node receive 3 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_3B
Master node receive 4 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_4B
Master node receive 5 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_5B
Master node receive 6 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_6B
Master node receive 7 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_7B
Master node receive 8 bytes response LIN2.1 mode	MASTER_LIN21_RX_RESPONSE_8B
Break signal with 9 dominant bits	BREAK_09BIT
Break signal with 10 dominant bits	BREAK_10BIT
Break signal with 11 dominant bits	BREAK_11BIT
Break signal with 12 dominant bits	BREAK_12BIT
Break signal with 26 dominant bits	BREAK_26BIT
Break signal with 27 dominant bits	BREAK_27BIT
Break signal with 28 dominant bits	BREAK_28BIT
Timeout after detection only break signal (without sync and pid fields)	BREAK_ONLY_TIMEOUT
Go to sleep command detection	SLEEP_CMD
Go to sleep command with errors	SLEEP_CMD_ERROR
Automatic anrty to sleep mode after bus inactivity detection	SLEEP_DETECT
Access to Idle detection timer	SLEEP_IDT_ACCESS
Wake-up signal send by master	WAKEUP_MASTER_SEND
Wake-up send in slave mode	WAKEUP_SLAVE_SEND
Wake-up signal detection	WAKEUP_EXTERNAL_SEND
Master send Wake-up signal with abort command	WAKEUP_MASTER_ABORT
Slave send wake-up signal with abort command	WAKEUP_SLAVE_ABORT
Errors generated during wake-up signal	WAKEUP_ERRORS
Break detection during sending wake-up signal	WAKEUP_IN_HEADER
Wake-up signal, the device is not in a sleep mode	WAKEUP_NORMAL_MODE
The test checks ABRD mode abort	ABR_ABORT
Entering in to ABRD mode when data is sent on the LIN bus	ABR_CMD_IN_DATA
Entering in to ABRD mode when header is sent on the LIN bus	ABR_CMD_IN_HEADER
Detecting low bit rate values	ABR_DEL_LOW
Detecting high bit values	ABR_DEL_HIGH
Sending header command with delay	LCR_DLY_HEADER_DELAY
Sending master command with delay	LCR_DLY_MASTER_CMD
Generate Overrun error with enabled LCR delay	LCR_DLY_OVERRUN
Abort command with enabled LCR delay	LCR_DLY_SLAVE_ABORT
LIN 1.3 Communication test with enabled LCR delay	LCR_DLY_SLAVE_LIN13_TX_RESPONSE_2B_1200
LIN 2.1 Communication test with enabled LCR delay	LCR_DLY_SLAVE_LIN21_TX_RESPONSE_2B_1200
Transmitter send correct bit stop and receiving dominant bit	SLAVE_STOP_BIT_ERROR

Table 1. DLIN tests

3. ORDERING INFORMATION AND SUPPORT

Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
e-mail: info@dcd-semi.com
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check http://dcd-semi.com/contact-us/