DLIN

LIN Bus Controller

INSTALLATION NOTE

ver. 1.02a.BS

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1. INTRODUCTION

This specification presents the structure of HDL core, their test bench and supplied files. It is intended to help with installation process of core in conjunction to simulation and synthesis tools.

2. INSTALLATION

Typically DLIN model is shipped on a CD-ROM. The following description details how to install the model onto a hard disc. To install the DLIN on the hard disk execute the following steps:

1. If you have the CD-ROM with the model copy the DLIN directory to your local hard disk, or
2. if you have a zipped file named DLIN.ZIP then copy it to local hard disk and extract them. The DLIN files will extract to directory of your choice.

At this point the model is ready for "soft" installation. The next chapters describe included files and their use with conjunction to ModelSim and Synopsys DC tools.

3. SUPPLIED FILES

3.1. DOCUMENTATION

The following documents are included in the delivered model:

./DLIN/DOC/

DLIN_INST.PDF	: This document file
DLIN_DS.PDF	: HDL core datasheet
DLIN_TESTS.PDF	: HDL core tests plan and code cover. report
DLIN_SPEC.PDF	: User manual

3.2. SUPPLIED MODEL FILES

3.2.1. PRIMARY SOURCE CODE FILES (SYNTHESIZABLE):

./DLIN/SRC/SOURCE/

/DLIN_PARAMS.(V)HD	*: DLIN Enumeration type declarations.*
/DLIN.(V)HD	*: Main DLIN unit*

3.2.2. TESTBENCH SOURCE CODE FILES (NOT SYNTHESIZABLE):

./DLIN/SRC/TB/

/TB.(V)HD	*: Basic Test Bench for DLIN*

3.2.3. ENVIRONMENT RELATED FILES (NOT SYNTHESIZABLE):

./DLIN/SRC/TB/ENV/

/CLKGEN.(V)HD	*: Clock signal generator*
/CPUSTIM.(V)HD	*: CPU simulation engine*
/NODESTIM.(V)HD	*: NODE simulation engine*
/TRANSCEIVER.(V)HD	*: LIN transceiver model*

3.3. COMPILATION AND SIMULATION SUPPORT MACROS

Compilation and simulation macros are intended to easily using of DLIN core with the conjunction to Active-HDL and ModelSim tools.

3.3.1. MODELSIM MACROS

./DLIN/SRC/MACROS/MODELSIM/

/COMPILE.DO	*: Compile all HDL files macro*
/FIRST_RUN.DO	*: Example macro to first run*
/ALL_TESTS.DO	*: Run automatically all standard tests*
/TEST_XX.DO	*: Parameterized macro used by the other macros.* **Should never be run as standalone.**

3.3.2. ACTIVE-HDL MACROS

./DLIN/SRC/MACROS/ACTIVEHDL/

/COMPILE.DO	*: Compile all HDL files macro*
/FIRST_RUN.DO	*: Example macro to first run*
/ALL_TESTS.DO	*: Run automatically all standard tests*
/TEST_XX.DO	*: Parameterized macro used by the other macros.* **Should never be run as standalone.**

3.4. SYNTHESIS SUPPORT SCRIPTS

Synthesis scripts are intended to easily using of DLIN core with the conjunction to Synopsys Design Compiler (called DC) tool.

DC scripts:

./DLIN/SYNTHESIS/DC_SCRPTS/

/DLIN.SCR	*: Top level architecture synthesis script*
/RUNALL.SCR	*: Run all synthesis script – Master script. This script should be run to produce complete EDIF/Verilog Netlist and synthesis reports*

Before using this scripts target technology libraries should be set in DC configuration files: ***.synopsys_dc.setup, .synopsys_vss.setup*** . Directories structure:

./DLIN/SYNTHESIS/DC_SCRIPTS/	*: Synthesis script sources*
./DLIN/SYNTHESIS/WORK/	*: DLIN_LIB library files*
./DLIN/SYNTHESIS/REPORTS/	*: Synthesis reports*
./DLIN/SYNTHESIS/NETLISTS/	*: EDIF/Verilog output Netlists*

3.5. TESTS SUPPORT FILES

In the current version of core have been included example set of tests. A tests suite is divided into a following subdirectories:

./DLIN/TESTS/CURTEST/ : Directory contains current tests.
./DLIN/TESTS/ALLTESTS/ : Directory contains all attached test's sources.
./DLIN/TESTS/RESULTS/ : Directory contains results of simulation for all tests.

3.5.1. SINGLE TEST STRUCTURE

Each test consists of the following files:
./DLIN/TESTS/CURTEST/

/CPUSTIM.TXT : Stimulus vectors file for CPU. It contains stimulation vectors and correct responses for appropriate tests. This file is read directly by test bench.
/CPULOG.TXT : CPU side simulation results. It contains responses for appropriate tests. This file is written directly by test bench.
/NODESTIM.TXT : Stimulus vectors file for DLIN. It contains stimulation vectors and correct responses for appropriate tests. This file is read directly by test bench.
/NODELOG.TXT : DLIN side simulation results. It contains responses for appropriate tests. This file is written directly by test bench.
/RESULT.TXT : Test summary result file. It contains information on whether the test passed or failed

3.5.2. INCLUDED TESTS

- Examples of bit error test is located in the following directory:

./DLIN/TESTS/ALLTESTS/BIT_ERROR

- Examples of checksum error test is located in the following directory:

./DLIN/TESTS/ALLTESTS/CHECKSUM_ERROR

- Examples of framing error test is located in the following directory:

./DLIN/TESTS/ALLTESTS/FRAMMING_ERROR

- Examples of frame header detection is located in the following directory:

./DLIN/TESTS/ALLTESTS/HEADER_DETECT

- Examples of received two headers frame test is located in the following directory:

./DLIN/TESTS/ALLTESTS/HEADER_HEADER

- Examples of receive response on send request header test is located in the following directory:

./DLIN/TESTS/ALLTESTS/HEADER_RX_RESPONSE_HEADER

- Examples of send response on receive response header test is located in the following directory:

./DLIN/TESTS/ALLTESTS/ HEADER_TX_RESPONSE_HEADER

- Examples of abort command on slave mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_ABORT_COMMAND

- Examples of overrun error in master mode is located in the following directory:

./DLIN/TESTS/ALLTESTS/MASTER_OVERRUN_ERROR

- Examples of overrun error in slave mode is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_OVERRUN_ERROR

- Examples of receive 2 bytes frame in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/ SLAVE_LIN13_RX_RESPONSE_2B

- Examples of receive 4 bytes frame in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/ SLAVE_LIN13_RX_RESPONSE_4B

- Examples of receive 8 bytes frame in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/ SLAVE_LIN13_RX_RESPONSE_8B

- Examples of transmit 2 bytes frame in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/ SLAVE_LIN13_TX_RESPONSE_2B

- Examples of transmit 4 bytes frame in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/ SLAVE_LIN13_TX_RESPONSE_4B

- Examples of transmit 8 bytes frame in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/ SLAVE_LIN13_TX_RESPONSE_8B

- Examples of receive 0 byte frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_0B

- Examples of receive 1 byte frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_1B

- Examples of receive 2 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_2B

- Examples of receive 3 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_3B

- Examples of receive 4 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_4B

- Examples of receive 5 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_5B

- Examples of receive 6 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_6B

- Examples of receive 7 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_7B

- Examples of receive 8 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_RX_RESPONSE_8B

- Examples of transmit 0 byte frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_0B

- Examples of transmit 1 byte frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_1B

- Examples of transmit 2 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_2B

- Examples of transmit 3 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_3B

- Examples of transmit 4 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_4B

- Examples of transmit 5 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_5B

- Examples of transmit 6 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_6B

- Examples of transmit 7 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_7B

- Examples of transmit 8 bytes frame in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_LIN21_TX_RESPONSE_8B

- Examples of short transmit response in slave mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_SHORT_TX_RESPONSE

- Examples of slave synchronization error test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_SYNC_ERROR

- Examples of slave synchronization test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SLAVE_SYNCHRONIZATION

- Examples of synchronization test is located in the following directory:

./DLIN/TESTS/ALLTESTS/SYNC_WITH_DELAY

- Examples of timeout event when waiting for 1 byte test is located in the following directory:

./DLIN/TESTS/ALLTESTS/TIMEOUT_ERROR_WAIT_1_BYTES

- Examples of timeout event when waiting for 2 bytes test is located in the following directory:

./DLIN/TESTS/ALLTESTS/TIMEOUT_ERROR_WAIT_2_BYTES

- Examples of timeout event when waiting for 4 bytes test is located in the following directory:

./DLIN/TESTS/ALLTESTS/TIMEOUT_ERROR_WAIT_4_BYTES

- Examples of timeout event when waiting for 8 bytes test is located in the following directory:

./DLIN/TESTS/ALLTESTS/TIMEOUT_ERROR_WAIT_8_BYTES

- Examples of checksum calculation in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/LIN13_CHECKSUM

- Examples of error flag generation in checksum calculation in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/LIN13_CHECKSUM_ERROR

- Examples of variable frame length in LIN1.3 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/LIN13_VAR_SIZE

- Examples of checksum error indicator working with variable frame length in LIN1.3 test is located in the following directory:

./DLIN/TESTS/ALLTESTS/LIN13_VAR_SIZE_PER

- Examples of frame timeout indicator working with variable frame length in LIN1.3 test is located in the following directory:

./DLIN/TESTS/ALLTESTS/LIN13_VAR_SIZE_TOER

- Examples of checksum calculation in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/LIN21_CHECKSUM

- Examples of error flag generation in checksum calculation in LIN2.1 mode test is located in the following directory:

./DLIN/TESTS/ALLTESTS/LIN21_CHECKSUM_ERROR

- Log mode

./DLIN/TESTS/ALLTESTS/LOG_MODE

- Switching Log mode

./DLIN/TESTS/ALLTESTS/LOG_MODE_SWITCH

- Enable Log mode before header receive

./DLIN/TESTS/ALLTESTS/LOG_MODE_BEFORE_HEADER

- Break signal with 9 dominant bits

./DLIN/TESTS/ALLTESTS/BREAK_09BIT

- Break signal with 10 dominant bits

./DLIN/TESTS/ALLTESTS/BREAK_10BIT

- Break signal with 11 dominant bits

./DLIN/TESTS/ALLTESTS/BREAK_11BIT

- Break signal with 12 dominant bits

./DLIN/TESTS/ALLTESTS/BREAK_12BIT

- Break signal with 26 dominant bits

./DLIN/TESTS/ALLTESTS/BREAK_26BIT

- Break signal with 27 dominant bits

./DLIN/TESTS/ALLTESTS/BREAK_27BIT

- Break signal with 28 dominant bits

./DLIN/TESTS/ALLTESTS/BREAK_28BIT

- Timeout after detection only break signal

./DLIN/TESTS/ALLTESTS/BREAK_ONLY_TIMEOUT

- Go to sleep command detection

./DLIN/TESTS/ALLTESTS/SLEEP_CMD

- Go to sleep command with errors

./DLIN/TESTS/ALLTESTS/SLEEP_CMD_ERROR

- Automatic entry to sleep mode after bus inactivity detection

./DLIN/TESTS/ALLTESTS/SLEEP_DETECT

- Access to IDLE detection timer

./DLIN/TESTS/ALLTESTS/SLEEP_IDT_ACCESS

- Wake-up signal send by master

./DLIN/TESTS/ALLTESTS/WAKEUP_MASTER_SEND

- Wake-up send in slave mode

./DLIN/TESTS/ALLTESTS/WAKEUP_SLAVE_SEND

- Wake-up signal detection

./DLIN/TESTS/ALLTESTS/WAKEUP_EXTERNAL_SEND

- Master send wake-up signal with abort command

./DLIN/TESTS/ALLTESTS/WAKEUP_MASTER_ABORT

- Slave send wake-up signal with abort command

./DLIN/TESTS/ALLTESTS/WAKEUP_SLAVE_ABORT

- Errors generated during wake-up signal

./DLIN/TESTS/ALLTESTS/WAKEUP_ERRORS

- Break detection during sending wake-up signal

./DLIN/TESTS/ALLTESTS/WAKEUP_IN_HEADER

- Wake-up signal then the device is not is sleep mode

./DLIN/TESTS/ALLTESTS/WAKEUP_NORMAL_MODE

- Automatic Bit rate detection with abort command with abort

./DLIN/TESTS/ALLTESTS/ABR_ABORT

- Run Automatic Bit rate detection command during data on LIN bus

./DLIN/TESTS/ALLTESTS/ABR_IN_DATA

- Run Automatic Bit rate detection command during header on LIN bus

./DLIN/TESTS/ALLTESTS/ABR_IN_HEADER

- Automatic Bit rate detection low bit rates

./DLIN/TESTS/ALLTESTS/ABR_DET_LOW

- Automatic Bit rate detection high bit rates

./DLIN/TESTS/ALLTESTS/ABR_DET_HIGH

4. USING MODELSIM TOOL

4.1. DESIGN PROJECT FILES

The design file is referenced to the following directory:
./**DLIN**/ *: ModelSim working directory*
The working directory should be changed to the directory listed above.

4.2. PREPARING A MODEL TO SIMULATION

To simulate the model, please follow the steps:

- Run the ModelSim software.
- Change the working directory to ./**DLIN**/ directory. Afterwards your model is ready to starts simulation.
- Run the ***FIRST_RUN.DO*** macro, which is prepared to easy start of interactive simulation.

OR
If you wish to run all supplied tests automatically and check if model works correctly, simply run the ***ALL_TESTS.DO*** macro. Afterwards all tests will be sequentially executed by the automatic test bench. In the "Console" window you will see which test is currently executed.

5. USING ACTIVE-HDL TOOL

Note: *The path to the project root can not contains any spaces in the directory name e.g. D:\My Designs is invalid, but D:\MyDesigns is correct. The project can be located on the any place on the HD disk.*

5.1. DESIGN PROJECT FILES

The main design file is located in the following directory:
./**DLIN**/
*/***DLIN.*ADF** *: Active-HDL main design file*
The other files are not listed here.

5.2. PREPARING A MODEL TO SIMULATION

To simulate the model, you have to do the following steps:

- Run the Active-HDL software.
- Open the design file named DLIN.adf located at the. **/DLIN/** directory. Afterwards your model is ready to start simulation.
- Run the ***FIRST_RUN.DO*** macro, which is prepared to easily start interactive simulation.

OR
If you wish to run all supplied tests automatically and check if model works correctly, simply run the ***ALL_TESTS.DO*** macro. Afterwards all tests will be sequentially executed by the automatic test bench. In the "Console" window you will see which test is currently executed.

6. USING SYNOPSYS DC

6.1. DESIGN PROJECT FILES

The design file is referenced to the following directory:
*./**DLIN**/ : Synopsys DC working directory*
The working directory should be changed to the directory listed above. The directories structure has to exist before synthesis process would be started (See 4.4 chapter).

6.2. PREPARING A MODEL TO SYNTHESIS

To synthesize the model, you have to do the following steps:

- Set an appropriate target technology library in DC setup files. Project library ***DLIN_LIB*** is automatically mapped by included scripts. The library files are located in ./**SYNTHESIS**/**WORK**/ directory.
- Run the DC software.
- Change the working directory to ./**DLIN**/ directory. Make sure that target technology configuration files have been already loaded and appropriate library files are available in search path. For more details please refer to DC help files. Afterwards your model is ready to start synthesis.
- Run the ***RUNALL.SCR*** script (type include ***RUNALL.SCR*** command), which is prepared to easily start automatic synthesis process. Afterwards all DLIN components will be sequentially alanyzed, elaborated and finally optimized by the DC tool. In the "Console" window you will see which component is currently processed.

All reports are located in ./**SYNTHESIS**/**REPORTS**/ directory. Finally optimized netlists are found in ./**SYNTHESIS**/**NETLISTS**/ directory.

7. ORDERING INFORMATION AND SUPPORT

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