Bandwidth Analysis of RF-DC Converters Under Multisine Excitation

Ning Pan, *Student Member, IEEE*, Daniel Belo, *Student Member, IEEE*, Mohammad Rajabi, *Student Member, IEEE*, Dominique Schreurs, *Fellow, IEEE*, Nuno Borges Carvalho, *Fellow, IEEE*, and Sofie Pollin, *Senior Member, IEEE*

***Abstract*— The use of multisine signals to improve the efficiency of wireless power transfer (WPT) for low average received power was proposed recently. Several measurement-based studies illustrated the gain that can be achieved for different circuit or waveform instances, focusing on the impact of a time-varying amplitude on the rectifying efficiency. This paper first establishes a model enabling a thorough analysis of the multisine-based WPT system focusing on the bandwidth of the signal and the rectifier. This model enables a codesign of signal and rectifier for optimal WPT. The proposed model provides insight into the output voltage and power, as a function of the input waveform for different circuit models. By including the input matching and the clamper, our model is generic and can include a wide range of rectifiers with different voltage multiplication approaches. The key insight gained from our analysis is that there is a tradeoff between the frequency spacing of the tones of the multisine signal and the cut-off frequency of the low-pass *RC* filter, as a main property of the rectifier circuit. Our model predicts the measured power conversion efficiency and voltage with an error below 0.1 and 0.2 V, respectively.**

***Index Terms*— Bandwidth (BW) impact, multisine signal, peak-to-average power ratio (PAPR), theoretical system model, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) is one of the most promising solutions for solving battery limitations in areas such as the Internet of things, where many, small, and battery-limited devices need to be wirelessly connected to the Internet [1]. WPT techniques enable wireless networks with smaller devices operating permanently without battery replacement [2]. Moreover, WPT allows powering devices in an on-demand fashion, which provides more quality of service control and higher overall energy efficiency [3].

However, the power that can be received in WPT is significantly lower than 0 dBm since the regulation limits the transmit power in the frequency band of interest. Given the low transmit power, far-field WPT dealing with high path loss because of the long transmission distance results in low received signal strength at the receiver [4]. The power conversion efficiency (PCE) of a rectifier is increasing with the increasing power of the input signal, typically leading to a higher average output power with high peak-to-average power ratio (PAPR) systems. In order to deal with the limited input power, a number of studies utilize high PAPR signals to improve the PCE by creating short duration high input power signals [5]–[13].

The majority of the studies concentrated on measurements to validate the benefits of high PAPR signals in an *ad hoc* way. Trotter *et al.* [5] used a power-optimized waveform (POW) with the largest PAPR to improve the charge pump efficiency. They proved that a POW enhances the range and reliability of radio-frequency identification by measurements. Researchers in CTTC observed a higher PCE by applying a chaotic signal of a high PAPR to a 433-MHz WPT system [7]. Lo *et al.* [8] improved the PCE of 50% by using an ultrawideband impulsive signal with a high PAPR at low input power (i.e., 0 dBm) on a voltage doubler. Collado and Georgiadis [9] selected the optimal waveform experimentally for a rectifier operating at 433 MHz. They observed that white noise, OFDM, and chaotic signals with a higher PAPR would lead to a higher PCE.

The studies as mentioned earlier provide concrete measurement results under various rectifier designs to verify the advantage of high PAPR signals. However, these studies lack sufficient theoretical arguments to explain the *ad hoc* choice of the used PAPR signals. Most importantly, these studies had not considered the codesign of waveform and rectifier circuit and hence did not provide insight into the impact of circuit properties on the optimal waveform.

Several attempts have been made to gain insight in the WPT optimization and how it depends on the waveform. Boaventura and Carvalho [10] carried out a theoretical and experimental analysis of the phase relationship between the tones of a multisine waveform. They found that multisine waveforms with zero phase difference between the neighboring tones would result in the highest output dc voltage. Their theoretical analysis, however, only optimizes the waveform, and does not explicitly consider the impact of the circuit bandwidth (BW). Yang *et al.* [11] studied the power distribution of two-tone UWB signals. They reported that due to the convex property

Manuscript received March 8, 2017; revised July 8, 2017 and August 23, 2017; accepted August 31, 2017. Date of publication October 24, 2017; date of current version February 5, 2018. This work was supported in part by EU COST IC1301 Wireless Power Transmission for Sustainable Electronics (WiPE) http://www.cost-ic1301.org/, in part by the Fonds Wetenschappelijk Onderzoek, and in part by the Hercules company. *(Corresponding author: Ning Pan.)*

N. Pan, M. Rajabi, D. Schreurs, and S. Pollin are with the TELEMIC Division, ESAT, Katholieke Universiteit Leuven, 3000 Leuven, Belgium (e-mail: ning.pan@kuleuven.be).

D. Belo and N. Borges Carvalho are with the Instituto de Telecomunicaes, Universidade de Aveiro, P-3810-193 Aveiro, Portugal.

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Digital Object Identifier 10.1109/TMTT.2017.2757473

of the diode I–V curve, the high PAPR signal outperforms the continuous wave (CW) signal. Their conclusions cannot be generalized easily as their study is limited to two-tone UWB signals only and they neglect BW limitations of the circuit. Valenta and Durgin [12] demonstrated the PAPR waveform effects on a single-shunt rectenna operating at 5.8 GHz by varying the number of tones. They showed that the subcarriers could be optimally placed to maximize the output voltage. A theoretical model is provided for the energy-conversion efficiency for rectifiers under high PAPR waveform excitation in [13]. They derived the closed-form expression of PCE as a function of measured dc voltage and the rectifier's characteristics, assuming high input power that simplifies the analysis. Bolos *et al.* [6] identified the optimal load value for WPT system using high PAPR waveforms. However, an analytical solution was achieved for CW excitations only.

While these studies focus on the impact of the PAPR, our analysis investigates the impact of BW and frequency spacing for a given PAPR. Thereby, we show that the BW of the circuit does have an impact on the overall system performance. The work in [14] details an initial exploration of the impact of tone separation and signal BW of multisine signals. This paper gives insight into the fact that the intermodulation product should be minimized to avoid strong ripples. The analysis and conclusions in [14] depend on the input matching network that also depends on the output low-pass RC filter of the rectifier. A full rectifier exploration, including the variation of R and C, hence also requires each time a novel matching network. As a result, their approach does not enable a full circuit exploration independently of the input matching network impact. To the best of our knowledge, very few studies have included the BW impact of the signal on the nonlinear rectification behavior as well as the BW limitations of the rectifier. As a result, all results so far cannot be compared or generalized easily, and most importantly some results lead to conflicting conclusions.

Without a comprehensive understanding of the codesign of both the waveform and the rectifier circuit, a convincing conclusion is not easy to achieve. We found some different studies with contradictory results in the literature. Sakaki *et al.* [15] showed that QPSK and 16 quadratic-amplitude-modulated signals with a higher PAPR decrease the PCE of the WPT system by measurements. Besides, the work in [16] demonstrated a theoretical model to compute the AC to DC PCE. This paper showed that the CW waveform outperforms the multisine waveforms by simulations, contradicting previous results claiming that multisine waveforms generate a better PCE.

The multisine waveform indeed benefits from the convex nature of the diode's I–V curve, making the diode bias at low input power [17]. There are multiple ways to create high PAPR signals in time domain, each with a different signal BW. As a result, not only the PAPR distribution over time but also the BW of the signal and how it will impact the rectifier should be studied to provide a complete insight into the system.

This paper investigates the multisine-based WPT as a whole, involving the impacts from the input waveform and the rectifier circuit itself. By linking the key parameters of both the waveform and the circuit, we can understand the system comprehensively. Since the multisine WPT is strongly influenced by BW of the signal and the system both, a model is necessary that includes BW of the signal and key components of the rectifier that may affect the system BW, e.g., input matching or output low-pass RC filter. Such a broad study cannot be done experimentally only, as this would require a lot of different rectifier designs for each studied parameter setting. In this paper, we propose a model that is verified experimentally for a subset of design parameters, yet allows a free and broad exploration of the designing space.

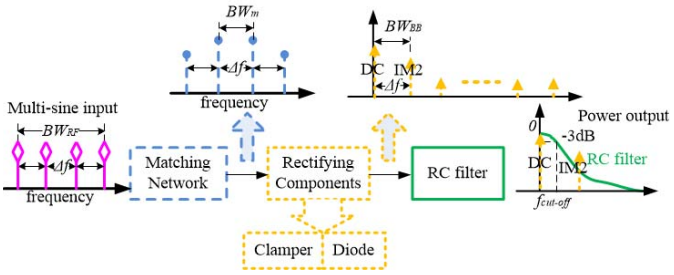


Fig. 1. Multisine-based WPT system overview.

The rest of this paper is organized as follows. Section II addresses the fundamental problem when designing the optimal multisine-based WPT system. Section III demonstrates the process to obtain the output dc voltage and PCE of the general WPT system as a function of input multisine waveform parameters, based on the rectifier circuit analysis. Section IV applies the general theoretical model adapting to the rectifiers under test and validates the model with measurement results, providing circuit and waveform design insights. Finally, in Section V, the key findings achieved with this paper are reported.

II. Problem Statement

Multisine-based WPT is typically a BW demanding system. When doing a codesign of the signal waveform and the rectifier circuit, we need to understand how we can balance the BW of the signal and the rectifier. For a multisine signal, the RF BW depends on the number of tones N_t and the frequency spacing between the tones Δf [$\mathrm{BW_{RF}} = (N_t - 1)\Delta f$]. For the rectifier, the BW depends on the input matching (BW_m) and the $f_{\text{cut-off}}$ of the output low-pass RC filter.

Fig. 1 shows the overview of a multisine-based WPT system. In this case, a four-tone signal of BW $\mathrm{BW_{RF}}$ represented by the solid magenta lines is received by the antenna, where depending on the BW of the input matching BW_m, part of the signal is reflected as represented by the blue dashed multisine signal. Then, the rectifying components transform the signal nonlinearly into a baseband (BB) signal of $\mathrm{BW_{BB}}$, consisting of a dc response, and several intermodulation products at the frequency Δf and multiples of that (see the yellow dotted signal in Fig. 1). Finally, the output low-pass RC filter determines the ultimate output signal represented in green.

Although dc often refers to "constant polarity," representing the signal at $f = 0$ Hz, it is used in this paper as the slowly varying local mean value of the output voltage, representing the time-varying dc output of the rectifier as also

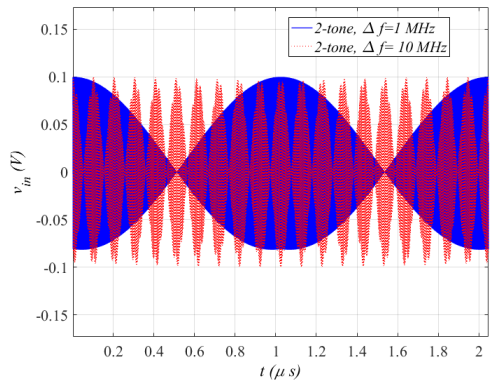


Fig. 2. Two-tone multisine signals with different frequency spacing and the same input power.

used in [18]. Thus, output dc of the rectifier in frequency domain consists of a power bin at 0 Hz and one power bin at BB frequency, the intermodulation products. Thus, both the component at 0 Hz and the strongest intermodulation product (IM2) are the main contributors to the output dc. However, it must be handled properly by the output low-pass *RC* filter; otherwise, this would lower the output dc.

To optimize the efficiency of the system, we need to understand the essential BW relation between the waveform and circuit. For a multisine WPT, the IM2 is present at Δf, while the $f_{\text{cut-off}}$ of output low-pass *RC* filter limits the level of IM2. We link this relation by introducing the ratio $(\Delta f / f_{\text{cut-off}})$ and study how it should be dimensioned in a well-designed multisine WPT system.

Before introducing the detailed system model, we elaborate on the factors influencing the $(\Delta f / f_{\text{cut-off}})$. The frequency spacing Δf is related to signal cycling period. As shown in Fig. 2, a multisine waveform with a larger frequency spacing Δf would have more frequently repeated peaks. Besides, $f_{\text{cut-off}}$ is decided by output low-pass *RC* filter, e.g., $f_{\text{cut-off}} = (1/2\pi RC)$. A larger output low-pass *RC* filter gives smaller $f_{\text{cut-off}}$ and vice versa.

On the one hand, when $(\Delta f / f_{\text{cut-off}})$ equals zero, either *RC* or Δf is zero. If *RC* is zero, the output dc voltage is a small finite number since the output low-pass *RC* filter does not filter IM2 and too many ripples are generated; if Δf approaches zero, the output dc voltage would be very small since the envelope period is very long resulting in long discharge time of the output after the low-pass *RC* filter. In other words, IM2 is not handled by the output low-pass *RC* filter, either. On the other hand, when $(\Delta f / f_{\text{cut-off}})$ is infinitely large, either *RC* or Δf is infinitely large. If *RC* is infinitely large, the output dc power is a small value since all IM products are filtered out; if Δf is infinitely large, the signal BW is so broad for the system that most of the signal will be filtered out by the output low-pass *RC* filter, in addition to the input mismatch problem. Thus, we expect there is an optimal region of $(\Delta f / f_{\text{cut-off}})$ that maximizes the output dc voltage.

A comprehensive understanding of the optimal region for $(\Delta f / f_{\text{cut-off}})$ is the objective of this paper. In the next section, we detail our system model for the exploration of the main parameters of interest. In Section IV, we show our model is a good approximation of the multisine-based WPT, by comparing with measurements.

III. System Model

In this section, we address the model to compute the output dc voltage and PCE based on the input multisine signal and the rectifying circuit. Clearly, a theoretical model that is able to properly describe the behavior of the rectifier from RF to BB is hard to achieve. Conventionally, harmonic balance tools are used to analyze such behavior. However, in a multisine-based WPT, more orders of harmonics and mixing terms are necessary, resulting in significant computational cost [13], not to mention the time cost for constructing different rectifier configurations with corresponding optimized input matching. Specifically, this paper first proposes a time-domain analysis based on the rectifier's key parameters. The adoption of a numerical solver not only speeds up the waveform analysis on one rectifier but also allows the possibility to study different rectifiers. To relax the analysis's complexity, the theoretical model is derived based on the following assumptions.

1) The input reflection coefficient S_{11} involves both the transmission line matching network and the input impedance of the rectifier. Theoretically, if the transmission line matching networks equals the conjugate of the circuit complex impedance, the rectifier is perfectly matched. For validation purposes, we apply the measured S_{11} to the model. Otherwise, we assume perfect input matching, allowing the evaluation of the rectifier's BW, not limited to the input matching.
2) We adopt the Shockley equation to describe the current and voltage curve of the diode. We focus on wireless sensor networks where the received power is very low (under -10 dBm). As a result, the input signal's highest peak is far from the breakdown voltage of the considered diode HSMS2852/SMS7630, which is 3.8 V/2 V.
3) We ignore the parasitic parameters at high frequencies when computing the output dc voltage and PCE with Kirchhoff's circuit law. However, we do include the parasitic effects in the equivalent circuit study. In particular, the parasitic effects explain the voltage enhancement α_v after the matching network. The simulation results show that our approximated model matches measurement results well.

This section is further structured following the functional block diagram as can be seen in Fig. 3, consisting of an input multisine source, a matching network, a one-stage clamper, a rectifying diode, and an output low-pass *RC* filter. First, the multisine signal is defined. Then we model the rectifier with the equivalent circuit as in Fig. 5 to derive the voltage on the rectifying diode. In the end, the rectifying behavior of the diode and the output low-pass *RC* filter is studied.

A. Multisine Signal Representation

We characterize the multisine signals in this section. We are considering an N_t-tone multisine signal of BW BW_{RF}, operating at carrier frequency f_c and at power level P_{in}. At each

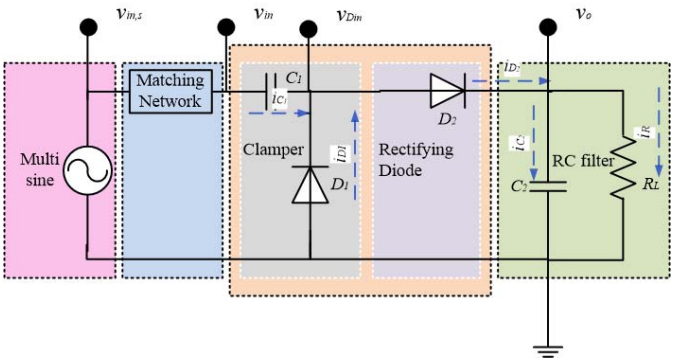


Fig. 3. General rectifier functional block diagram consisting of an RF source, a clamper, a rectifying diode, and an output low-pass *RC* filter.

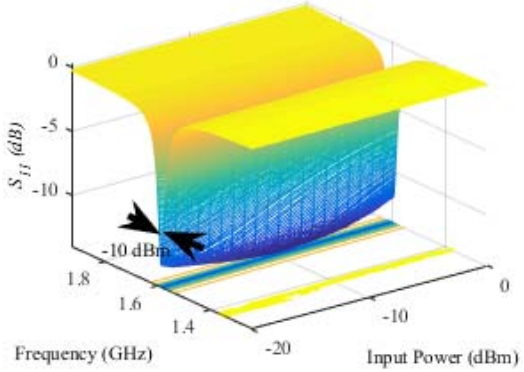


Fig. 4. Measured S_{11} curve of the rectifier under test and the matched BW region as a function of frequency and input power.

tone, a CW of input power (P_{in}/N_t) is created. The source multisine signal $v_{\text{in},s}(t)$ can be expressed as follows:

$$v_{\text{in},s}(t) = \sum_{n=1}^{N_t} v_{\text{am}} \times \cos\left\{2\pi\left[f_c + \left(-\frac{N_t-1}{2}+n-1\right)\Delta f\right]t+\phi_n\right\} \quad (1)$$

where the voltage amplitude, phase of each tone, frequency spacing between tones, number of tones, and time are denoted by $v_{\text{am}} = (2P_{\text{in}}R_{\text{antenna}}/N_t)^{1/2}$, ϕ_n, Δf, N_t, and t, respectively.

Boaventura and Carvalho [10] show that a multisine signal with zero phase difference between the tones generates the highest dc output voltage, which means that we can assume $\phi_n = 0°$ to reduce the complexity of this analysis. Then, this multisine signal can be represented by the envelope $A(t)$ modulated with carrier frequency f_c as $v_{\text{in},s} = A(t)\cos(2\pi f_c t)$.

The signal envelope is given by

$$A(t) = v_{\text{am}}\sin(\pi N_t \Delta f t)\frac{1}{\sin(\Delta f \pi t)}. \quad (2)$$

Looking at (2), the multisine signal envelope $A(t)$ is a periodic function with periodic cycle $\tau = (1/\Delta f)$. The shape of the signal envelope is determined by N_t as it is part of the function $\sin(\pi N_t \Delta f t)$.

For a given BW, the signal PAPR increases with increasing number of tones. But on the other hand, that means that the frequency spacing decreases. Note that if the frequency spacing is too small, the resulting waveform peak frequency is also very low and equal to Δf [19].

B. Return Loss Caused by Matching Network

As the first part of the rectifier, the input matching network of a wireless power receiver should be properly designed to minimize the unnecessary return loss. The circuit is considered as matched when the reflection coefficient $S_{11} = -10$ dB or less.

We measured the S_{11} of the first manufactured rectifier, which is marked as the red diamond mark in Fig. 8, as an example. Fig. 4 shows the measured 3-D S_{11} of the rectifier in both frequency and input power dimensions. As for the frequency dimension, the S_{11} is a quasi-concave curve and reaches the minimum around $f_c = 1.6$ GHz for all input powers from -20 dBm until 0 dBm. Additionally, for the input power dimension, the S_{11} behaves as a concave curve where the lowest point is at -10 dBm. This indicates that the input matching should depend on the input power, because of the variation of the diode input impedance with input power [20].

Thus, for a particular power level, the matching BW BW_m should be adjusted. Considering the -10 dBm input power, BW_m is 16 MHz. This implies RF signals centered at 1.6 GHz within 16 MHz BW are considered as matched for the rectifier under test. Thus, the BW of the multisine signal excitation should be limited to 16 MHz, to keep the input matched. In addition, the input matching network has a strong influence on the input voltage to the circuit v_{in}, which will be demonstrated in Section III-C.

C. Voltage Enhancement in Rectifiers

From empirical measurements of rectifiers, the voltage enhancement after the input matching has been confirmed, yet no study has analyzed this phenomenon in depth. A voltage multiplier is often adopted in rectifiers to enhance the output dc voltage by adding a clamper circuit. Hence, these two factors should not be neglected when estimating the output dc voltage of the rectifier. This paper provides a fundamental theory to calculate the input voltage to the rectifying diode. We provide a theoretical and simulation-based analysis of the voltage enhancement after the input matching and the clamper efficiency. Moreover, the corresponding voltage enhancement coefficient is proposed to represent each voltage enhancement.

The modeling starts from the voltage enhancement after the input matching (from $v_{\text{in},s}$ to v_{in}) based on the equivalent circuit study; then, the real voltage on the diode after the clamper is computed based on Kirchhoff's law (from v_{in} to $v_{D_{\text{in}}}$) as denoted in Fig. 5.

1) Voltage Enhancement After Input Matching: The voltage enhancement of the input matching follows the voltage divider principle. To compute this improvement, it is necessary to calculate the complex impedance of each function block. We represent the rectifier scheme in Fig. 3 as a detailed voltage doubler circuit, assuming high frequencies and including the diode parasitic elements.

The RF signal goes into the rectifier, followed by an input matching network. After the input matching network,

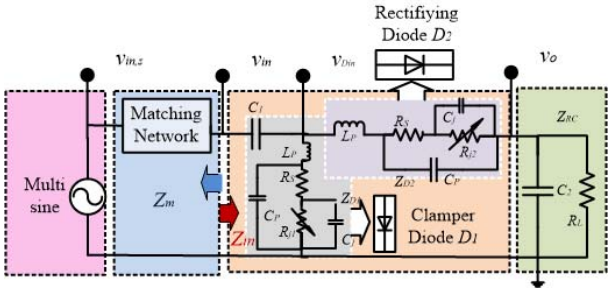


Fig. 5. Equivalent circuit diagram of the voltage doubler rectifier.

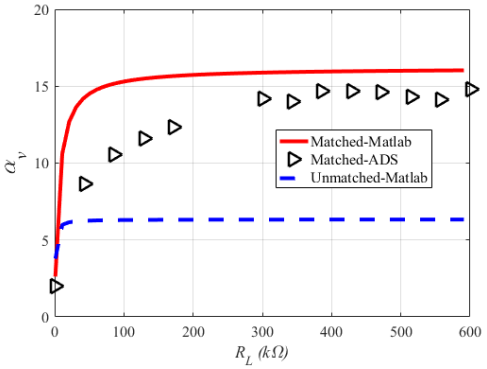


Fig. 6. Voltage improvement coefficient with increasing R_L when inputting a CW signal at −10 dBm.

the capacitor C_1 and D_1 represent the equivalent lumped element circuit of the clamper. Diode D_2 is used to rectify the ac signal. The diode model consists of a junction capacitor C_j, a series resistor R_s, a parasitic inductor L_P, a parasitic capacitor C_P, and a nonlinear resistor R_{ji} for diode i. Since D_1 used in the clamper and the rectifying diode D_2 are from the same series, we assume all parameters in the diode model are the same, except R_{ji} that strongly depends on the voltage applied to the diode. Finally, the output low-pass RC filter consists of the capacitor C_2 and the load R_L.

We denote the transmission line complex impedance by Z_m and the impedance of the circuit seen from the matching network by Z_{in}. The complex impedance of a perfect input matching network is the conjugate of the circuit's complex impedance. Due to the strong capacitive influence in the diodes of the rectifier, the rectifier complex impedance typically has a large imaginary component compared with the real part. Since both the input matching network and the lumped elements have an impedance, the voltage v_{in} seen by the clamper is different than the voltage over the rectifier $v_{\text{in},s}$. Based on voltage divider principle, the input voltage v_{in} after the matching network is computed as

$$v_{\text{in}} = \frac{Z_{\text{in}}}{Z_{\text{in}} + Z_m} v_{\text{in},s}. \tag{3}$$

We denote the amplitude scaling between v_{in} and $v_{\text{in},s}$ by the voltage enhancement coefficient, given by

$$\alpha_v = \left| \frac{Z_{\text{in}}}{Z_{\text{in}} + Z_m} \right|. \tag{4}$$

It should be noted that there exists a phase shift between $v_{\text{in},s}$ and v_{in} since $(Z_{\text{in}}/Z_{\text{in}} + Z_m)$ has a phase. This phase shift is caused by the traveling time of the RF signal pass through the input matching network.

Next, we demonstrate how to derive α_v. First of all, we have to know Z_{in}. Based on Fig. 5, the ith diode impedance Z_{D_i}, RC's impedance Z_{RC}, and the input impedance Z_{in} are computed as the following equations:

$$Z_{D_i} = j\omega L_p + \frac{1}{j\omega C_P + \frac{1}{R_s + \frac{1}{j\omega C_j + \frac{1}{R_{ji}}}}} \tag{5a}$$

$$Z_{RC} = \frac{1}{j\omega C_2 + \frac{1}{R_L}} \tag{5b}$$

$$Z_{\text{in}} = \frac{1}{j\omega C_1} + \frac{1}{\frac{1}{Z_{D_2} + Z_{RC}} + \frac{1}{Z_{D_1}}}. \tag{5c}$$

The junction impedance R_{ji} strongly depends on the diode behavior. In our scheme, the first diode and the second diode are not conducting at the same time. Thus, we adopt a two-phase study: in the negative cycle of the RF signal, the first diode is ON, and the second is OFF, while in the positive cycle, the first diode is OFF, and the second one is ON. The diode behavior is simplified as two modes: the linear mode where the diode junction impedance is constant as R^*_{ji} for a specific input power and the off-mode where R_{ji} is infinitely large. Since the diode used in the clamper circuit is the same as the rectifying diode, we assume that R^*_{ji} is the same as R_j when the ith diode is ON for a specific input power. Thus, the impedance of the diode when it is ON or OFF is

$$Z^{\text{OFF}}_{D_i} = j\omega L_p + \frac{1}{j\omega C_P + \frac{1}{R_s + \frac{1}{j\omega C_j}}} \tag{6a}$$

$$Z^{\text{ON}}_{D_i} = j\omega L_p + \frac{1}{j\omega C_P + \frac{1}{R_s + \frac{1}{j\omega C_j + \frac{1}{R_j}}}}. \tag{6b}$$

If the rectifier is matched, Z_m is the complex conjugate of Z_{in}, and thus $\alpha_v = |(Z_{\text{in}}/2\text{Re}(Z_{\text{in}}))|$. This enhancement is typical for rectifier circuits whose reactance is larger than the resistance, due to the strong capacitive elements in the diode equivalent circuit.

We plot how the voltage enhancement coefficient changes with increasing R_L in Fig. 6. R_L is studied here because it is one of the most important factors determining the output voltage. The simulation parameters are selected to represent one of the four rectifiers we will use in our measurement study, more specifically the rectifier marked by the red diamond in Fig. 8(a). The diode parasitic parameters follow the data sheet of the HSMS-2852 series diodes.

The voltage enhancement coefficient α_v increases with increasing load resistance and saturates around 300 KΩ. This is because the capacitive part of the circuit is fixed. The load resistance reaches the ceiling to improve the input voltage when it is far more than the circuit reactance. The corresponding ADS simulation results (black diamond) confirm the simulated trend. When the rectifier is matched, the voltage enhancement can reach 16; when the rectifier is not perfectly matched, the voltage enhancement is only a factor 2.3.

In practice, the matching network is optimized for a particular power level as illustrated in Section III-B. Thus, the matching network's quality depends on the input power, which will affect the voltage enhancement level.

2) Clamper Voltage Enhancement: After the matching network, a clamper is used to improve the input voltage level further. Looking at Fig. 3, a clamper is used directly after the input matching network. Clamping circuits are used widely in rectifiers to construct voltage multiplier circuits by adding a dc value to the input signal. We investigate the voltage enhancement factor η_C depending on the circuit configuration under study. The ideal clamper exploits the peak negative value of the incoming signal to construct a positive shift of the signal during its positive part, equals to the peak voltage during the negative part. With high PAPR signals, the build-up voltage during the negative part of the signal is lower because the peak negative voltage is present only during a very short time of the entire period. As a result, the clamper voltage enhancement is seriously degraded for high PAPR signals.

Since this analysis has to deal with a time-varying signal, we adopt a time-domain analysis. The parasitic effects of the diode are ignored to relax the mathematical complexity. We denote v_{in}, v_{C_1}, v_{D_1}, i_{C_1}, and i_{D_1} by the input voltage of the clamper, the voltage on the capacitor C_1, the voltage on the diode D_1, the current flowing on C_1, and the current on D_1.

The clamper is activated when D_1 is conducting during the negative cycle of v_{in}, when C_1 is in charging. During the positive cycle of v_{in}, D_1 acts as open circuit and C_1 behaves as a dc voltage source of v_{C_1}. Applying Kirchhoff's law, we derive the equations when D_1 is conducting

$$v_{\text{in}} = v_{C_1} + v_{D_1} \tag{7a}$$

$$i_{C_1} = \frac{dv_{C_1}}{dt} \times C_1 = -i_{D_1} = -I_s\left(e^{\frac{v_{D_1}}{nV_T}} - 1\right) \tag{7b}$$

where $v_{D_{\text{in}}} = v_{D_1}$. I_s, V_T, and n represent the reverse bias saturation current, thermal voltage, and ideality factor, respectively. We define the clamper voltage enhancement factor as an average ratio between the peak of the input voltage $v_{D_{\text{in}}}$ to the rectifying diode with the clamper and the peak of the input voltage v_{in} without the clamper circuit as

$$\eta_C = \frac{\text{peak}(v_{D_{\text{in}}})}{\text{peak}(v_{\text{in}})}. \tag{8}$$

The perfect clamper would move the whole signal to a dc offset, equaling to peak(v_{in}) as built up during the negative input voltage phase. Thus, $\eta_C = 2$ for an ideal CW excited voltage doubler. However, in a multisine-based WPT, the clamper would suffer from the signal low amplitude period, so we expect a lower enhancement.

Fig. 7 shows how η_C changes with increasing the number of tones for the multisine signals with BW_{RF} 10 and 15 MHz. We observe that for both signals, η_C degrades nonlinearly as a function of N_t. For the 10-MHz BW signal, η_C degrades from 1.43 for the two-tone signal to about 1.34 in the case of a 10-tone signal; while for the 15-MHz BW signal, η_C decreases from 1.4 for the two-tone signal to 1.32 for the 10-tone signal. ADS simulation results confirm the decreasing trend with the number of tones, showing even a higher influence since the parasitic effects are included in ADS.

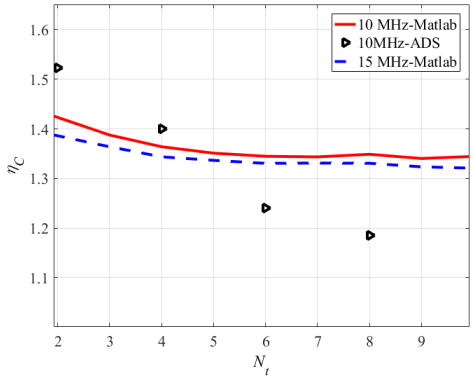


Fig. 7. Clamper voltage enhancement factor as a function of N_t for signal BW of 10 (blue dashed line) and 15 MHz (red solid line) at −10 dBm.

Knowing η_C for each multisine signal, we are able to extend the general rectifier model to a doubler by adding a clamper dc level to the input RF source to derive $v_{D_{\text{in}}}$.

D. Rectifying Behavior Modeling

Obtained the voltage going through the diode, the output dc voltage could be computed by a time-domain analysis on the rectifying circuit including the rectifying diode and the output low-pass *RC* filter.

The basic rectifying circuit configuration consists of a rectifying diode D_2, and the output low-pass filter consisting of a capacitor C_2 and a resistor R_L as in Fig. 3. We denote the multisine input voltage into the diode by $v_{D_{\text{in}}}$, the voltage drop on the diode by v_D, the instantaneous output voltage in time domain by v_o, and the current flowing on the diode, the capacitor, and load resistor by i_{D_2}, i_{C_2}, and i_R, respectively.

We list the equations to compute the dc output voltage applying Kirchhoff's circuit laws as follows:

$$v_D = v_{D_{\text{in}}} - v_o \tag{9a}$$

$$i_{D_2} = i_{C_2} + i_R \tag{9b}$$

where

$$i_{D_2} = I_s\left(e^{\frac{v_D}{nV_T}} - 1\right) \tag{9c}$$

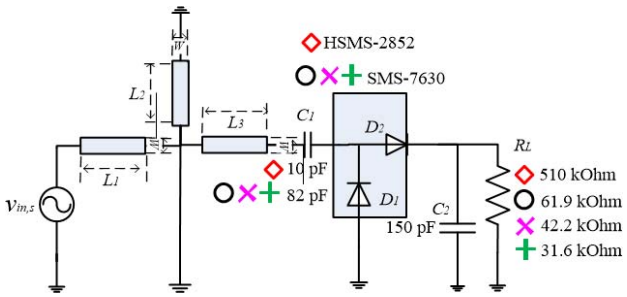
$$i_{C_2} = C_2\frac{dv_o}{dt}, \quad i_R = \frac{v_o}{R_L}. \tag{9d}$$

The nonlinear behavior of the diode is characterized by the Shockley model as (9c). By proper transformation, the equation can be written as an ordinary differential equation (ODE) as

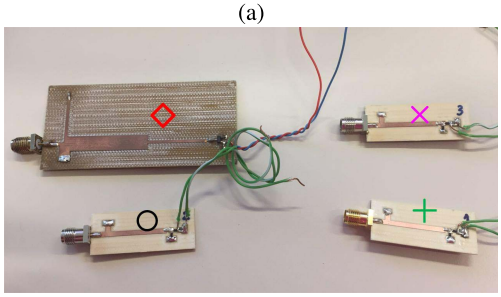
$$\frac{dv_o}{dt} = \frac{i_s}{C_2}\left(e^{\frac{v_{D_{\text{in}}} - v_o}{nV_T}} - 1\right) - \frac{v_o}{R_L C_2}. \tag{10}$$

Clearly, the right-hand side of this ODE function (10) is a nonlinear formula. As a result, the unique analytical solution is very hard or unable to achieve. However, the numerical solution is always achievable using an ODE solver. Having obtained the output voltage in time domain through an ODE solver, the dc output voltage is the local mean value of this slow-varying output voltage

$$V_{\text{DC}} = \frac{1}{T - t_{\text{steady}}}\int_{t_{\text{steady}}}^{T} v_o(t)dt \tag{11}$$



(a)



(b)

Fig. 8. Voltage doublers under test. (a) Lumped element model of the rectifiers with the corresponding parameters. (b) Photograph of the prototyped rectifiers.

where t_{steady} is the starting time of charging steady state and $T = n\tau$ represents the total examined n periods of the output signal. Then the PCE is computed ($V_{\text{DC}}^2/R_L P_{\text{in}}$).

IV. Experimental Validation

We adjust our general circuit model to rectifiers of voltage doubler structure by tuning the parameters following Fig. 8(a), and validate the model by comparing simulation results with measurements. Four rectifiers are constructed to validate the theoretical model. Schottky diodes are used in our design because their zero-bias characteristic provides excellent performance at low input power.

First, we test the accuracy of the model as the function of the output low-pass *RC* filter, since this block mainly limits the BW of the circuit, assuming a high BW input matching network. Second, we provide waveform design insight by analyzing multiple waveforms employing the constructed model. Measurement results confirm the simulation results' reliability. Both simulation and measurement results highlight the importance to consider the multisine-based WPT as a whole, including not only the input signal waveform and also the rectifier circuit BW.

A. Output Low-Pass RC Filter Choice

In this section, the *RC* circuit analysis based on the theoretical model is demonstrated to provide a vision for designing efficient rectifier circuits specifically for WPT system with a predetermined multisine signal. In this case, we assume the WPT system cannot rely on a custom-designed transmitter, and a given multisine waveform has to be considered. In this case, the best strategy is to optimize the *RC* filter for the given waveform parameters. This theoretical analysis can study the influence of the output low-pass *RC* filter, independently of the input matching network. A broad exploration of different circuits is difficult in practice, as each novel *RC* filter instance would require the design of a novel input matching network.

TABLE I
Input Matching Microstrip Parameters

Ref.Des	Value (mm)	Ref.Des	Value (mm)
◯W	1.73	×L_2	4.75
◯L_1	5.33	×L_3	20.33
◯L_2	5.30	+W	1.92
◯L_3	21.13	+L_1	5.53
×W	1.93	+L_2	5.53
×L_1	5.84	+L_3	20.25

Our study started with one voltage doubler as the rectifier denoted by the red diamond marker in Fig. 8 [19]. This rectifier is fabricated on substrate FR4 with a thickness of 0.8 mm and a dielectric constant of 4.3. More details can be found in [21]. Later, three other rectifiers (indicated by a black circle, a pink cross, and a green plus marker, respectively) with the same structure are constructed to validate the theoretical model further. The three rectifiers are fabricated on substrate Isola Astra3 of thickness 0.76 mm and dielectric constant of three. Detailed component parameter values are listed in Fig. 8(a). The corresponding microstrip parameters of the input matching network are listed in Table I. Fig. 8(a) is the lumped element model, while Fig. 8(b) shows the photograph of the prototyped rectifiers. After the input voltage source, transmission lines with different sizes constitute the matching network to reduce return loss. Following the matching network, one capacitor and one diode form the clamper circuit. The ac wave clipped by the clamper passes through the rectifying diode and is filtered by the *RC* circuit at the output. The *RC* circuit has a fixed 150-pF capacitor and varying loads of 510, 31.6, 42.2, and 61.9 kΩ. Schottky diodes are used in all the rectifiers since it has low turn-ON voltage. The original circuit uses the HSMS 2850 diodes, while the others employ the Schottky diodes from series SMS7630. All the rectifiers' matching networks are optimized to 1.6 GHz. Due to the varying R_L, the input impedance Z_{in} is not constant, and therefore each input matching network is optimized separately for each rectifier to achieve complex conjugate matching.

We are mainly interested in the impact of the *RC* filter on the output dc. For *RC* circuits, $f_{\text{cut-off}}$ determines how much the IM2 is suppressed. The output power degrades by 3 dB at $f_{\text{cut-off}}$ and decreases 10 dB per *RC* decade ($2\pi RC$) from the highest level.

We introduce the ratio between Δf and $f_{\text{cut-off}}$ to represent the BW of the circuit and the signal in a single figure. A small value of ($\Delta f / f_{\text{cut-off}}$) indicates a relatively wide *RC* filter, which means that the IM2 is not suppressed.

We simulate a WPT system excited with a two-tone signal of 1 MHz BW. Thus, the frequency spacing Δf is fixed as 1 MHz. Output low-pass *RC* filters with increasing $f_{\text{cut-off}}$ from 1 to 100 kHz are simulated by changing the load resistance. The other parameters correspond to the lumped element model of the three smaller rectifiers, as in Fig. 8.

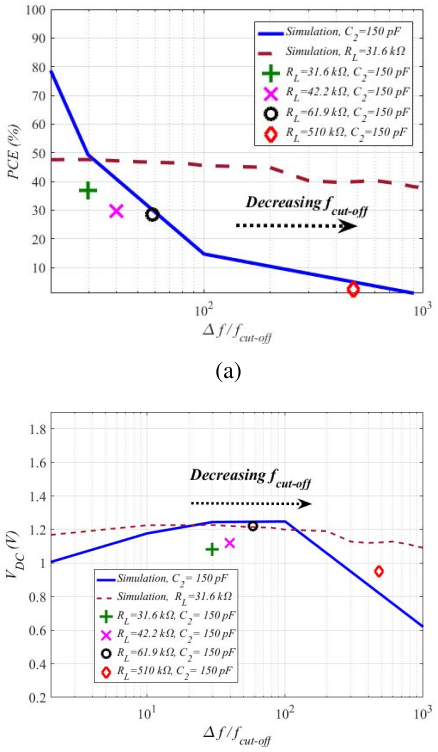


Fig. 9. Simulated and measured (a) PCE of the rectifier and (b) output dc voltage with increasing $(\Delta f/f_{\text{cut-off}})$ of 1-MHz two-tone multisine-based WPT at −10 dBm.

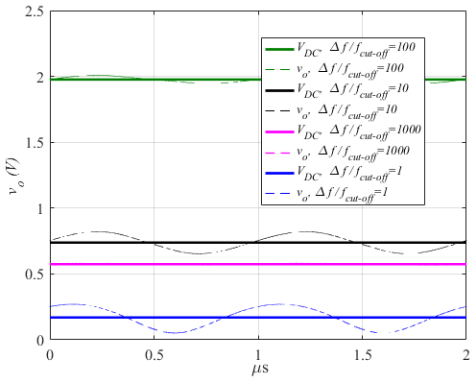


Fig. 10. v_o in time domain with (a) $(\Delta f/f_{\text{cut-off}}) = 1000$, (b) $(\Delta f/f_{\text{cut-off}}) = 100$, (c) $(\Delta f/f_{\text{cut-off}}) = 10$, and (d) $(\Delta f/f_{\text{cut-off}}) = 1$ and of a 1-MHz two-tone multisine-based WPT at −10 dBm in ADS simulations.

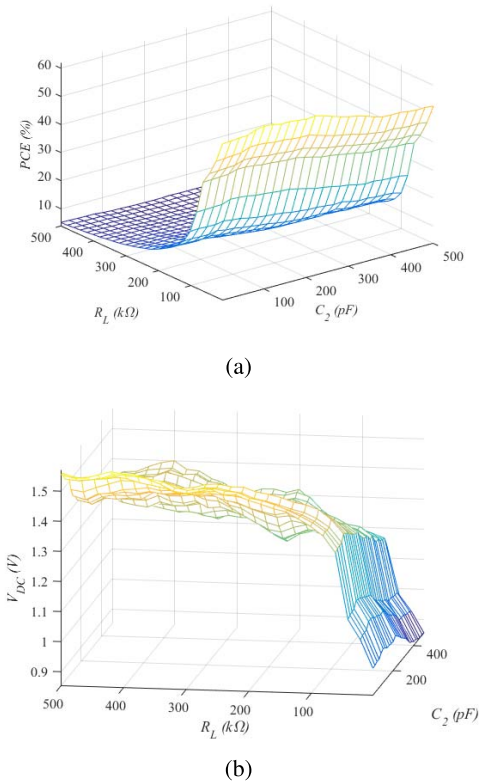


Fig. 11. 3-D simulated (a) PCE of the rectifier and (b) output dc voltage with increasing R_L and C_2 of 1-MHz two-tone multisine-based WPT at −10 dBm.

The blue solid lines in Fig. 9 show how the PCE and voltage change with growing $(\Delta f/f_{\text{cut-off}})$ in simulation. The red diamond, black round, pink cross, and green plus markers represent the measured results corresponding to the voltage doublers in Fig. 8(a), respectively.

To analyze how the *RC* filter influences the rectifier performance, we vary the $(\Delta f/f_{\text{cut-off}})$ by two approaches. The first approach is to fix C_2 to 150 pF and vary load resistance as the blue solid lines indicate. The other is to fix R_L to 31.6 kΩ and vary the *RC* filter capacitor as the brown dashed lines indicate.

First, Fig. 9(a) plots the PCE of the rectifier as a function of increasing $(\Delta f/f_{\text{cut-off}})$. We observe that PCE decreases with increasing $(\Delta f/f_{\text{cut-off}})$ for both simulation and measurement because the IM2 is suppressed more with a larger $(\Delta f/f_{\text{cut-off}})$. The theoretical results are close to the measurement for the three newly constructed circuits (with 61.9, 42.2, and 31.6 kΩ load resistance and 150-pF capacitor within 5% difference). The simulation results show that the load resistance (the blue solid line) has a stronger impact on PCE than the capacitor (the brown dashed line). Then, Fig. 9(b) plots how the output dc voltage varies with rising $(\Delta f/f_{\text{cut-off}})$. V_{DC} first increases until it reaches the maximum around $(\Delta f/f_{\text{cut-off}}) = 100$ and then decreases. This concave behavior is illustrated further by looking at the instantaneous output voltage for different $(\Delta f/f_{\text{cut-off}})$ as in Fig. 10. The simulation difference compared with measurement is under 0.1 V. The measurements confirm the validity of our model that there is a strong influence of the *RC* filter on the performance of a rectifier excited by a multisine. In addition, the simulation result of varying capacitor behaves flatter compared with the result of varying load resistance. In Fig. 10, it is observed that with the increase of $(\Delta f/f_{\text{cut-off}})$, the v_o curve becomes smoother since a narrower output low-pass *RC* filter is applied and IM2 is suppressed more. The highest v_o curve occurs when $(\Delta f/f_{\text{cut-off}}) = 100$. Fig. 10 justifies that a too wide output low-pass *RC* filter suffers from too much time variance while a too narrow output low-pass *RC* filter would remove too much IM2 power. In both cases, the dc output voltage will be lowered.

To further explore how different *RC* combinations would influence the PCE and the output dc voltage, we plot

3-D figures showing the PCE and V_{DC} trend as a function of load resistance and capacitor of the *RC* filter in Fig. 11. We can observe from Fig. 11(a) that the PCE decreases with both increasing R_L and C_2 since the *RC* filter becomes narrower thus more IM2 is removed. Fig. 11(b) shows that there is an optimal value for both R_L and C_2 since $(\Delta f / f_{\text{cut-off}})$ has an optimal value, which also corresponds to the result in Fig. 9(b). Both PCE and V_{DC} are impacted more by the load than the capacitor in the *RC* filter. This is because the load resistance has a stronger influence on the dc component while the capacitor influences the IM2 more, which is smaller than the dc. Thus, we propose to first choose the load resistance depending on the output dc voltage requirement; then the capacitor is chosen based on the optimal $(\Delta f / f_{\text{cut-off}})$.

In conclusion, it is possible to improve the PCE of the rectifier and output dc voltage by adjusting the *RC* filter based on the optimal $(\Delta f / f_{\text{cut-off}})$ value. To achieve a higher PCE, a smaller value of $(\Delta f / f_{\text{cut-off}})$ is necessary, indicating a wider *RC* filter; to have the highest output dc voltage, the optimal $(\Delta f / f_{\text{cut-off}})$ is around 100 in this case.

B. Waveform Design

In this section, we analyze the impact of the input signal BW, for a given circuit. By this approach, the optimal transmit multisine waveform can be designed based on the circuit cut-off frequency. All measurements and simulations are performed on the second, third, and fourth rectifier, which marked as the black circle, pink cross, and green plus as in Fig. 8. In practice, the signal power level is usually very low, typically under -10 dBm due to the transmission regulation and the path loss. Thus, we aim at choosing the proper multisine signal BW and the number of tones to achieve highest RF-dc conversion efficiency. The measured S_{11} mask of each rectifier is considered.

As the first step, we vary the signal BW for given N_t and input power of -10 dBm. Since the load resistance is fixed for each rectifier, the PCE depends only on the output dc voltage, e.g., $\mathrm{PCE} = (V_{\mathrm{DC}}^2 / R_L P_{\mathrm{in}})$.

Fig. 12(a) shows how the PCE of the rectifier varies with increasing signal BW. It is observed that there exists an optimal BW value to achieve the highest PCE for all the three circuits. Moreover, the circuit with 31.6 kΩ generally has the highest PCE, corresponding to the result in Fig. 9(a).

Fig. 12(b) plots the simulation and measurement results of the output dc voltage as a function of increasing signal BW. It is observed, e.g., for the second rectifier with 61.9-kΩ load, that V_{DC} grows from 0.8 to 1.2 V and then slightly decreases after 4 MHz. It is clear that V_{DC} first increases because the high power peaks appear more frequently in the time domain. The output dc voltage decreases because $(\Delta f / f_{\text{cut-off}})$ is too large indicating a very narrow *RC* filter removing all IM2. Fig. 12 shows that the influence of BW is higher for the model than seen in the measurements. The main reason for the discrepancy between the simulation and measurement result is the use of the Shockley equation as to keep the model formulation general, as opposed to using a more complicated diode current model tailored to the actual physical behavior of the diode used

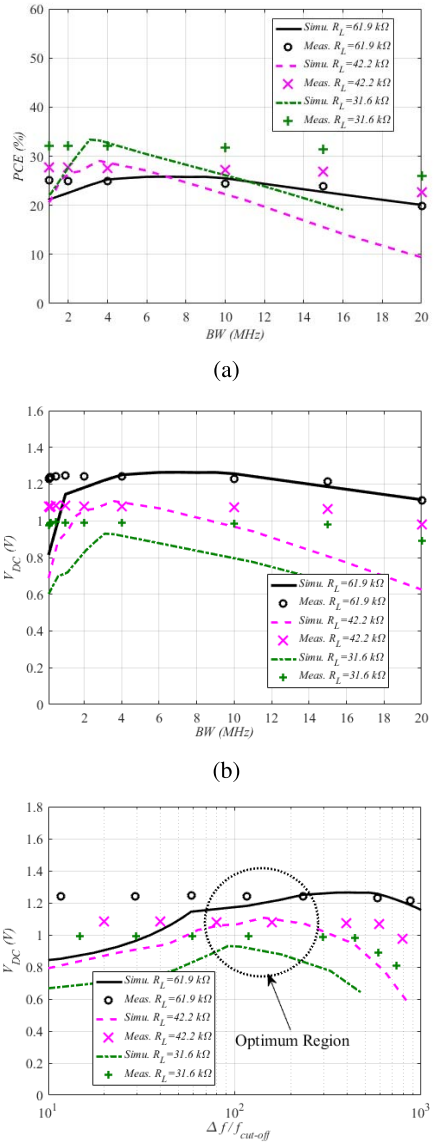


Fig. 12. Simulated and measured (a) PCE, (b) output dc voltage with increasing BW, and (c) V_{DC} with increasing $(\Delta f / f_{\text{cut-off}})$ of multisine-based WPT with fixed $N_t = 2$ at -10 dBm.

in the experimental boards as in the Shockley diode HSMS 2850 data sheet. In addition, the model is further simplified relative to models in commercial microwave simulators, as the model in this paper does not include the RF model elements, i.e., the junction capacitor, resistor, and the parasitic packaging effects. All of the three circuits show the maximum output dc voltage occurs when $f_{\text{cut-off}}$ is around 100–200 as in Fig. 12(c).

In another way, we studied how to select the optimal number of tones when the signal BW is fixed. The change of N_t not only changes the signal PAPR but also alters the frequency spacing between the neighboring tones.

Fig. 13 shows how the PCE varies with the increase in the number of the tones for the three rectifiers. It is shown that there is an optimal value of N_t for each rectifier. Besides, the circuit with $R_L = 31.6$ kΩ has the highest PCE in average. Within the input matching BW 10 MHz, V_{DC} first increases

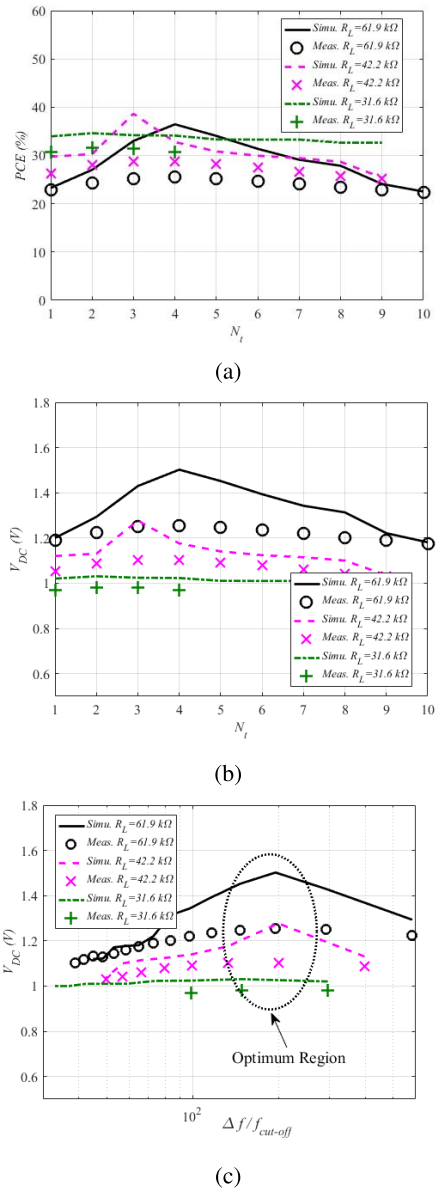


Fig. 13. Simulated and measured (a) PCE, (b) output dc voltage with increasing N_t, and (c) V_{DC} with increasing $(\Delta f/f_{\text{cut-off}})$ of multisine-based WPT with fixed $\mathrm{BW_{RF}} = 10$ MHz at -10 dBm.

in both simulation and measurement, since higher PAPR is generated as can be seen in Fig. 13(b). Afterward, V_{DC} decreases, because the frequency spacing is too small causing a long period between the neighboring peaks. In this case, the time-domain output voltage of the low-pass *RC* filter has very long discharging time. In other words, IM2 is not handled well by the output low-pass *RC* filter. By checking Fig. 13(c), the optimal $(\Delta f/f_{\text{cut-off}})$ is around 100–200.

With this insight, the optimal Δf can be determined based on the optimal value of $(\Delta f/f_{\text{cut-off}})$ when the values of *RC* are known. Besides, the frequency spacing between the tones is up bounded by the input matching BW BW_m and the number of tones as $\Delta f \leq (\mathrm{BW}_m/N_t - 1)$.

In short, the theoretical model we constructed can predict output dc behavior due to different multisine excitations depending on the circuit. The essential relation between the signal waveform and circuit's influence on the output dc is validated by both circuit and waveform study.

V. Conclusion

In this paper, we propose a model to analyze the impact of signal and circuit BW on the RF-dc conversion efficiency of multisine signals.

A numerical solution is achieved for a general rectifier circuit by solving a simple and clear ODE function. By adapting the model with S_{11} mask and equivalent circuit model, we show that our model could approximate a voltage doubler within 0.2 V voltage error and 0.1 PCE error at low input RF power, i.e., -10 dBm.

Moreover, our model is able to analyze the output low-pass *RC* filter in an isolated way without interference of the input matching network. We showed how different *RC* filter designs would influence the dc output for a multisine-based WPT system. The essential relations of multisine signal and the output low-pass *RC* filter are investigated by looking at the ratio between the multisine signal's frequency spacing and the output low-pass *RC* filter's cut-off frequency.

Multisine signals can improve the WPT system performance at low input power if the frequency-spacing between the neighboring tones is properly selected. Based on the model constructed in this paper, we are able to improve the PCE by selecting the optimal frequency spacing by tuning the signal's BW or the number of tones with a fixed rectifier circuit.

The optimal $(\Delta f/f_{\text{cut-off}})$ answers the question how much the IM2 component should be suppressed by the *RC* filter to achieve the maximal output dc voltage or PCE. This paper has not studied how the optimal $(\Delta f/f_{\text{cut-off}})$ would be influenced by the rectifier topology, e.g., adding more diodes. As the optimal $(\Delta f/f_{\text{cut-off}})$ depends on the IM2 level after the rectifying diode, the optimal $(\Delta f/f_{\text{cut-off}})$ might be larger since IM2 will increase with more diodes in the rectifier. In addition, the influence of the input power on the optimal $(\Delta f/f_{\text{cut-off}})$ was not addressed in this paper. The input power would influence the IM2 level because of the nonlinearity of the diode. However, how much IM2 would increase with a higher input power or more diodes still needs careful analysis depending on the diode characteristics. The two questions mentioned above would be interesting for future study.

Overall, we justified multisine-based WPT can be improved by proper output low-pass *RC* filter and waveform designing. Our model can also give insight in the region where multisine power transfer is optimal, and how it depends on the circuit properties. The signal waveform and rectifier circuit interact with each other. Thus, studying the multisine-based WPT considering both the hardware and software is vital.

Acknowledgment

The authors would like to thank A. J. S. Boaventura, High-Speed Measurements Group, NIST, for the support in initial measurement.

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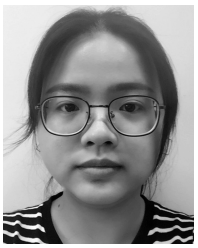

Ning Pan (S'16) was born in Dongyang, China, in 1989. She received the B.Sc. degree in electronic and information engineering from Harbin Engineering University, Harbin, China, in 2011, with a specialization in underwater acoustics, and the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2014. She is currently pursuing the Ph.D. degree in electrical engineering at the Katholieke Universiteit Leuven, Leuven, Belgium.

Her current research interests include simultaneous wireless information and power transfer, nonlinear device modeling, resource allocation, and green networks.

Dr. Pan was a recipient of the Best Student Paper Award of WPTC 2017.

Daniel Belo (S'16) received the M.Sc. degree in electronics and telecommunications engineering from the University of Aveiro, Aveiro, Portugal, in 2014, where he is currently pursuing the Ph.D. degree.

Since 2013, he has been a Researcher with the Instituto de Telecomunicaes, Aveiro. His current research interests include microwave electronic circuits, wireless power transmission, and analogue/digital control.

Mohammad Rajabi (S'15) was born in Esfahan, Iran. He received the master's degree in electronics and information technology from Vrije Universiteit Brussel, Brussels, Belgium, in 2013. He is currently pursuing the Ph.D. degree at the Katholieke Universiteit Leuven, Leuven, Belgium.

Since 2013, he has been with the TELEMIC Division, Departement Elektrotechniek-ESAT, Katholieke Universiteit Leuven. His current research interests include RF circuit design, measurement, and modeling of high-frequency measurement equipment, and simultaneous wireless information and power transfer.

Dominique Schreurs (S'90–M'97–SM'02–F'12) received the M.Sc. degree in electronic engineering and Ph.D. degree from the Katholieke Universiteit Leuven, Leuven, Belgium.

She is currently a Full Professor with KU Leuven. She has been a Visiting Scientist with Agilent Technologies; ETH Zurich, Zürich, Switzerland; and the National Institute of Standards and Technology, Gaithersburg, MD, USA. Her current research interests include the microwave and millimeter-wave characterization and modeling of active devices and bioliquids, as well as the system design for wireless telecommunications and biomedical applications.

Prof. Schreurs was an IEEE MTT-S Distinguished Microwave Lecturer and the Editor-in-Chief of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. She was the General Chair of the 2007, 2012, and 2018 ARFTG Conference. She was the Co-Chair of the European Microwave Conference in 2008. She is currently serving on the AdCom of the IEEE MTT-S. She is the Chair of IEEE MTT-S Meetings and Symposia Committee. She serves as the Vice-President of the Executive Committee of the ARFTG organization.

Nuno Borges Carvalho (S'97–M'00–SM'05–F'15) was born in Luanda, Angola, in 1972. He received the Diploma and Ph.D. degrees in electronics and telecommunications engineering from the University of Aveiro, Aveiro, Portugal, in 1995 and 2000, respectively.

He is currently a Full Professor and a Senior Research Scientist with the Institute of Telecommunications, University of Aveiro. He has recently been involved in the design of dedicated radios and systems for newly emerging wireless technologies. He co-authored *Intermodulation in Microwave and Wireless Circuits* (Artech House, 2003), *Microwave and Wireless Measurement Techniques* (Cambridge Univ. Press, 2013), and *White Space Communication Technologies* (Cambridge Univ. Press, 2014). He has authored over 200 papers in magazines and conferences and was also a reviewer for those papers. He is the co-inventor of six patents. His current research interests include software-defined radio front-ends, wireless power transmission, nonlinear distortion analysis in microwave/wireless circuits and systems, and measurement of nonlinear phenomena.

Dr. Borges Carvalho was the recipient of the 1995 University of Aveiro and the Portuguese Engineering Association Prize for the best 1995 student at the University of Aveiro, the 1998 Student Paper Competition (Third Place) of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium, and the 2000 IEE Measurement Prize. He was an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He was the Chair of the IEEE Portuguese Section and MTT-11 and also with the Technical Committees, MTT-24, and MTT-26. He is the Chair of the IEEE MTT-20 Technical Committee. He is also the Vice-Chair of the URSI Commission A (Metrology Group). He is an Associate Editor of *IEEE Microwave Magazine* and the *Cambridge Wireless Power Transfer Journal*.

Sofie Pollin (S'02–M'06–SM'13) received the Ph.D. degree (Hons.) from Katholieke Universiteit Leuven, Leuven, Belgium, in 2006.

From 2006 to 2008, she continued her research on wireless communication, energy-efficient networks, crosslayer design, coexistence, and cognitive radio with the University of California at Berkeley, Berkeley, CA, USA. In 2008, she joined the Green Radio Team, Imec, as a Principal Scientist. Since 2012, she has been a Tenure Track Assistant Professor with the Electrical Engineering Department, KU Leuven. Her current research interests include networked systems that require networks that are ever more dense, heterogeneous, battery powered, and spectrum constrained.

Prof. Pollin is a BAEF and Marie Curie Fellow.