A Model for μ-Power Rectifier Analysis and Design

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***Abstract*—This paper proposes a linear two-port model for an N-stage modified-Greinacher full-wave rectifier. It predicts the overall conversion efficiency at low power levels where the diodes are operating near their threshold voltage. The output electrical behavior of the rectifier is calculated as a function of the received power and the antenna parameters. Moreover, the two-port parameter values are computed for particular input voltages and output currents for the complete N-stage rectifier circuit using only the measured I–V and C–V characteristics of a single diode. To validate the model a three-stage modified-Greinacher full-wave rectifier was realized in an silicon-on-sapphire (SOS) CMOS 0.5-μm technology. The measurements are in excellent agreement with the values calculated using the presented model.**

***Index Terms*—Micropower, model, rectenna, rectifier, wireless power transmission.**

I. Introduction

SINCE Tesla's experiences on wireless power transmission (WPT), there has been more than one century of research. Especially after 1958, applications concerning high-power transmission such as solar-powered satellite-to-ground systems (SPS) [1] and helicopter powering have been developed. Typical efficiency of those systems is about 85% at lower microwave frequencies (<2.45 GHz).

In the mid-1980s [2], radio frequency identification systems (RFID) appeared. In these systems, an inductive or electromagnetic coupling antenna is used as both power transmission and communication link. Other applications of WPT include biomedical implants with passive telemetry as a communication link [3]. More recently, the recycling issue of the ambient microwave energy was addressed [4].

Considering today's typical regulations, the monolithic cascaded rectifier is a viable candidate for short range micropowered devices. RFIDs make extensive use of such a power supply both in the low frequency range and in the UHF range. Working range of about 15 m is announced by industrials [5] for an emitted power of 30 W at 869 MHz or 915 MHz (U.S. licensed site). Wireless distributed sensor networks could also benefit from such a technology, e.g., for automatic tire temperature or pressure control [6]. Microbatteries, e.g., thin-film lithium ion cells, could store energy during idle time or a dedicated frequency band could be used (as proposed by the ITU [7]) to supply the necessary power to a sensor when demanded.

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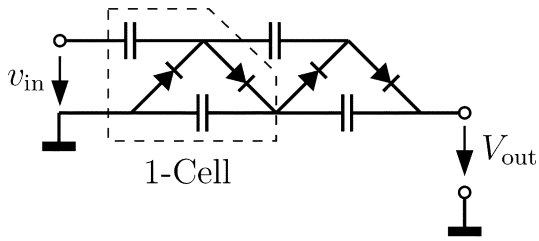

Fig. 1. Two-stage Greinacher half-wave rectifier.

The data obtained could then be captured using typical RFID communication techniques, e.g., backscattering [8].

The μ-power rectifier has not been extensively studied [9]–[11] and, in the aforementioned applications, the realm in which the available voltages are near the diodes' threshold voltages cannot be neglected. To address this issue and in order to ease the design of WPT systems, a steady-state-based model in the time domain to analyze and predict the behavior of multistage rectifying circuits for micropower applications is presented in this paper. In addition to this, a web based interface [12] has been developed to evaluate a diode (or diode-connected transistor) performances for rectifying purposes.

II. Analysis of Rectifying Circuits

A typical Greinacher structure is shown in Fig. 1. For a given sinusoidal signal of about 200 mV, it is possible to obtain a relatively high output voltage (1–2 V) using low-threshold voltage and low-reverse-current diodes and capacitors. Furthermore, these values depend on the received power, the dc output current delivered to the load, and the impedance matching quality between the antenna and the rectifier's input.

In order to decrease the capacitor losses along the RF path (see Fig. 1), this structure can be slightly (see Fig. 2). The Greinacher rectifier is first symmetrized and then the capacitors are rearranged so that every rectifying diode is excited with the same input signal amplitude. The difference between the two structures is a smaller input impedance for the second one, that can be of great benefit when dealing with the antenna impedance matching issue. Moreover, the modified structure reduces the reflected harmonic content thanks to its symmetry. To achieve a higher output voltage, the structure can easily be cascaded.

A. Introduction to the Model

The rectifier presents an input impedance $R_{\text{in}} \parallel C_{\text{in}}$ whose real part diminishes when I_{out} raises, whereas the imaginary part comes from the parasitic capacitors associated to the diodes

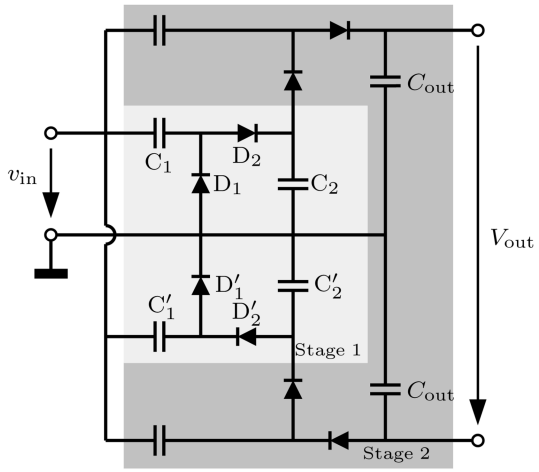

Fig. 2. Two-stage modified-Greinacher full-wave rectifier.

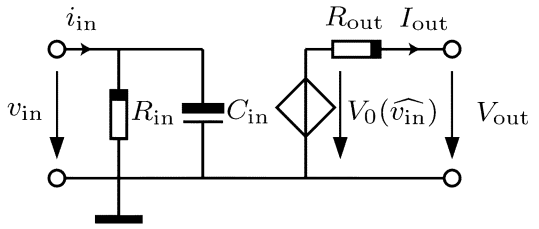

Fig. 3. Rectifier equivalent circuit.

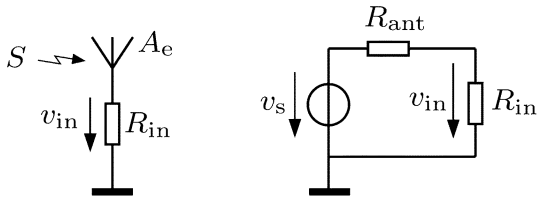

Fig. 4. Antenna equivalent circuit.

and the layout. An output resistor R_{out} and a controlled voltage source are added (Fig. 3).

The input resistance R_{in} is connected to a receiving antenna that supplies a power $P_{\text{AV}} = SA_{\text{e}}$, where S is the power density at the antenna and A_{e} is its effective aperture (see Fig. 4 left). A lossless antenna can be modeled as an equivalent voltage v_{s} in series with a radiation resistance R_{ant}. In the power-match case, the load resistance R_{in} completely absorbs the power available from the antenna P_{AV}. Furthermore, in this case, the voltage v_{in} is equal to the half of the source voltage amplitude v_{s} and is given by

$$v_{\text{s}} = 2\sqrt{P_{\text{AV}} R_{\text{ant}}}. \tag{1}$$

The *peak voltage amplitude* $\widehat{v_{\text{in}}}$ at the input of the rectifier is then calculated as [1]

$$\widehat{v_{\text{in}}} = \sqrt{2} v_{\text{in}} = 2\sqrt{2 R_{\text{ant}} P_{\text{AV}}} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{ant}}}. \tag{2}$$

[1]The input capacitor is not taken into account for the moment; this issue is addressed in the *antenna and matching issues* subsection.

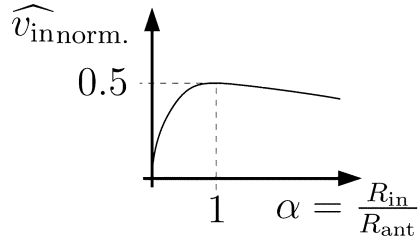

Fig. 5. Normalized input voltage. When R_{in} is bigger than R_{ant}, $\widehat{v_{\text{in}}}_{\text{norm.}}$ decreases slowly.

As the diodes are sensitive to the voltage at their terminals, the amplitude $\widehat{v_{\text{in}}}$ should be maximized. Hence, *power matching at a high impedance level is essential*.

Since R_{in} decreases as I_{out} increases, there is an issue about the choice of R_{in} optimal value to power-match R_{ant}. To answer this, the factor $\alpha = R_{\text{in}}/R_{\text{ant}}$ is introduced and $\widehat{v_{\text{in}}}$ is normalized to $2\sqrt{2R_{\text{in}}P_{\text{AV}}}$

$$\widehat{v_{\text{in}}}_{\text{norm.}} = \frac{\sqrt{\alpha}}{\alpha + 1}. \tag{3}$$

In order to keep $\widehat{v_{\text{in}}}$ at a sufficiently high level when mismatch between R_{ant} and R_{in} occurs, it is more efficient [see (3) and Fig. 5] to power match R_{ant} to R_{in} when the output current I_{out} is maximum, i.e., when R_{in} is minimum. By doing so, when R_{in} increases $\widehat{v_{\text{in}}}$ will be less influenced. It should be mentioned that when $\widehat{v_{\text{in}}}_{\text{norm.}}$ is denormalized, the amplitude $\widehat{v_{\text{in}}}$ reaches a maximum when R_{in} approaches infinity, but the absorbed power by the rectifier simultaneously approaches 0.

B. Analysis Strategy

Rectifiers are essentially nonlinear circuits in their nature due to the presence of diodes. It is a difficult task to analyze them in the time domain during their startup. However, we model these circuits in the steady state as a constant input impedance (R_{in} and C_{in} for a constant input voltage amplitude $\widehat{v_{\text{in}}}$ and a constant output current I_{out}), a constant output resistor (R_{out} for a constant input voltage amplitude $\widehat{v_{\text{in}}}$, and a constant output current I_{out}) and an output voltage source V_0 (see Fig. 3). R_{in}, R_{out} and C_{in} are controlled as we will demonstrate by both the output current I_{out} and the input sinusoidal voltage peak $\widehat{v_{\text{in}}}$, whereas V_0 depends only on $\widehat{v_{\text{in}}}$. In other words, the input current, which is pulsed, is transformed into an equivalent sinusoidal input current that induces an identical power transfer. Finally, using the model, we derive the characteristic charts relating the received power and the antenna (or generator) radiation resistor R_{ant} to the output power consumption of a complete WPT system for micropower applications.

After the transient mode, the rectifier enters the steady-state mode. The circuit operates in a very symmetrical fashion of which we take advantage for the analysis.

For the present paper, the following assumptions are made.

1) The rectifier operates in steady-state mode.
2) The output current is constant.
3) All the diodes are identical.

4) The coupling capacitors are considered as short-circuits at the frequency of analysis.[2]

In Sections III and IV, the ideal case where all elements are lossless and the real case are studied.

III. Ideal Case

A one-stage rectifier based on ideal diodes is considered, i.e., 0-V threshold voltage, no reverse current and infinite conductance in forward mode. The working principle is the following. Capacitor C_1 and diode D_1 (Fig. 2) shift the voltage $v_{\rm in}(t)$ up at B, as C_1' and D_1' shift the voltage $v_{\rm in}(t)$ down at B$'$. Diode D_2 and capacitor C_2 rectify the voltage at B (ac and dc components), as D_2' and C_2' rectify the voltage at B$'$. After the transient, equilibrium is reached and the circuit enters its steady-state mode. In this mode, the rectifier delivers a constant output current $I_{\rm out}$ and a constant output voltage $V_{\rm out}$.

A. Steady-State Solution of the Ideal Rectifier

For $I_{\rm out}=0$ and according to steady-state analysis, the value of $R_{\rm in}$ and $C_{\rm in}$ are computed (see Fig. 3). In the case where the input voltage source $v_{\rm in}$ is an ideal alternating voltage source, the continuous output voltage $V_{\rm out}$ is equal to $4\widehat{v_{\rm in}}$. The circuit is indeed symmetrical, and since the output voltage is continuous, and the voltage applied to the diodes contains an alternative component, the only possible steady-state solution for the voltage on the diodes is

$$\begin{aligned} v_1(t) &= -\widehat{v_{\rm in}} + v_{\rm in}(t) \quad v_2(t) = -\widehat{v_{\rm in}} - v_{\rm in}(t) \\ v_1'(t) &= -\widehat{v_{\rm in}} + v_{\rm in}(t) \quad v_2'(t) = -\widehat{v_{\rm in}} - v_{\rm in}(t) \end{aligned} \tag{4}$$

leading to

$$V_{\rm out} = -v_1(t) - v_2(t) - v_1'(t) - v_2'(t) = 4\widehat{v_{\rm in}}. \tag{5}$$

In the case of the N-stage version, all the diodes are driven with the voltage expressed in (4). The output voltage for an N-stage configuration is

$$V_{\rm out} = 4N\widehat{v_{\rm in}}. \tag{6}$$

When an output current $I_{\rm out}$ is delivered to a load, it tends to discharge C_2 (and likewise C_2') which recharges rapidly through D_2 (and D_2') at every positive (and, respectively, negative) alternation of $v_{\rm in}$. In steady state, the charge quantity pulsed by the current $i_2[t]$ compensates exactly the one drawn off by $I_{\rm out}$. We have at equilibrium (see node C on Fig. 6)

$$\int_0^T i_2[t]dt = \int_0^T I_{\rm out}dt + \underbrace{\int_0^T i_{C_2}[t]dt}_{=0} \Rightarrow \int_0^T i_2[t]dt = I_{\rm out}T \tag{7}$$

and for $i_2'[t]$

$$\int_0^T i_2'[t]dt = I_{\rm out}T.$$

[2]The value of the output or charging capacitors affects the output voltage swing caused by an output current spike. Their value is thus determined as a tradeoff between the output current swing and the maximal allowed output voltage drop. The capacitors are also limited in size by the total charging time.

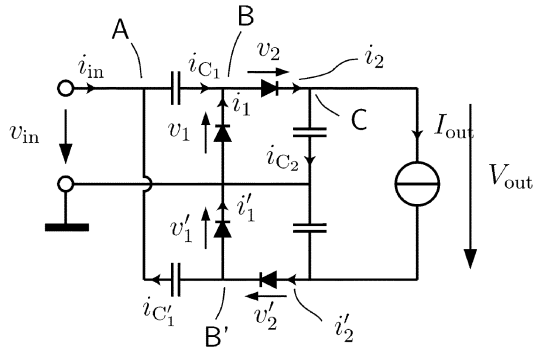

Fig. 6. One-stage full-wave rectifier.

During the recharge of C_2 (or C_2'), diode D_1 (or D_1') is reverse biased and the current $i_2[t]$ can only come from C_1 (or C_1'). This capacitor thus accumulates the same charge quantity $I_{\rm out}T$ which is released at the next negative (or positive) peak through D_1 (or D_1'). We also have

$$\int_0^T i_1[t]dt = \int_0^T I_{\rm out}dt + \underbrace{\int_0^T i_{C_1}[t]dt}_{=0}$$

$$\Rightarrow \int_0^T i_1[t]dt = I_{\rm out}T \tag{8}$$

and for $i_1'[t]$

$$\int_0^T i_1'[t]dt = I_{\rm out}T.$$

Expressions (7) and (8) represent the equations of the rectifier that we use to compute the steady-state solutions throughout the paper.

In steady state, (7) and (8) are valid for all diodes of an N-stage rectifier. In order to sustain an output current $I_{\rm out}$, every diode lets flow over one period of signal the charge quantity $I_{\rm out}T$. (They operate like a water-bucket chain.) The next step is to determine $R_{\rm in}$ in order to address the antenna impedance matching issue.

B. Determination of $R_{\rm in}$

Due to the nonlinear behavior of the diodes, the current that enters the rectifier is pulsed. *The input impedance is thus not constant*. Nevertheless, our goal is to model the input of the rectifier using a *time constant* input resistor $R_{\rm in}$ which represents the mean power $\overline{P_{\rm in}}$ that enters the rectifier during one period of signal $v_{\rm in}(t)$, i.e.,

$$\overline{P_{\rm in}} = \frac{1}{T}\int_0^T v_{\rm in}(t)i_{\rm in}(t)dt. \tag{9}$$

By doing so, we convert the pulsed input current to a sinusoidal current

$$i_{\rm in,sin}(t) = \frac{v_{\rm in}(t)}{R_{\rm in}} = \frac{\widehat{v_{\rm in}}\sin\omega t}{R_{\rm in}}. \tag{10}$$

In the ideal case, the rectifier is nondissipative. As a consequence, the power that enters the network is equal to the dc power delivered to the load $P_{\rm dc}$ and written as

$$\overline{P_{\rm in}} = P_{\rm dc} = V_{\rm out} I_{\rm out}. \tag{11}$$

Using (6), we get for an N-stage ideal rectifier

$$\frac{\widehat{v_{\rm in}}^2}{R_{\rm in}} \int_0^T \sin^2 \omega t dt = 4N\widehat{v_{\rm in}} I_{\rm out} \Rightarrow R_{\rm in} = \frac{\widehat{v_{\rm in}}}{8NI_{\rm out}}. \tag{12}$$

To take into account the imperfections of the diode, e.g., reverse current, threshold voltage, etc., we need to consider the real current-voltage (I–V) characteristic of the diodes. Furthermore, the calculation of $R_{\rm out}$ and $C_{\rm in}$ makes more sense in the real case studied in Section IV.

IV. Real Case

The preceding study shows that once the steady-state equilibrium is reached, every diode sees at its terminals the input signal $v_{\rm in}(t)$ (or $-v_{\rm in}(t)$) shifted up a constant voltage $\overline{V_D}$ equal to $\widehat{v_{\rm in}}$ if all diodes are ideal.

The real case only differs in that the voltage on each diode at equilibrium $\overline{V_D}$ isn't equal to $\widehat{v_{\rm in}}$ anymore. It is calculated as a function of $\widehat{v_{\rm in}}$ for a given output current $I_{\rm out}$.

A. Steady-State Solution

In the real case, $\overline{V_D}$ is necessarily smaller than $\widehat{v_{\rm in}}$, which allows the crossing of the diodes' threshold voltage during every charge cycle in C_1 and C_2. Since the circuit operates in the steady-state mode, the balance of charges entering and leaving the capacitor C_2 equals zero. This remark is also valid for C_1. Equations (7) and (8) are still valid and the output voltage $V_{\rm out}$ stabilizes at

$$V_{\rm out} = 4N\overline{V_D}. \tag{13}$$

The value of $\overline{V_D}$, trivial in the ideal case, is obtained in the real case by solving the following equation:

$$\int_0^T i_D\left[v_D(t)\right] dt = I_{\rm out} T \tag{14}$$

where $v_D(t) = \overline{V_D} \pm \widehat{v_{\rm in}} \sin \omega t$ is the voltage that appears on every diode of the network at equilibrium and i_D is the current that flows through each diode.

There is not a sufficiently accurate continuous model to cope with every operating mode of the diode, i.e., from the reversed bias mode up to the weak and strong inversion conditions. Furthermore, experiments we carried out show that only extracted I–V characteristics (simulations or measurements) are able to predict the behavior of rectifiers at low input power levels. The problem has to be addressed using a numerical method based on the dc I–V characteristics extracted from measurements or simulations of a real world device. Typical measured I–V curves (Fig. 7) are shown in Fig. 8 for a diode-connected low-threshold voltage transistor fabricated in the SOS fully depleted UTSi process [13]. In the calculations that follow, we use the $10\ \mu\text{m} \times 0.5\ \mu\text{m}$ diode which offers better performance.

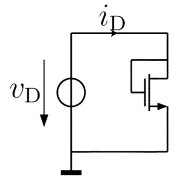

Fig. 7. Measurement setup for the I–V curves extraction of the diode-connected transistor.

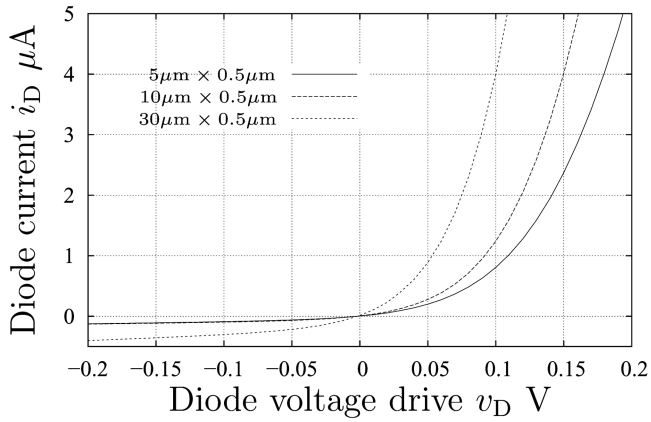

Fig. 8. I–V characteristics of typical measured devices.

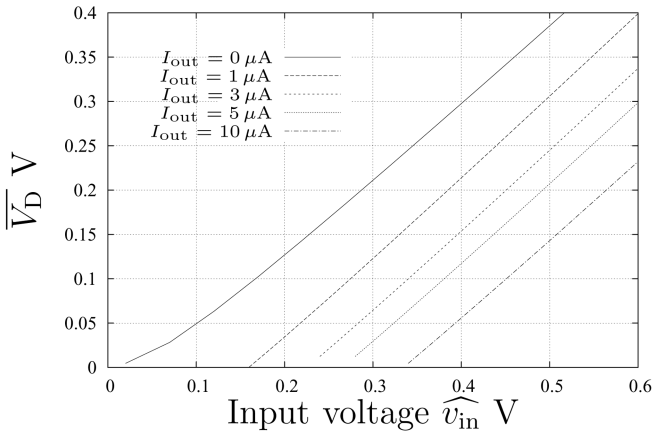

Fig. 9. $\overline{V_D}$ for different output currents for the $10\ \mu\text{m} \times 0.5\ \mu\text{m}$ diode.

The steady-state voltage $\overline{V_D}$ that appears on each diode as a function of $\widehat{v_{\rm in}}$ for typical values of $I_{\rm out}$ is obtained using (14) and is plotted in Fig. 9 for a diode realized in the aforementioned process. The output voltage can then be calculated using (13).

B. Determination of $C_{\rm in}$

Parasitics of real devices are of importance at high frequency. There are two sources of capacitance in a diode-connected transistor: the extrinsic part due to the layout geometry of the device, and the intrinsic part due to the channel formation. Source-bulk and drain-bulk capacitances were negligible in our process, but should be taken into account in typical bulk CMOS or partially depleted SOI technology. Although capacitor models exist, these are not easily integrable. Hence, we measured the input capacitance of a single diode as a function

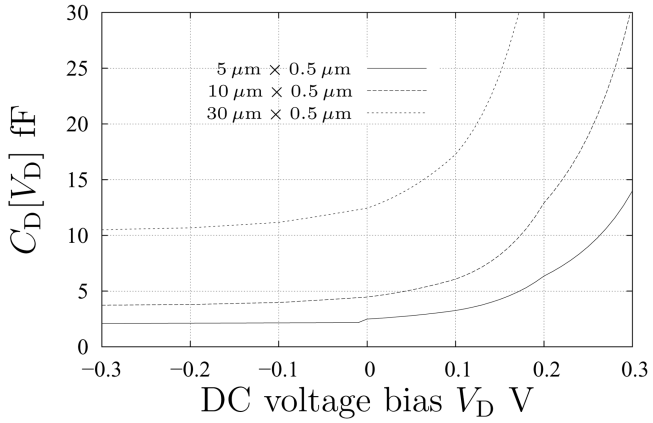

Fig. 10. C–V curves for different diode-connected transistors.

of its bias voltage and performed a numerical analysis. The *C-V* curves for different transistor geometries are shown in Fig. 10.

At high frequency, the equivalent capacitor seen at the input of the rectifier reduces the input voltage amplitude. This in turn has an unfavorable impact on the output voltage. It is also the reason that we cannot cascade too many rectifying stages. Every device appears in parallel at the input where their capacitances sum up (see Fig. 6). If the input impedance drops too low, the voltage swing on each diode is too small to charge the capacitors leading to an efficiency drop.

Our approach to calculate the equivalent capacitor is to compute the mean capacitance over one period of signal using the steady-state voltage solution and the measured *C-V* curves $C_D[V_D]$, which gives

$$C_{\rm in,rectifier} = \frac{4N}{T}\int_0^T C_D[\overline{V_D} + \widehat{v_{\rm in}}\sin\omega t]dt. \qquad (15)$$

The found capacitor $C_{\rm in,rectifier}$ appears finally in parallel with $R_{\rm in}$.

The sum of the RF input pad capacitors and layout capacitors (line to line, etc.) constitute a nonpredictable capacitor $C_{\rm added}$. It can be estimated using existing CAD parasitics extraction tools. Particular care during layout is necessary to keep all added input capacitors at the RF front end circuit to a minimum.

The total input capacitor is finally

$$C_{\rm in} = C_{\rm in,rectifier} + C_{\rm added}.$$

C. Determination of $R_{\rm in}$

As in the ideal case, we compute the mean power that enters the circuit and we find the *equivalent* input resistor $R_{\rm in}$ that induces the same amount of power in identical conditions. The dc I–V characteristic of the diodes is used since we are interested in the *absorbed active power*.

The mean power that enters the circuit during one period of signal is calculated as

$$\overline{P_{\rm in}} = \frac{1}{T}\int_0^T v_{\rm in}(t)i_{\rm in}(t)dt. \qquad (16)$$

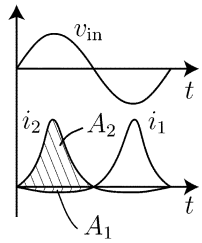

Fig. 11. Internal diode current.

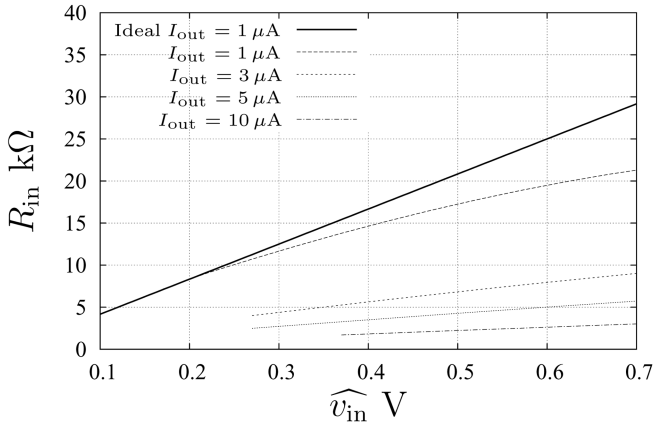

Fig. 12. $R_{\rm in}$ as a function of $\widehat{v_{\rm in}}$ for a three-stage rectifier.

From node A, B, B′ and due to the symmetry of the circuit (Fig. 11), we get

$$\overline{P_{\rm in}} = \frac{2}{T}\int_0^T v_{\rm in}(t)i_2(t) - \frac{2}{T}\int_0^T v_{\rm in}(t)i_1(t). \qquad (17)$$

Furthermore, the phase shift between signals $i_1[t]$ and $i_2[t]$ is equal to half a period (Fig. 11). We can simplify (17) to

$$\overline{P_{\rm in}} = \frac{4}{T}\int_0^T v_{\rm in}(t)i_D(t)dt \qquad (18)$$

which can be generalized for the N-stage case

$$\overline{P_{\rm in}} = \frac{4N}{T}\int_0^T v_{\rm in}(t)i_D(t)dt. \qquad (19)$$

We note here that the characteristic of only one diode is sufficient to compute $\overline{P_{\rm in}}$ (if they are all identical).

With the value of $\overline{P_{\rm in}}$, obtained using a numerical method, we can calculate the *equivalent time constant resistor* $R_{\rm in}$ that satisfies the power equivalence

$$\overline{P_{\rm in}}\frac{1}{T} = \int_0^T \frac{\widehat{v_{\rm in}}\sin^2\omega t}{R_{\rm in}}dt = \frac{\widehat{v_{\rm in}}^2}{2R_{\rm in}} \Rightarrow R_{\rm in} = \frac{\widehat{v_{\rm in}}^2}{2\overline{P_{\rm in}}}. \qquad (20)$$

A typical input resistor curve as a function of the input voltage for a varying output current $I_{\rm out}$ is shown in Fig. 12.

The equivalent input real part $R_{\rm in}$ increases with $\widehat{v_{\rm in}}$. This behavior can be explained since the output current is maintained at a constant value, and due to (12), $R_{\rm in}$ has to rise with an

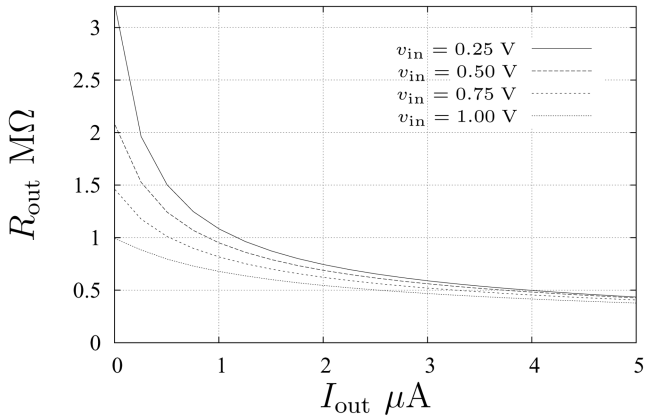

Fig. 13. $R_{\rm out}$ as a function of $I_{\rm out}$ for a three-stage rectifier.

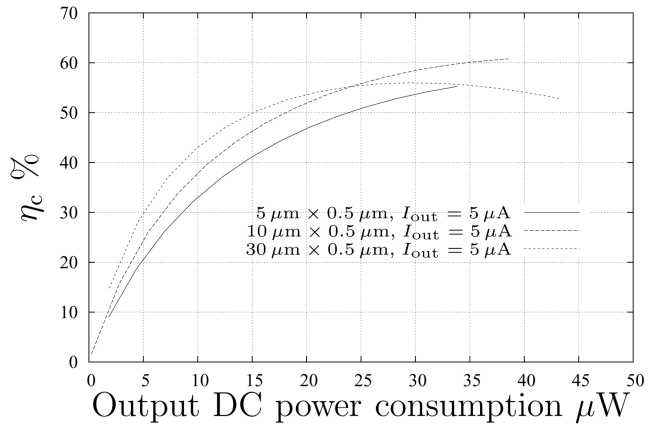

Fig. 14. Conversion efficiency for a three-stage rectifier.

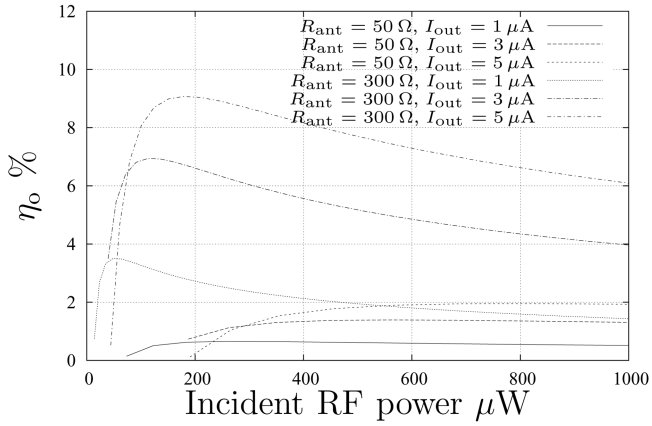

Fig. 15. Overall efficiency of the three-stage rectifier at 915 MHz.

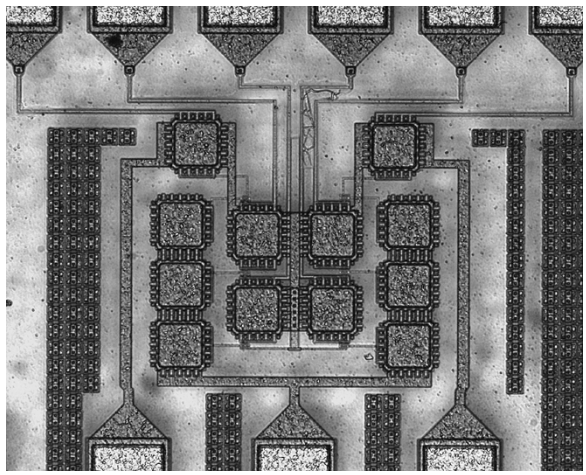

Fig. 16. Chip microphotograph of the three-stage rectifier.

increasing $\widehat{v_{\rm in}}$. $R_{\rm in}$ decreases dramatically with an increase in the output current. The higher the output current, the smaller the difference between the ideal and the real case.

D. Determination of $R_{\rm out}$

From Fig. 3, we can write for the output resistor $R_{\rm out}$

$$V_{\rm out} = V_0 - I_{\rm out}R_{\rm out} \quad \Rightarrow \quad R_{\rm out} = \frac{V_0 - V_{\rm out}}{I_{\rm out}} \tag{21}$$

where $V_0 = 4N\overline{V_D}\big|_{I_{\rm out}=0}$ is the output voltage with no output current $I_{\rm out} = 0$ (see Fig. 9 for this particular case). $R_{\rm out}$ as a function of $I_{\rm out}$ for different values of $v_{\rm in}$ is computed using (13) and (14) for $I_{\rm out} = 0$, and (13), (14) and (21) for $I_{\rm out} > 0$ and plotted in Fig. 13.

E. Rectifier Efficiency

The *conversion efficiency* η_c is defined as [9], [14]

$$\eta_{\rm c} = \frac{\text{dc Output Power}}{\text{Incident RF Power} - \text{Reflected RF Power}} \tag{22}$$

whereas the *overall efficiency* $\eta_{\rm o}$ is equal to

$$\eta_{\rm o} = \frac{\text{dc Output Power}}{\text{Incident RF Power}}. \tag{23}$$

As we have seen before, the power that enters an N-stage rectifier is given by (19). The dc output power $P_{\rm dc}$ is simply

$$P_{\rm dc} = V_{\rm out}I_{\rm out} = 4N\overline{V_D}I_{\rm out}. \tag{24}$$

Using (19) and (24) we compute the conversion efficiency for any rectifier. As an illustration, the conversion efficiency for a three-stage rectifier based on three different diode-connected transistors (see legends on Fig. 14 and Fig. 8) is shown in Fig. 14.

The overall efficiency for the $10\ \mu$m $\times\ 0.5\ \mu$m diode is also calculated and shown in Fig. 15 for different output currents.

V. Results and Comparisons

A three-stage rectifier was designed and fabricated in the aforementioned process (Fig. 16). Diode-connected transistors were also integrated to extract both I–V and C–V characteristics. The measurements were done in a traditional 50-Ω system. Based on these devices measurements, $R_{\rm in}$, $C_{\rm in}$, given the design variables $I_{\rm out}$ and the 50-Ω generator impedance (which corresponds to $R_{\rm ant}$ in the model), we compute the output voltage of the rectifier $V_{\rm out}$ as a function of the generated power $P_{\rm AV}$. The obtained results are compared with the

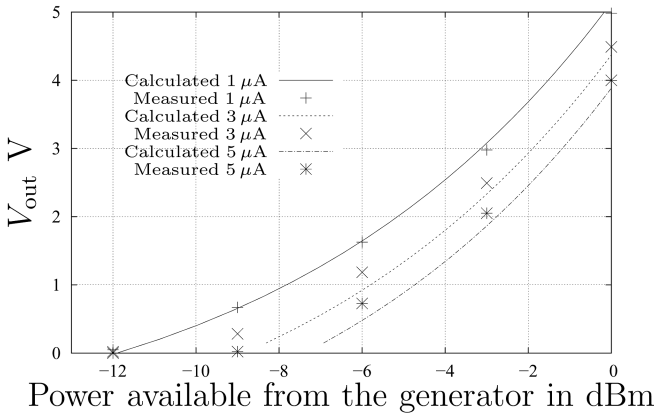

Fig. 17. $V_{\rm out}$ measured at 915 MHz for $R_{\rm ant} = 50\ \Omega$.

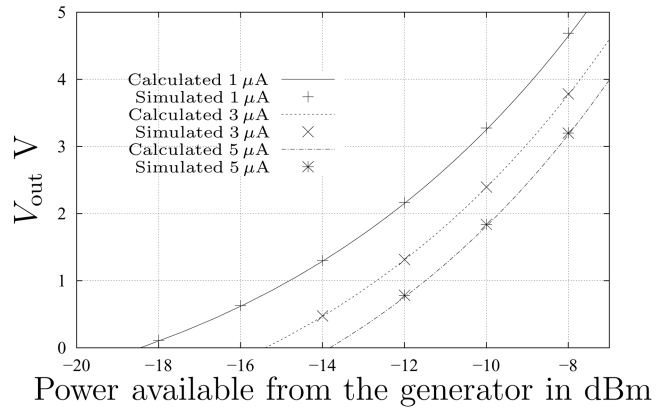

Fig. 18. $V_{\rm out}$ simulated at 915 MHz for $R_{\rm ant} = 300\ \Omega$.

measurements of the fabricated rectifier and are presented in Fig. 17 for different values of output current $I_{\rm out}$. *Model based calculations* and *measurements* are in excellent agreement and thus validate both the assumptions and the model. Furthermore, this also validates the efficiency curves of Figs. 14 and 15 as these can be derived from the values plotted in Fig. 16.

As shown before, a high impedance level $R_{\rm ant}$ is desirable in order to optimize the circuit's performance. The case of a $R_{\rm ant} = 300\ \Omega$ antenna is illustrated in Fig. 18 using *transistor based simulations*. In this particular case, the results given by the model using a *simulated I–V curve* are compared to transistor level simulation results. The results are also in excellent agreement.

VI. Design Considerations

A. Tradeoffs

The design of the rectifying device, i.e., the diode or the diode-connected transistor in our case involves a tradeoff between three fundamental factors: the reverse current, the direct current (threshold voltage and slope), and the capacitance behavior. To increase the direct current slope to achieve a higher efficiency, the width of the transistor should be raised. Unfortunately, increasing the width increases the reverse current and, hence, losses (see Fig. 8 for an illustration). Furthermore, the capacitance is proportional to the transistor size (the extrinsic part at least, see Fig. 10) thus limiting the number of stages we can cascade. In that sense, the use of Shottky diodes, if well controlled at the process level, would improve the overall performance. When cascading stages, one should notice that in order to produce an output current $I_{\rm out}$, every diode of the rectifier has to integrate a charge quantity of $I_{\rm out}T$ [see (7) and (8)]. Since the charge quantity is limited by the received power in the complete system case (rectifier and antenna), the number of stages is also limited. Furthermore, the optimal number of stages may vary with respect to the received power. The only certainty to improve the circuit is to use minimal length transistors. Although increasing the length usually reduces the reverse current, the forward current and the parasitic capacitances degrade more rapidly.

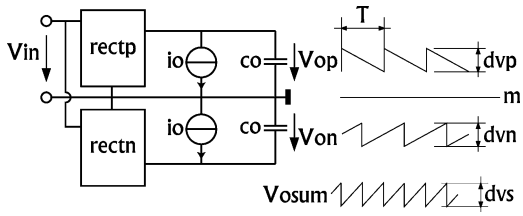

Fig. 19. Calculation of the output ripple.

B. Capacitors Design

A good starting point to design the capacitors consists in choosing the maximal admissible voltage ripple $\Delta V_{\rm max}$ at the output of one rectifier (see Fig. 19). The necessary output capacitance $C_{\rm out}$ that insure a voltage ripple lower than $\Delta V_{\rm max}$ is then equal to

$$C_{\rm out} \geq \frac{I_{\rm out}T}{\Delta V_{\rm max}} \left(\frac{1}{k} - \frac{\delta}{2\pi} \right) \tag{25}$$

where k is the number of rectifying alternation per rectifier circuit (1 in the present case), $I_{\rm out}$ is the output current of the rectifier, T is the period of the RF signal, and δ corresponds to the conducting angle [15]. The conducting angle δ can be calculated based on the steady-state solution and its value is given by

$$\delta = \frac{1}{2} - \frac{\arcsin\left(\frac{V_D}{v_{\rm in}}\right)}{\pi}. \tag{26}$$

It should be mentioned that the ripple of the output voltage $V_{\rm out} = V^+ - V^-$ is equal to[3] $\Delta V_{\rm max}/2$. As a result, its frequency is doubled.

Concerning the "intermediate capacitors," i.e., all the capacitors except $C_{\rm out}$ (see Fig. 2), their value doesn't affect significantly the output ripple. The only necessity is to keep their corresponding impedance as small as possible compared to the impedance of the diodes in order not to decrease the conversion efficiency. These capacitors act like voltage dividers and, it is preferable that they represent a short-circuit at the frequency of interest.

[3]In Fig. 19, the electrical signals are simplified to sawtooth signals for the explanation.

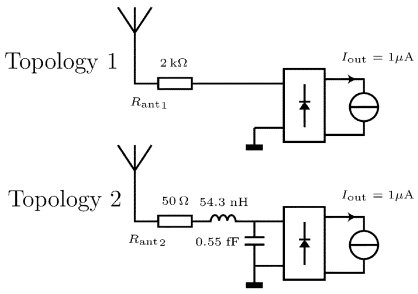

Fig. 20. Equivalent topologies at 915 MHz.

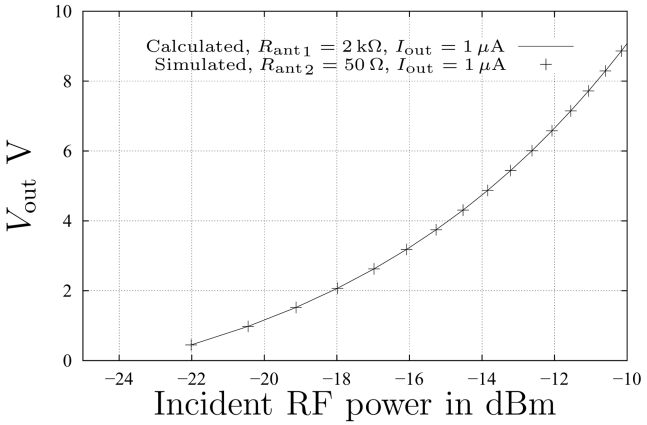

Fig. 21. Output voltage of the three-stage rectifier at 915 MHz.

In the case where these "intermediate capacitors" cannot be considered as short circuits, it can be shown that the overall input capacitance C'_{in} is approximately[4] equal to

$$C'_{\text{in}} = C_{\text{in,rectifier}} \frac{\gamma(1+2\beta)}{2(1+2\beta+\gamma+\gamma\beta)} \tag{27}$$

where $\beta = C_2/C_d$, $\gamma = C_1/C_d$ are the normalization factor with respect to the diode's overall capacitance C_d, and $C_{\text{in,rectifier}}$ corresponds to the input capacitance with the "intermediate capacitors" shorted. The second term in the right-hand side of (27) tends toward 1 as β and γ raises. To satisfy assumption 4 of Section II, a value of 30 for both β and γ is sufficient. In this case, the "intermediate capacitors" are equal to 900 fF that was rounded up to 1 pF in the design of Fig. 16.

C. Antenna and Matching Issues

As we have seen before, power matching between the antenna and the rectifier at a high impedance level is essential. In Fig. 20, the impedance level is equal to 2 kdΩ, which is optimal for the three-stage rectifier of this paper when delivering an output current $I_{\text{out}} = 1\ \mu$A. Both topologies in Fig. 20 are equivalent at one frequency (915 MHz in this case) and result in the same performance (see Fig. 21 where the calculated curves using the present model and the transistor level simulated points correspond, respectively, to topology 1 and topology 2). By introducing the *LC* matching circuit, a degree of freedom in the design of the antenna is added. In fact, one can choose a realistic value for the antenna and design the matching circuit in order to achieve a given impedance level. *the higher this level is, the more selective the system becomes*. The parasitics also limit the maximal achievable value. In the case where I_{out} is not constant, it is preferable to choose the worst case value, i.e., when I_{out} is maximum. Finally, it is the application that defines the constraints for the antenna and the matching circuit design.

[4]The approximation is to consider a high diode real part impedance, which is generally the case.

VII. Conclusion

The study of the μ-power rectifier has been made possible by transforming the input pulsed current into a sinusoidal one. The circuit input is, thus, modeled as a simple resistor R_{in}. We have also shown that the parasitic capacitors associated with each diode can be modeled with the help of an equivalent input capacitor C_{in}. Finally, a voltage source controlled by the input signal amplitude $\widehat{v_{\text{in}}}$ and an output resistor R_{out} complete the model.

The resistor R_{in} respects the power transmitted to the rectifier and allows the prediction of its conversion and overall efficiency.

A three-stage rectifier was integrated in an SOS CMOS 0.5-μm process and the measurement results validate the model. A complete study of rectifiers in the framework of μ-power applications is made possible using the presented model.

References

[1] W. C. Brown, "The history of power transmission by radio waves," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-32, no. 9, pp. 1230–1242, Sep. 1984.

[2] M. M. Ollivier, "RFID—a practical solution for problem you didn"t even know you had!," in *IEE Colloq. on Wireless Tech. Dig.*, Nov. 14, 1996, pp. 3/1–3/6.

[3] M. Leonardi *et al.*, "A soft contact lens with a MEMS strain gauge embedded for intraocular pressure monitoring," in *Transducers, 12th Int. Conf. Actuators and Microsystems*, vol. 2, Jun. 2003.

[4] J. A. Hagerty *et al.*, "Recycling ambient microwave energy with broadband rectenna arrays," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-52, no. 3, pp. 1014–1024, Mar. 2004.

[5] Microwave engineering Europe, in RFID comes up to a standard, Mar. 2004.

[6] Michelin Embeds RFID Tags in Tires (2003, Jan. 17). [Online]. Available: http://www.rfidjournal.com/article/articleprint/269/-1/1/

[7] Question ITU-R 210/1, Wireless Power Transmission, International Telecommunication Union (ITU). (1997). [Online]. Available: http://www.itu.int/itudoc/itu-r/publica/que/rsg1/que210_ww9.doc

[8] K. Finkenzeller, *RFID Handbook, Radio-Frequency Identifications Fundamentals and Applications*. New York: Wiley, 1999.

[9] J. O. McSpaden *et al.*, "Design and experiments of a high conversion efficiency 5.8 GHz rectenna," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-46, no. 12, pp. 2053–2060, Dec. 1998.

[10] Y. Suh *et al.*, "A high efficiency dual frequency rectenna for 2.45 and 5.8 GHz wireless power transmission," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-50, no. 7, pp. 1784–1789, Jul. 2002.

[11] T. Yoo *et al.*, "Theoretical and experimental development of 10 and 35 GHz rectennas," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-40, no. 6, pp. 1159–1266, Jun. 1992.

[12] J. P. Curty. (2004) A web interface for diode rectification ability evaluation. [Online]. Available: http://legwww.epfl.ch/direct

[13] High performance silicon on sapphire technology, J. C. S. Woo. (1998). [Online]. Available: http://www.ucop.edu/research/micro/97_98/97_208.pdf

[14] W. C. Brown, "An experimental low power density rectenna," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 10–14, 1991, pp. 197–200.

[15] J. D. Chatelain and R. Dessoulavy, *Electronique*, 2nd ed. Lausanne, Switzerland: Presses Polytechniques et Universitaires Romandes, 1995.

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