Power Management System for Online Low Power RF Energy Harvesting Optimization

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Abstract—For many years, wireless RF power transmission has been investigated as a viable method of power delivery in a wide array of applications, from high-power space solar power satellites to low-power wireless sensors. However, until recently, efficient application at the low sub-milliwatt power levels has not been realized due to limitations in available control circuitry. This paper presents a "smart" microcontroller-based power management system with online power stage efficiency optimization and maximum power point tracking (MPPT). The system is experimentally evaluated using a new, more accurate four-quadrant rectenna model and circuit realization that enables rigorous testing of the power management system for a wide range of rectenna arrays and power characteristics. Hardware results are presented with online optimization over a converter input power range from 10 μW to 1 mW. Results are also shown based on the application of harvesting RF power from a nearby cellular tower, where the power management system collects up to seven times more energy when compared to a direct battery connection.

Index Terms—DCM resistor emulation, maximum power point tracking, MPPT, power management, rectenna, SMPS boost, wireless power.

I. INTRODUCTION

THE concept of wireless power transmission via far-field RF radiation has been considered since the beginning of the 20th century. Wireless powering can be differentiated into near- and far-field. In the former case, the powering device is small compared to the wavelength and is inductively (or capacitively) coupled to the source, making it sensitive to its relative position. Far-field powering implies plane wave propagation between antennae at longer range, can be done without line of sight, and is less sensitive to the orientation and position relative to the transmitting antenna. The work in this paper addresses far-field powering at low incident power densities (below 10 μW/cm^2). It differs from radio frequency identification (RFID) devices in that the powering is independent of signal transmission and is done at different time scales, power levels and ranges. Few applications have taken advantage of this technology for harvesting energy at sub-milliwatt power levels. This can be
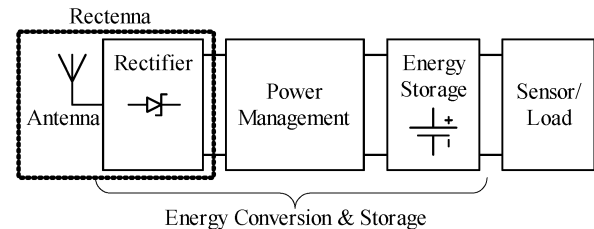
Fig. 1. System diagram for typical energy harvesting sensor application. This paper focuses on the power management block and its interface to the rectenna and energy storage device.

attributed to the challenges associated with optimizing the interface between the rectifying antenna, or "rectenna", and typical low-power sensor loads to achieve high overall efficiency [1]–[3]. A block diagram is shown in Fig. 1 for a typical wireless sensor with RF energy harvesting. The passive RFID tag is one example of a solution that operates successfully under good matching and well-known operating conditions [4]. However, there are many applications for general wireless sensors that operate in a variety of unknown conditions, with uncertainties and large variations in the RF field and rectenna characteristics. These time-varying conditions create significant challenges in maximizing the harvested energy and motivate use of power management circuitry with online optimization.

The primary application areas of RF energy harvesting can be categorized by the RF field power density, total rectenna output power and by the dynamic nature (both spatial and temporal) of the RF energy being harvested. Much of the early application research was devoted to achieving high transfer efficiency at power levels in the kilowatt range and higher, where such a system could be used as a means to deliver power to the ground from an orbiting solar power satellite (SPS) [5]. Here, the RF power density and, hence, rectenna operating point (terminal voltage and current) is high and remains virtually constant with time, requiring minimal power management circuitry to extract peak power.

RF power transmission applications with more variation in the power density and overall lower power levels require more complex power management and maximum power point tracking (MPPT) circuitry. Examples of this include satellite-to-satellite power transmission [6] and an orbit boosting system [7], which uses terrestrial transmitters to power an ion engine of an orbiting spacecraft. At the lowest end of the scale, with RF power densities of less than 10 μW/cm^2, energy-harvesting embedded sensors have to capture sporadic energy from the environment to power a useful load.

One specific example is a wireless sensor for monitoring cell tower communications. Such sensors could be placed near or
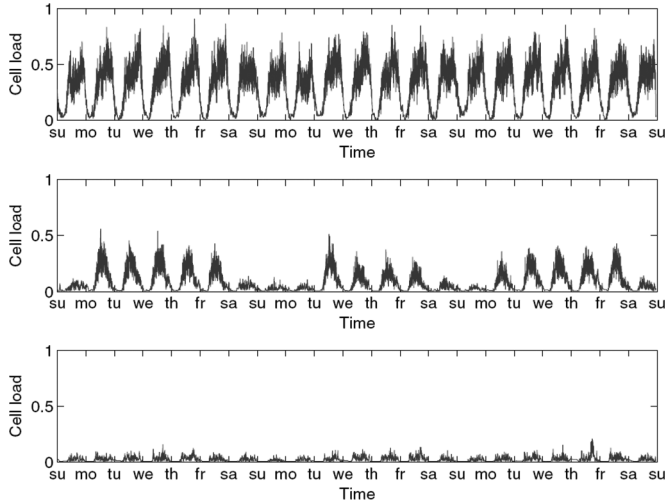
Fig. 2. Normalized CDMA base station output power for three different cell locations over a 3-week period [9]. It can be seen that in all three cases, there is periodic variation in the output power. An RF energy harvesting system must be designed to have high power conversion efficiency regardless of the ambient power level and dynamics.
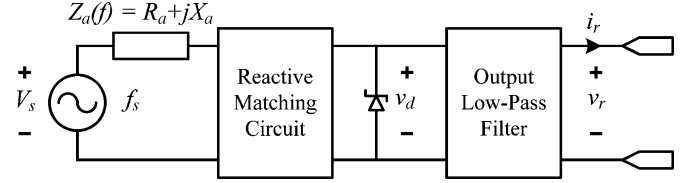

Fig. 3. High-level functional diagram of typical rectenna. An input matching circuit interfaces the antenna feed to the rectifier. The output filter prevents AC content from reaching the load. The frequency-dependent antenna impedance and matching network can be modeled as a radiation resistance R_a and a narrowband filter, reducing it to the model in [11].

on a cell base station such that the rectenna could capture side-lobe or reflected RF power and simultaneously monitor tower activity [1]. Multiple studies have been performed, such as [8], which showed that power densities within 50 m of a cell tower exceed 1 μW/cm^2 but vary widely with location and time of day. The total available RF power may vary as shown in Fig. 2, which depicts experimentally measured total normalized output power for several different base stations (results shown are reproduced from the study in [9]). It can be seen that there are daily cyclic variations in power as the number of users in the cell changes. Further, different cells have drastically different maximum and average power levels.

This paper presents design details and experimental results for a power management system that performs online optimization of the RF energy harvesting system to allow efficient operation over a wide range of operating conditions. In addition, a new four-quadrant low-frequency circuit model of the rectenna is introduced to facilitate rigorous system testing and intuitive understanding of the rectenna-converter interface and dynamics. The paper is organized as follows: a description of the rectenna array is given in Section II, followed by the development of a low frequency rectenna model and emulator circuit in Section III. Power management design details are given in Section IV and experimental results of the power management circuit and cell tower application example are presented in Section V.

II. RECTENNA ARRAY

A rectenna is a microwave rectifier which converts RF energy directly into DC current. Many different designs exist, but nearly all consist of three basic elements [5], as shown in Fig. 3: an antenna, either broadband or narrowband, an input matching circuit between the antenna feed and rectifying element, a recti-fier circuit, and a low-pass output filter to remove the AC content from the DC output. The rectifier can range from half-wave or full-wave rectifiers to multi-stage multipliers. In this work, the

half-wave rectifier approach is adopted using a single high-fre-quency, zero-bias Schottky diode due to its high efficiency using commercial components at low incident RF power densities in the 1 μW/cm^2 to 50 μW/cm^2 range and frequencies in the 1 GHz to 10 GHz range [10].

The effective area which collects RF power can be increased with multiple rectenna elements which are not RF-connected so that the DC is summed after rectification. A 20-element 22 cm by 28 cm patch rectenna array was designed to receive and rectify microwatt-level power densities found near cell tower base stations. The rectennas are narrowband, centered at the expected transmitter frequency of 1960 MHz. Each dual-polarized antenna is printed on a 0.75 mm thick substrate with a relative permittivity of $\varepsilon_r = 6$ and is 32 mm square. Two Skyworks SMS7630 zero-bias Schottky diodes are connected to the two feeds corresponding to the two orthogonal linear polarizations. The outputs of the two rectifiers are added in either series or parallel, depending on the array configuration.

In order to design a suitable converter for this DC output, the rectenna I-V characteristics under RF input must be well understood. The most widely used rectenna DC terminal model described in [11] and [12] is the linear voltage-source resistor model, where the rectenna is viewed as a high-efficiency recti-fier in the first I-V quadrant, behaving like an ideal DC source with a series resistance. This model can be derived using Fourier series analysis, assuming ideal filters as in [11], which gives the following linear equation for the first-quadrant I-V curve

$$v_r = \frac{\pi}{4} V_s - \frac{\pi^2}{8} R_a \cdot i_r \tag{1}$$

where the variables are defined according to Fig. 3. The maximum power point (MPP) occurs at the optimal load resistance

$$R_{L,OP} = \frac{\pi^2}{8} R_a. \tag{2}$$

Fig. 4 shows experimentally measured four-quadrant I-V curves of the baseline rectenna design. It can be seen that, indeed, the rectenna I-V characteristic can be approximated as being resistive in the power-generating first quadrant, although the approximation breaks down somewhat near the open-circuit voltage, $V_{r,OC}$ and short-circuit current, $I_{r,SC}$. Due to the extremely low power levels and resulting small voltages inside the rectenna, the diode turn-on characteristics make the I-V curve non-linear near the $V_{r,OC}$ point.

Another significant and rarely discussed aspect of the full four-quadrant rectenna I-V curves is the behavior for operating points in the second or fourth quadrants. These situations may
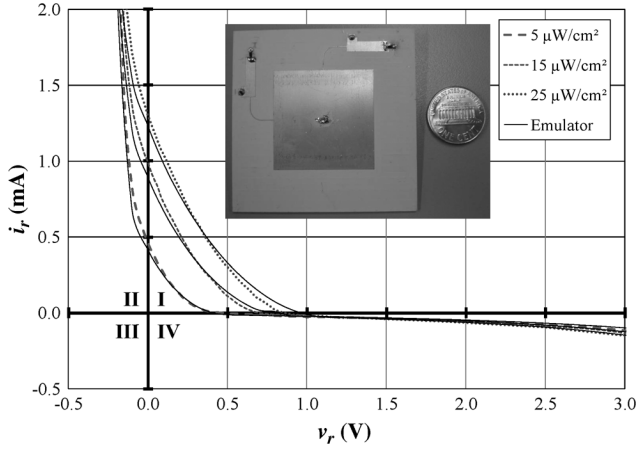
Fig. 4. Experimentally measured I-V characteristics of patch rectenna (inset) for several incident RF power densities compared to measured rectenna emulator I-V curve based on DC model. The Cartesian coordinate quadrants are labeled to show the convention used in the text.
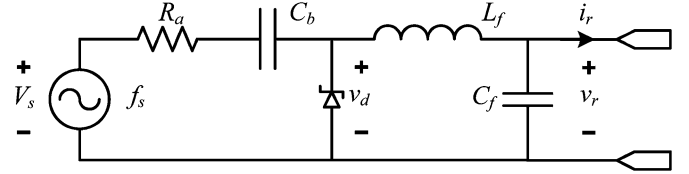

Fig. 5. Low-frequency four-quadrant rectenna model schematic. The antenna element is represented by a Thévenin equivalent at the RF frequency and an ideal DC blocking capacitor. The output low-pass filter is ideal.
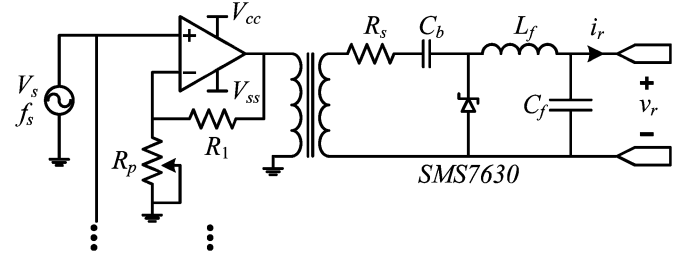

Fig. 6. Rectenna emulator schematic. An adjustable-gain amplifier is used to implement the AC source of the model and an isolation transformer is added to allow parallel/series configuration of multiple rectenna cells.

occur when there is severe impedance mismatch of the rectenna to its load or in series and parallel rectenna arrays when there is variation of the incident power density across the array. These array effects were investigated in [13], but mostly considering "small" parameter variations that did not push the operating point of any elements out of the first quadrant. However, in cases of very large power density variations and multipath effects, such as those that can occur in uncontrolled "harvesting" environments, a full four-quadrant model is needed to accurately predict the behavior of the complete array.

III. FOUR-QUADRANT RECTENNA MODEL

A. Low-Frequency Model Derivation

The proposed four-quadrant rectenna model builds on the basic principles of the linear model by including the diode characteristics, which significantly improves the valid I-V range of the model. The derivation proceeds in a fashion similar to [11]. First, the antenna component of the rectenna is assumed to be narrowband and the incident RF power density is at one frequency within the antenna bandwidth. This simplifies the model by removing any frequency dependence so that complex RF effects can be ignored. Second, no dissipative effects or inefficiencies are modeled and all filters are considered to be ideal. Next, the RF model of the rectifying diode is replaced with a low-frequency SPICE model obtained from the manufacturer. Finally, the antenna component is replaced with its Thévenin equivalent at the incident RF frequency. The resulting model topology is shown in Fig. 5. The source voltage amplitude V_s determines the maximum power output of the rectenna as in the linear model and depends on the specific rectenna design. The AC source gives rise to the transitions between the different I-V quadrants due to its interaction with the diode.

The model shown in Fig. 5 can be matched with the experimental results of Fig. 4. As mentioned above, the diode bias point determines the behavior of the rectifier, which depends on the DC voltage applied to the rectenna terminals, v_r. When v_r grows above $V_{r,OC}$, the rectenna supplies no current since

the diode is always reverse-biased. Eventually, v_r exceeds the diode breakdown voltage, V_{BD}, and the I-V curve moves into the fourth quadrant where the diode is in the breakdown region and the rectenna consumes power. For negative v_r, the diode is always forward-biased and no rectification is performed, so the rectenna again consumes power.

The above analysis shows the improved insight gained by the addition of a realistic diode to the standard rectenna model. Since the circuit in Fig. 5 uses the Thévenin equivalent of the antenna at the operating frequency, a low-frequency diode model and ideal filters, it can be easily simulated using low-frequency SPICE software with other power management components for design purposes, or realized as a physical circuit as discussed below.

B. Rectenna Emulator Prototype

A prototype rectenna emulator (Fig. 6) was built to function as a test bed for verifying the operation of the power management circuitry described in the following section by producing the same I-V characteristics as the baseline rectenna element design described in Section II. The prototype rectenna emulator is a simple physical implementation of the low-frequency model presented above. An individual emulator cell consists of an adjustable-gain amplifier, resistor, DC blocking capacitor, Schottky rectifier, and LC output filter, as shown in Fig. 6. An optional isolation transformer is included in this design to facilitate the construction of an emulated rectenna array, composed of multiple independent emulator cells. The isolation transformers ideally do not significantly change the I-V characteristics of the cells, but allow the cell output to float so that only one ground-referenced power supply is needed for the entire array and the individual cells can be connected together in series and parallel combinations.

The component values of the model can be selected over a wide range, since they are only meant to represent the low-frequency behavior of the rectenna. The AC source frequency is

chosen at a reduced frequency suitable for time domain circuit simulation and hardware component selection. Once a frequency is chosen, the output filter values can be found such that the cutoff frequency is much lower than the source frequency to best approximate an ideal filter. The blocking capacitor is chosen to be large enough to have negligible attenuation of the AC source amplitude. For the prototype described above, a source frequency of $f_s = 250$ kHz was chosen, so that $C_b = 10$ μF, $C_f = 20$ μF, $L_f = 680$ μH and the same diode as in the rectenna was used, the Skyworks SMS7630.

The measured emulator I-V curves for one rectenna cell with the values given above are shown in Fig. 4 for several incident RF power densities. It can be seen that the curves closely match that of the rectenna in all four quadrants. Further, any array configuration of the emulator cells will give the correct I-V curve for the corresponding rectenna array.

IV. ADAPTIVE POWER MANAGEMENT

A. Previous Work: Resistor Emulation

The goal of the power management circuit is to harvest maximum power over a wide range of operating conditions independent of the load behavior. Prior work shown in [14], [15] utilized a switching converter operating in discontinuous conduction mode (DCM) or critical conduction mode (CRM) to naturally emulate a resistor at the input port of the power converter. For a boost converter operating in DCM or CRM, the emulated input resistance is

$$R_{em,DCM} = \frac{2 \cdot L \cdot T_{hf}}{t_1^2 \cdot k} \left(\frac{V_o - V_{in}}{V_o} \right) \tag{3}$$

$$R_{em,CRM} = \frac{2 \cdot L}{t_1 \cdot k} \tag{4}$$

where L is the inductance, T_{hf}, t_1, and k are timing parameters as defined in Fig. 7, and V_{in} and V_o are the input and output voltages of the power converter, respectively. This approach works well because a rectenna looks like a nearly constant resistance in the first (power-producing) quadrant over a wide range of power levels (Fig. 4). The power converter maintains nearly the same input resistance over a wide range of input power levels, providing good matching to the rectenna so that maximum power is extracted with minimal control effort. This technique was realized on a custom IC for ultra low power energy harvesting in [16]. This "passive" tracking technique works well at low power levels and over a limited range of operating conditions, and requires manual matching of the converter timing parameters in (3) and (4) to the rectenna characteristics.

B. Proposed Approach: System Architecture

The proposed rectenna power management approach leverages the previous work [14], [15] with the addition of an intelligent controller that performs maximum power point tracking (MPPT) and online converter efficiency optimization. The goal is to improve operation in the presence of unknown or varying optimal rectenna source resistances and input power levels by
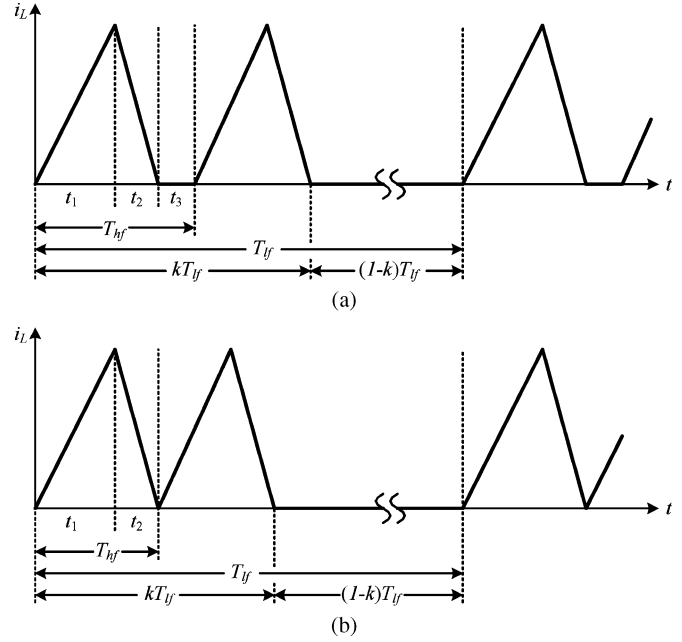

Fig. 7. Inductor current waveforms of boost converter operating in (a) DCM and (b) CRM.

addressing the shortcoming of having fixed power stage parameters. An off-the-shelf microcontroller (MCU) is used for low-cost and easily accessible realization. The microcontroller runs a simple MPPT algorithm to periodically tune the emulated input resistance to match the rectenna characteristic and adjusts the timing parameters for maximum efficiency.

Fig. 8 shows the power management system architecture, consisting of several main components, including a Texas Instruments MSP430F247 ultra low-power microcontroller responsible for running all control, tracking and optimization algorithms, a dual-FET boost power stage, a comparator and analog switch for high-side gate drive and a few low-power discrete logic gates. The control logic is designed to be powered directly from the battery so that no additional power conversion is required. The circuit components were carefully designed and selected using low cost, readily available commercial hardware in order to achieve a practical solution for small-scale commercial or scientific applications. The selected hardware and control concepts and algorithms described below could also be integrated into a custom IC such as [16]. The PCB prototype is shown in Fig. 9 and power stage parameters are listed in Table I.

Clock System Design: One of the most critical components in an adaptive low-power system is an adjustable and flexible clock system. The optimal frequency required to drive the power stage is significantly different than what is required for the MCU, and both of these frequencies need to be adjusted online depending on the power level to maximize the system efficiency. Fig. 8 shows that the system utilizes several different oscillators and adjustable clock dividers for maximum flexibility. *Timer A* is a digital pulse-width modulator (DPWM) and software-controlled clock divider used to generate the power stage gate-drive signal and sourced by two different clocks. An external, fixed-
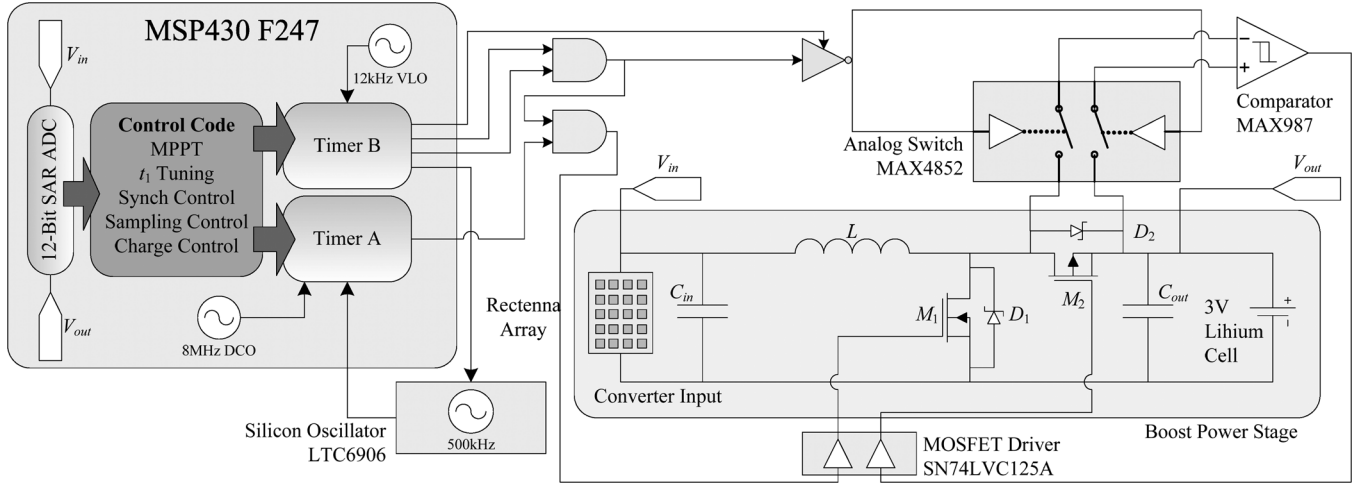
Fig. 8. Rectenna power management system architecture. A low-power Texas Instruments MSP430 microcontroller generates power stage control signals and runs optimization and MPPT algorithms. The rectenna voltage is sensed to calculate input power and the output voltage is used for battery charge control.
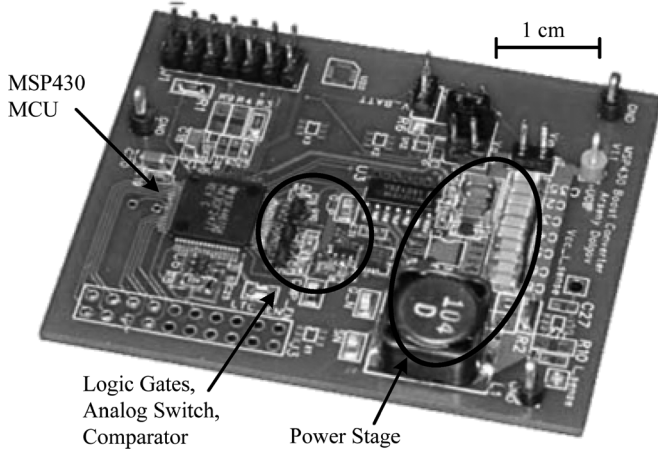

Fig. 9. Rectenna power management system prototype PCB.

TABLE I
SUMMARY OF POWER STAGE PARAMETERS

Component	Description/Value
Inductor, L	MSS1278, 100 μH
MOSFETs M_1, M_2	Si1563EDH (Complementary)
Diodes D_1, D_2	BAT43WS Schottky
Capacitor, C_{in}	1 mF Ceramic
Capacitor, C_{out}	100 μF Ceramic

frequency 500 kHz LTC6906 silicon oscillator is utilized for lower power levels where a slower switching frequency is required. For higher power operation where a more precise and faster clock is needed, *Timer A* can be sourced by an 8 MHz digitally-controlled oscillator (DCO) inside the MSP430. The MCU control code can switch between these oscillators in real-time and precisely adjust the power stage switching frequency, f_{hf}, by changing the counter value that sets the period of *Timer A*.

At very low power levels, the converter is not run continuously but operated in a pulsed manner for time kT_{lf}, as shown in [14] and in Fig 7. All unnecessary electronics are shut down while the converter is not switching during the $(1 - k)T_{lf}$ time

period. Since the value of R_{em} is directly dependent on the power stage activity duty cycle, k, as shown in (3) and (4), another lower-frequency clock system is needed to precisely control R_{em}. *Timer B* creates the adjustable low-frequency duty cycle kT_{lf}, sourced by the MSP430's onboard 12 kHz very low-power oscillator (VLO), which generates a 20 ms low-frequency period, T_{lf}. The timer also generates several other software-controlled DPWM signals which enable/disable peripheral electronics such as the comparator and analog switch, thereby allowing the converter to operate in various modes, as described below.

Converter Operating Modes: Another benefit of the proposed power management system that allows the converter to maintain very high efficiency over a wide range of power levels is the ability to operate in several different modes, as described below. The transition point between the different modes of operation is governed by the control losses of the circuitry and/or algorithms required to operate in the corresponding modes. At low input power levels, the converter operates in single-FET mode (using a Schottky diode as the high-side switch) to prevent the losses caused by the high-side gate drive. At higher input power levels, the MCU activates the comparator across the high-side Schottky diode, as shown in Fig. 8. This enables the dual-FET synchronous rectification operating mode, where the high-side FET clamps the diode during the conduction interval to reduce conduction losses. This "ideal-diode" method is a technique often used in low-power rectifier circuits [17], [18]. Traditional synchronous designs usually rely on a high-frequency (and high-power) clock in the range of several megahertz to generate a short, precise dead-time interval between the turn-off and turn-on transitions of the two FETs to prevent shoot-through current. The use of a comparator to generate the high-side gate-drive, on the other hand, effectively enables soft-switching of the FET and only a clock on the order of the switching frequency needs to be generated for the low-side FET. In addition, the ideal-diode circuit also performs the high-side turn-off before the inductor current goes negative, which would require an additional zero-crossing detector in a traditional synchronous design in order to achieve DCM operation.

Component	Active Power [μW]	Shutdown Power [μW]
MCU w/ fast algorithms	10	1.2
LTC6906 oscillator	48	0
MAX987 comparator	144	0
MAX4852 analog switch	1.2	0
SN74LVC125A driver	0.3	0.3 (always on)

The active power represents the power draw of the component from a 3 V battery when it is operated during the k interval in DCM or CCM mode. The shutdown power represents the power draw during the $(1 - k)$ interval.

The power stage is also operated in CRM at low power levels to reduce control losses during the t_3 interval present in DCM mode during which no power is being transferred (Fig. 7). This mode of operation is achieved with software running on the MCU which computes and adjusts the switching period T_{hf} to maintain CRM based on the measured input and output voltages and the formula

$$T_{hf} = t_1 \left(1 + \frac{V_{in}}{V_o - V_{in}} \right). \tag{5}$$

This procedure incurs very little additional power loss on top of the main MPPT algorithm already running on the MCU and is preferred over the method of using a comparator to detect inductor current zero-crossings and restart the switching period to maintain CRM. However, due to the limited resolution of *Timer A*, the algorithm is unable to always precisely maintain CRM and a small error in R_{em} is created when t_3 is not exactly zero. For this reason, the converter is operated in DCM at higher power levels where the efficiency gain due to CRM is negligible but R_{em} can be controlled more accurately, reducing tracking losses. In DCM mode, the MCU chooses the high-frequency period T_{hf} based on the power stage input voltage. The duty cycle $D = t_1/T_{hf}$ is 0.5 for $V_{in} < 1/2V_o$ and 0.25 for $V_{in} > 1/2V_o$. This enables the converter to operate with a wide range of input voltages.

There are several shutdown modes where the converter switching and optimization algorithms cease for an extended period of time. When the measured input power drops below the zero-efficiency point of the converter, the MCU goes into a 1.5 μW sleep mode, periodically measuring the input power and resuming operation when the conversion efficiency is greater than zero. The battery voltage is also monitored and the converter is shut off when an overcharge condition is detected. Another shutdown mode occurs when the MPP reaches or exceeds the output voltage. When this operating point is detected, the converter goes into pass-through mode by turning on the high-side MOSFET, effectively connecting the input directly to the battery, which removes switching and control losses and reduces conduction losses. The power consumption of the components described above is summarized in Table II.

Online MPPT & Optimization Algorithm: One of the main improvements of the proposed design over previous systems is the integration of a low-power MCU with the power stage that has the ability to run an optimization and MPPT algorithm, among others. Various MPPT algorithms exist, such as ripple-correlation control [19], incremental conductance [20] and fuzzy logic [21]. The perturb and observe (P&O) method [22], [23] is simplest and least power-hungry, making it ideal for this application where computational resources are limited [24]. Also, since the rectenna impedance is resistive in the first quadrant, there is precisely one peak power point ($R_{em,MPP}$ is unique) according to the theorem of maximum power transfer. The above argument, coupled with the nearly power-independent emulated resistance behavior of the converter means the MPPT algorithm does not need to be overly complex or high-bandwidth. The MPPT algorithm mainly allows the converter to extract maximum power from a rectenna design that is not fully characterized and removes the $(V_o - V_{in})/V_o$ correction factor from (3) which degrades tracking performance in non-adaptive converter designs.

The second main function of the MCU software is to optimize the switching frequency of the converter over a wide range of input power levels and select the clock source that minimizes the control losses. Since this optimization aspect does not depend on the particular rectenna source but only on the total input power, the optimization is done offline in MATLAB to conserve computational power on the MCU. The optimal transistor on-time values t_1 for a given power level computed in MATLAB are stored in a look-up-table (LUT) on the MCU and then accessed during online operation.

A high-level flow diagram of the MCU software is shown in Fig. 10. The software is divided into two main procedures, as described above, that run in a linear fashion. The system depends heavily on correct sensing of input power, which is computed based on the measured input voltage and the current emulated resistance commanded by the MCU,

$$P_{in} = \frac{V_{in}^2}{R_{em,MCU}}. \tag{6}$$

After the input power has been computed, the MCU performs one iteration of the P&O MPPT algorithm. The P&O method relies on the converter input power being a smooth function of R_{em}, and therefore k, with one global maximum located at the MPP as derived using the linear rectenna model in (1), (2). Each iteration of the algorithm perturbs R_{em} by changing k, which moves the rectenna operating point either towards or away from the MPP. If the MCU observes that the current measured input power $P_{in}[n]$ is greater than the previous iteration $P_{in}[n-1]$, k is incremented in the same direction during the next iteration, otherwise the increment direction is reversed. In this way, the P&O method continually searches for the global maximum of the function by measuring the polarity of the instantaneous slope of the P_{in} versus R_{em} curve.

After one P&O iteration has been completed, the second half of the algorithm shown on the right hand side of Fig. 10 is executed. This procedure uses the input power measured in the MPPT procedure, as well as the current R_{em}, as an index into a LUT of optimal t_1 switching period values. The optimal operating mode (CRM, DCM, single- or dual-FET) is also determined from the measured input power. Finally, *Timer A* and *Timer B* are configured to the new operating mode and the optimal t_1.
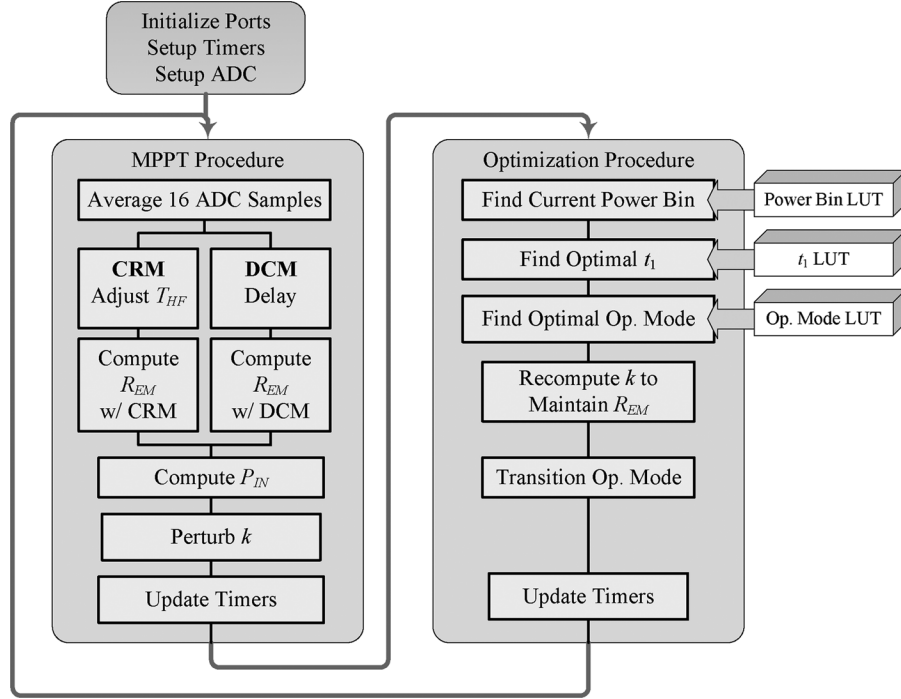
Fig. 10.   Diagram showing the MCU software flow of the MPPT and power stage optimization algorithms. The MPPT algorithm is based on the P&O method [22], [23]. The optimization procedure uses the measured input power to index into LUTs that hold optimal converter operating parameters.

C. Power Stage Design and Offline Optimization

While the presented architecture implements several techniques for online optimization of the power stage, much work was also done offline in designing the converter and support circuitry and choosing component values to maximize efficiency over the widest possible range of power levels. The system was modeled and simulated numerically in MATLAB, utilizing some of the same loss modeling techniques as in [14]. The main power loss equations are given below for DCM single-FET operation

$$P_{loss} = P_{cond} + P_{sw} + P_{ctrl} \tag{7}$$

$$P_{ctrl} = P_{fix} + P_{PWM}(T_{HF}) \cdot k \tag{8}$$

$$P_{cond} = \left(R_{l,esr} \left(I_{L,rms1}^2 + I_{L,rms2}^2 \right) \right.$$
$$\left. + R_{on,n} \cdot I_{L,rms1}^2 + P_{diode} \right) \cdot k \tag{9}$$

$$P_{sw} = \left(Q_{g,n} \frac{V_o}{2} + C_{oss,n} \frac{V_{in}^2}{2} \right) \frac{k}{T_{LF}}. \tag{10}$$

In (7)–(10), $R_{l,esr}$ is the inductor series resistance, $I_{L,rms1}$ and $I_{L,rms2}$ are the inductor current rms values during the first and second boost converter DCM subintervals, respectively, $R_{on,n}$ is the NMOS on-resistance and P_{diode} is a numerically integrated diode loss due to $I_{L,rms2}$. The switching loss equations depend on the NMOS gate charge and output capacitance, $Q_{g,n}$ and $C_{oss,n}$, respectively. The total power loss is broken up into three components in (7): the power stage conduction (9) and switching (10) losses, and the power dissipated by the control and optimization circuitry (8), including the clock, MCU, comparator and digital logic.

In dual-FET mode, the conduction and switching losses become

$$P_{cond} = \left(R_{l,esr} \left(I_{L,rms1}^2 + I_{L,rms2}^2 \right) + R_{on,n} \cdot I_{L,rms1}^2 \right.$$
$$\left. + R_{on,p} \cdot I_{L,rms2}^2 \right) \cdot k \tag{11}$$

$$P_{sw} = \left((Q_{g,n} + Q_{g,p}) \frac{V_o}{2} + C_{oss,n} \frac{V_{in}^2}{2} \right) \frac{k}{T_{LF}}. \tag{12}$$

Fig. 11 shows a plot of the converter efficiency for various values of transistor on-time t_1. It can be seen that the optimal value of t_1 decreases (switching frequency increases) as the power levels grow. This can be attributed to two factors: higher power levels permit higher-frequency clocks to be used and conduction losses are lowered due to shorter t_1. Fig. 12 shows the converter efficiency versus power level for single- and dual-FET operation. It can be seen that below approximately 100 μW it is better to operate the converter in single-FET mode because the control losses associated with running the comparator for the high-side driver are greater than the resulting reduction in conduction losses.

V. EXPERIMENTAL RESULTS

A. Converter Efficiency

The steady-state converter efficiency over the expected range of power levels was measured with a power supply and series resistor of 1 kΩ instead of a real rectenna. The converter MCU software was running all of the MPPT and optimization algorithms as in the final application so that the measured efficiency includes the control, conduction and switching losses. The converter was allowed to reach steady-state at each power level before the measurement was made. The result is shown in Fig. 13,
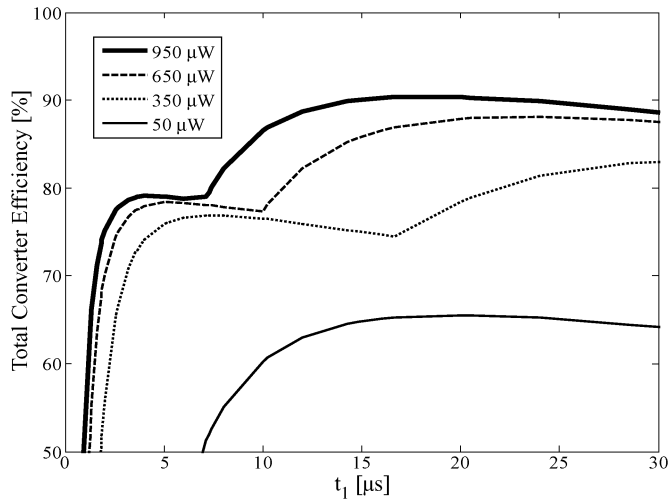
Fig. 11. MATLAB simulation of converter efficiency versus transistor on-time, t_1, for $R_{em} = 1$ kΩ. The maximum efficiency values for several different power levels are stored in a LUT on the MCU for online converter optimization.
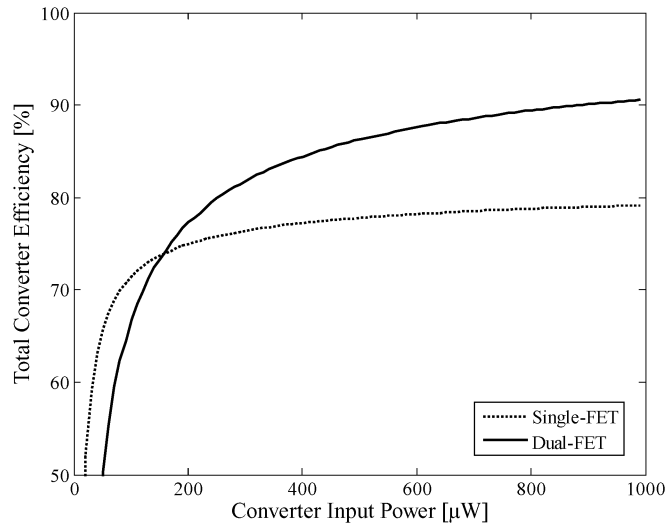

Fig. 13. Experimentally measured total power system efficiency with overlays showing the operating modes used by the converter.

Fig. 12. MATLAB simulation of converter efficiency with optimized t_1 values, for $R_{em} = 1$ kΩ, showing the need to transition between single- and dual-FET operation to maintain maximum efficiency over a wide range of power levels.

with an overlay of the combined maximum efficiency predicted with the MATLAB simulations, showing a good correlation to the measured results. The converter is over 60% efficient at input power levels over 30 μW and can function down to 10 μW at 10% efficiency. If the input power drops below 10 μW, the converter enters the ultra low-power sleep mode as mentioned above, using 1.5 μW. The converter can stay in this mode for approximately 5 years with a fully-charged, 3 V, 100 mAH lithium-ion battery, until power is again applied. This makes the converter truly maintenance-free and robust for use in unknown or changing RF environments.

B. Rectenna Emulator and Converter MPPT Results

The dynamic performance of the converter was also evaluated with the rectenna emulator circuit using the varying cell phone tower data described in Section I. The experiment used
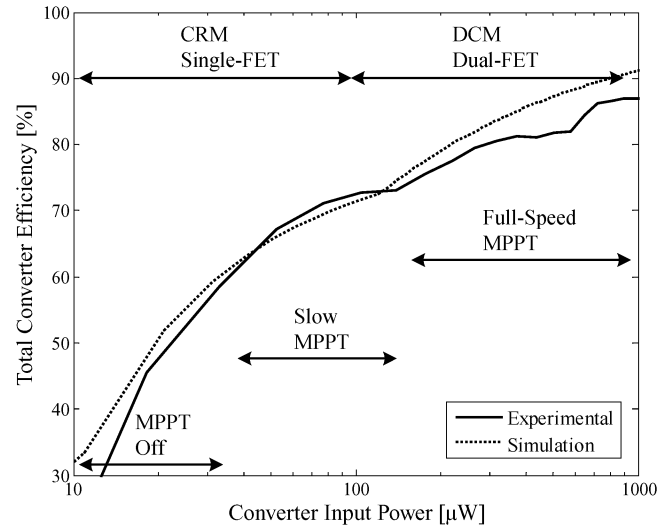
a 24-hour segment of the power data shown in Fig. 2 to update the power density of the rectenna emulator presented in Section III at 1-minute intervals. A series of two separate experiments were conducted as shown in Fig. 14 to compare the performance of the converter against a direct-connect scenario in which the rectenna would be connected to the battery through a diode, as is often done in simple systems, such as RFID. Two experimental configurations were used: (1) rectenna emulator connected to the power converter, and the power converter connected to the battery as shown in Fig. 14(a), and (2) with the power converter removed and the rectenna emulator connected directly to the battery as shown in Fig. 14(b). A 3 V 100 mAh lithium rechargeable battery was used. Each test case (1) and (2) was first run with the emulator array configured with all of the elements in series to achieve an effective 20 kΩ rectenna resistance. The experiment was also performed with high mismatch of the array to the battery with an effective 5 kΩ rectenna resistance to demonstrate a case where the operating conditions and/or rectenna design did not match well to the battery. Each experiment was performed with two different average rectenna power profiles of 250 μW and 125 μW to simulate various cell towers, as shown in Fig. 2, or positions within the RF field.

The converter and direct-connect output power was continuously logged for the duration of the 24-hour experiments by measuring the current flowing into the battery. The current measurement was performed with a 6 1/2 digit Agilent 34411A digital multimeter using a 1 mA range (+/−30 nA). Since the output power was measured at the battery, the resulting power management system efficiency measurement includes the control, switching and conduction losses. The results are shown in Fig. 15(a) for the 125 μW average power, 5 kΩ array case, along with the theoretical maximum available power. Fig. 15(b) and Fig. 15(c) show the fraction of the total available energy that is extracted from the array for the above cases by integrating the experimental power data. In the case of very good matching of the rectenna to the battery, the total integrated energy is larger with the converter for both the 125 μW and 250 μW average power profiles. In the high-mismatch array case, the converter
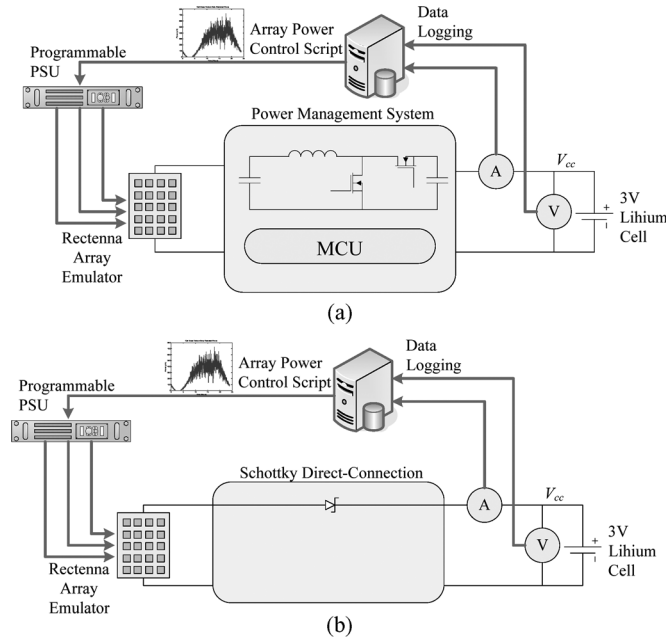
Fig. 14. Experimental test setups. Two different series of experiments were performed in which the total harvested energy of the power management system (a) was measured and compared to a direct-connect case (b) in which the rectenna emulator was connected to the battery through a Schottky diode.

harvests several times more energy, because the MPPT algorithm is able to adapt to the different array resistance. Considering that even the direct-connect approach would require a battery charge-controller or monitor that is already built into the adaptive power management system and would consume extra power, the addition of the proposed power management system is justified.

VI. CONCLUSIONS

An adaptive MPPT power management system was demonstrated, showing that an off-the-shelf microcontroller and other discrete components can be used to construct a "smart" power converter capable of extracting near-maximum power from an arbitrary rectenna array at sub-milliwatt power levels. The design can also be easily scaled to different power levels by changing the size of the rectenna array. High conversion efficiency will be maintained due to the adaptive optimization algorithms. Such a converter significantly improves the harvested power relative to a direct-connect system often employed in rectenna harvesting applications.

In addition, a rectenna emulator circuit was designed to show how the developed low-frequency model can be used to emulate any rectenna design and assist in understanding low-frequency rectenna behavior in general, as well as in testing and debugging power management circuitry.
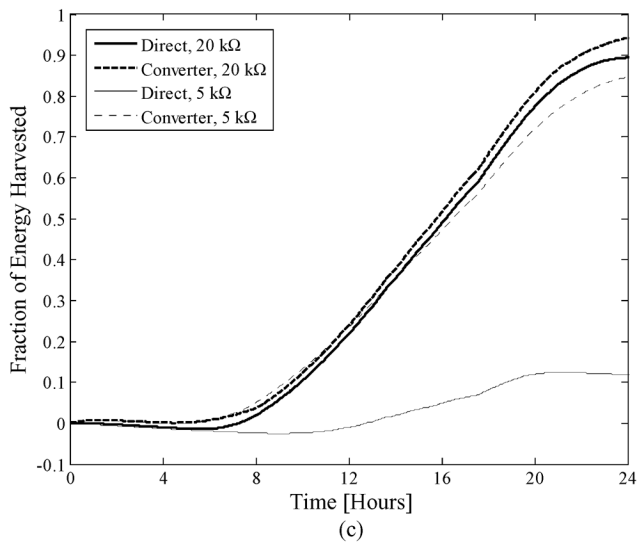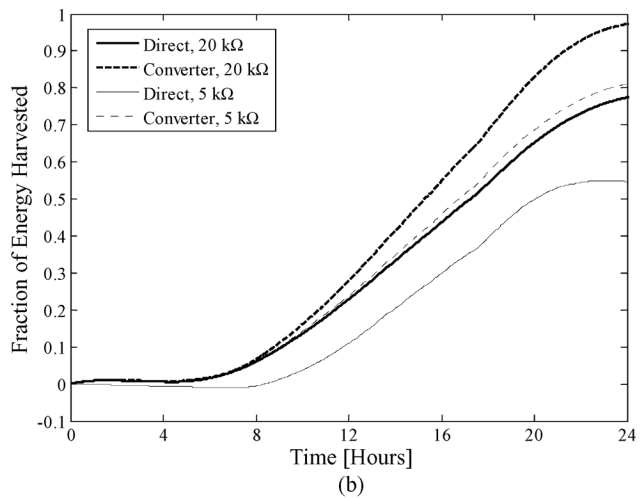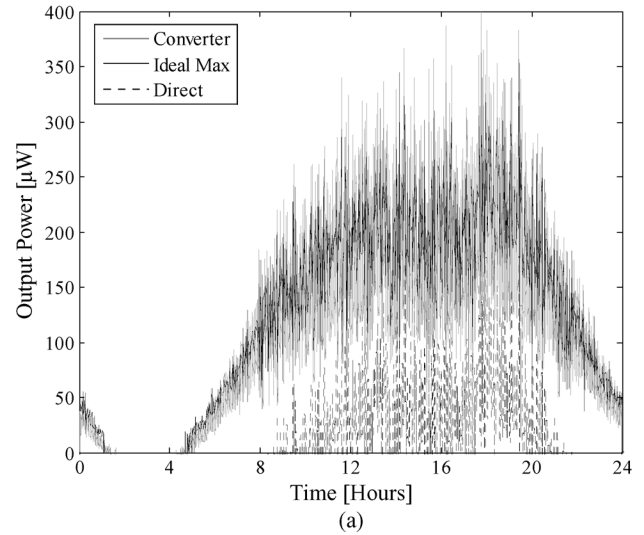
Fig. 15. Experimentally measured improvement in rectenna energy extraction with MPPT boost converter compared to a direct connection to a 3 V battery. (a) Output power over a 24-hour period for a 5 kΩ array and 125 μW average power. Fraction of total possible energy harvested over a 24-hour period for (b) 250 μW average power profile and (c) 125 μW average power. For the 250 μW power profile, the MCU adjusted t_1 over the range from 6 μs to 28 μs and the value of k varied from 0.17% to 0.58%.

REFERENCES

[1] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, May 2008.

[2] H. Lhermet, C. Condemine, M. Plissonnier, R. Salot, P. Audebert, and M. Rosset, "Efficient power management circuit: From thermal energy harvesting to above-IC microbattery energy storage," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 246–255, Jan. 2008.

[3] C. Alippi and C. Galperti, "An adaptive system for optimal solar energy harvesting in wireless sensor network nodes," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 55, no. 6, pp. 1742–1750, Jul. 2008.

[4] B. Jiang, J. Smith, M. Philipose, S. Roy, K. Sundara-Rajan, and A. Mamishev, "Energy scavenging for inductively coupled passive RFID systems," in *Proc. IEEE Instrumen. Meas. Technol. Conf., IMTC 2005*, May 16–19, 2005, vol. 2, pp. 984–989.

[5] R. J. Gutmann and J. M. Borrego, "Solar power satellite rectenna design study: directional receiving elements and parallel-series combining analysis," NASA Final Rep. NAS9- 15453, Dec. 1978, Ch. 3.

[6] J. O. McSpadden, F. E. Little, M. B. Duke, and A. Ignatiev, "An in-space wireless energy transmission experiment," in *Proc. IECEC Energy Conversion Eng. Conf.*, Aug. 1996, vol. 1, pp. 468–473.

[7] W. C. Brown and E. E. Eves, "Beamed microwave power transmission and its application to space," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 6, pp. 1239–1250, Jun. 1992.

[8] T. Haumann, U. Munzenberg, W. Maes, and P. Sierck, "HF-radiation levels of GSM cellular phone towers in residential areas," in *Proc. 2nd Int. Workshop on Biological Effects of EMFS*, Oct. 2002, vol. 1, pp. 327–333.

[9] D. Willkomm, S. Machiraju, J. Bolot, and A. Wolisz, "Primary users in cellular networks: A large-scale measurement study," in *Proc. 3rd IEEE Symp. New Frontiers in Dynamic Spectrum Access Networks, DySPAN 2008*, Oct. 14–17, 2008, pp. 1–11.

[10] J. Hagerty, F. Helmbrecht, W. McCalpin, R. Zane, and Z. Popovic, "Recycling ambient microwave energy with broadband rectenna arrays," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 3, pp. 1014–1024, Mar. 2004.

[11] R. J. Gutmann and J. M. Borrego, "Power combining in an array of microwave power rectifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 12, pp. 958–968, Dec. 1979.

[12] N. Shinohara and H. Matsumoto, "Dependence of dc output of a rectenna array on the method of interconnection of its array elements," *Elect. Eng. Jpn.*, vol. 125, no. 1, pp. 9–17, 1998.

[13] J. Appelbaum, M. Shechter, J. Bany, and G. Yekutieli, "Array representation of nonidentical electrical cells," *IEEE Trans. Electron Devices*, vol. 29, no. 8, pp. 1145–1151, Aug. 1982.

[14] T. Paing, J. Shin, R. Zane, and Z. Popovic, "Resistor emulation approach to low-power RF energy harvesting," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1494–1501, May 2008.

[15] T. Paing, J. Morroni, A. Dolgov, J. Shin, J. Brannan, R. Zane, and Z. Popovic, "Wirelessly-powered wireless sensor platform," in *2007 European Conf. Wireless Technologies*, Oct. 8–10, 2007, pp. 241–244.

[16] T. Paing, E. Falkenstein, R. Zane, and Z. Popovic, "Custom IC for ultra-low power RF energy harvesting," in *Proc. Applied Power Electronics Conf. (APEC)*, Washington DC, Feb. 15–19, 2009, pp. 1–7.

[17] P. Niu and P. Chapman, "Design and performance of linear biomechanical energy conversion devices," in *Proc. 37th IEEE Power Electron. Spec. Conf., PESC'06*, Jun. 18–22, 2006, pp. 1–6.

[18] M. D. Seeman, S. R. Sanders, and J. M. Rabaey, "An ultra-low-power power management IC for wireless sensor nodes," in *Proc. IEEE Custom Integrated Circuits Conf., CICC'07*, Sep. 16–19, 2007, pp. 567–570.

[19] T. Esram, J. W. Kimball, P. T. Krein, P. L. Chapman, and P. Midya, "Dynamic maximum power point tracking of photovoltaic arrays using ripple correlation control," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1282–1291, Sep. 2006.

[20] E. Koutroulis, K. Kalaitzakis, and N. C. Voulgaris, "Development of a microcontroller-based, photovoltaic maximum power point tracking control system," *IEEE Trans. Power Electron.*, vol. 16, no. 1, pp. 46–54, Jan. 2001.

[21] B. M. Wilamowski and L. Xiangli, "Fuzzy system based maximum power point tracking for PV system," in *Proc. IEEE 28th Conf. Indust. Electron. Soc., IECON'02*, Nov. 2002, vol. 4, pp. 3280–3284.

[22] A. Pandey, N. Dasgupta, and A. K. Mukerjee, "A simple single-sensor MPPT algorithm," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 698–700, Mar. 2007.

[23] X. Liu and L. A. C. Lopes, "An improved perturbation and observation maximum power point tracking algorithm for PV arrays," in *Proc. IEEE 35th Power Electron. Spec. Conf.*, Jun. 2004, vol. 3, pp. 2005–2010.

[24] D. P. Hohm and M. E. Ropp, "Comparative study of maximum power point tracking algorithms using an experimental, programmable, maximum power point tracking test bed," in *Conf. Rec. 28th IEEE Photovoltaic Specialists Conf.*, 2000, pp. 1699–1702.

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