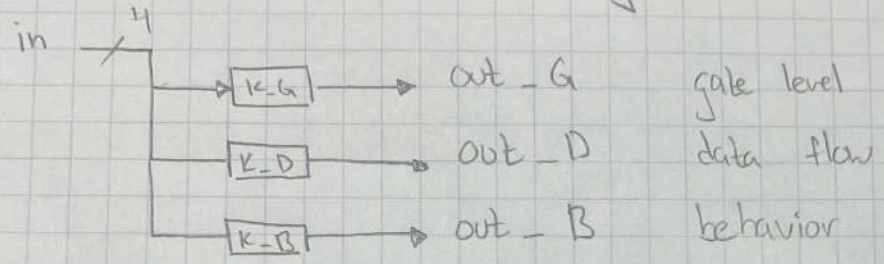
ab \ cd	c'd'	c'd	cd	cd'
a'b'	0	1	3	2
a'b	4	5	7	6
ab	12	13	15	14
ab'	8	9	11	10

2) K-map

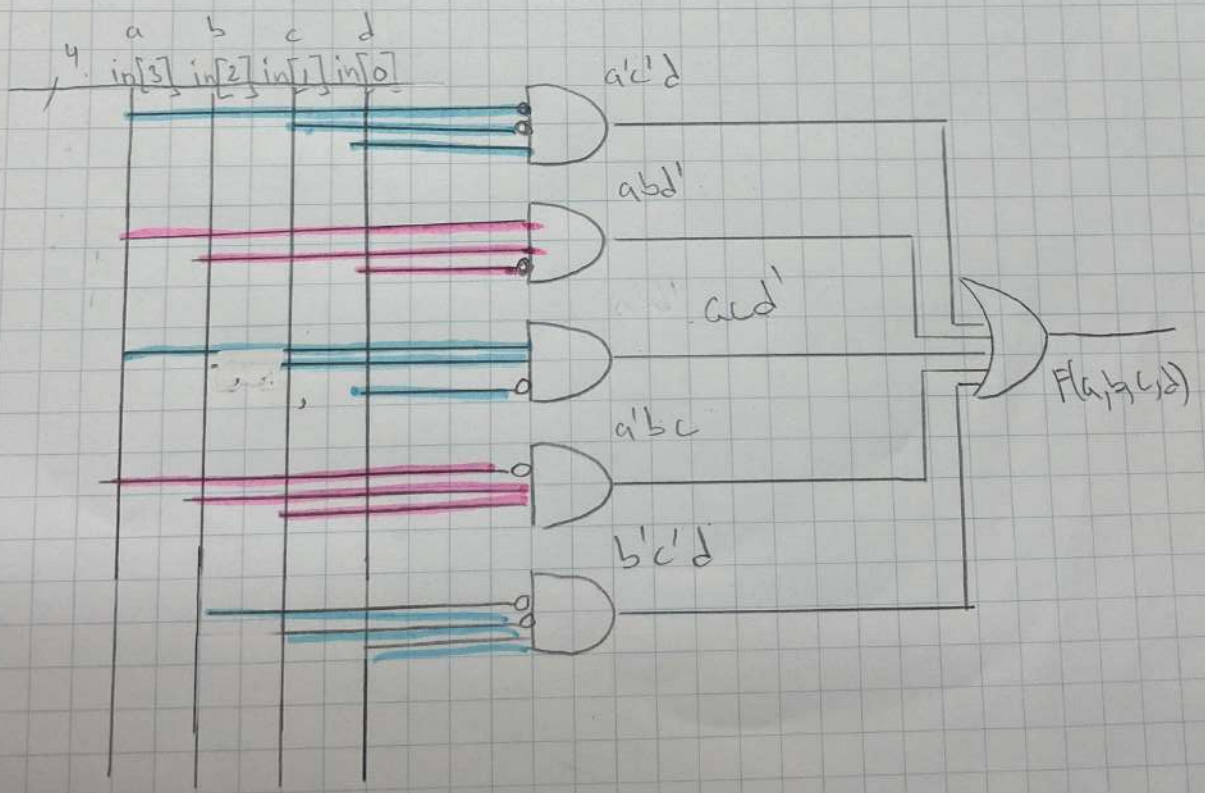
$da'c' + abd' + acd' + a'cb + b'c'd$

1) Design Process



3) Structure

$F(a,b,c,d) = a'c'd + abd' + acd' + a'bc + b'c'd$



Design Process =>

1) Figured out the k-map algorithm
2) Structurally designed the circuits
3) Implemented the codes from happy verilog

Problems faced =>

In coding verilog, realising it is spare sensitive

For example =>

in != 6 ==ϕ in != 6