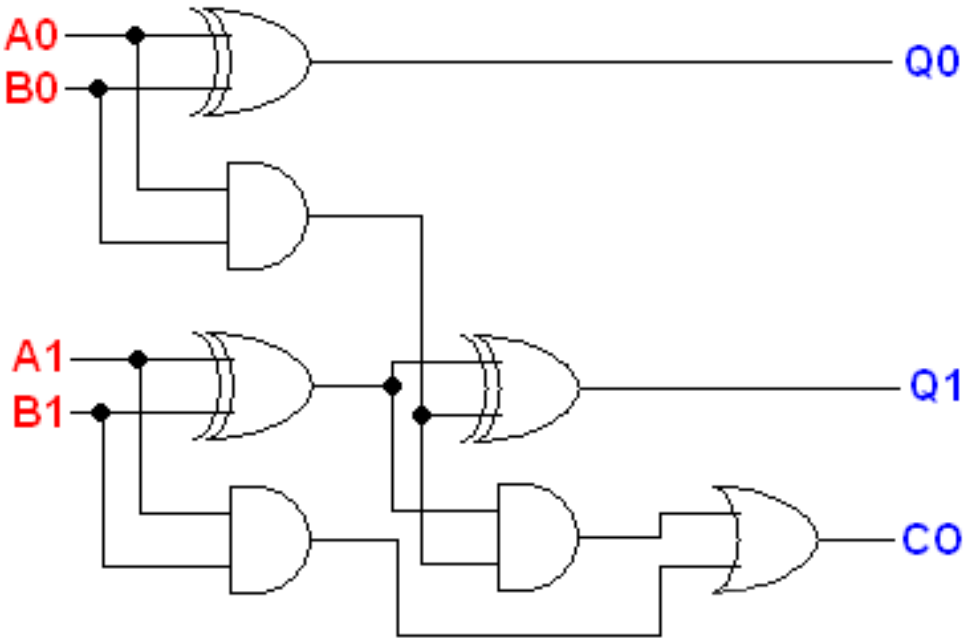
Logic Design Spring 2021 Midterm Exam II

Name: Student ID Number:

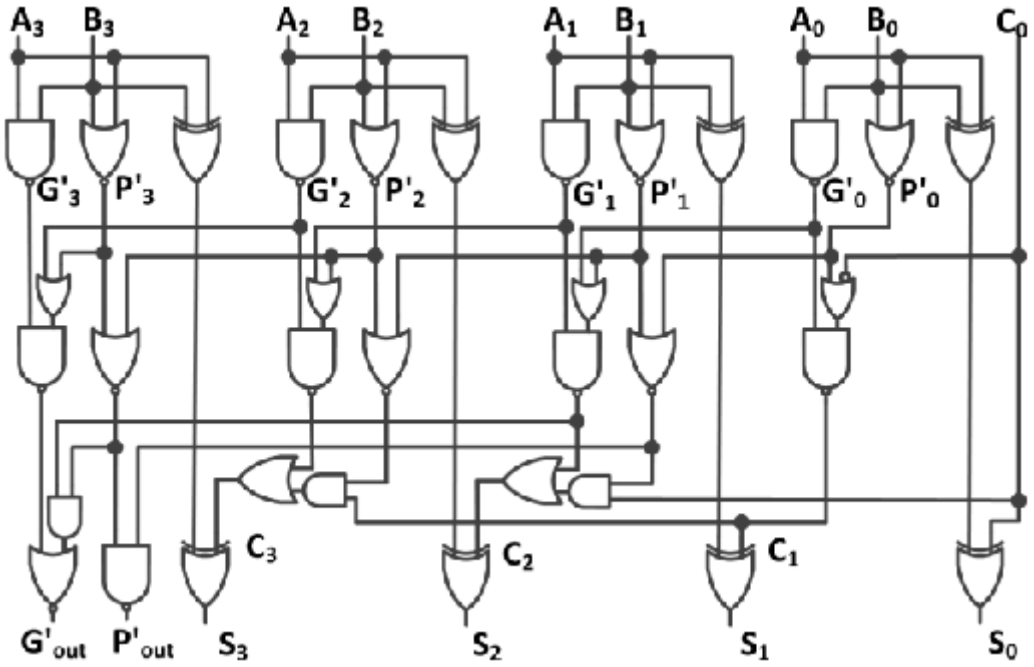
1. For each of the following statements, answer if it is true or false.
   a. “And” gate is functionally complete. (2 points)
   b. In Verilog, the symbols “~” and “!” are functionally different for one bit operand. (2 points)
   c. In Verilog, when declaring module outputs, they can only be “reg” type. (2 points)
   d. In Verilog, when declaring module inputs, they can be either “reg” type or “wire” type. (2 points)
   e. Both combinational and sequential circuits contain memory elements and logic gates.(2 points)

2. Convert 2’s complement binary number 11101111 to a decimal number. (5 points)
3.
   a. Using a decoder and OR gates only to construct a combinational circuit that implements the following two Boolean functions. (5 points)
      F1 = yz + x’y + y’z’
      F2 = (x’ + y)z + xy’z
   b. Redo 3(a) using a decoder and NAND gates only. (3 points)

4. Assume the delays of “not”, “nand”, “nor”, “and”, “or” and “xor” gates are 1, 2, 2, 3, 3 and 4 units, respectively.
   a. Given the following 2-bit adder, compute the delays of outputs Q1 and C0. (5 points)



b. Given the following 4-bit carry lookahead adder, compute the delays of outputs S_3, G'_{out} and P'_{out} .(5 points)



5.

a. Design a combinational circuit with input X[2 : 0] and outputs A, and Y[1 : 0] When (X mod 3) equals zero, A is one and Y is don't care. Otherwise, A is zero and Y is the integer part of X / 3. (10 points)

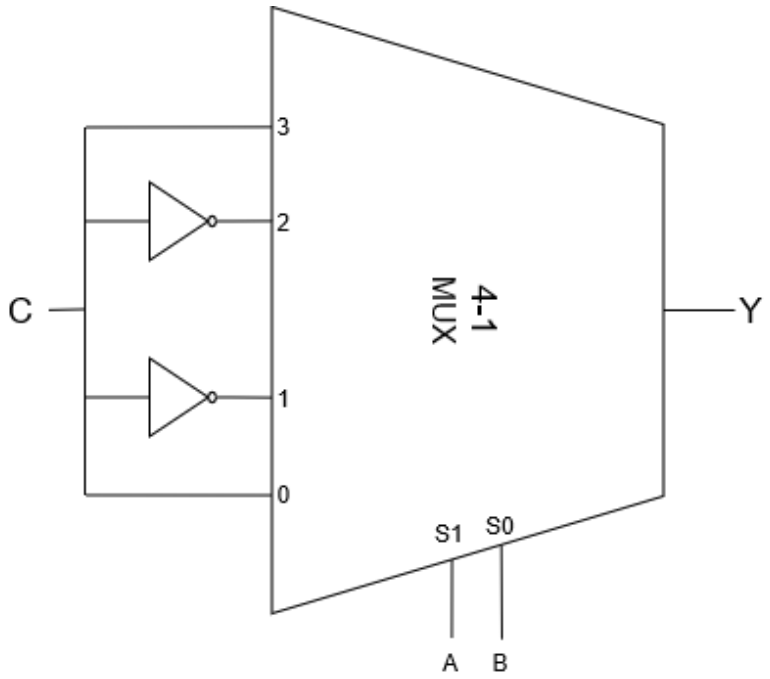
b. Finish the Verilog code of the above circuit. (5 points)

```
module NTHU(X, A, Y);
    input [2:0] X;
    output A;
    output [1:0] Y;

    assign A = ?
    assign Y[1] = ?
    assign Y[0] = ?

endmodule
```

6. Given a four-input function f(w, x, y, z) = Σm(0, 2, 4, 5, 7, 8, 10, 11, 15) + Σd(3, 13) Please answer the following questions for the function f.
   a. List all prime implicants. (5 points)
   b. List all essential prime implicants. (5 points)

7. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components. (5 points)

8. Given a 4-to-1 multiplexer below.
   What is the function Y = f(A, B, C) it implements? (5 points)



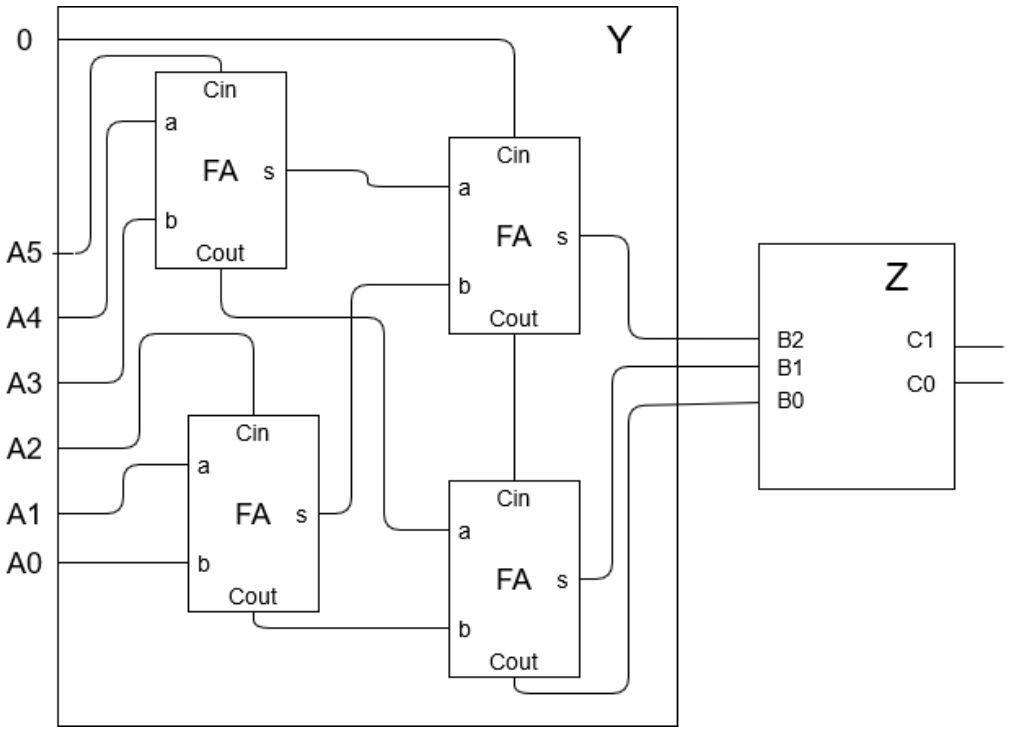
9. Implement a full adder in two different ways below.
   a. Using two 8-to-1 MUXes. Connect X, Y, and Cin to the control inputs of the MUXes and connect 1 or 0 to each data input. (5 points)

   b. Using two 4-to-1 MUXes and one inverter. Connect X and Y to the control inputs of the MUXes, and connect 1, 0, Cin or Cin' to each data input. (5 points)

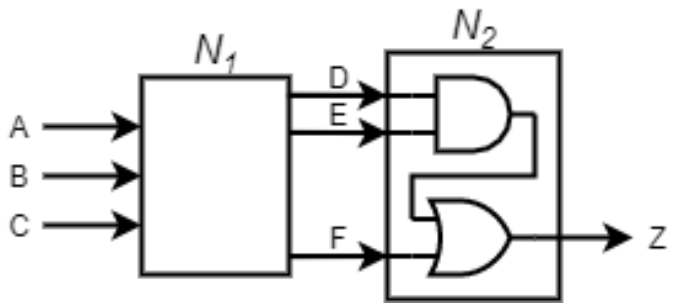
10. The circuit below contains two sub-circuits, a sub-circuit Y with input A[5: 0] and output B[2: 0], and a sub-circuit Z with input B[2: 0] and output C[1: 0].

    a. The “FA” components inside Y are one-bit full adders. What is the function of Y? (5 points)

    b. Design the combinational circuit Z, when the input B is larger than 3, the output is 2’b01, when it is smaller than 3, output is 2’b00, and when the input equals 3, C[1] is 1 and C[0] is don’t care. (5 points)



11. A combinational circuit *N* is divided into two subcircuits N_1 and N_2 as shown. The truth table for N_1 is given.
    a. Find the output Z as a function of A, B and C. (6 points)



    b. Assume that the input combinations ABC=110 and ABC=010 never occur. Change as many of the values of D, E and F to don't care as you can without changing the value of the output Z. (6 points)

A	B	C	D	E	F
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	1	0	0	0