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|---|---|
| 文档版本 | |
| 发布日期 | |

# CH2201 数据手册

芯片开放社区
Open Chip Community

# 前言

## 概述

本文为 CH2201 的数据手册。

## 产品版本

与本文档相对应的产品版本如下。

| 产品名称 | 产品版本 |
| --- | --- |
| CH2201 数据手册 | V01 |

## 读者对象

本文档（本指南）主要适用于使用 CH2201 嵌入式开发。

## 修订记录

修订记录累积了每次文档更新的说明。

| 修订日期 | 修订版本 | 修订说明 |
| --- | --- | --- |
| | 修订前：无<br>修订后：无 | |

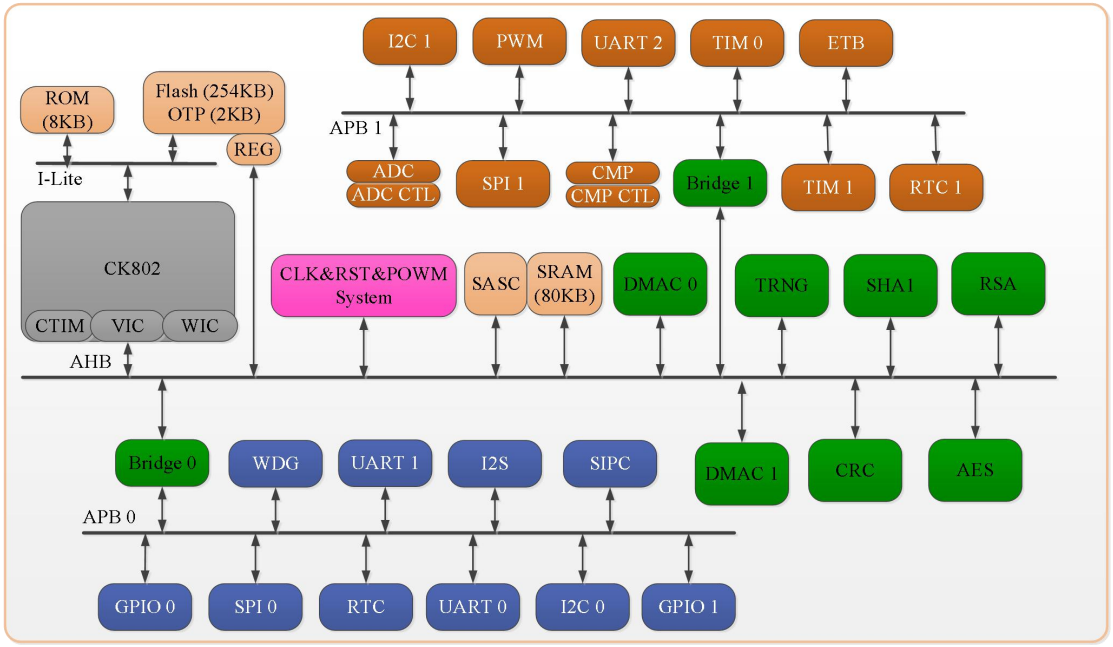
# 目录

# 1. Overview

## 1.1 Block Diagram

CH2201 is a CK802T based platform typically for many kinds of ultra-low power applications. CK802T are C-SKY Company's independently developed 32-bits processors which C-SKY Company owns its intellectual property. CK802T provide high performance with lower power cost. The CH2201 architecture block diagram is shown in Figure 1- 1

Figure 1- 1 CH2201 Block Diagram




CH2201 contains 256K EFLASH and 32+32K+16K internal SRAM. The 8K SRAM is security SRAM for TEE operating system. The 80K SRAM is retention SRAM for low power mode.

## 1.2 Functional Features

- ✧ **CPU Part**
  - ■ **32-bit general purpose CPU CK802T**
    - ◆ In-order issue, execution and retiring

- 32-bit Data Length and 32-bit/16-bits length Instructions
- Tightly coupled IP: System Timer (Core Timer), Vector interrupt (VIC) and Wakeup interrupt (WIC).
- Support anti-Differential Power analysis
- Performance: 0.9DMIPS/MHz

**CoreTim**

- The circulating decrement counter is 24-bit count width
- Two clock sources: CPU clock and external reference clock that connects to external high speed clock and external low speed clock

**VIC**

- Supports 32 Interrupts nesting
- Each interrupt has corresponding priority

**WIC**

- Used for wake up system when enters low power mode

✧ **Interconnection & Memory Part**

**Bus interconnection**

- One 32-bit instruction AHB-Lite bus
- One 32-bit AHB bus for CPU operation, memory access and APB bus interconnection
- Two 32-bit APB bus for low speed peripheral connection

**Memory**

- 80KB on-chip SRAM
- 256KB on-chip flash
- 8K ROM for boot

✧ **Characteristics of Peripherals**

- **DMAC (×2)**
  - 2 channels
  - 16 handshake interfaces
  - Handshaking interface supports single or burst DMA transactions
- **CRC**
  - **8-bit/16-bit fast verify functionality**
- **AES**
  - supports three different length of key, which are called AES-128, AES-192, AES-256
  - Supports both ECB (Electronic Code Book) mode and CBC (Cipher Block Chaining) mode
- **SHA1/256/512**
  - Supports 1 hash algorithm: SHA-1
- **TRNG**
  - Random number generator
- **RSA**
  - It supports 192, 256, 512, 1024, 2048 bits modular exponentiation operations
- **SIPC**
  - Connects to APB0
  - Controls all peripherals' security attributes
- **ETB**
  - Connects to APB1
  - Up to 5 trigger input sources and 1 software trigger source
    - 1 input source for CMP output

- 2 input source for external (PAD) input
- 1 input source for PWM event output
- 1 input source for TIM event output
- 1 input source for software trigger

◆ Up to 4 trigger output

- 1 output channel for ADC
- 3 output channel for three counters in PWM

■ **RTC (×2)**

◆ RTC 0 connects to APB0, RTC 1 connects to APB1

◆ 32-bit count width

◆ Incrementing counter and comparator for interrupt generation

■ **PWM**

◆ Connects to APB1

◆ 12 input/output channels

◆ 6 PWM generators, each with 1 16-bit counter, 2 PWM comparator, 1 PWM signal generator, 1 interrupt generator

◆ Each PWM signal generator contains 2 channels

◆ Prescaler divide-by 1, 2, 4, 8, 16, 32, 64 or 128

◆ PWM output enable or disable of each PWM signal

◆ Optional output inversion of each PWM signal (polarity control)

◆ 6 16-bit counter and each has the following characteristics:

- Up or Up/Down mode
- Output frequency controlled by a 16-bit load value

- 16-bit input capture modes
  - Input edge count mode
  - Input edge time mode
- ADC event trigger
  - Can trigger an ADC sample sequence

■ **WDT**

- 1 watch dogs WDT in APB0
- Each WDT has 32 count width
- Counter counts down from a pre-set value to zero to indicate the occurrence of a timeout

■ **GPIO (×2)**

- Connects to APB0
- Gpio0 supports 28-bit width
- Gpio1 supports 4-bits width
- Each bit of GPIO supports interrupt generation
- Individually configurable pull-up or pull-down resistors
- GPIO0 is non-secure port, GPIO1 is secure port

■ **I2S**

- Connects to APB0
- Serial-Master or serial-slave operation
- FIFO-The depth of the transmitter and receiver FIFO is 32 while the width is 32-bit
- support 16-bit, 44.1/48 KHz sample rate

- DMA request generation

- **ADC**
  - Connects to APB0
  - 16 external input channels
  - 12-bit resolution
  - Up to 1M KSPS conversion rate
  - Interrupt generation at the end of regular conversion
  - Single and continuous conversion modes
  - Supports external trigger input
  - ADC input range: AGND≤Vin≤AVDD
  - DMA request generation during regular channel conversion
- **CMP**
  - Connects to APB1
  - 2 external input channels
  - Interrupt generation capability
  - Hysteresis function
- **TIM (×2)**
  - connects to APB1
  - All of timers are 32-bit count width
  - All of timers support for two operation modes: free-running and user-defined count
- **SPI (×2)**
  - 1 SPI in APB0 supports 1 slave selection when function as master, 1 SPI in APB1 supports 3 slaves selection when function as master
  - Each SPI module supports master and slave

- The depth of transmit/ receive FIFO buffers is 32 words deep
- DMA Controller Interface

- **I2C (×2)**
  - 1 I2C connects to APB0 and 1 I2C connects to APB1
  - Both I2Cs support master or slave I2C operation
  - Transmit and receive FIFO_DEPTH is 8 , data is 8 bits width
  - DMA handshaking interface
- **UART (×3)**
  - 2 UARTs that UART 0 and UART 1 in APB0 and UART 2 in APB1
  - Transmit and receive FIFO depths of 16
  - Additional DMA interface signals

# 2. Clock Domain

CH2201 has five clock sources such as EHS, IHS, PLL, ELS, ILS. EHS is 8-24MHz. HIS is 8MHz. PLL is 20-48MHz. EHS, IHS, PLL are high speed clock source. ELS is 32.768 KHz and ILS is 10KHz for RTC and low power mode.

EHS and ELS are external clock sources. ILS, IHS, PLL are internal clock sources. When the chip powers up, the default clock source is IHS.

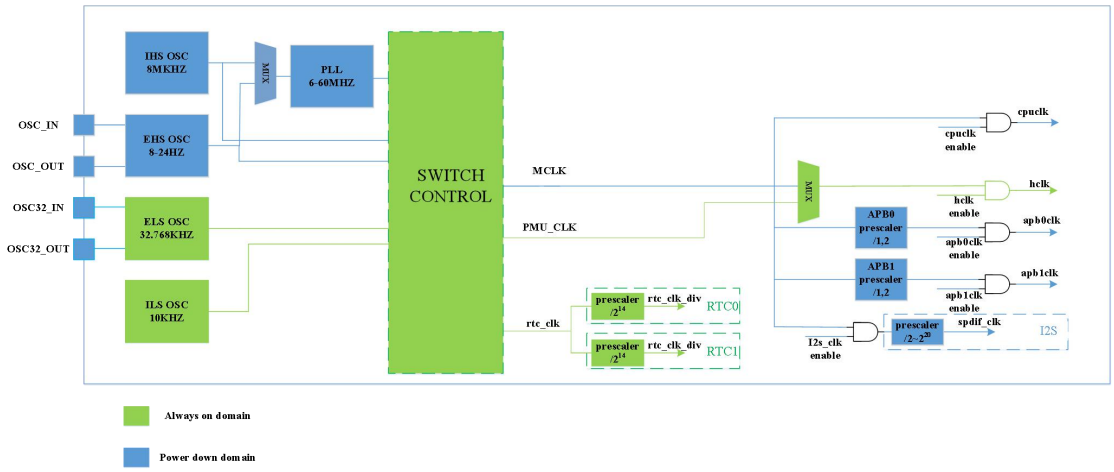
The max frequency of CK802T is 48M.

CPU, SRAM and EFLASH are in the same clock domain using CPU_CLK. Security Sub System is in DIV clock domain using SEU_CLK. All peripherals are in the same clock domain using APB_CLK. APB_CLK should be more than one if there are two or more APB bus.

In low power mode except the wait mode the main clock is low speed clock such as ELS or ILS selected by user.

The clock source dynamic switch is supported in CH2201 and the clock divider dynamic switch is also supported.

Figure 2- 1 CH2201 clock domain




## 3. Reset Domain

CH2201 has three function reset and one low power reset. If function reset is enable all chip will be reset. If low power reset is enable only the function logic will be reset, the wake-up logic will not be reset.

When stop mode and standby mode exited the low power reset will be enabled.

All reset in chip are asynchronous reset.

## 4. Power Domain

CH2201 has five power modes: run mode, wait mode, doze mode, stop mode and standby mode.

- Run Mode: CPU is free run and most peripheral is active.
- Wait Mode: CPU is clock gated and peripherals' clock statuses are configurable by the program.

- Doze Mode: All clocks except the wake-up logic are gated.
- Stop Mode: Some critical register data stored in SRAM, so that system can restore quickly.
- Standby Mode: Some critical register data and data in SRAM stored in Eflash, which results to restore system slowly.

CH2201 has three power domain: always on power domain, SMS power domain and power down power domain.

Always on power domain has wake up logic, RTC, and IO. The clock is very slowly such as 32.768 KHz. In standby mode only the always on power domain is active.

SMS power domain has retention SRAM.

Power down domain has other logic.

In run mode, wait mode, doze mode all power domains are power on. In stop mode power down domain is power off but the SMS power domain and always on power domain are power on. In standby mode only always on power domain is power on.

After wait mode, doze mode program will be executed from the instruction after wait or doze instruction or from the interrupt service routine.

Before stop mode the critical context will be store in the 80KB retention SRAM. After waked up the context will be restored from the retention SRAM for performance.

Before standby mode the critical context will be store in the FLASH. After waked up the context will be restored from the FLASH for low power.

In run mode the active power is less than 300uA/MHZ.

In wait mode the power is less than 1mA.

In doze mode the power is less than 70uA.

In stop mode the power is less than 20uA.

In standby mode the power is less than 3uA.

# 5. Address Map

## 5.1 Address Overview

For this chip, the memory address is divided into several parts: on-chip memory, off-chip memory, TCIP and peripherals. The detailed address map is shown as below.

Table 5- 1 Memory Address Map

| Address Range | Size | Usage |
|---|---|---|
| 0x0000_0000~0x0000_1FFF | 8KB | ROM for boot |
| 0x1000_0000~0x1003_F7FF | 256KB | EFlash |
| 0x4003_F000~0x4003_FFFF | 2KB (OTP) + 2KB (REG) | |
| 0x4000_0000~0x5001_FFFF | 262272KB | Peripherals |
| 0x6000_0000~0x6001_3FFF | 80KB | On-chip SRAM |
| 0xE000E000~0xE000ECFF | | TCIP |
| Others | | Reserved |

## 5.2 Peripheral Address Map

The register blocks for all on-chip peripheral devices are located on 4KB boundaries. Those modules that may require additional address space are assigned additional 4KB blocks. Within a 4KB block, peripheral registers may be incompletely decoded. The description of each peripheral will define the result of accesses to unimplemented registers. For registers that do not implement all 32 bits, the unimplemented bits will return zero when read, and write to the unimplemented bits will have no effect. In general, unimplemented bits should return zero to ensure future compatibility.

Table 5- 2 Peripheral Address Map

| Address Range | IP name | Master/Slave | Description |
|---|---|---|---|
| I-AHB Lite | | | |
| | CK802 | M | Core |
| 0x0000_0000~0x0000_1FFF | ROM | S0 | ROM for boot |
| 0x1000_0000~0x1003_F7FF | EFC | S1 | 256KB Flash |
| AHB | | | |
| | CK802 | M1 | Core |
| 0x4000_0000~0x4000_0FFF | AHB Arb | S0 | AHB Arbiter |
| 0x4000_1000~0x4000_1FFF | DMAC0 | M2/S1 | DMA Controller0 |
| 0x4000_2000~0x4000_ | CLKGEN | S2 | CLK&RST&POW |

| | | | |
|---|---|---|---|
| 2FFF | | | M Management |
| 0x4000_3000~0x4000_3FFF | CRC | S3 | CRC Check |
| 0x4000_4000~0x4000_5000 | DMAC1 | M3/S4 | DMA Controller1 |
| 0x4003_F000~0x4003_FFFF | 2KB (OTP) + 2KB (REG) | S5 | Flash |
| 0x4000_6000~0x4000_6FFF | AES | S6 | AES |
| 0x4000_7000~0x4000_7FFF | SRAM SASC | S7 | SRAM SASC |
| 0x4000_8000~0x4000_8FFF | SHA-1 | M4/S8 | SHA-1 |
| 0x4000_9000~0x4000_9FFF | TRNG | S9 | TRNG |
| 0x4000_A000~0x4000_AFFF | RSA | S10 | RSA |
| 0x5000_0000~0x5000_FFFF | APB 0 Bridge | S11 | APB 0 Bridge |
| 0x5001_0000~0x5001_FFFF | APB 1 Bridge | S12 | APB 1 Bridge |
| 0x6000_0000~0x6001_3FFF | SRAM | S13 | 80KB on-chip SRAM |
| APB 0 | | | |
| 0x5000_1000~0x5000_ | WDT | P00 | Watch Dog |

| | | | |
|---|---|---|---|
| 1FFF | | | |
| 0x5000_2000~0x5000_2FFF | SPI 0 | P01 | SPI 0 |
| 0x5000_3000~0x5000_3FFF | RTC 0 | P02 | Real Time Clock 0 |
| 0x5000_4000~0x5000_4FFF | UART 0 | P03 | UART 0 |
| 0x5000_5000~0x5000_5FFF | UART 1 | P04 | UART 1 |
| 0x5000_6000~0x5000_6FFF | GPIO 0 | P05 | GPIO 0 |
| 0x5000_7000~0x5000_7FFF | I2C 0 | P06 | I2C 0 |
| 0x5000_8000~0x5000_8FFF | I2S | P07 | I2S |
| 0x5000_9000~0x5000_9FFF | GPIO 1 | P08 | GPIO 1 |
| 0x5000_A000~0x5000_AFFF | SIPC | P09 | Secure IP Controller |
| APB 1 | | | |
| 0x5001_1000~0x5001_1FFF | TIM 0 | P10 | Timer A |
| 0x5001_2000~0x5001_2FFF | SPI 1 | P11 | SPI 1 |

| | | | |
|---|---|---|---|
| 0x5001_3000~0x5001_3FFF | I2C 1 | P12 | I2C 1 |
| 0x5001_4000~0x5001_4FFF | PWM | P13 | PWM |
| 0x5001_5000~0x5001_5FFF | UART 2 | P14 | UART 2 |
| 0x5001_6000~0x5001_6FFF | ADC CTL | P15 | ADC Controller |
| 0x5001_7000~0x5001_7FFF | CMP CTL | P16 | CMP Controller |
| 0x5001_8000~0x5001_8FFF | ETB | P17 | Event Trigger Block |
| 0x5001_9000~0x5001_9FFF | TIM 1 | P18 | Timer B |
| 0x5001_A000~0x5001AFFF | RTC 1 | P19 | Real Time Clock 1 |

## 5.3 TCIP Address Map

There are some IPs integrated to CK802T closely, which are called TCIPs. The address map of these IPs is shown below.

Table 5- 3 TCIP Address Map

| Address Range | TCIP Name |
|---|---|
| 0xE000E010~0xE000E0FF | Core Timer |
| 0xE000E100~0xE000ECFF | Vector Interrupt Controller(VIC) |

# 6. Pin List

Table 6- 1 Pin List

| P 64 | PIN NAME | DEFAULT | | |
|---|---|---|---|---|
| | | FUNC | SEL | FUNCTION |
| 1 | DVSS | Digital Ground | | |
| 2 | DVSS | Digital Ground | | |
| 17 | DVDD | 3.3V Power Supply | | |
| 18 | DVSS | Digital Ground | | |
| 19 | AVDD | 3.3V Power Supply | | |
| 20 | AVSS | Analog Ground | | |
| 23 | AVDD | 3.3V Power Supply | | |
| 26 | AVSS | Analog Ground | | |
| 27 | AVDD | 3.3V Power Supply | | |
| 28 | AVSS | Analog Ground | | |
| 37 | DVSS | Digital Ground | | |
| 40 | DVSS | Digital Ground | | |
| 43 | DVSS | Digital Ground | | |
| 46 | DVDD | 3.3V Power Supply | | |
| 49 | VCORECP | 1.5V Coupling | | |
| 50 | VCORECP | 1.5V Coupling | | |
| 51 | VCORECP | 1.5V Coupling | | |
| 52 | VCORECP | 1.5V Coupling | | |
| 53 | DVDD | 3.3V Power Supply | | |
| 54 | DVSS | Digital Ground | | |
| 59 | VCORECP | 1.5V Coupling | | |
| 60 | VCORECP | 1.5V Coupling | | |

| | | | | |
|---|---|---|---|---|
| 31 | PIN_EHS | EHS_I | | osc input |
| 32 | POUT_EHS | EHS_O | | osc output |
| 21 | PIN_ELS | ELS_I | | osc input |
| 22 | POUT_ELS | ELS_O | | osc output |
| 25 | ADC_VREFP | ADC Refernce Positive Input | | power supply |
| 24 | ADC_VREFN | ADC Refernce Negative Input | | power supply |
| 30 | MCURST | MCURST | | external reset |
| 29 | TEST_MODE | DFT | | test mode enable |
| 33 | PA0_TRIG0_ACMP1P_TCK | JTAG.TCK | 0 | ETB.TRIG0 |
| | | (GPIOA.0) | 1 | |
| | | | 10 | JTAG.TCK |
| 34 | PA1_TRIG1_ACMP1N_TMS | JTAG.TMS | 0 | ETB.TRIG1 |
| | | (GPIOA.1) | 1 | |
| | | | 10 | JTAG.TMS |
| 39 | PA2_TXD0_SPI0TXD | GPIOA.2 | 0 | UART0.TX |
| | | | 10 | SPI0.TXD |
| | | | 11 | UART0.SIROUT |
| 42 | PA3_RXD0_SPI0RXD | GPIOA.3 | 0 | UART0.RX |
| | | | 10 | SPI0.RXD |
| | | | 11 | UART0_SIRIN |
| 41 | PA4_CTS0_PWM0_SPI0SCK_TRIG0 | GPIOA.4 | 0 | UART0.CTS |
| | | | 1 | PWM.CH0 |
| | | | 10 | SPI0.CLK |
| | | | 11 | ETB.TRIG0 |
| 38 | PA5_RTS0_PWM1_SPI0SSN_TRIG1 | GPIOA.5 | 0 | UART0.RTS |

| | | | | |
|---|---|---|---|---|
| | | | 1 | PWM.CH1 |
| | | | 10 | SPI0.CS |
| | | | 11 | ETB.TRIG1 |
| 64 | PB0_SCL0_PWM2_I2SMCLK | GPIOB.0 | 0 | I2C0.SCL |
| | | | 1 | PWM.CH2 |
| | | | 10 | I2S.MCLK |
| 63 | PB1_SDA0_PWM3_I2SSCK | GPIOB.1 | 0 | I2C0.SDA |
| | | | 1 | PWM.CH3 |
| | | | 10 | I2S.SCLK |
| 62 | PB2_SPI0SCK_PWM4_I2SWS | GPIOB.2 | 0 | SPI0.CLK |
| | | | 1 | PWM.CH4 |
| | | | 10 | I2S.WSCLK |
| 61 | PB3_SPI0TXD_PWM5_I2SSD | GPIOB.3 | 0 | SPI0.TXD |
| | | | 1 | PWM.CH5 |
| | | | 10 | I2S.SDA |
| 35 | PA6_SPI0RXD_PWM6_SCL0 | GPIOA.6 | 0 | SPI0.RXD |
| | | | 1 | PWM.CH6 |
| | | | 10 | I2C0.SCL |
| 36 | PA7_SPI0SSN_PWM7_SDA0 | GPIOA.7 | 0 | SPI0.CS |
| | | | 1 | PWM.CH7 |
| | | | 10 | I2C0.SDA |
| 3 | PA8_WKUP_ADC0_ACMP0P | GPIOA.8 | 0 | SYS_WKUP |
| | | | 1 | ADC.A0 |
| | | | 10 | ACMP.P0 |
| 4 | BOOT | | | |
| 5 | PA10_ADC2_TXD0 | GPIOA.10 | 1 | ADC.A2 |
| | | | 10 | UART0.TX |

| | | | | |
|---|---|---|---|---|
| | | | 11 | UART0.SIROUT |
| 6 | PA11_ACMP0N_ADC3_RXD0 | GPIOA.11 | 0 | ACMP.N0 |
| | | | 1 | ADC.A3 |
| | | | 10 | UART0.RX |
| | | | 11 | UART0.SIRIN |
| 7 | PA12_PWM8_TCK_ADC4 | GPIOA.12 | 0 | PWM.CH8 |
| | | | 1 | JTAG.TCK |
| | | | 10 | ADC.A4 |
| 8 | PA13_PWM9_TMS_ADC5 | GPIOA.13 | 0 | PWM.CH9 |
| | | | 1 | JTAG.TMS |
| | | | 10 | ADC.A5 |
| 9 | PA14_PWM10_ADC6 | GPIOA.14 | 0 | PWM.CH10 |
| | | | 1 | ADC.A6 |
| 10 | PA15_PWM11_ADC7 | GPIOA.15 | 0 | PWM.CH11 |
| | | | 1 | ADC.A7 |
| 48 | PA16_RXD1_ADC8 | GPIOA.16 | 0 | UART1.RX |
| | | | 1 | ADC.A8 |
| | | | 11 | UART1.SIRIN |
| 47 | PA17_TXD1_ADC9 | GPIOA.17 | 0 | UART1.TX |
| | | | 1 | ADC.A9 |
| | | | 11 | UART1.SIROUT |
| 58 | PA18_SPI1SSN0_ACMP0O | GPIOA.18 | 0 | SPI1.CS0 |
| | | | 1 | ACMP.O0 |
| 57 | PA19_SPI1SSN1_ACMP1O | GPIOA.19 | 0 | SPI1.CS1 |
| | | | 1 | |
| 56 | PA20_SPI1SSN2_TRIG0_RXD1 | GPIOA.20 | 0 | SPI1.CS2 |
| | | | 1 | ETB.TRIG0 |

| | | | | |
|---|---|---|---|---|
| | | | 10 | UART1.RX |
| | | | 11 | UART1.SIRIN |
| 55 | PA21_SPI1SCK_TRIG1_TXD1 | GPIOA.21 | 0 | SPI1.SCK |
| | | | 1 | ETB.TRIG1 |
| | | | 10 | UART1.TX |
| | | | 11 | UART1.SIROUT |
| 11 | PA22_SPI1RXD_PWM0_ADC10 | GPIOA.22 | 0 | SPI1.RXD |
| | | | 1 | PWM.CH0 |
| | | | 10 | ADC.A10 |
| 12 | PA23_SPI1TXD_PWM1_ADC11 | GPIOA.23 | 0 | SPI1.TXD |
| | | | 1 | PWM.CH1 |
| | | | 10 | ADC.A11 |
| 45 | PA24_TXD2_I2SMCLK_SPI1SSN0 | GPIOA.24 | 0 | UART2.TX |
| | | | 1 | I2S.MCLK |
| | | | 10 | SPI1.CS0 |
| | | | 11 | UART2.SIROUT |
| 44 | PA25_RXD2_I2SSCK_SPI1SSN1 | GPIOA.25 | 0 | UART2.RX |
| | | | 1 | I2S.SCLK |
| | | | 10 | SPI1.CS1 |
| | | | 11 | UART2.SIRIN |
| 13 | PA26_CTS2_I2SWS_ADC12 | GPIOA.26 | 0 | UART2.CTS |
| | | | 1 | I2S.WSCLK |
| | | | 10 | ADC.A12 |
| 14 | PA27_RTS2_I2SSD_ADC13 | GPIOA.27 | 0 | UART2.RTS |
| | | | 1 | I2S.SDA |
| | | | 10 | ADC.A13 |
| 15 | SCL1_CTS1_PWM10_ADC14 | I2C1.SCL | 0 | I2C1.SCL |

| | | | | |
|---|---|---|---|---|
| | | | 1 | UART1.CTS |
| | | | 10 | PWM.CH10 |
| | | | 11 | ADC.A14 |
| 16 | SDA1_RTS1_PWM11_ADC15 | I2C1.SDA | 0 | I2C1.SDA |
| | | | 1 | UART1.RTS |
| | | | 10 | PWM.CH11 |
| | | | 11 | ADC.A15 |

ATTENTION:

1. the function of each pin is selected individually
2. the base address of the reuse registers that control each pin multiplexing function is GPIO0_BADDR+0x100, the first and second reuse 32-bit registers control GPIOA.0~GPIOA.27, GPIOB.0~GPIOB.3 multiplexing function, the third reuse 4-bit register controls PC0_SCL1_CTS1_PWM10 and PC1_SDA1_RTS1_PWM11
3. VCORECP must be connect with 1uF capacitor to Ground
4. Boot I/O is suggest connect to ground with 1Ku resistor and 1uF capacitor
5. PIN_ELS and PIN_EHS is suggest connect to ground if no oscillator is placed
6. POUT_ELS an PIUT_EHS is suggest leave floating if no oscillator is placed

# 7. Electrical characteristics

Unless otherwise specified, typical data are based on TA = 25 ℃, VDD = 3.3 V .

## 7.1 Limiting values

| Symbol | Parameter | Conditions | Min | Ma | Un |
|---|---|---|---|---|---|

| | | | | x | it |
|---|---|---|---|---|---|
| VDD–VSS | External main supply voltage | | -0.3 | 4 | V |
| VIN | Input voltage(1) | VDD=3.3V | VSS-0.5 | 4 | V |
| \|ΔVDDx\| | Variations between different VDD power pins | | - | 100 | mV |
| \|ΔVSSx\| | Variations between all the different ground pins | | - | 100 | |
| IVDD | Total current into VDD/VDDA power lines (source) | | - | 200 | mA |
| IVSS | Total current out of VSS ground lines (sink) | | - | 200 | |
| IINJ(PIN) | Injected current(2) | Floating input | -5 | 5 | |
| ΣIINJ(PIN) | Total injected current (sum of all I/O and control pins) | | -25 | 25 | |
| VESD(HBM) | Electrostatic discharge voltage | HUMAN BODY MODE | 2000 | | V |
| VESD(MM) | | MACHINE MODE | 200 | | |
| VESD(CDM) | | CHARGE DEVICE MODE | 500 | | |
| TSTG | Storage temperature range | | -65 | 150 | °C |
| TJ | Maximum junction temperature | instantaneous values | - | 150 | °C |

(1) Refer to the maximum allowed injected current values.

(2) IINJ(PIN) must never be exceeded. Refer to the maximum allowed input voltage values.

## 7.2 General operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fHCLK | Internal AHB clock frequency | - | | | 48 | MHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| fPCLK1 | Internal APB1 clock frequency | - | | | 48 | |
| fPCLK2 | Internal APB2 clock frequency | - | | | 48 | |
| Performance | CoreMark score | CoreMark 1.0 : 57.315874 / GCC6.3.0 / STACK | | 2.39 | | (Iterations/s) / MHz |
| | Dhrystone score | Dhrystone Benchmark, Version 2.1 (Language: C, 1000000 runs) | | 1.32 | | DMIPS/MHz |
| | ULPMark score | ULPMark-Core Profile(1) | | | | |
| | | ULPMark-Peripheral Profile(2) | | | | |
| VDD | Standard operating voltage | - | 2.1 | 3.3 | 3.6 | V |
| VDDA | Analog operating voltage | - | 2.1 | 3.3 | 3.6 | |
| VBAT | Backup operating voltage | - | | N/A | | V |

(1) Refer to "ULPMark(tm) Core Profile User Guide 1.1.x" for more infomation.

(2) Refer to "ULPMark(tm) Peripheral Profile User Guide 2.5.x" for more information.

## 7.3 Embedded reset and power control block characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tVDDr | VDD rise time rate(1)(3) | | 20 | - | ∞ | µs/V |
| tVDDf | VDD fall time rate(2)(3) | | 20 | - | ∞ | |
| VPOR | Power on reset threshold(1)(3) | | N/A | - | - | V |
| VPDR | Power down reset threshold(2)(3) | | - | - | N/A | |

(1) VDD rise must be quick enough to meet internal reset and LDO timming sequence.

(2) BOD reset circute is not included, power capacity must be ensured for heavy load.

(3) External reset IC is recommended for reliable reset of system.

## 7.4 NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST Input low level voltage | | -0.5 | | 1.4 | V |
| $V_{IH(NRST)}$ | NRST Input high level voltage | | 2 | | VDD+0.5 | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | | 500 | | mV |
| VF(NRST) | NRST Input filtered pulse | – | – | – | – | nS |
| $R_{PU}$ | internal weak pull-up equivalent resistor | – | – | – | – | kΩ |
| TRSTTEMPO | Reset temporization | – | – | – | – | ms |

## 7.5 I/O port characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VIL | Standard IO input low level voltage | - | | | 1.45 | V |
| VIH | Standard IO input high level voltage | - | 1.93 | | | |
| Vhys | Standard IO Schmitt trigger voltage hysteresis | - | | 0.5 | | |
| $I_{IL}$ | input leakage current | VSS ≤VIN ≤VDD | | | 1 | nA |
| RPU | Weak pull-up equivalent resistor | shorted toVSS | | 46 | | kΩ |

| | | | | | | |
|---|---|---|---|---|---|---|
| RPD | Weak pull-down equivalent resistor | shorted toVDD | | 54 | | |
| CIO | I/O pin capacitance | - | | 5 | | pF |
| VOH | Output high level voltage | IOH =0 mA | VDD-0.001 | | | V |
| | | IOH =–6 mA | | VDD-0.3 | | V |
| VOL | Output low level voltage | IOL =0mA | | | 0.001 | V |
| | | IOL =+6mA | | | 0.21 | V |
| IOH | HIGH-level output current | VOH = VDD – 0.4 V | | 8 | | mA |
| IOL | LOW-level output current | VOL = 0.4 V | | 10 | | |
| IOHS | drive HIGH; connected to ground; | | | 34 | | |
| IOLS | drive LOW; connected to VDD | | | 48 | | |
| tf(IO)out | Output high to low level fall time | push-pull | | 4.6 | | nS |
| tr(IO)out | Output low to high level rise time | push-pull | | 5.4 | | nS |
| Fmax(IO)out | Maximum frequency(1) | CL=50 pF, IO confirged as PP out | 24 | | | MHz |

(1) Maximum frequency is achived if (tr+tf)<2/3T, D=(45~55)% .

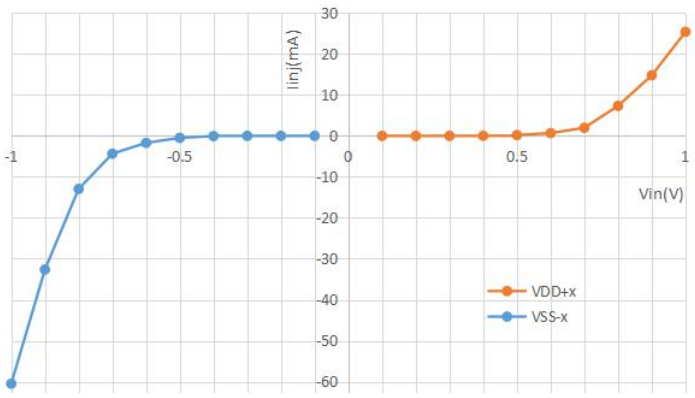



Fig. 2 typical injected current curve

## 7.6 Clock and PLL characteristics

### 7.6.1 PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fPLL_IN | PLL input clock(1) | | 6 | 8 | 60 | MHz |
| | PLL input clock duty cycle | | 45 | 50 | 55 | % |
| fPLL_OUT | PLL multiplier output clock | | 8 | | 60 | MHz |
| tLOCK | PLL lock time | | | | 200 | uS |
| Jitter | period jitter time | | | | 200 | pS |

(1) Guaranteed by design.

### 7.6.2 IHS oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fIHS | Frequency of 8M RC | | 7.5 | | | MHz |
| $ACC_{IHS}$ | accuracy of the IHS oscillator | | | | | % |

### 7.6.3 ILS oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fILS | Frequency of 10K RC | | 6.7 | | | KHz |
| $ACC_{ILS}$ | curacy of the ILS oscillator | | | | | % |

### 7.6.4 EHS user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fEHS_ext | User External clock source frequency | | | 8 | | MHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| VEHSH | OSC_IN input pin high level voltage | | | N/A | | V |
| VEHSL | OSC_IN input pin low level voltage | | | N/A | | |
| IL | OSC_IN Input leakage current | VSS ≤VIN ≤VDD | | N/A | | μA |

### 7.6.5 EHS oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fOSC_IN | EHS Oscillator frequency | | | 8 | | MHz |
| tSU(EHS) | Startup time | VDD is stabilized | | 1.5 | | ms |
| C | Recommended load capacitance versus equivalent serial resistance of the crystal | ESR = 30Ω | | 10 | | pF |
| IEHS | EHS driving current | | | N/A | | mA |
| RF | Feedback resistor | | | | | kΩ |
| gm | Oscillator transconductance | Startup | | | | mA/V |

### 7.6.6 ELS user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fELS_ext | User External clock source frequency | | | 32.768 | | KHz |
| VELSH | OSC32_IN input pin high level voltage | | | N/A | | V |
| VELSL | OSC32_IN input pin low level voltage | | | N/A | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leqslant V_{IN} \leqslant V_{DD}$ | | N/A | | μA |

### 7.6.7 ELS oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| f32_IN | ELS Oscillator frequency | | | 32.768 | | KHz |
| C | Recommended load capacitance | | | N/A | | pF |
| IELS | ELS driving current | | | N/A | | mA |
| tSU(ELS) | Startup time | VDD is stabilized | | N/A | | ms |

## 7.7 Power consumption

### 7.7.1 Current consumption in run mode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IDD | Supply current in Run mode, all peripherals clock enabled(1)(2) | 8 MHZ(4) | | 6.1 | | mA |
| | | 16 MHZ | | 11.6 | | |
| | | 24 MHZ | | 17.0 | | |
| | | 32 MHZ | | 22.5 | | |
| | | 40 MHZ | | 27.9 | | |
| | | 48 MHZ | | 33.4 | | |
| | | 56 MHZ(5) | | 38.7 | | |
| | Supply current in Run mode, all unused peripherals clock gated(1)(3) | 8 MHZ(4) | | 2.3 | | |
| | | 16 MHZ | | 3.7 | | |
| | | 24 MHZ | | 5.0 | | |
| | | 32 MHZ | | 6.4 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | 40 MHZ | | 7.8 | | |
| | | 48 MHZ | | 9.2 | | |
| | | 56 MHZ(5) | | 10.4 | | |
| | Power consumption per MHz | (1)(2) | | 681 | | uA/MHz |
| | | (1)(3) | | 176 | | |

(1) IHS 8M RC and PLL is always used. Code run from Flash. CoreTimer,UART0,GPIO0/1 and APB0/1 is used/enabled in the basic test program.

(2) The IP clock register CGCR,SCGCR remains default value after reset.

(3) Clock of unused peripherals in the test program is gated,all SCGCR clock is gated.

(4) PLL is used with multiplier of 1 at 8 MHz..

(5) Maximum MCLK is limited to 48MHz, 56MHz data just for test use.

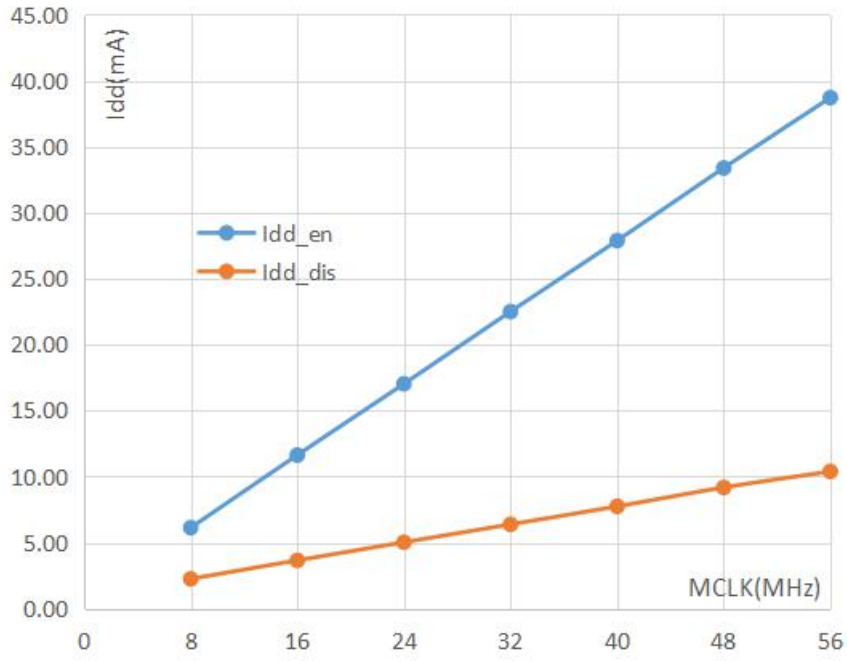



Fig. 3 Current consumption at different MCLK frequency

### 7.7.2 Current consumption in low power mode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| IDD | Supply current in wait mode(1) | 24MHz | | 13.7 | | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Supply current in doze mode(2) | - | | 63 | | uA |
| | Supply current in stop mode(2) | - | | 16 | | |
| | Supply current in standby mode(2) | - | | 2.7 | | |

(1) The IP clock register CGCR,SCGCR remaines default value after reset.

(2) ILS clock is selected, external wakeup, RTC power down.

### 7.7.3 Peripheral current consumption

Tab. 5 Peripherals clock controled by CGCR

| Symbol | Parameter | Conditions(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Idd | ALL_ON | 4E3FFFFF | | 4.040 | | mA |
| | SMS | 40000000 | | 0.143 | | |
| | APB0 | 08000000 | | 0.030 | | |
| | APB1 | 04000000 | | 0.033 | | |
| | SASC | 02000000 | | 0.107 | | |
| | TRC1 | 00400000 | | 0.094 | | |
| | TIM1 | 00200000 | | 0.033 | | |
| | NONSEU DMAC | 00100000 | | 0.429 | | |
| | CoreTimer | 00080000 | | 0.015 | | |
| | CRC | 00040000 | | 0.017 | | |
| | SEU DMAC | 00020000 | | 0.437 | | |
| | GPIO1 | 00010000 | | 0.015 | | |
| | ETB | 00008000 | | 0.008 | | |
| | CMPCTRL | 00004000 | | 0.013 | | |
| | SPIM | 00002000 | | 0.211 | | |
| | ADCCTRL | 00001000 | | 0.090 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | I2S_APB/I2S_SRC | 00000800 | | 0.369 | | |
| | TIM | 00000400 | | 0.028 | | |
| | UART2 | 00000200 | | 0.141 | | |
| | UART1 | 00000100 | | 0.140 | | |
| | I2C1 | 00000080 | | 0.354 | | |
| | I2C0 | 00000040 | | 0.371 | | |
| | UART0 | 00000020 | | 0.140 | | |
| | PWM | 00000010 | | 0.422 | | |
| | RTC | 00000008 | | 0.089 | | |
| | WDT | 00000004 | | 0.017 | | |
| | SPIS | 00000002 | | 0.246 | | |
| | GPIO0 | 00000001 | | 0.157 | | |

(1) MCLK=24MHz, in debug mode. CGCR resigter is configured to disable some peripheral's clock.

Tab. 6 Peripherals clock controled by SCGCR

| Symbol | Parameter | Conditions(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Idd | ALL_ON | 1F | | 7.771 | | mA |
| | SIPC | 10 | | 0.010 | | |
| | RSA | 08 | | 0.115 | | |
| | AES | 04 | | 7.132 | | |
| | TRNG | 02 | | 0.029 | | |
| | SHA1 | 01 | | 0.494 | | |

(1) MCLK=24MHz, in debug mode. SCGCR resigter is configured to disable some peripheral's clock.

## 7.8 Memory characteristics

### 7.8.1 Flash memory characteristics

| Symbol | Parameter | Conditions(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tprog | word programming time (2) | TA = 25 °C, 48MHz | | 83 | | us |
| tERASE | sector erase time(2) | TA = 25 °C, 48MHz | | 0.85 | | ms |
| tME | Mass erase time | TA = –40 to +105 °C | | | | ms |
| Idd | Read current | 24MHz | | | 3 | mA |
| | Program current | | | | 5 | mA |
| | Sector erase current | | | | 2 | mA |
| $V_{prog}$ | Programming voltage | inner power supply | 1.35 | | 1.65 | V |

(1) EFlash is configured for maximum MCLK frequency.

TRC=0x01,TNVS=0x13e,TPGS=0x88,TPROG=0x141,TRCV(erase)=0xa56.

(2) More data refer to "EFlash sector earse/word programming time" curve.

### 7.8.2 Flash memory endurance and data retention

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| NEND | Endurance | TA = –40 to +85 °C | | 20 | | kCycles |
| tRET | Data retention | TA = 85 °C | | 25 | | Years |
| | | 1 kcycle at TA = 85 °C | | | | |
| | | 10 kcycles at TA = 55 °C | | | | |

(1) Guaranteed by characterization results.

## 7.9 Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PD | Power dissipation | QFN64, at TA = 85 °C | | | | mW |
| TA | Ambient temperature | Maximum power | -40 | | 105 | °C |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | dissipation | | | | |
| TJ | Junction temperature range | | –40 | | 125 | |
| Θja | thermal resistance from junction to ambient | | | | | C/W |
| Θjc | thermal resistance from junction to case | | | | | |

## 7.10 EMC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VFESD | Functional Electrostatic discharge | IEC 61000-4-2 | | N/A | | Level /Class |
| VEFTB | Fast transient voltage burst | IEC 61000-4-4 | | N/A | | |
| VESD(HBM) | Electrostatic discharge voltage (human body model) | ANSI/ESDA/JEDEC JS-001-2017 Zap 1 pulse(s), Interval: 0.3 Sec. | 2000 | | | V |
| | | | | 2 | | Class |
| VESD(MM) | Electrostatic discharge voltage (machine model) | JEDEC EIA/JESD22-A115C Zap 1 pulse(s), Interval: 0.5 Sec. | 200 | | | V |
| | | | | 2 | | Class |
| VESD(CDM) | Electrostatic discharge voltage (charge device model) | JEDEC EIA/JESD22-C101F | 500 | | | V |
| | | | | C2 | | Class |
| Ilatch | I/O latch-up current | –(0.5VDD) < VI < (1.5VDD);Tj < 125 °C | | 200 | | mA |
| LU | Static latch-up class | JEDEC STANDARD NO.78E, NOVEMBER 2016 | | I | | Class |

## 7.11 ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDDA | Power supply | | 2.1 | 3.3 | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | | | VDDA | V |
| $V_{REF-}$ | Negative reference voltage | | 0 | | | |
| $f_{ADC}$ | ADC clock frequency | | | | 16 | MHz |
| $f_S$ | convertion rate | | | | 1000 | KSPS |
| $V_{AIN}$ | Conversion voltage range | | 0 | | $V_{REF+}$ | V |
| $R_{AIN}$ | External input impedance | | | N/A | | kΩ |
| $t_{CONV}$ | Total conversion time(including sampling time) | MCLK = 24 MHz | | 1.5 | | μs |
| ET | Total unadjusted error | | 0 | 3 | 5 | LSB |
| EO | Offset error | | - | 3.3 | - | |
| EG | Gain error | | - | 2.9 | - | |
| ED | Differential linearity error | | - | ±1 | 2 | |
| EL | Integral linearity error | | - | 2 | 3 | |
| ENOB | Effective number of bits | | | | | bits |
| SINAD | Signal-to noise and distortion ratio | | | | | dB |
| SNR | Signal-to noise ratio | | | | | |
| THD | Total harmonic distortion | | | | | |
| INL | Integral Non-Linearity | | | ±2 | | LSB |
| DNL | Differential Non-Linearity | | | ± 1 | | |

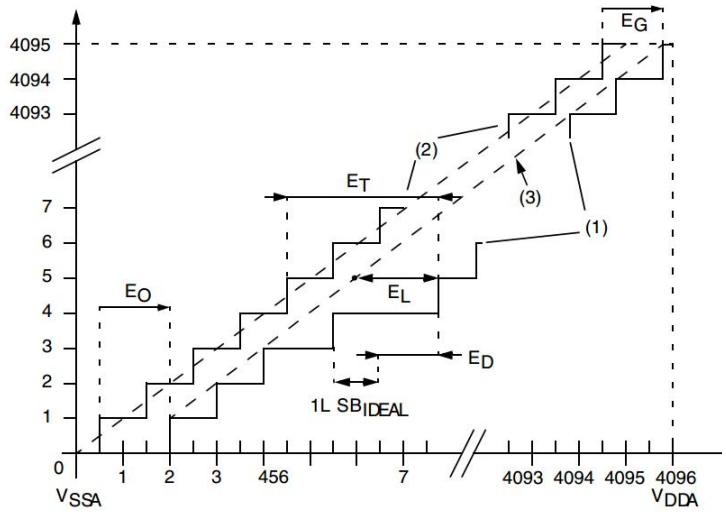



Fig. 5 ADC accuracy characteristics

1. Example of an actual transfer curve.

2. Ideal transfer curve.

3. End point correlation line.

4. ET = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.

EO = Offset Error: deviation between the first actual transition and the first ideal one.

EG = Gain Error: deviation between the last ideal transition and the last actual one.

ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.

EL = Integral Linearity Error: maximum deviation between any actual transition and the best straight-line.

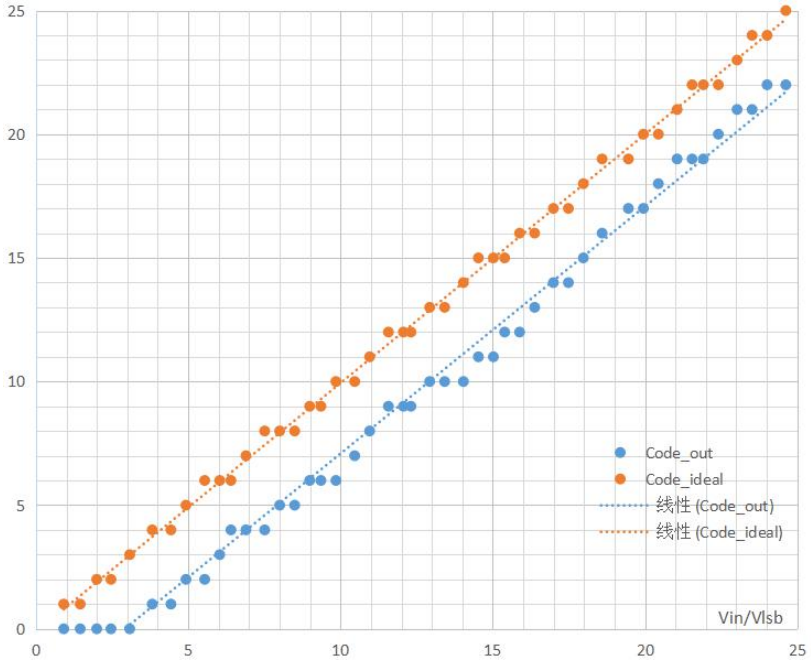



Fig. 6 ADC transfer curve and offset error

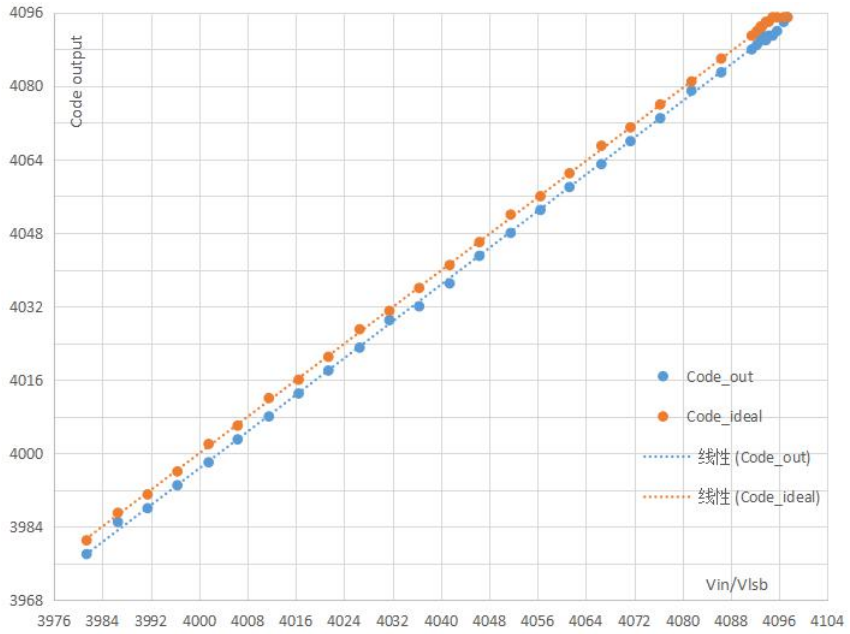


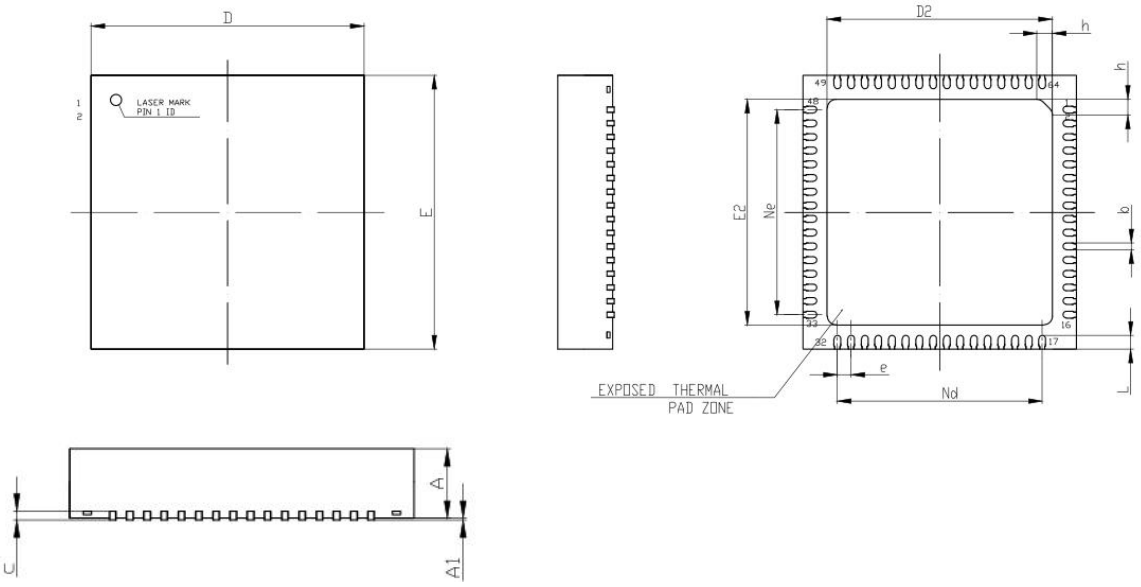

Fig. 7 ADC transfer curve and gain error

## 7.12 Analog comparator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | | 2.1 | 3.3 | 3.6 | V |
| $V_{IN}$ | Comparator input voltage range | | 0.3 | | VDDA-0.3 | |
| $V_{offset}$ | Comparator offset error | | -10 | | 10 | mV |
| Vhys | Comparator hysteresis | High-speed, $V_N$=VDD/2 | | 124 | | mV |
| tD | Propagation delay | High-speed mode | | 15 | | ns |
| | | Low-speed mode | | 31 | | ns |

# 8 Package information

QFN Package outline dimensions




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.9 | 1.00 | 1.10 |
| A1 | —— | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 7.90 | 8.00 | 8.10 |
| D2 | 6.50 | 6.60 | 6.70 |
| e | 0.40BSC | | |
| Ne | 6.00BSC | | |
| Nd | 6.00BSC | | |
| E | 7.90 | 8.00 | 8.10 |
| E2 | 6.50 | 6.60 | 6.70 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.25 | 0.30 | 0.35 |

# 9 Storage

Chip is stored in a vacuum-sealed bag. After the vacuum-sealed bag is opened,Mounted within 168 hours at the factory environment of ≤30° C/60% RH.

Devices require baking before mounting, if any circumstance below occurs:

(1) When the ambient temperature is 23°C±5°C and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.

(2) Device mounting cannot be finished within 72 hours at factory conditions of ≤30°C/60%