CpE 313 Fall 2004 – Solution to HW 7

Question 1.

A) 64K8 unified cache has miss rate of 1.35% (from table)

Overall miss rate for split cache is calculated as follows.

%age of memory references that access instruction cache = 1/1.5=0.667

%age of memory references that access data cache = 0.5/1.5=0.333

Miss Rate of split cache = 0.667 * 0.39% (from table) + 0.333 * 4.82% (from table) = 1.87

Thus, unified cache has lower miss rate than split cache.

B) Unified cache: AMA T = 0.667*(2+ 1.35% * 75) + 0.333*(3+1.35% *75) = 3.35 cycles

Split cache: AMAT=0.667(2+0.39%*75)+0.333(2+4.82% * 75) = 3.40 cycles.

Thus, unified cache has lower AMA T than split cache.

Question 2.

$$
\begin{aligned}
\mathbf{CPU\ time} &= \mathbf{IC} \times \left(\mathbf{CPI_{exec}} + \frac{\mathbf{memory\ accesses}}{\mathbf{instruction}} \times \mathbf{miss\ rate} \times \mathbf{miss\ penalty} \right) \times \mathbf{cycle\ time} \\
&= \mathbf{IC} \times \Big[\left(\mathbf{CPI_{exec}} \times \mathbf{cycle\ time} \right) \\
&\quad + \left(\frac{\mathbf{memory\ accesses}}{\mathbf{instruction}} \times \mathbf{miss\ rate} \times \mathbf{miss\ penalty} \times \mathbf{cycle\ time} \right) \Big]
\end{aligned}
$$

You have to remember that the product (miss penalty * cycle time) equals 70 ns.

A) For DMC, CPU time=IC * (2*2 + 1.33 * 1.4% * 70) =5.30*IC

B) For 2-way set associative cache, CPU time = IC * (2*2*1.2+1.33*1.0% * 70) =5.73*IC

C) Because DMC has a smaller CPU time value, and because ultimately it is the CPU time which is the fundamental metric, DMC is better than the 2-way set associative cache.