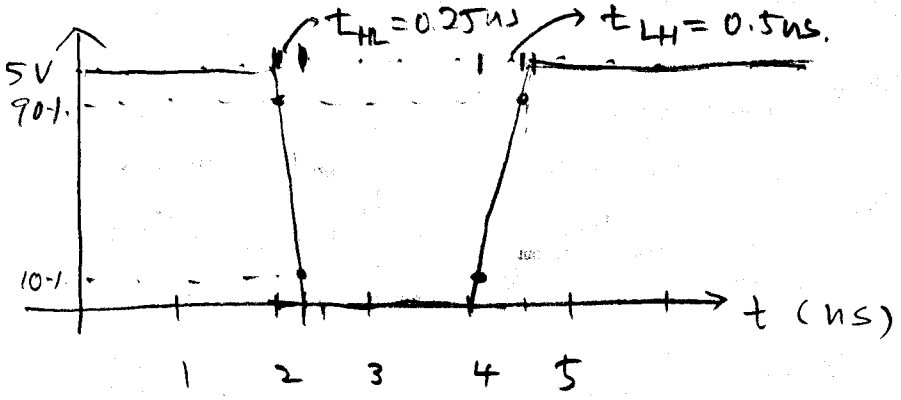
CpE111 HW #4 solutions.

1. a) $P = 0.1\,A \times 2.5\,V = 0.25\,W.$

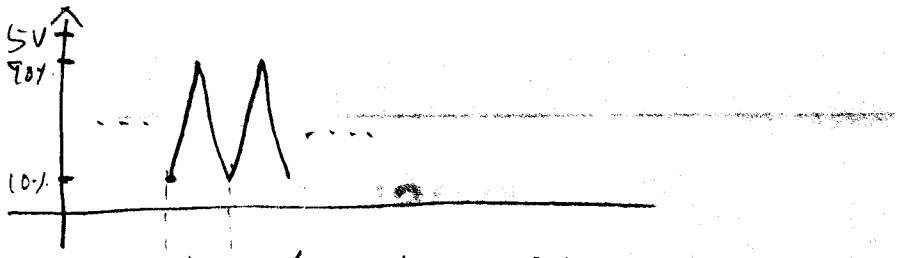
b) $P = 5\,V \times 0.5\,A = 2.5\,W$

c) $I = 12\,W / 6\,V = 2\,A.$

2. a)



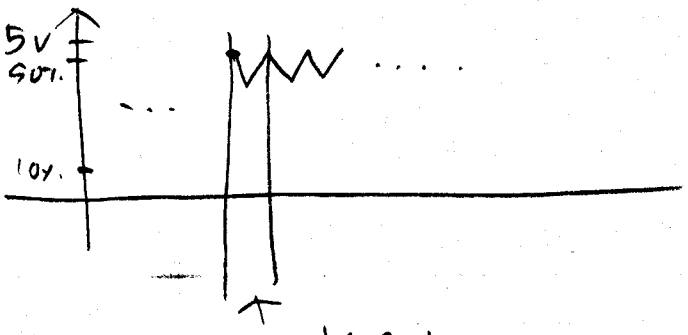
b)



$t_{min} = t_{HL} + t_{LH} = 0.75\,ns.$

$f_{max} = 1/t_{min} = 1/(0.75 \times 10^{-9}) = 1.\overline{3}\,GHz$

c. Assume that the initial voltage level is 90% of V_{DD}.



$\frac{1}{2}(t_{HL} + t_{LH})$

⇐ There is not enough time for Vout to settle down in the right voltage level. (in the give example logic 0 can't be achieved)

3. propagation delay for NAND gate

Total delay = $t_{PD,NAND}$ + ($t_{PL,NOT} + t_{PL,NOR}$)

load delay for NAND.

+ $t_{PD,NOR}$ + ($t_{PL,NOT} + t_{PL,NOR}$)

PD for NOR

load delay for NOR

+ $t_{PD,NOT}$ + ($t_{PL,NOT}$)

PD for NOT

load delay for NOT.

$= 0.85ns + (0.4ns + 0.9ns)$

$+ 0.75ns + (0.4ns + 0.9ns)$

$+ 0.5ns + (0.4ns)$

$= 5.1ns.$

4. $Q = CV.$

So, $Q = (10 \times 10^{-6}) \cdot 2 = 20 \times 10^{-6} C$

$= 20\mu C$

5. $V = Q/C$

So, $V = 2.8 \times 10^{-9} / 100 \times 10^{-15} = 28000V = 28kV$

6. $\tau = RC \iff R = \tau/C$

So, $R = 7 \times 10^{-9} / 10 \times 10^{-12} = 700\Omega.$

7. a) $\tau = R \cdot C = 1400 \times 5 \times 10^{-12} = 7ns$

b) $V_c(t=\tau) = 3(1 - e^{-1}) = 1.9V$ ($\approx 2/3 V_{DD} = 2V.$)

c) $V_c(t=\tau) = 3 \cdot e^{-1} = 1.1V.$ ($\approx 1/3 V_{DD} = 1V$)