Digital System Modeling (CpE 318)

Section A: Winter 2004 Class Hours: T R 12:30 – 1:45 Room: G31 EECH

Instructor: Dr. Scott C. Smith
Office: 133 EECH
Office Hours: T R 2:00 – 4:00, or by appointment
E-mail: smithsco@umr.edu
Phone: (573) 341-4232

Grader: Anshul Singh
Office: 106 EECH
Office Hours: M W 10:30 – 12:00
E-mail: astxb@umr.edu

Prerequisites: CpE 111 and CpE 112, or CSc 234 (By topic: digital logic design and optimization, including both combinational and sequential circuits).

Text: Peter J. Ashenden, The Designer's Guide to VHDL, second edition, Morgan Kaufmann Publishers, 2001.

Goals: To learn the VHDL modeling language such that both combinational and sequential circuits can be designed for synthesis at the behavioral, dataflow, or structural level and then be simulated to test for functional correctness.

Schedule:

Introduction to Modeling with VHDL	Chapters 1-4, 13
Entity and Architecture Statements	Chapter 5
Test Benches	Chapter 1
Packages	Chapter 8
Design Project 1*	
Exam 1†	
Generic Constants	Chapter 12
Generate Statements	Chapter 14
Text I/O	Chapter 18
Introduction to Verilog Modeling Language	
Other Miscellaneous Topics (time permitting)	
Design Project 2*	
Final Exam† (Tuesday, May 11, 8:00 am – 10:00 am, G31 EECH)	

* Design Projects are due AT THE BEGINNING OF CLASS on the specified date. No late projects will be accepted.

† Prior notification is required if unable to attend an examination period.

Homework: Homework assignments are due AT THE BEGINNING OF CLASS on the specified date. No late homework will be accepted. Homework will consist of problems from the text and/or handouts; and will account for 1/6 of your final grade.

Grading:

Design Project 1	100 points
Exam 1	100 points
Design Project 2	100 points
Homework	100 points
Final Exam	200 points
Total	600 points

[100% - 90%]	A
(90% - 80%]	B
(80% - 70%]	C
(70% - 60%]	D for undergraduates, F for graduate students
(60% - 0%]	F

- Final grades may be curved depending on class average.

Unix Accounts: A Unix account is required for all students and will be necessary to complete projects and homework. Apply for an account ASAP, if you do not already have one, using the web application form at: http://www.ece.umr.edu/web-cgi/account.pl

References:

[1] Donald D. Givone, Digital Principles and Design, McGraw-Hill, 2003.
[2] Allen Dewey, Analysis and Design of Digital Systems with VHDL, PWS Publishing Company, 1997.
[3] Behrooz Parhami, Computer Arithmetic Algorithms and Hardware Designs, Oxford University Press, New York, 2000.
[4] Donald E. Thomas and Philip R. Moorby, The Verilog Hardware Description Language, second edition, Kluwer Academic Publishers, 1995.

- These reference materials are on reserve at the library.