CpE 213
Digital Systems Design
Address Decoding
Intro to Computer Organization

Lecture 4

Monday 8/29/2005

UNIVERSITY OF MISSOURI-ROLLA

The Name. The Degree. The Difference.

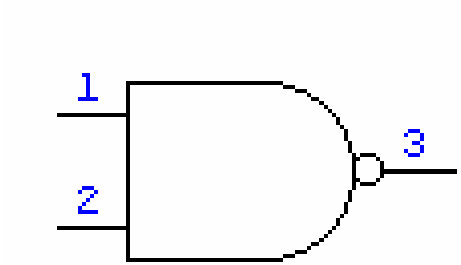
Overview

- Announcements
- Hardware review
- Address decoding

Announcements

- Homework 1 is due on Friday.
- Picture deadline is Friday.
- Group deadline is Friday.
- Learning Center
  - Wednesday and Thursday from 5:00 - 7:00
  - In EECH 101
  - You are strongly encouraged to attend.

Hardware review



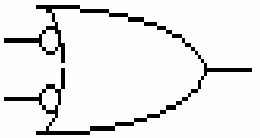
P1	P2	P3
0	0	1
0	1	1
1	0	1
1	1	0

Name: NAND2

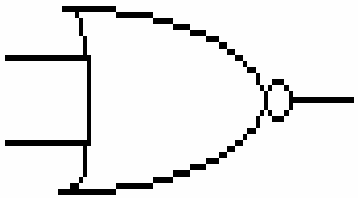
Logic equation: P3 = not (P1 and P2);

DeMorgan equivalent:

P3 = not P1 or not P2



Hardware review



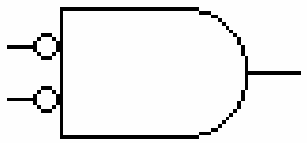
P1	P2	P3
0	0	1
0	1	0
1	0	0
1	1	0

Name: NOR2

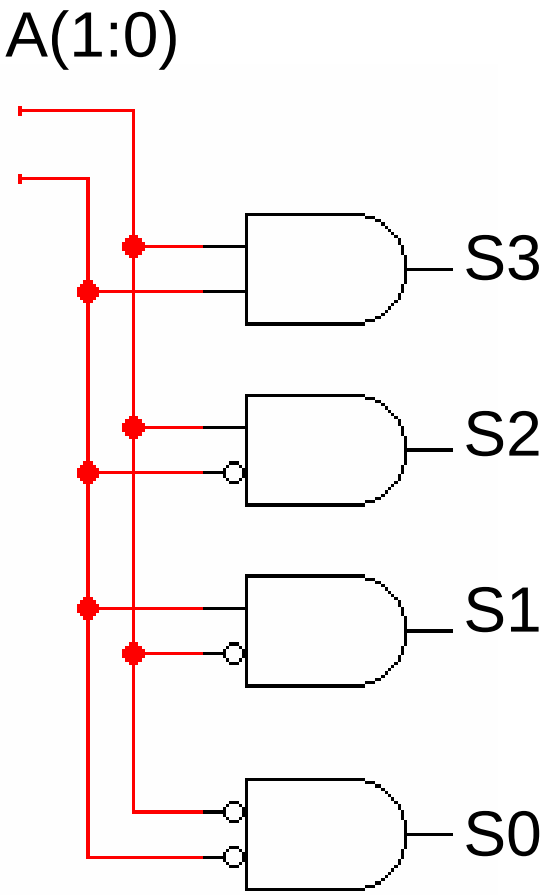
Logic equation: P3 = not (P1 or P2);

DeMorgan equivalent:

P3 = not P1 and not P2



Hardware review

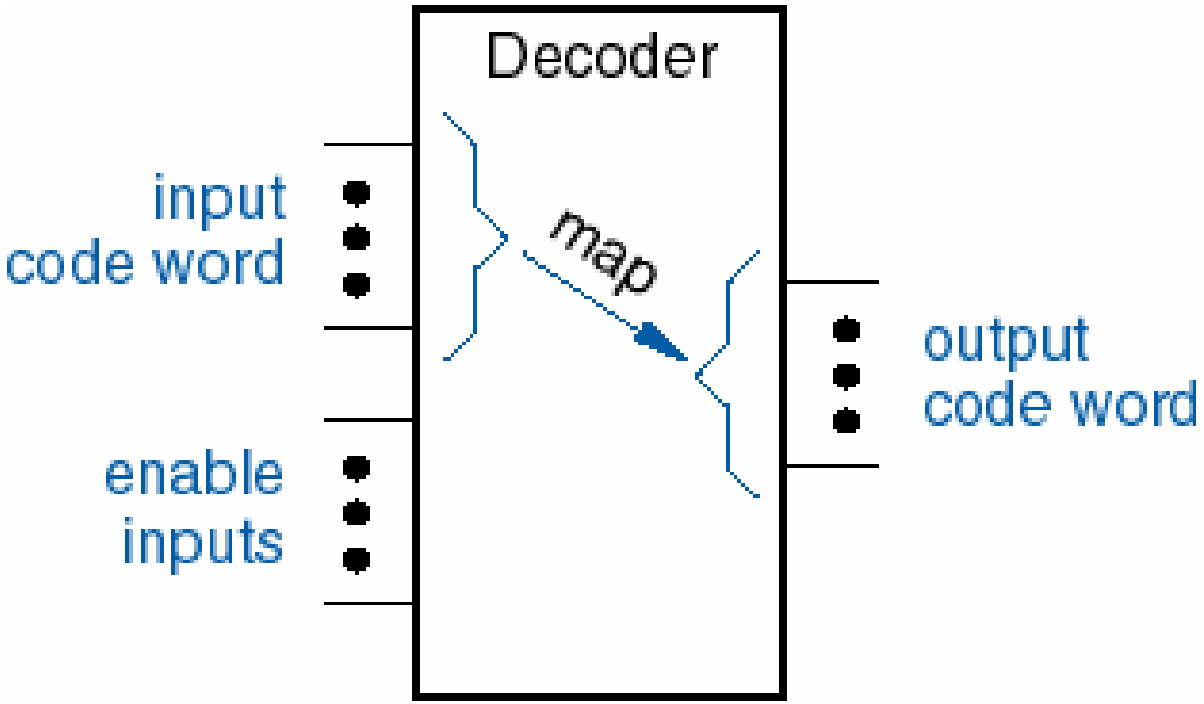


- What is it? decoder
- What is it used for?
  address decoding
  (more later)

```
S3 = 1 when A= 11 else  0;
S2 = 1 when A= 10 else  0;
S1 = 1 when A= 01 else  0;
S0 = 1 when A= 00 else  0;
```

Decoders

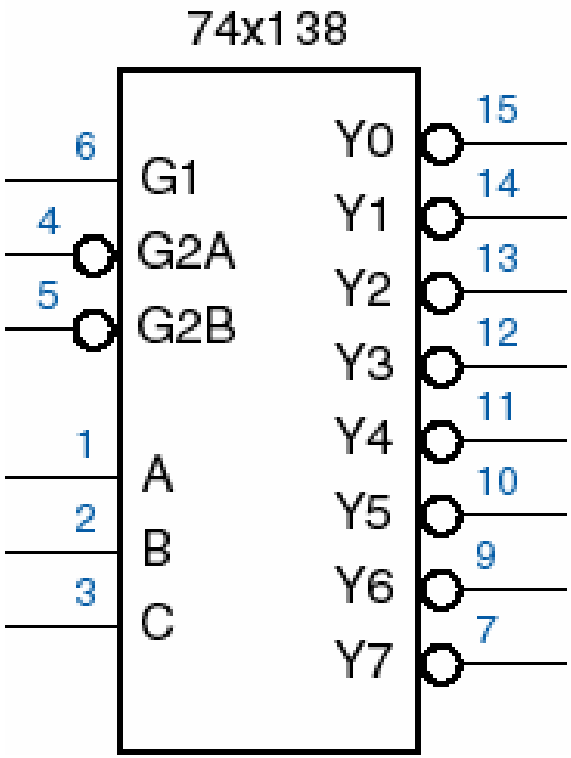
- general decoder structure



Some logic review slides adapted from Dr. Shoukat Ali.

74x138 – A 3-to-8 Decoder

- three enable inputs (**unusual! why not just one?**)
  - all must be asserted to enable the decoder
    - that is, G1 = __, G2A = __ and G2B = __
- active high select inputs
- active low outputs

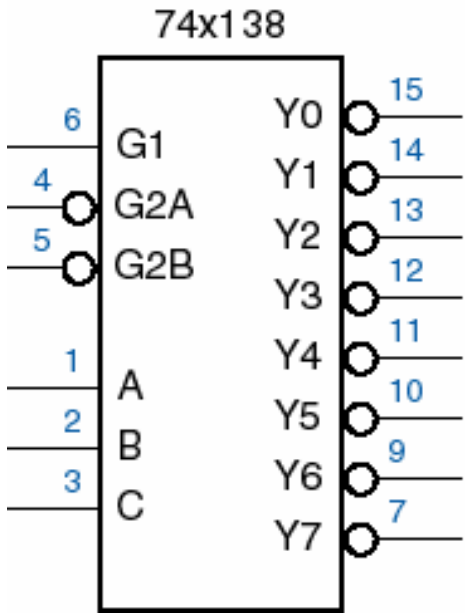


What is the state of output bits when ABC = 101 and the decoder is enabled?

What is the state of output bits when ABC = 101 and the decoder is disabled?

Truth table

enable		select			output							
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	1	X	X	X	1	1	1	1	1	1	1	1
0	X	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0

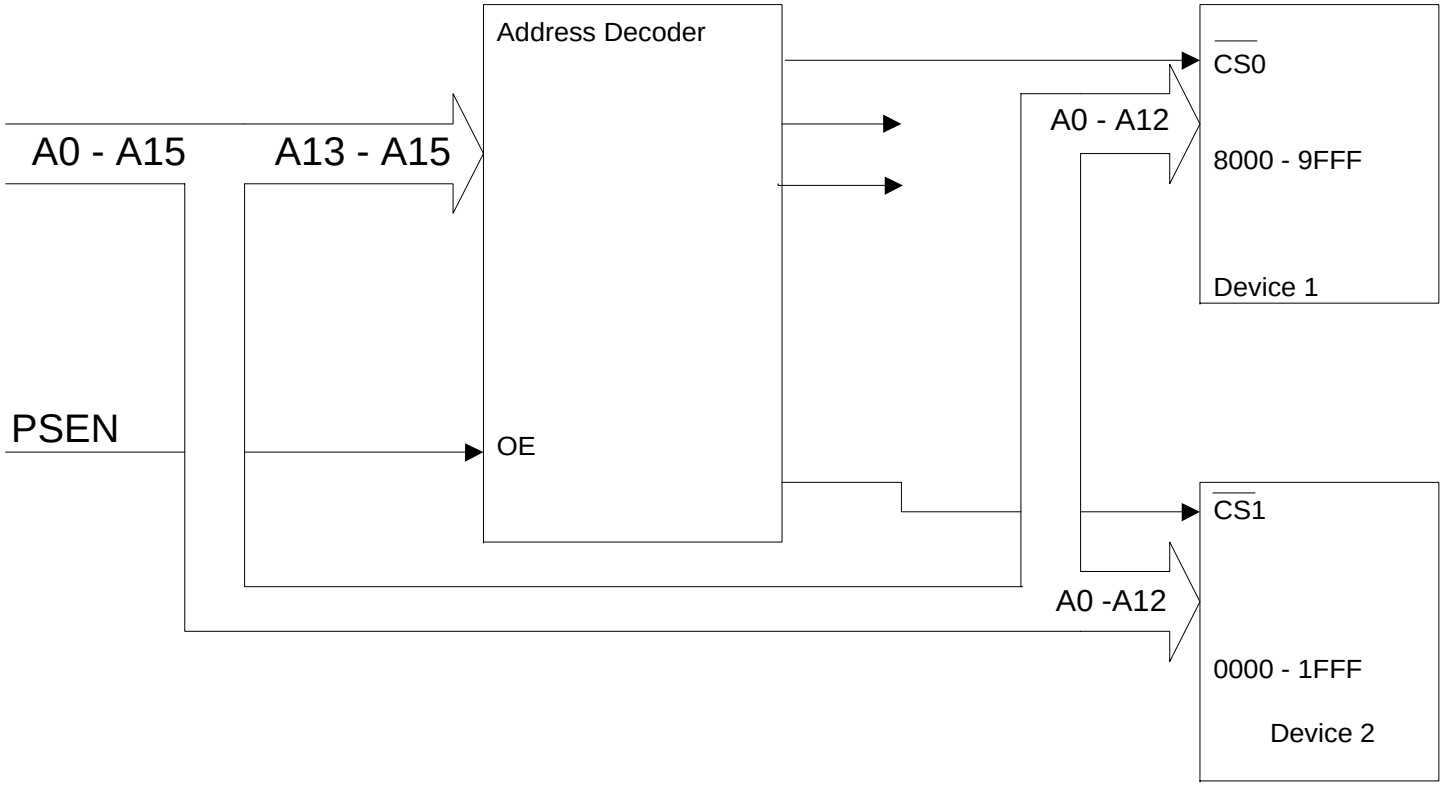


Address Decoding

Some slides adapted excerpted from Dr. Brewer Ward's
CECS 347 Notes at CSULB

Address decoder

- Computer logic that will use address and timing information from the processor to generate Chip Select (CS) lines used to enable external devices.



Steps of address decoder design

- Draw an address table showing the address range for each device to be decoded.
- Determine address lines that need to be connected to chip select of device.
- Design the logic circuit needed to generate chip select signal from these lines.

Address table

- Draw an address table showing the address range for each device to be decoded.
- The table must also show the contents of each bit of the address range.
  - If a bit must be high to address the device denote it with a “1” in that address bit position.
  - If a bit must be zero to address the device, denote it with a “0” in that address bit position.
  - If the bit can either be a “1” or a “0” then denote this with an “X”.

	Add. Range	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device 1	8000 – 9FFF	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X
Device 2	0000 – 1FFF	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X

Select address lines

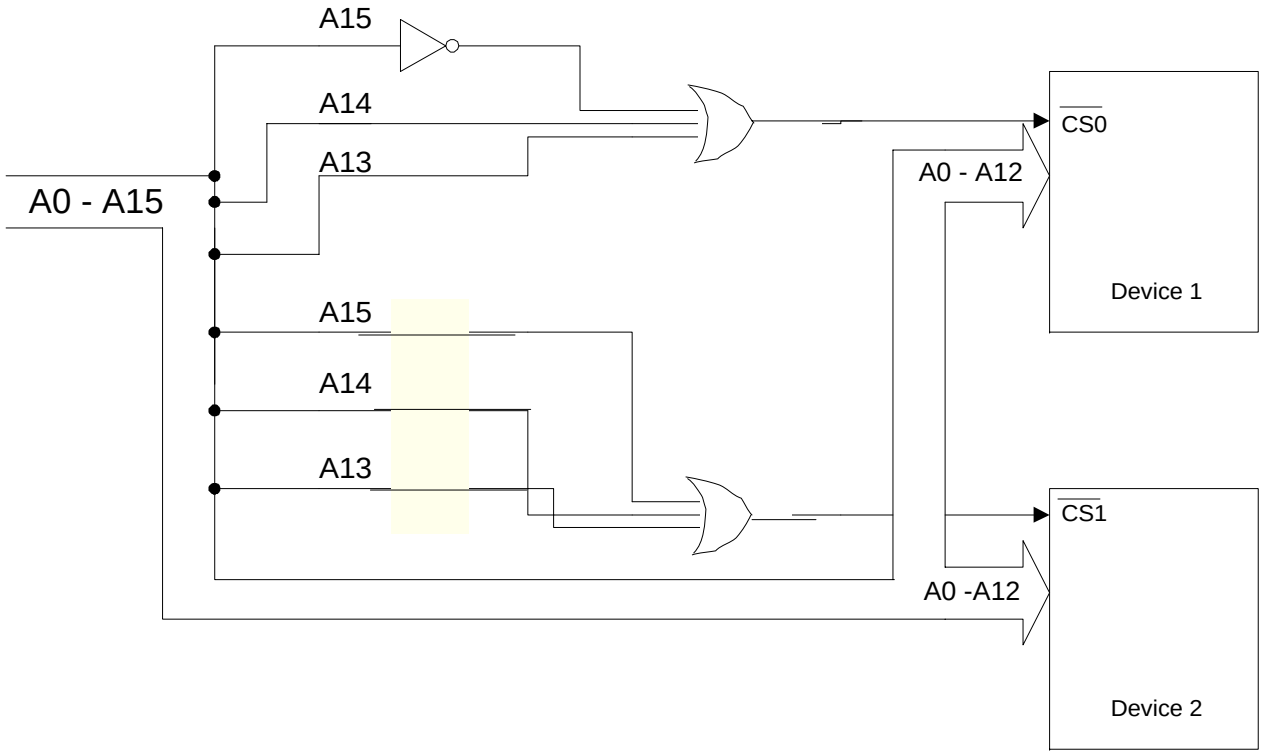
- From the table the address lines with either a “1” or a “0” will be used to generate the chip select signal.
- The address lines with an “X” in their box will go directly from the processor to the device. These lines will be used by the device to select either the memory cell desired or to set an internal register in the device.

	Add. Range	**15**	**14**	**13**	12	11	10	9	8	7	6	5	4	3	2	1	0
Device 1	8000 – 9FFF	**1**	**0**	**0**	X	X	X	X	X	X	X	X	X	X	X	X	X
Device 2	0000 – 1FFF	**0**	**0**	**0**	X	X	X	X	X	X	X	X	X	X	X	X	X

- By looking at the table it can be seen that address lines A15, A14, and A13 need to be decoded to generate a unique chip select line for each device.

Designing decoding logic

- By setting A15=1, A14=0, and A13=0, device 1 will be selected.
- Similarly, setting A15, A14, and A13 to 0 will select device 2.
- We can simplify the design by setting A15=1 for device 1 and A15=0 to select device 2.



Chip select logic using 74LS138

- Using discrete gates to decode the chip select lines can be the most cost-effective solution if you have a small, dedicated system.
- For larger applications requiring many peripheral devices (each requiring their own chip select lines) it is best to use a commercial address decoder such as the 74LS138.
- Designing a chip select decoder circuit around the 74LS138 simplifies the circuit while providing eight or more unique chip selects.
- In addition to providing the address inputs (select A, B, and C) it also provides enable lines G1 and G2. This are used to enable the output and would typically be tied to the PSEN line from the 8051.

Group exercise

- Design chip select logic for the previous example using a 74LS138 instead of discrete logic gates.

For Wednesday

- Review today's lecture notes and textbook.
- Begin Assignment 1.
- Print lecture notes for Lecture 5.
- Come to my office and have your picture taken for bonus 5%.
- Email me names of your group members (one email per group).