97
paper

Cp Eng 111, Section B
Fall 1999

Exam 2
10/20/99

Name: Jane Doe

Show all work on the exam papers. If you need additional space, use the reverse side of the paper. Closed book, closed notes, no calculator.

1. (12) (a) Re-arrange the following integration levels in increasing order of size:

S M L V U

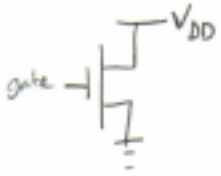
LSI MSI SSI ULSI VLSI

SSI → MSI → LSI → VLSI → ULSI

(b) What does the acronym MOSFET stand for?

Metal Oxide Semiconductor Field Effect Transistor

(c) Draw the circuit symbol for an n-channel MOSFET.



(d) State or otherwise describe Moore's Law.

The number of transistors on ICs doubles every two years.

Name: Jane Doe

2. (12) Determine whether each of the following is True (T) or False (F). Circle the appropriate choice.

(a) Propagation delay decreases with fan-in . T F

(b) TTL logic family is based on bipolar transistors. T F

(c) An advantage of ECL is its switching speed. T F

(d) The reserved word **downto** is part of the syntax definition of binary words in VHDL. T F

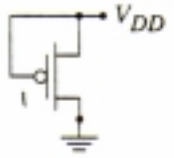
3. (9) (a) Given the following truth table, what gate is represented in negative logic?

x	y	f
L	L	H
L	H	H
H	L	H
H	H	L

x	y	f
1	1	0
1	0	0
0	1	0
0	0	1

NOR

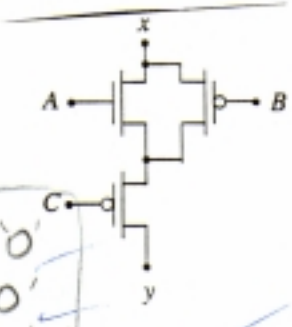
(b) Determine the conducting state (OFF or ON) for the following:



pFet

OFF

(c) Determine the values of the inputs that must be applied to insure that x and y are electrically connected.



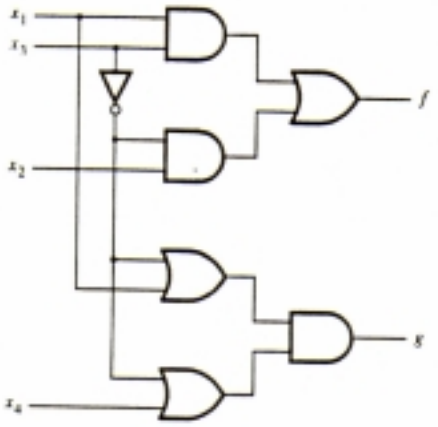
$(A+\overline{B})\overline{C}$

A = '0' and B = '0' and C = '0'
A = '1' and B = '0' and C = '0'
A = '1' and B = '1' and C = '0'

A	B	C	$\overline{B}$	$\overline{C}$	$A+\overline{B}$	$(A+\overline{B})\overline{C}$
0	0	0	1	1	1	1
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	1	0	1	0
1	1	0	0	1	1	1
1	1	1	0	0	1	0

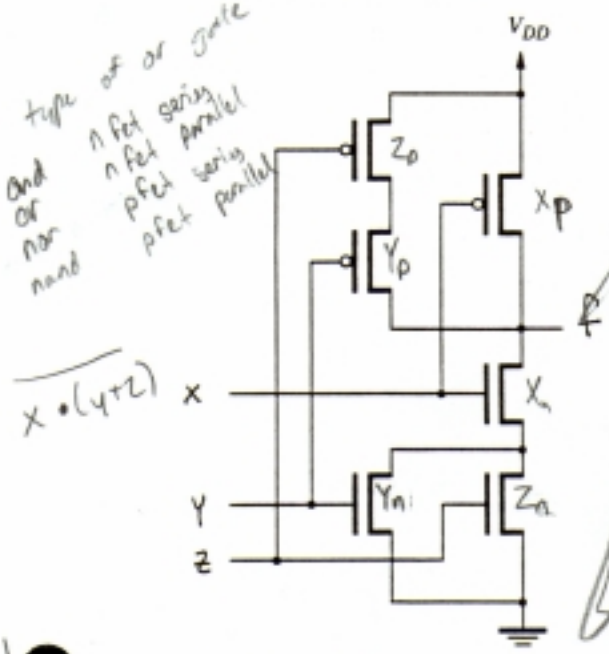
Name: Jesse Li

4. (20) Construct the VHDL listing that describes the logic circuit shown below:




```
entity Question_4 is
    port (x1, x2, x3, x4: in bit;
          f, g: out bit);
end Question_4;
architecture Structural of Question_4 is
begin
    f <= (x1 and x3) or (x2 and not(x3));
    g <= (x1 or not(x3)) and (not(x3) or x4);
end Structural;
```

5. (20) Given the following CMOS circuit, determine the function f(x, y, z).



type of or gate
and
or
nor
nand
n fet series
n fet parallel
pfet series
pfet parallel

X	Y	Z	X_n	Y_n	Z_n	X_p	Y_p	Z_p	f
0	0	0	Off	Off	Off	On	On	On	1
0	0	1	Off	Off	On	On	On	Off	1
0	1	0	Off			On			1
0	1	1	Off			On			1
1	0	0	On	Off	Off	Off	On	On	1
1	0	1	On		On	Off			0
1	1	0	On						0
1	1	1	On						0

$f(x,y,z) = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + \bar{x}yz + x\bar{y}\bar{z}$

$X \cdot (y+z)$

n fets in parallel
p fets in series
n fp in series

$f(x,y,z) = \bar{X} + \overline{y+z} = \overline{X \cdot (y+z)}$

$yz = 11$

$yz = 00$

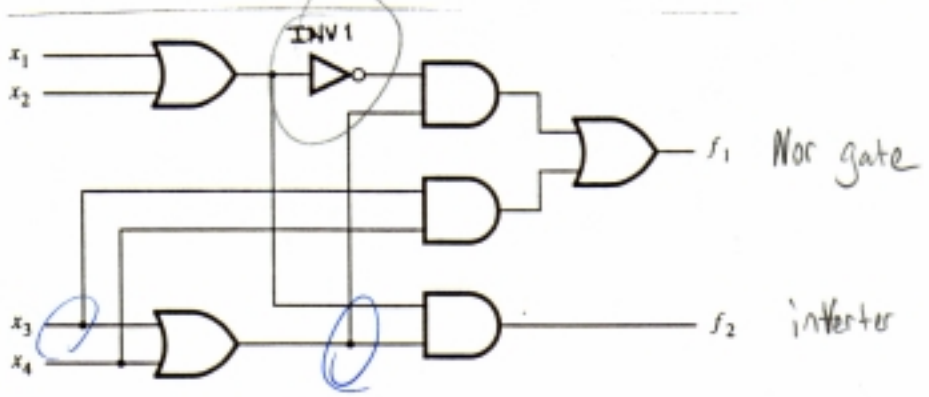
NOR

Name: Jesse Lee

6. (20) For the circuit below, calculate each of the requested delays, given the following parameters and assuming that the output $f_1(t)$ drives one NOR gate and that the output $f_2(t)$ drives one inverter:

$t_{p0,NOT} = 0.5$ ns $t_{pL,NOT} = 0.4$ ns $t_{p0,AND} = 0.85$ ns

$t_{pL,AND} = 0.95$ ns $t_{p0,OR} = 0.8$ ns $t_{pL,OR} = 0.9$ ns



(a) delay of INV1

$t_{Delay} = t_{p0,NOT} + t_{pL,and} = 0.5ns + 0.95ns = \boxed{1.45ns}$

(b) delay from x_3 to $f_2(t)$

$t_{delay} = t_{p0,or} + t_{pL,and} + t_{p0,and} + t_{pL,NOT}$

$= 0.8ns + 0.95ns + 0.85ns + 0.4ns = \boxed{3.0ns}$

-3

7. (7) Using $3x10^{10}$ cm/sec for the speed of light, "how long" is a nanosecond? In other words, what is the longest distance a signal can travel before inducing a 1 ns delay?

$d = 3\times10^{10}\frac{cm}{s} \cdot 1\times10^{-9}s = \boxed{30cm}$