CpE 318 Extra Credit (due 5/6/04) (10 points)

* use the revised architecture with the branching instructions for all questions.

[2] 1) In the microprocessor architecture without the branching instructions, `MOV R3 R1` could have been performed by its equivalent instruction `ADD R3 0000 R1`. However, in the new architecture this can no longer be done since the `MOV` instruction does not affect the FLAG register, while the `ADD` instruction does. Explain how `MOV R3 R1` can be performed in the new architecture. Does anything in the architecture, combinational logic, or function tables need to be modified? Explain.

[1 each] 2) What is the machine code, in binary, for the following instructions (use don't cares where applicable):
   a) `MOV R2 R1`
   b) `STR R3 [1100010]`
   c) `LD [1110010] R2`
   d) `BRZ [0101010]`
   e) `NOP`

[1 each] 3) What is the instruction corresponding to the following machine code:
   a) $2EE73A_{16}$
   b) `076D67h`
   c) `3670A1h`