CpE 313 Fall 2004
Microprocessor Systems Design
Homework 9
This HW is due in class on Oct 26, 2004.

Problem 1

In the issue stage of Tomasulo's algorithm you do not

(a) check for structural hazards
(b) read data operands if available
(c) read "tag" if data operand is unavailable
(d) grab pending operands from CDB and issue to FU

Problem 2

What is not a step of Tomasulo Algorithm

(a) issue
(b) execute
(c) load
(d) write result

Problem 3

Which of the following is NOT true for a scoreboard and Tomasulo's method?

(a) RO in scoreboard is divided into RAO and RPO stages in Tomasulo's algorithm
(b) IS and RAO are incorporated in the IS unit in Tomasulo's method
(c) In Tomasulo's method both instructions and operands are buffered but not in scoreboard
(d) In both the methods all operands need to be read at the same time

Problem 4

A reservation station DOES NOT

(a) buffer destination register value before it can be transferred to register file
(b) buffer an instruction
(c) fetch and buffer available operands
(d) buffer the tag of pending operands

Problem 5

Consider Tomasulo's Alg. Write back stage DOES NOT broadcast result and tag to:

(a) Register file.
(b) Instruction queue.
(c) Reservation stations.
(d) Store buffers.

Problem 6

In Tomasulo's Alg., all available operands are read at issue stage. Which hazard is reduced by this early reading?

(a) WAW.
(b) WAR and WAW.
(c) RAW.
(d) WAR.

Problem 7

Which of the following is a reason that Tomasulos Algorithm is better than Scoreboard?

(a) Scoreboard reads the available source operands immediately, which takes more time, while Tomasulos Algorithm does not
(b) Scoreboard does not use pipeline forwarding, while Tomasulos does
(c) Tomasulos algorithm has a special feature that stops the issuing of instructions to prevent WAW hazards
(d) Tomasulos algorithm implementation requires less transistors

Problem 8

Tomasulos algorithm does

(a) not prevent RAW Hazards
(b) not prevent WAR Hazards
(c) not prevent WAW Hazards
(d) prevent all three data hazards

Problem 9

A reservation station does **NOT** do the following.

(a) Buffer an instruction
(b) Buffer the available operands
(c) Buffer the output of the functional unit
(d) Buffer the tags of any pending operands

Problem 10

div r1,r2,r3
sub r4,r5,r1
mul r12,r13,r15

Consider the code above. Assume that div takes 60 cycles to execute. Is the statement that "mul cannot be reordered by hardware to precede sub because sub is fetched 1 cycle before mul is fetched" correct?

(a) Yes, because sub and mul instructions cannot be fetched simultaneously
(b) No, because although sub is fetched 1 cycle earlier than mul, sub waits in the issue stage for more than 1 cycles. This allows mul to bypass sub.
(c) No, because mul always has priority over sub
(d) No, because although sub is fetched 1 cycle earlier than mul, sub waits in the read operand stage for more than 1 cycles. This allows mul to bypass sub.

Problem 11

What is stored in the RPO buffer space?

(a) The operands that are immediately available
(b) The tags of the operands not yet available
(c) The opcode for the instruction
(d) A, B, and C are all true

Problem 12

Which the following is NOT true for pipelines dynamically scheduled using Tomasulos algorithm?

(a) Forwarding of results from ALL functional units to ALL reservation stations and store buffers is allowed.
(b) Operands could be read at different time.
(c) RO stage is effectively split into RAO and RPO
(d) All operands must be read at the same time

Problem 13

What will the Tomasulos algorithm do in the RPO stage?

(a) Read a data operand if it is available and read tag if operand is unavailable
(b) Wait until a pending operand becomes available on CDB and then grab it
(c) Broadcast result and tag to all reservation stations, store buffers and register files via CDB
(d) Only write the register file if CDB tag matches the tag in the register file

Problem 14

How does Tomasulo's algorithm resolve WAR hazards better than Scoreboard?

(a) In Tomasulo's algorithm, the result of the functional unit is forwarded to the instruction that needs it. Scoreboard, however, does not employ forwarding.
(b) In Tomasulo's algorithm, all operands are read at the same time. Scoreboard, however, reads only the available operands.
(c) In the case where only one operand, Rx, is available, Tomasulo's algorithm reads Rx as soon as possible so that a later instruction can write to Rx right away instead of being stalled in WB stage.
(d) Instructions are buffered and held in reservation station until they can be executed.

Problem 15

What is the function of the common data bus?

(a) To forward the output of any functional unit back only to other functional units
(b) To forward data from the instruction queue to all functional units
(c) To forward data from the FP register to all functional units
(d) To transfer data from output of functional units to other functional units, store buffers, and FP register

Problem 16

What kind of data cannot be found **waiting** in a reservation station?

(a) instruction
(b) available operands of the instruction
(c) tags of the pending operands
(d) pending operands

Problem 17

In the write result stage of Tomasulo's Algorithm, which unit will not receive the result and tag of the instruction from CDB?

(a) reservation stations
(b) store buffers
(c) load buffers
(d) register file

Problem 18

In Tomasulos' dynamic pipelining scheme, what is the significance of a tag?

(a) One tag is associated with every source operand of an instruction and is also associated with every register in the register file.
(b) A tag is associated only with a pending source operand of an instruction and is also associated with every register in the register file.
(c) A tag is associated with a functional unit.
(d) A tag is placed on a data item to indicate whether it is valid or not

Problem 19

In Tomasulo's algorithm the number of tag bits would be

(a) Log2(Number of functional units)
(b) Number of functional units
(c) 2(Number of functional units)
(d) Number of bits in a pending operand

Problem 20

In what stage for Tomasulo's Algorithm are unavailable registers renamed? Why?

(a) In stage "Issue", to indicate the producer of the unavailable operand.
(b) In stage "Read Pending Operands", to indicate the producer of an unavailable operand.
(c) In stage "Write Result", to specify the tag of the result that is being written on the common data bus.
(d) In stage "Read Pending Operands", to specify the register that the instruction needs to write to.

Problem 21

Which of the following is not a task for the reservation stations of the Tomasulo algorithm?

(a) Buffer an instruction.
(b) Fetch and buffer "ready" operands.
(c) Buffer the tag of any pending operands.
(d) Record the status of the instruction that will produce the pending operand

Problem 22

Which of the following most accurately describes how the information that is put on the CDB is used, according to the Tomasulo algorithm?

(a) The reservation stations keep track of the status of the instruction that will supply the desired operand and blindly use the data on the buss when the instruction finishes.
(b) Two pieces of information are put on the bus, a "tag" and the data. The tag is the number of the FU that produced the data and the data is the product of the instruction. The reservation stations pick up the data from the bus when the tag matches the one they are waiting for.
(c) Two pieces of information are put on the bus, the destination register address and the data itself. When a reservation station sees the destination register it is waiting for on the bus, it stores the data.
(d) The only data on the bus is the result of the instruction. A control unit tells the reservation stations when to store the data on the bus.

Problem 23

When will the tag of the register file be written in dynamical pipeline scheduled by Tomasulo's Algorithm?

(a) IF stage
(b) IS stage
(c) RAO stage
(d) WB stage

Problem 24

If there are 6 functional units in a dynamic pipeline scheduled by Tomasulo's algorithm, how many bits should the tag in register file have?

(a) 1
(b) 2
(c) 3
(d) 4

Problem 25

During which stage of Tomasulo's Algorithm are the result and tag broadcasted to all reservation stations, buffers stored, and file registered via the CDB?

(a) Issue
(b) RPO
(c) Execute
(d) Write result