Closed Book, Cheat-sheet portion
CpE311 – Final Exam, F02

Name _____

Show all your work in the space provided. Answers with a simple "yes", "no", or a single number are typically incomplete and will not be given full credit. Answers in non-reduced form, like (a+sqrt(b))/c, are fine where appropriate. Good English on essay/short answer questions is required. ON MULTIPLE CHOICE QUESTIONS, IF YOU'RE NOT SURE GUESS CAREFULLY– you will get points off for wrong answers. If you know part of an answer, write what you know for partial credit.

1. (15 Points) Briefly discuss the following points about JTAG: a) What is it, b) what is it good for, c) how does it work (briefly). Please stay within the space provided.

2. (5 Points) Scan testing is most useful for testing: (mark all that apply):

a) before manufacture	b) after manufacture	c) combinational logic
d) sequential logic	e) Systems	f) None of the above

3. (15 Points) There are several causes of power loss within an IC. Briefly explain what they are and how they occur. Note which cause is responsible for most IC power loss.

4. (15 Points) What is the cause of power supply noise in the logic core? Identify some strategies for eliminating this problem. Please stay within the space provided.

Name _____

Open Book, Open Notes Portion.

(You must turn in your closed book portion before opening your book or notes!)

5. (7 Points) How much current can be supplied reliably by a 40λ wide power line in a pad ring, assuming a 0.5 micron process and T = 125 degrees C. State any assumptions.

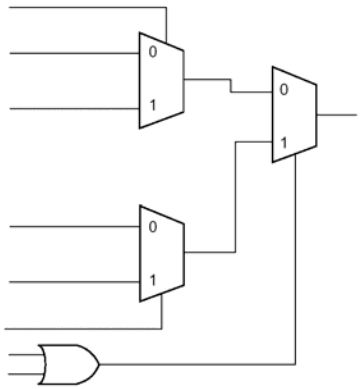
6. (13 Points) Following is a VHDL model intended for synthesis to a 40MX02 part. What is the likelihood that it will fit? Explain your reasoning.
   HINT: the package numeric_std allows definition of signed and unsigned integers as vectors of std_logic and provides the associated mathematical operations. Thus, signals a, b, and f are all std_logic_vectors.

```
library IEEE;
use IEEE.std_logic_1164.all;
use ieee.numeric_std.all;

entity e1 is
    port(a,b: in signed(7 downto 0);
        f:out signed(15 downto 0));
end entity e1;

architecture a1 of e1 is
begin
    f <= a*b;
end;
```

7. (15 Points) Implement the following logic using ACT1 logic modules:

   Z <= not (A and (B or C));

   Only A, B, and C are available (not their complements). Try to use as few modules as possible. Show your work. One module is given for you. (Note: a bit tricky).



8. (15 Points) Provide the layout for the following circuit, similar to what you did in lab 4 using IC station. You may use stick diagrams if you like (i.e. you do not have to provide proper sizing of or spacing between elements but must show general geometry). You do not need to show well connections. Please use color if possible and identify the material associated with each color.