CpE 318 HW#5 (due 4/15/04) (15 points)

1) Design a generic unsigned MAC

* entity name: *MAC*
* generic constants: *X_len*, *Y_len*: positive, default to 8 (X_len ≤ Y_len); *A_len*: positive, default to 24
* inputs: *X*, *Y*: arbitrary length std_logic_vector (assume ≥ 4); *clk*, *reset*: std_logic
* outputs: *A*: arbitrary length std_logic_vector (assume ≥ X_len+Y_len); *OV*: std_logic

* name your file: lastname_student#_5.vhd
* include as comments: name and student number (-- precedes a comment line)

* components to use: FA, HA, AND2, DFF0

* email your main design and components as attachments from the PC (ftp to PC) to: cpe318@umr.edu
* your design will then be run on my testbench
* you should write your own testbench to test your design, however you should not turn this in
* make sure that all names and input/output order match those on this sheet, otherwise your design will not run on my testbench and you will receive 0 points

Hints:
- use the array structured multiplication algorithm
- register the overflow and take both *OV* and *A* from the FF output
- the following constructs may be helpful:
  type twoD_array is array(3 downto 0, 3 downto 0) of std_logic;
  signal intermediate: twoD_array;
  intermediate(3, 0) <= '1';