CpE 213
Digital Systems Design
8051 I/O Programming
8051 External Memory Access

Lecture 16

Monday 10/17/2005

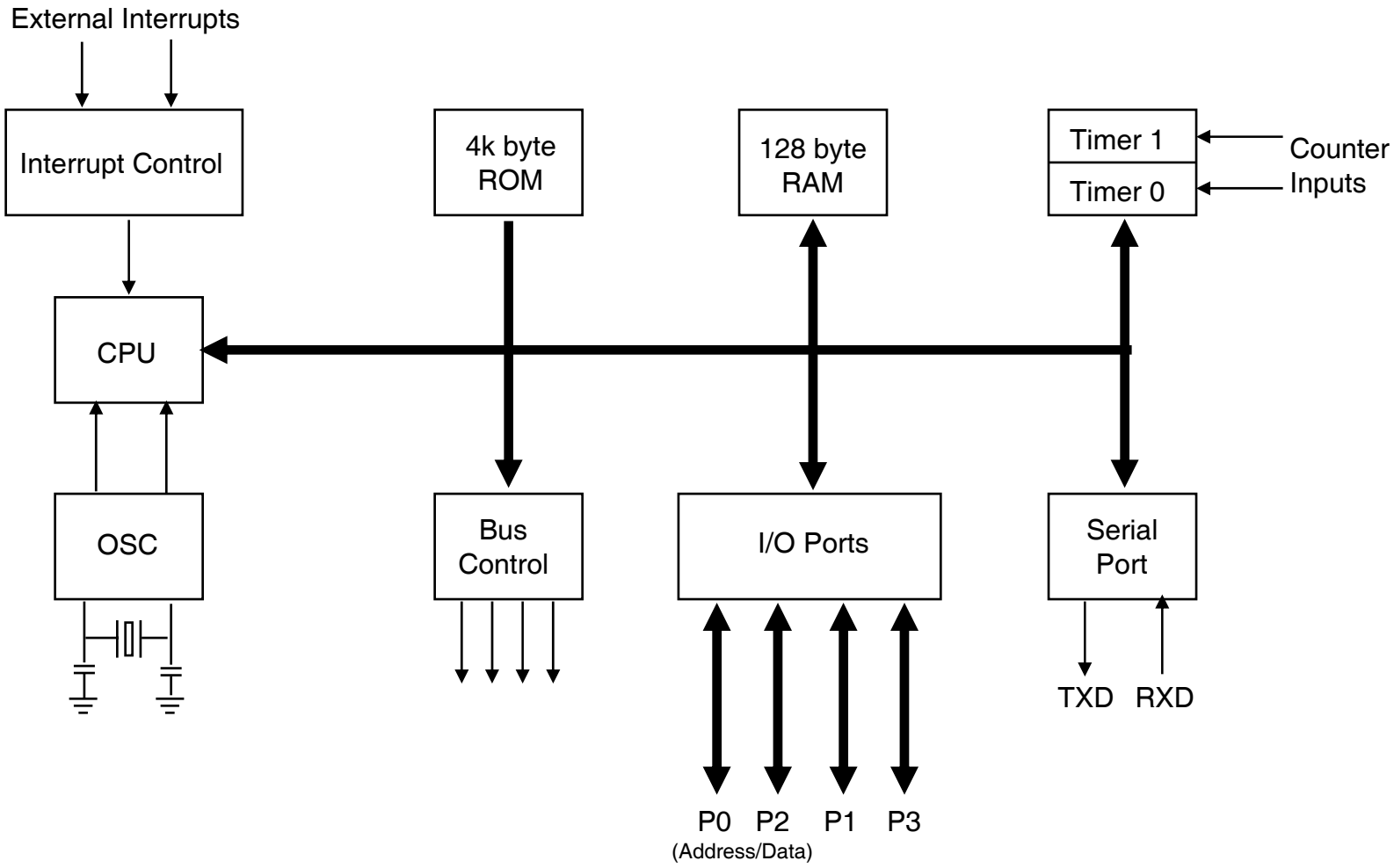
Overview

- 8051 I/O port programming
- 8051 external memory access

8051 I/O Port Programming

Some slides adapted from Mr. K. T. Ng and Mr. P. Kanan

8051 Block Diagram

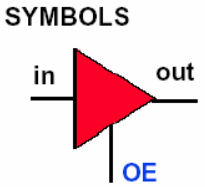


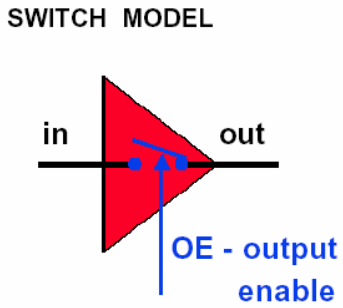
Why Are I/O Ports Needed?

- Controllers need to get external inputs and produce external outputs.
- I/O ports serve this purpose.
- 8051 has 4 built-in I/O ports.
  - All ports have multiple functions (except P1)
- Too many ports increase pin-count and device
- cost.
- Too few make the microcontroller inadequate for complex control needs
- Ports are generally scarce and port usage and allotment are critical engineering decisions.
- To increase the number of ports for the 8051, use a parallel port interface chip, such as the *8255.*

Tri-state Buffer Gate

- A tri-state buffer has the ability to provide three different output modes
  - current sinking ("low" logic level)
  - current sourcing ("high")
  - floating ("high-Z," or *high-impedance*).
- Such gates require an extra input terminal to control the "high-Z" mode, and this input is usually called the *enable*.



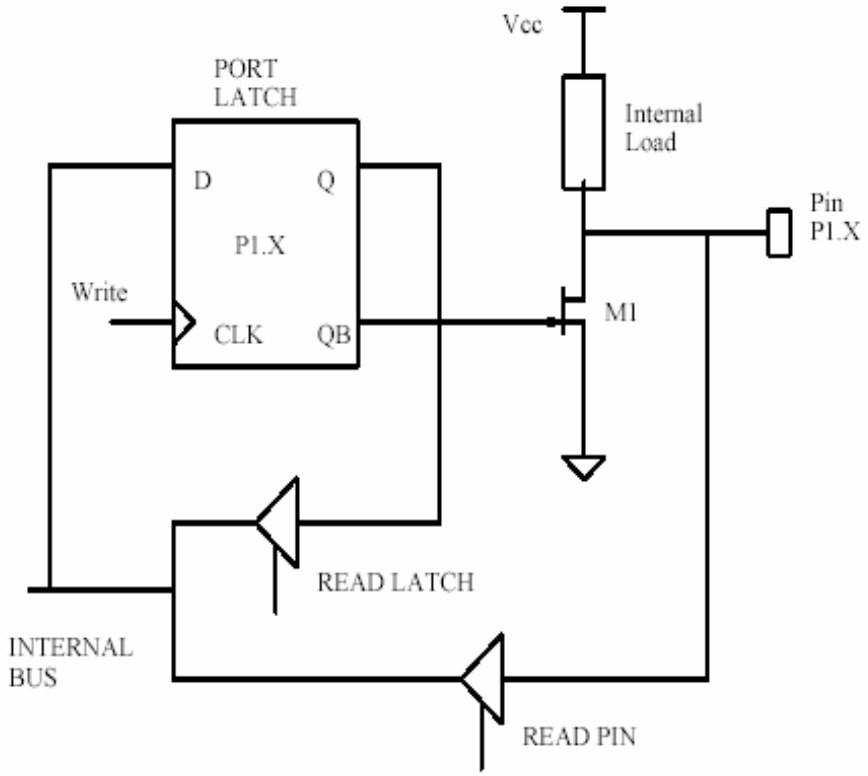


OE	in	out

Z = High Impedance output not connected to input

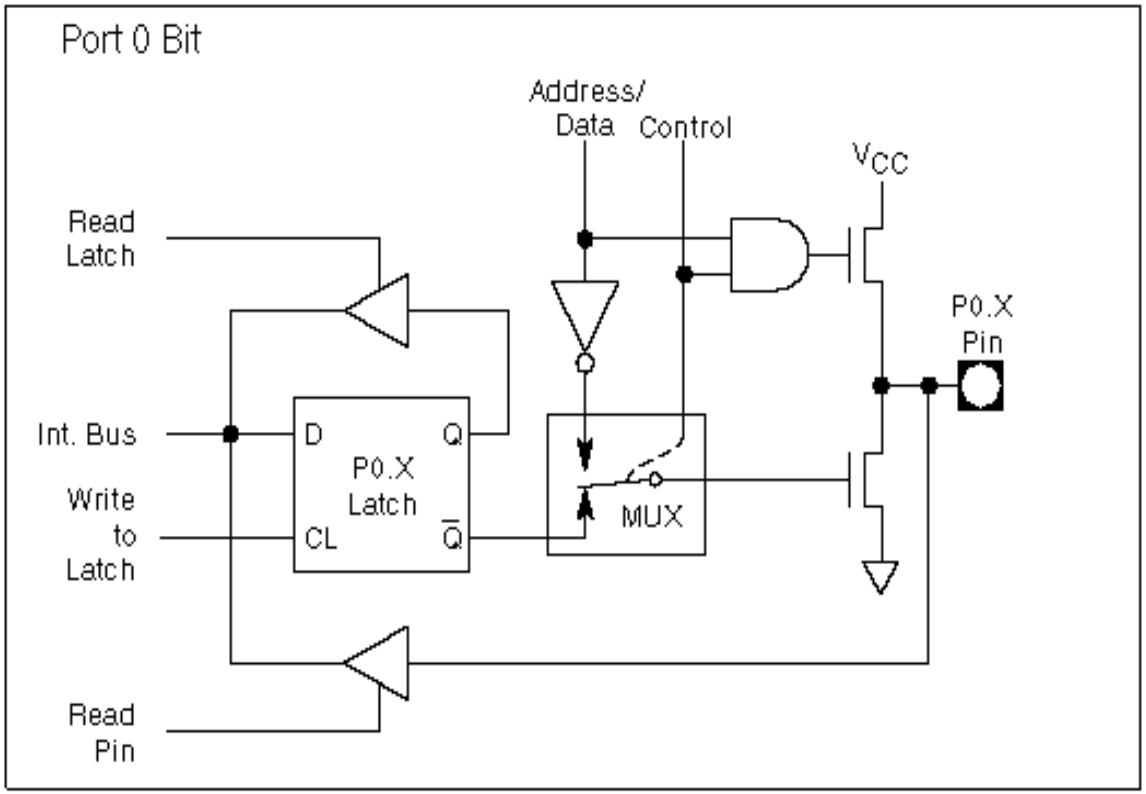
Internal I/O Port Structure

- 32 pins are allotted for 4 eight bit I/O ports.
- P0, P1, P2, P3
- At power-on all are _____ ports by default.



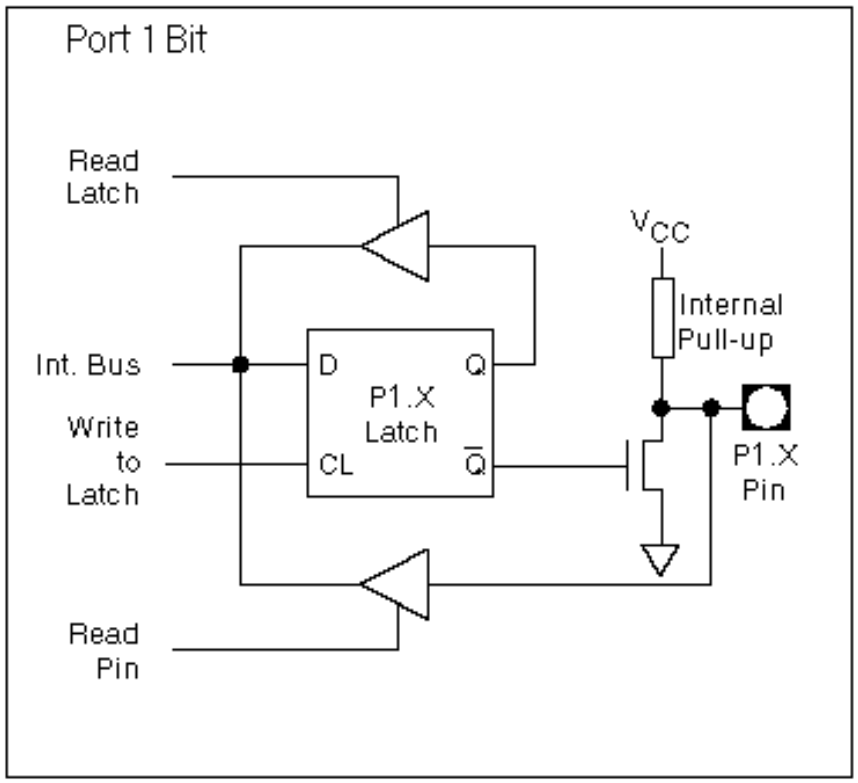
- To configure any port bit for input, write a 1 to the port bit.
  - Q=__, QB=__, M1=____,
  - Read_Pin asserted by read instruction

Port 0



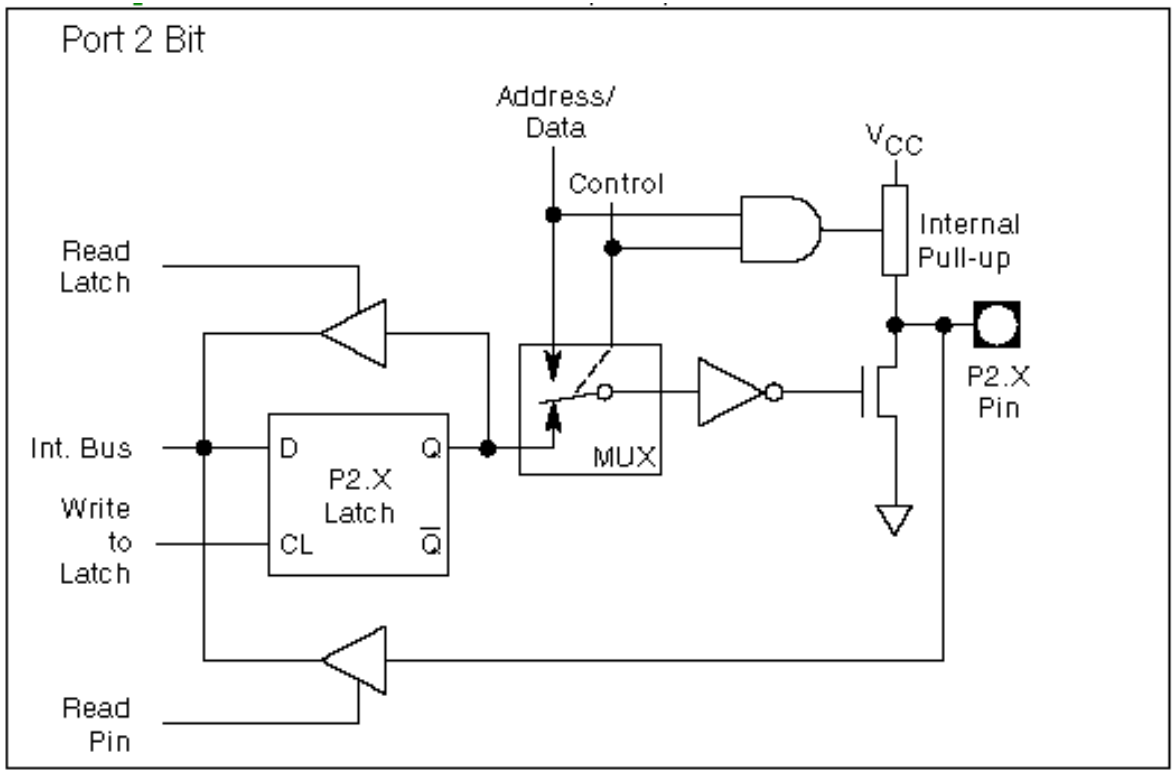
- Port 0 is dual-purpose:
  -
  -

Port P1



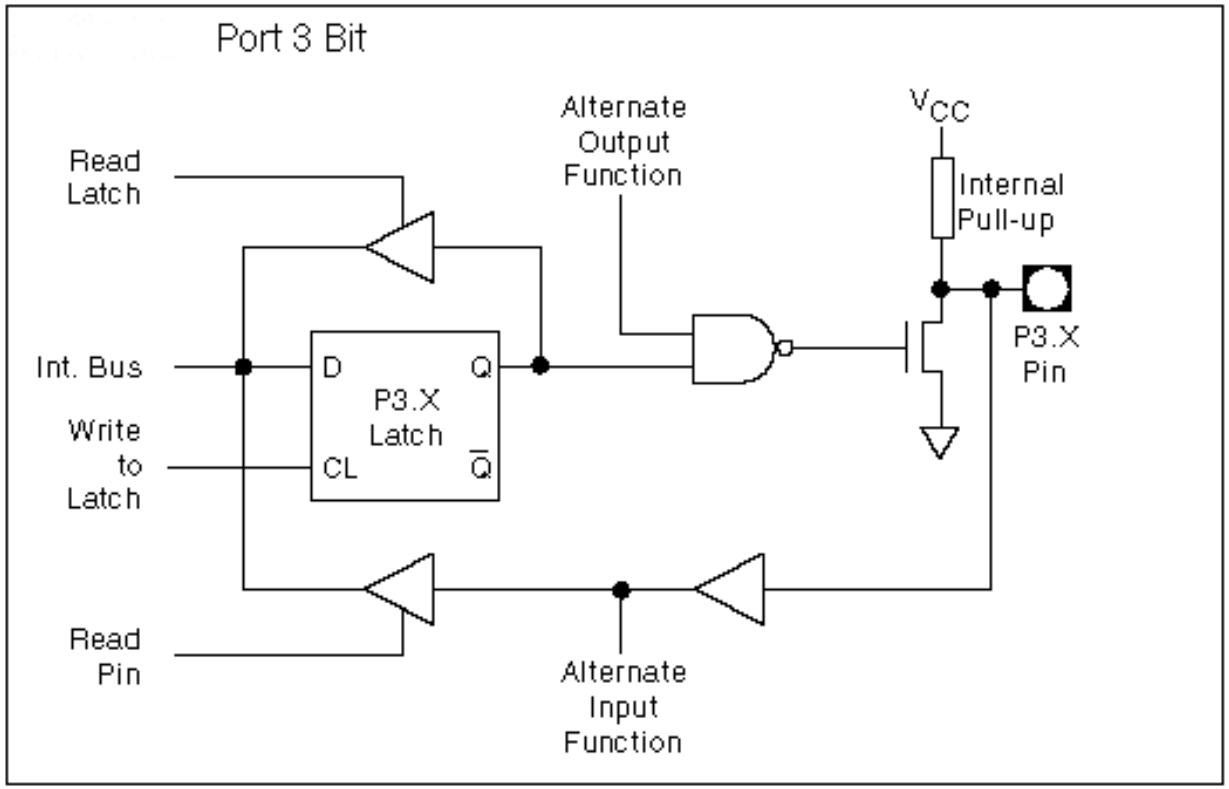
- Port 1 is a _____ I/O port.

Port P2



- Port 2 is dual-purpose:
  -
  -

Port P3



- Port 3 is dual-purpose:
  -
  - _____: serial, external interrupt, timer/counter, external data read and write.

Hardware Specifications

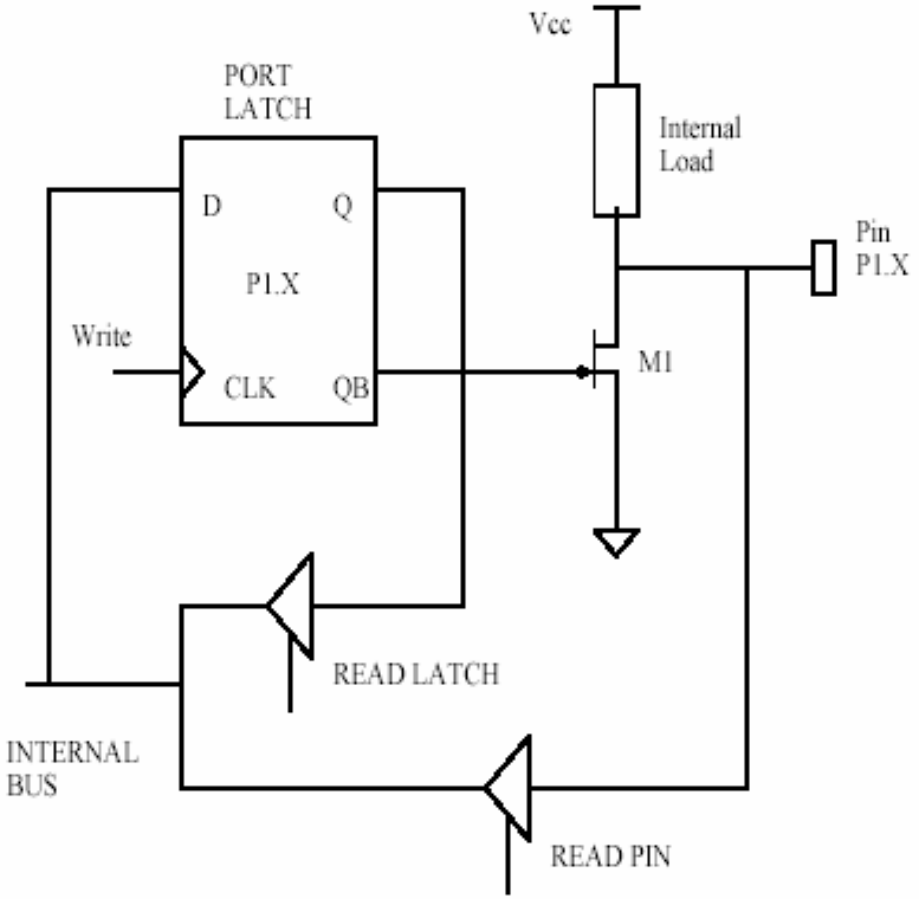
- P0 is open drain.
  - Has to be pulled high by external 10K resistors.
  - Not needed if P0 is used for address/data lines.
- P1, P2, P3 have internal pull-ups.
- Port fan-out (number of devices it can drive) is limited.
  - Use buffers (74LS244, 74LS245, etc) to increase drive.
  - P1, P2, P3 can drive up to 4 LS-TTL inputs
  - P0 fan-out is dependent on the pull-up resistor value, limited by the max current it can sink on the output stage.

8051 I/O Port Instructions

- Ports can be read from and written to like normal registers
  - `mov A, #55H   ; can use A`
  - `mov P0, A     ; write A to P0`
  - `mov P1, A`
  - `mov P2, #0AAH ; can use immediate mode`
  - `xlr P1, #0FFH ; read-modify-write (ex-or)`
  - `mov P0, #0FFH ; configure P0 for input`
  - `mov A, P0     ; read from P0`
- Ports can be bit-manipulated (are single bit-addressable) using cpl and setb instructions
  - `cpl P1.2     ; complement bit 2 of Port1`
  - `setb P1.3    ; set bit 3 for Port1 to 1`
  - `clr P0.0     ; clear bit 0 of Port0`

Input Quirks

- Port read instructions either
  - Read from the 8051 pins ("voltage" levels on the pins)
  - Read from an internal latch on the ports
- Writing 1 to the latch
  - Q=__, QB=__
  - M1 ____
  - P1.x is available at tristate buffer
- Writing 0 to the latch
  - Q=__, QB=__
  - M1 ____
  - Input always gets 0
  - Can **damage** the port (M1) if P1.x is Vcc
  - Use 10K resistance between switch on P1.x and Vcc
  - Or use a SPST switch connected to GND

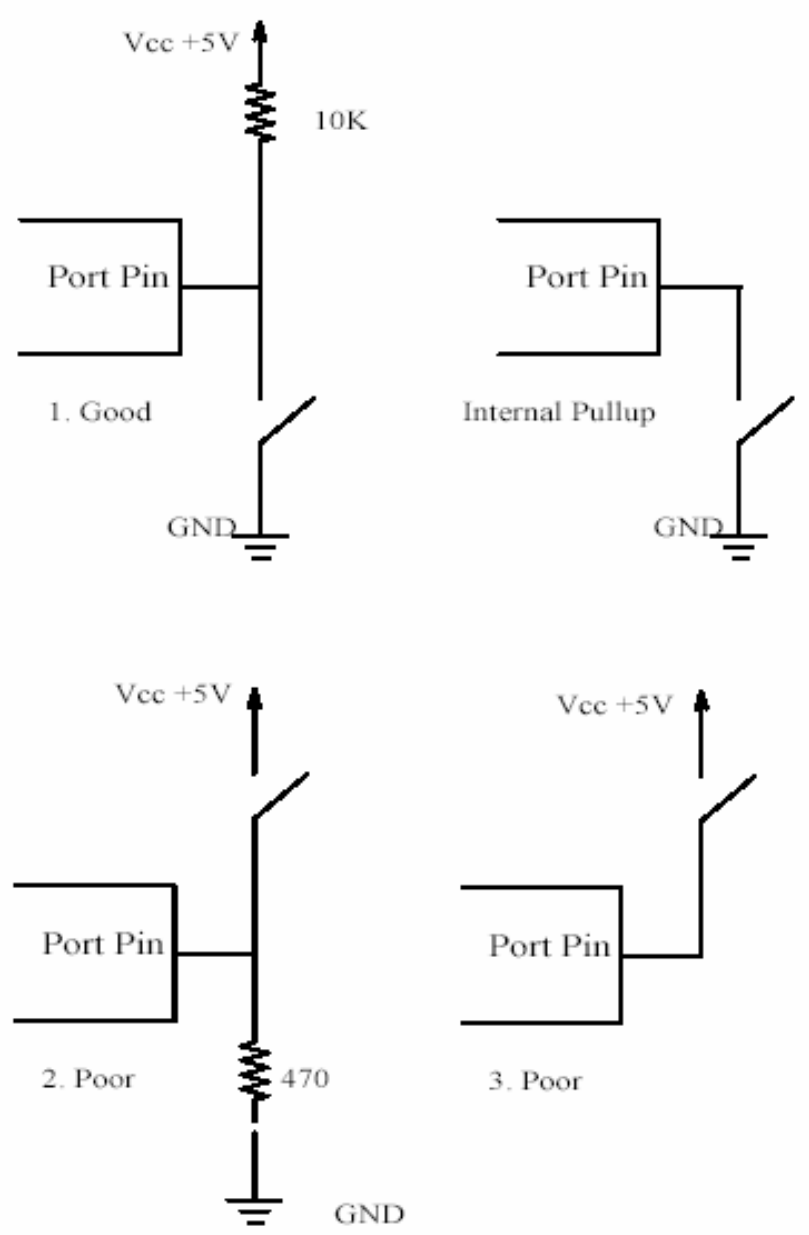


Input Quirks

- Instructions that read the pins (READ_PIN is asserted)
  - **`mov A, Px`**
  - **`jnb Px.y …`**
  - **`jb Px.y …`**
  - **`mov C, Px.y`**
- Instructions that read the latch (READ_LATCH is asserted)
  - They read the last output value and not the value on the pins
  - **`[anl, orl, xrl] Px`**
  - **`[jbc, djnz] Px.y, target`**
  - **`[cpl, clr, setb] Px.y`**
  - **`[inc, dec] Px`**

Switch on I/O Ports

- Case 1 (top left and right):
  - Gives a logic ___ on switch close
  - Current is 0.5ma on switch close
  - Pull-up needed if P0
- Case 2:
  - Gives a logic __ on switch close
  - High current on switch close
- Case 3:
  - Can damage port if 0 is output



8051 External Memory Access

Some slides adapted from Mr. K. T. Ng

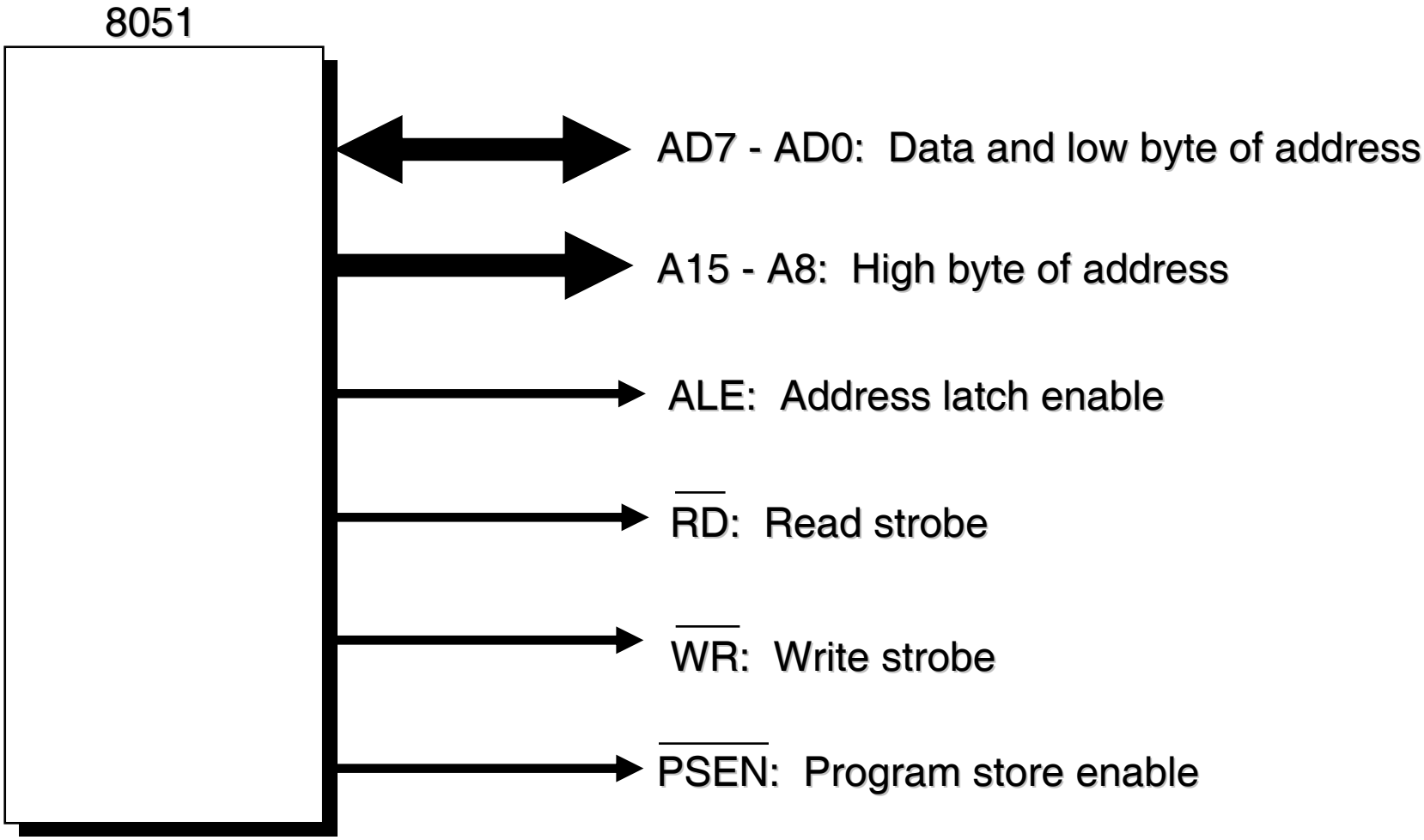
8051 Memory Expansion

- Some applications require more memory than the on-chip resources of a microcontroller provide.
- The 8051 architecture provides expansion capabilities in form of _____ external code memory space and ____ external data memory space.
- Peripheral interface ICs can also be added to expand the I/O capability.
- These become part of the external data memory space using memory-mapped I/O.
  - Memory-Mapped I/O: A method of input/output that addresses each I/O device as a memory location selected by a ___-bit address.
- The only drawback of using external code or data memory is the _____ of parallel I/O ports.
  - The I/O function of port __ and port __ is disabled.

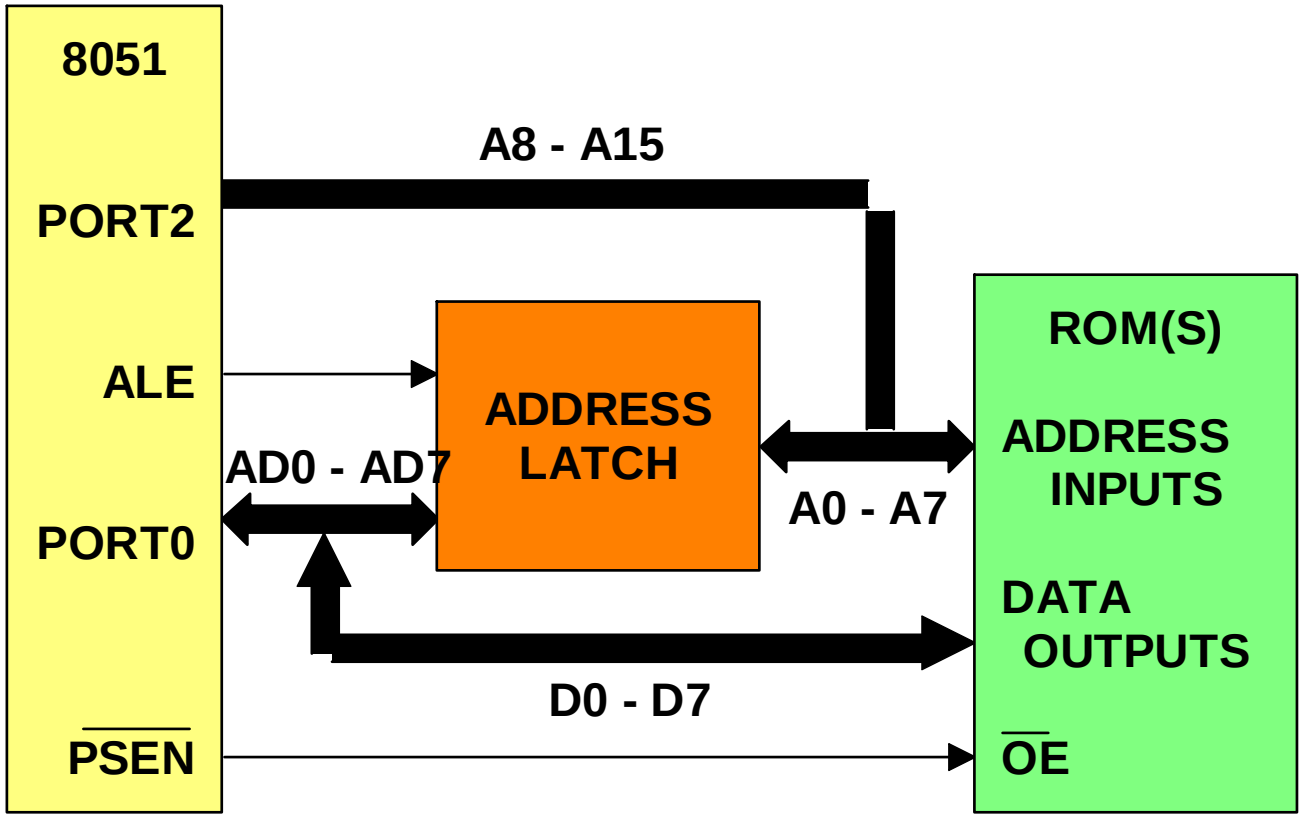
External Memory

- When external memory is used:
  - Port ___ is unavailable as an I/O port. It becomes a multiplexed address (A0 - A7) and data (D0 - D7) bus.
  - Port ____ is usually (but not always) employed for the high-byte of the address bus.
  - Control signals to be used:
    - ALE (Address Latch Enable): to latch the low byte of an address during access to external memory.
    - EA (External Access): tied low to access program code memory from external ROM.
    - PSEN (Program Store Enable): used as the read signal for external program memory.
    - RD (Read): read signal to access external data memory.
    - WR (Write): write signal to access external data memory.

External Bus Expansion



External Program Memory Access



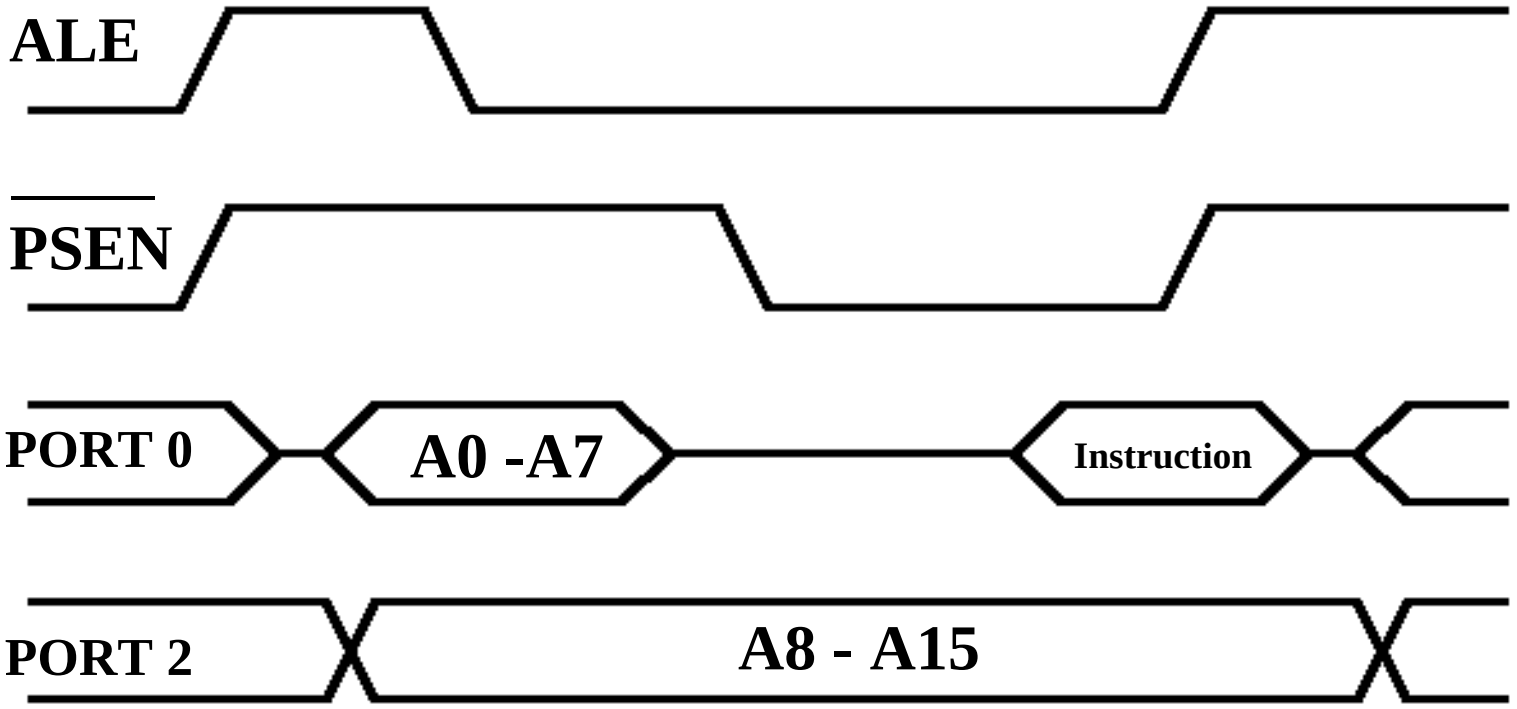
External Program Memory Access

- External Program Memory is accessed under two conditions:
  - Whenever the signal $\overline{EA}$ is active (i.e. tied LOW), or
  - Whenever the program counter (PC) contains an address greater than the size of its internal program memory.
- Accesses to external program memory use the signal $\overline{PSEN}$ (program store enable) as the read strobe.
- Fetches from external program memory always use a 16-bit address. Thus all 8 bits of port 2 are dedicated to an output function and cannot be used for general purpose I/O.

Timing Sequence for External Program Memory Access

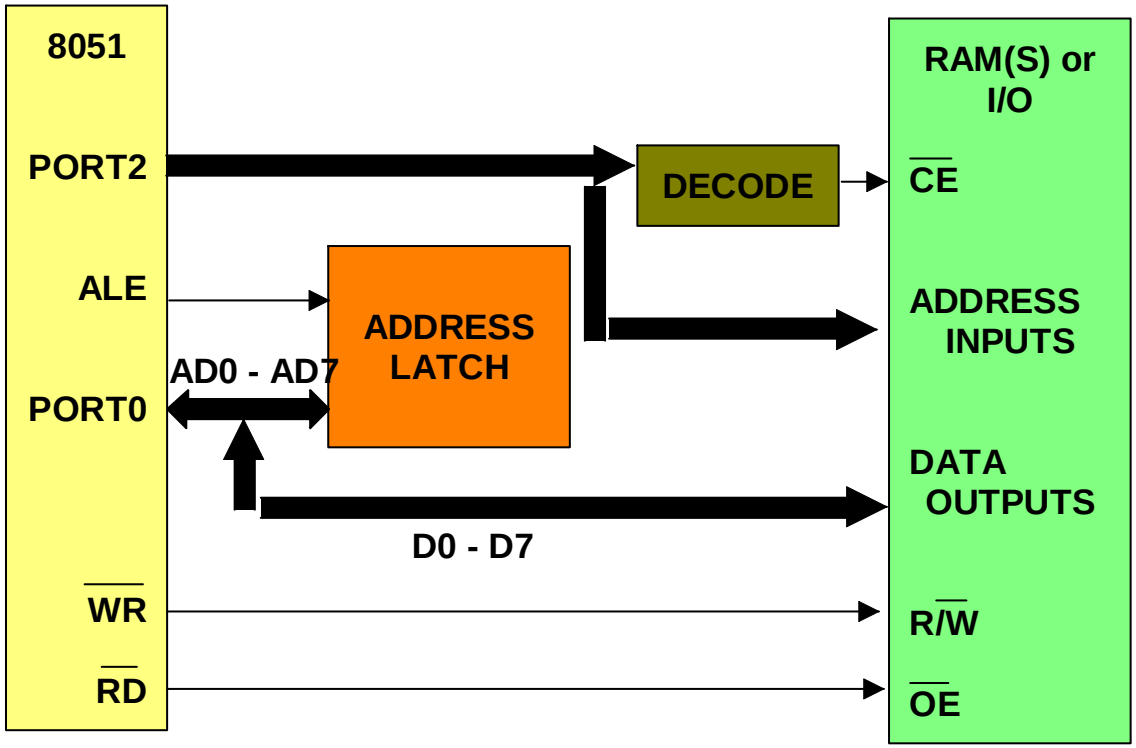
- Output a stable address:
  - Output the high byte of the address on the address bus (port ___).
  - Raise the _____ line.
  - Output the low byte of the address on the data bus (port ___).
  - Lower the ____ to latch the low address byte.
- For a code memory read:
  - Lower _____.
  - Read data supplied by code memory on data bus (port ___).
  - Raise _____.

8051 External ROM Read Cycle



External Data Memory Access

- 64K byte address space.
- Indirectly addressable via R0 and R1 in 256 byte segments.
- Entire space in indirectly addressable via the data pointer DPTR.



External Data Memory Access

- Access to external data memory uses $\overline{RD}$ or $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory.
- Access to external data memory can use either a 16-bit address (MOVX @ DPTR) or an 8-bit address (MOVX @ Ri).
- One byte addresses are often used in conjunction with one or more other I/O lines to page the RAM.
  - Using port lines to page RAM is an economical way to use external memory since any port lines not used for paging can be used for normal I/O functions.

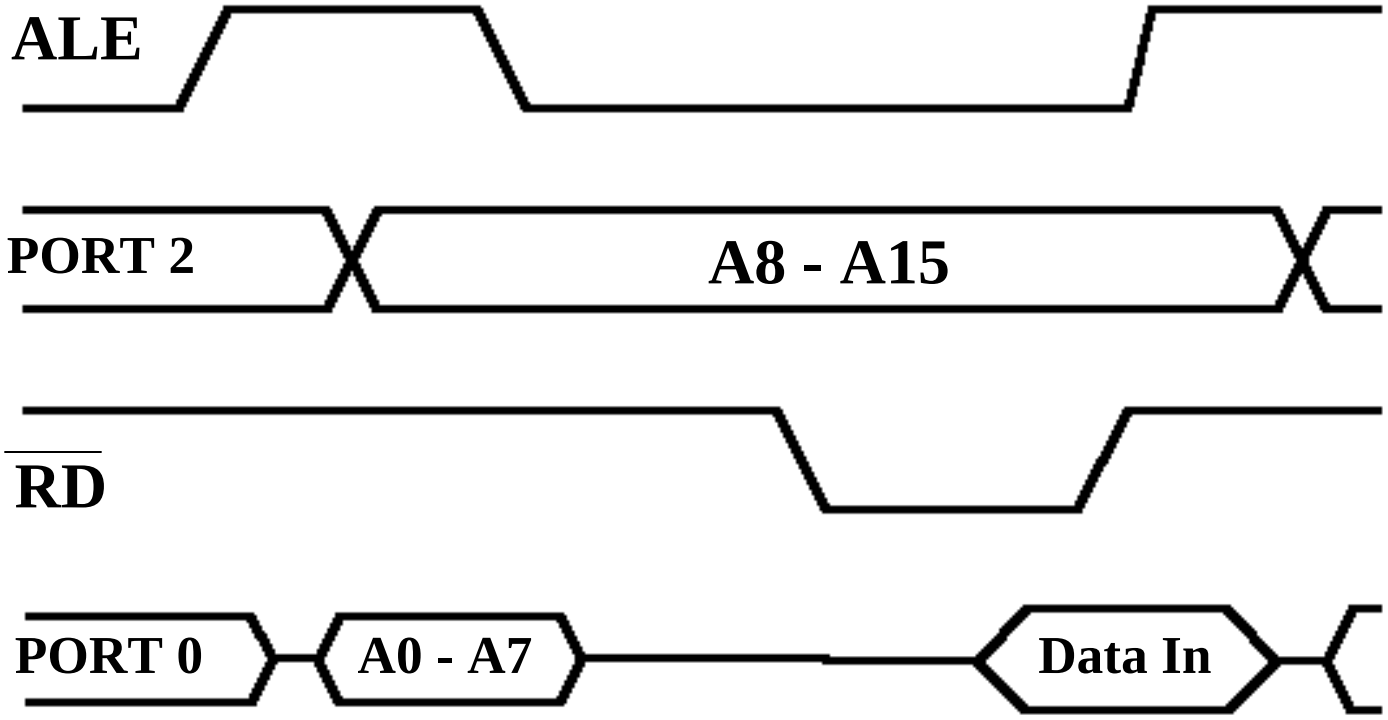
Timing Sequence for External Data Memory Access

- Output a stable address:
  - Output the high byte of the address on the address bus (port ___).
  - Raise the ____ line.
  - Output the low byte of the address on the data bus (port __).
  - Lower the ALE to latch the low address byte.
- For an external data memory read:
  - Lower ____.
  - Read data from external data memory on data bus (port 0).
  - Raise ____.

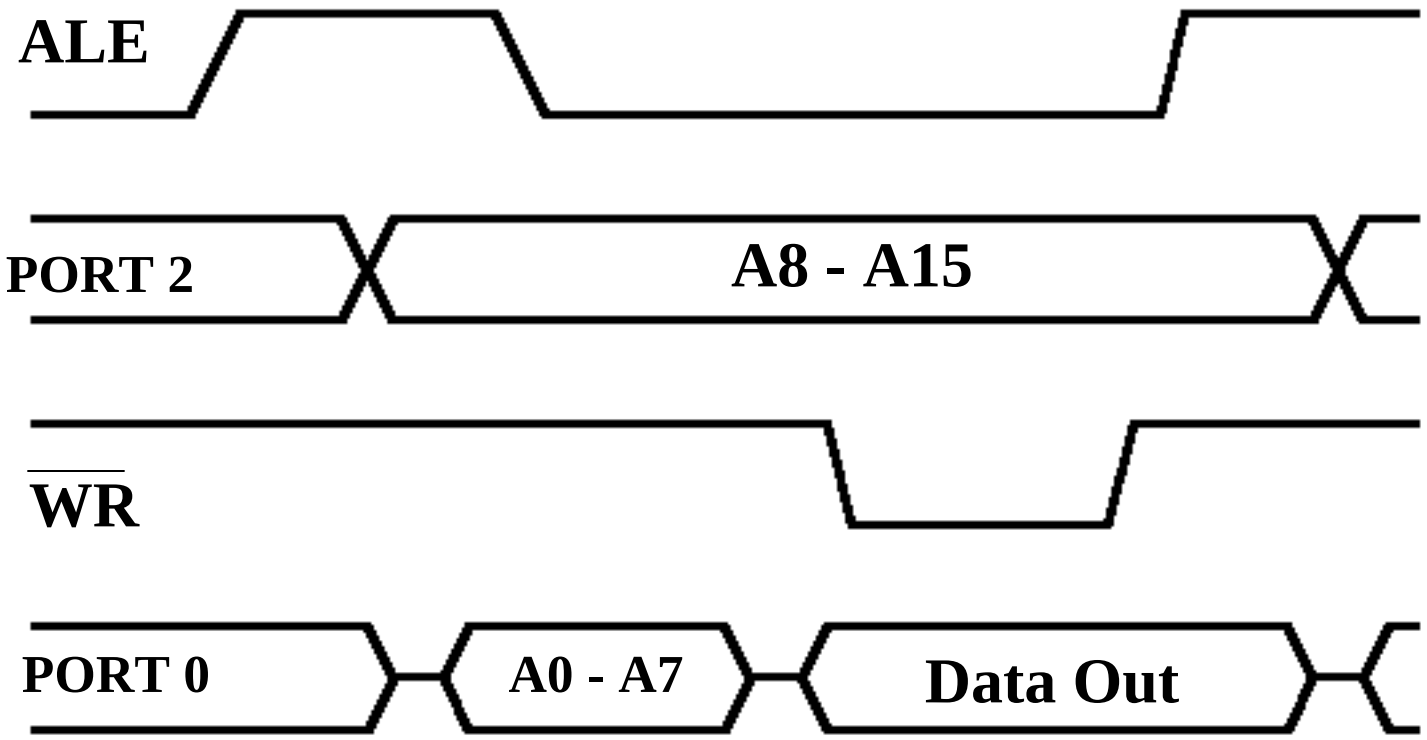
Timing Sequence for External Data Memory Access

- Output a stable address:
  - Output the high byte of the address on the address bus (port 2).
  - Raise the ____ line.
  - Output the low byte of the address on the data bus (port ___).
  - Lower the _____ to latch the low address byte.
- For an external data memory write:
  - Output data to data bus (port __).
  - Lower ____.
  - Raise ____.

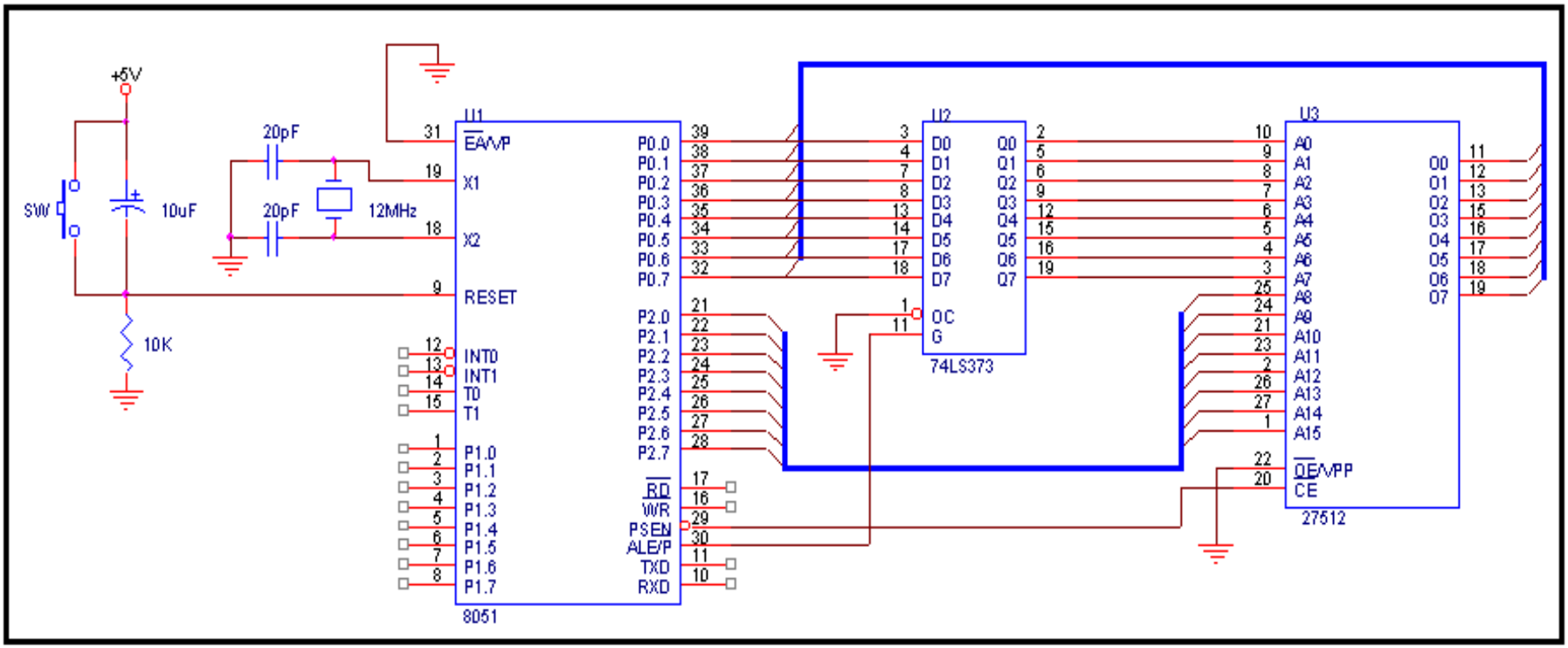
8051 External RAM Read Cycle



8051 External RAM Write Cycle

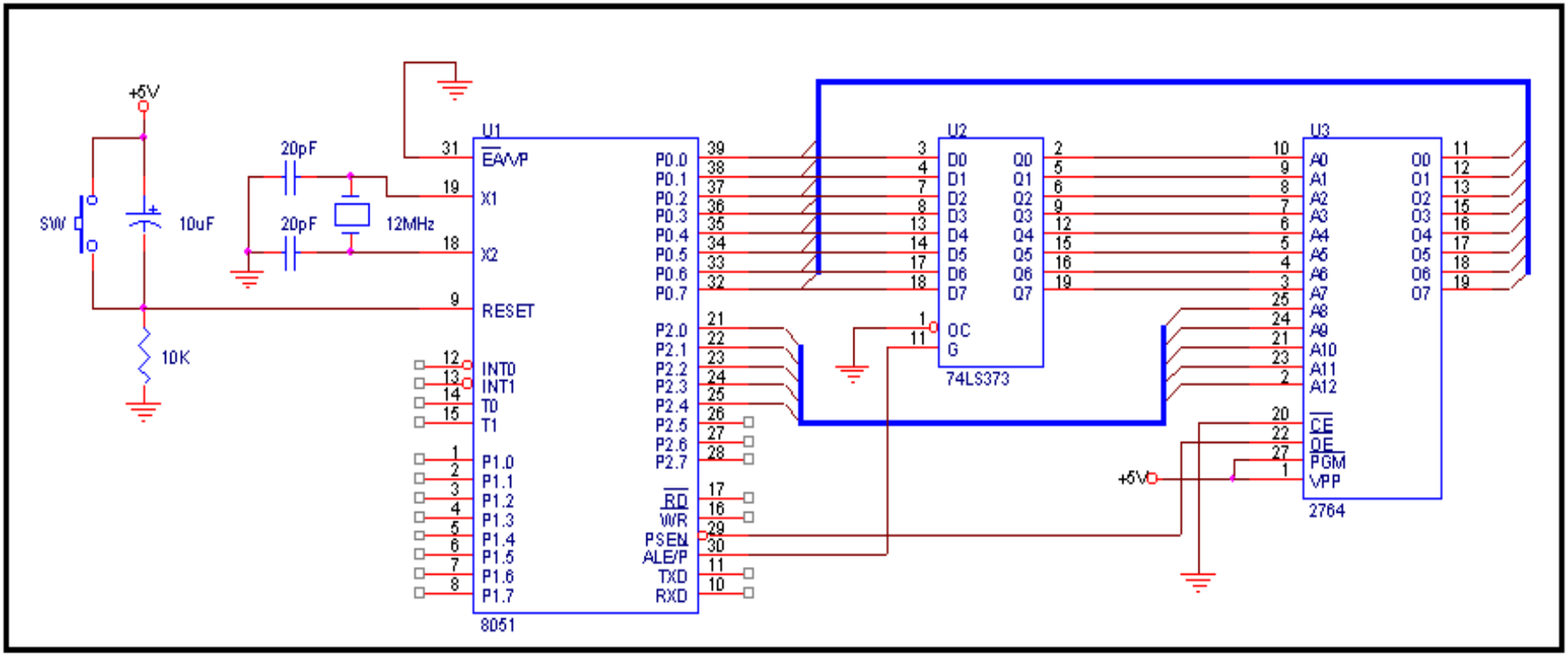


External Memory Expansion Example 1



Interface to 64K EPROM

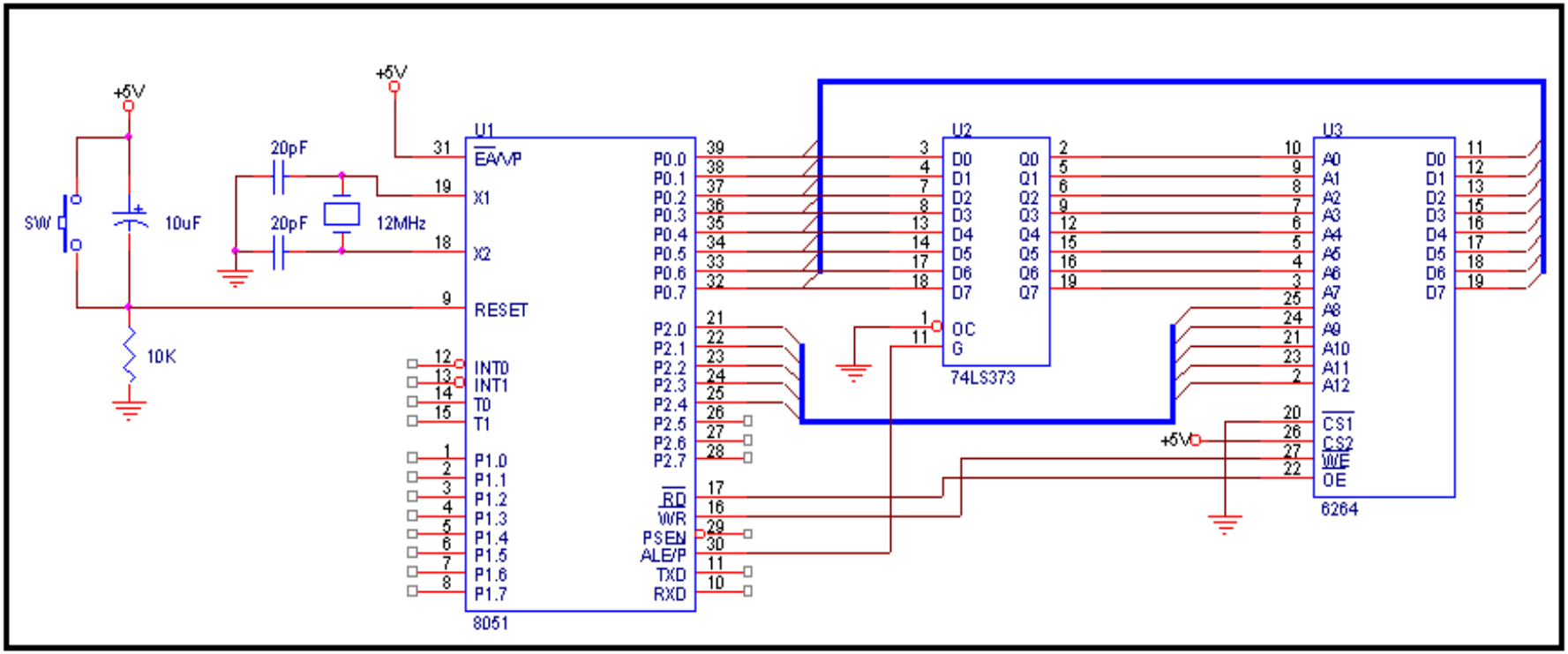
External Memory Expansion Example 2



Interface to 8K EPROM Only

Note: the remaining 3 lines of Port 2 CANNOT be used for I/O

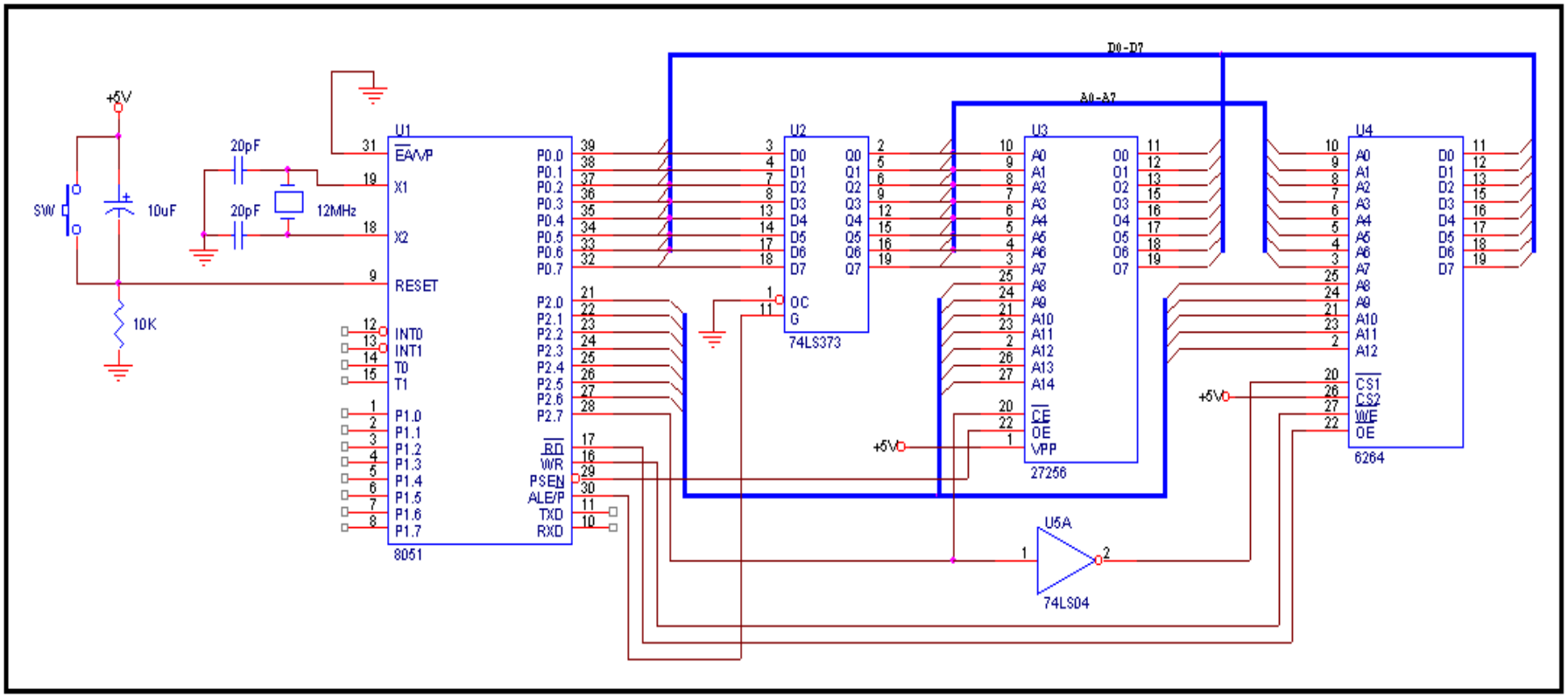
External Memory Expansion Example 3



Accessing external data memory.

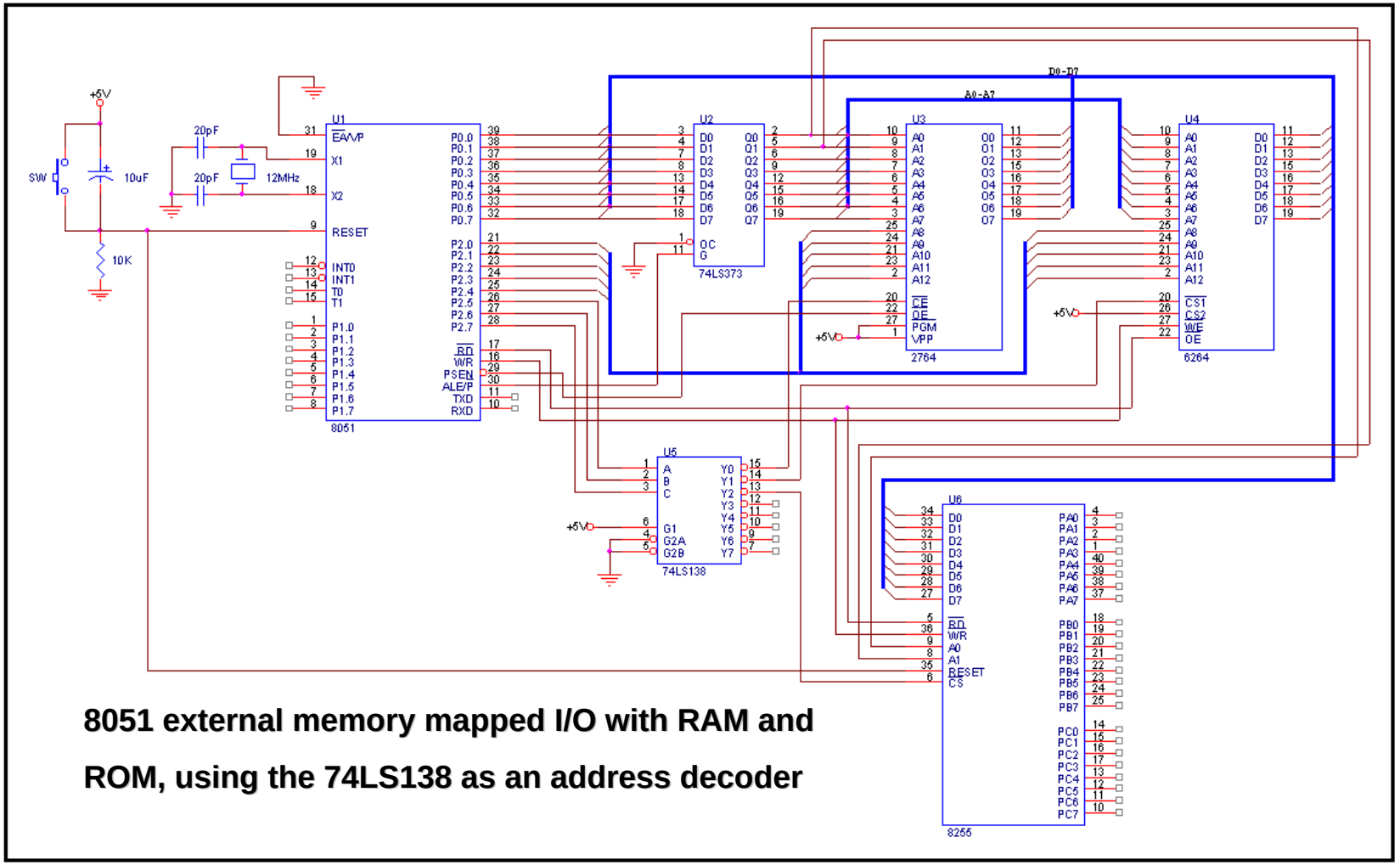
If the program memory is internal, the other bits of port2 are available as I/O.

External Memory Expansion Example 4



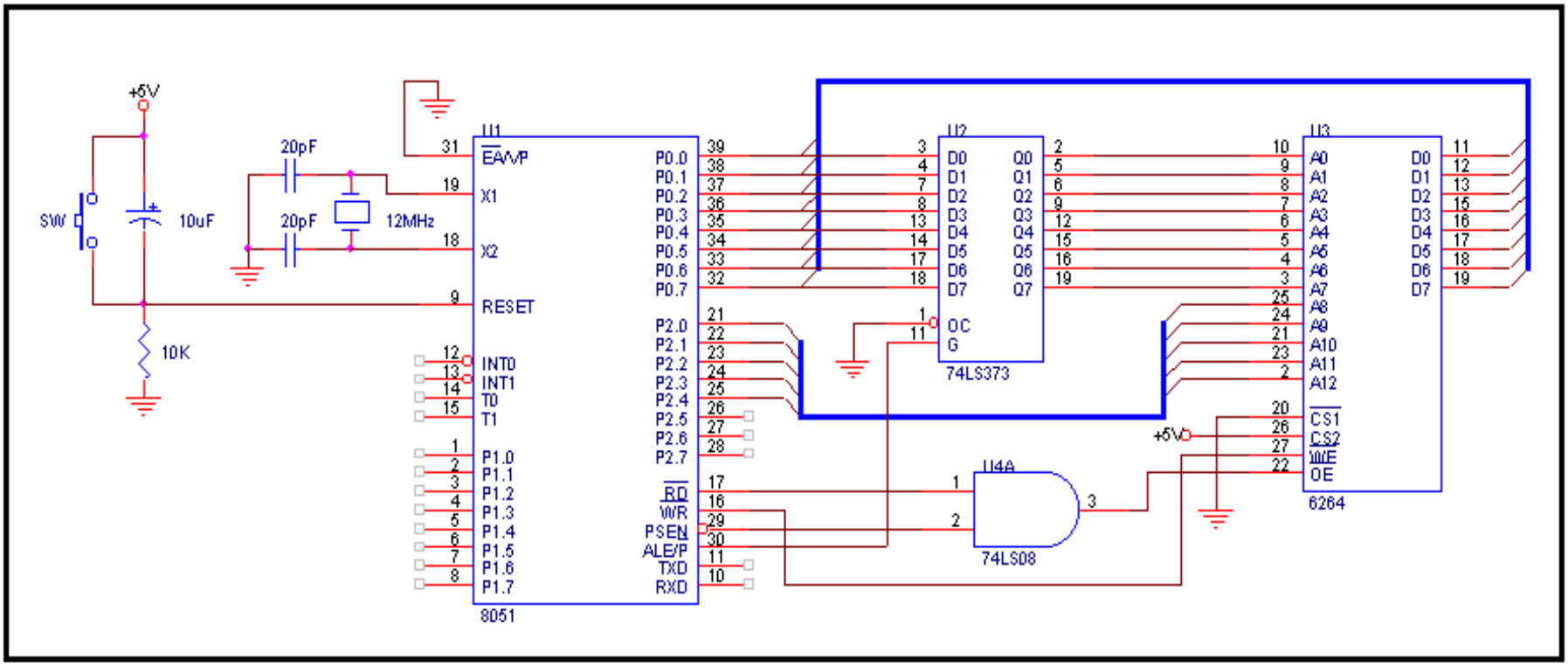
8051 with expanded RAM and ROM

External Memory Expansion Example 5



8051 external memory mapped I/O with RAM and ROM, using the 74LS138 as an address decoder

External Memory Expansion Example 6



8051 shared control program/data space

For Wednesday

- Review today's lecture notes.
- Review Chapter 4, Section 8.3, and Appendix C.
- Read Sections 14.3 and 14.4.