CpE318 – TEST I Closed-Book section

Identifier (NOT name)

Show all your work in the space provided. Answers with a simple "yes", "no", or a single number are typically incomplete and will not be given full credit. Answers in non-reduced form, like (a+sqrt(b))/c, are fine where appropriate. Good English on essay/short answer questions is required. ON MULTIPLE CHOICE QUESTIONS, IF YOU'RE NOT SURE DON'T GUESS – you will get points off for wrong answers.

1. (10 Points) Given the following declarations, answer questions a through e below.

```
type blah is array (natural range 0 to 7) of positive;
type blab is range 42 downto 0;
variable x: blah := (3, 1, 4, 1, 5, 9, 2);
```

- a. (2 Points) What is blah'range (specify the value as well as the type)?
- b. (2 Points) What is x(3) (specify value as well as type)?
- c. (2 Points) What is blab'pos(3) (specify value as well as type)?
- d. (2 Points) What is blab'high (specify value as well as type)?
- e. (2 Points) What is blab'rightof(27) (specify value as well as type)?
- 2. (10 Points) For the following code, draw a timing diagram for X. Please label the diagram with the time(s) where changes take place.

```
architecture blah of blab is
      signal x:integer:=0;
begin
      pl: process is
            signal z:integer:=0;
      begin
                                          time —
            wait for 5 ns;
            x <= 42;
            wait for 5 ns;
            for y in 0 to 3 loop
                  z := z + y;
                  x <= z;
            end loop;
            wait for 5 ns;
            wait;
      end process p1;
```

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3. (10 Points) Describe the difference between a signal and a variable

4. (10 Points) Given the following type declarations, choose which of the following may be <u>valid</u> assignments within a process. (There are between 0 and 9 correct answers. Note that some answers show <u>two</u> steps).

```
type blah is range 0 to 3;
type blab is range 0 to 5;
type blob is (what, am, I, doing, here, '?');
subtype blub is blob range what to I;
variable w: blah;
variable x: blab;
variable y: blob;
variable z: blub;

a. x = 1; w = x; b. x = w; c. y = z; d. z = y; e. x = y;
f. y = "blah"; g. y = am; h. w = 4; i. x=3; x = x+3;
```

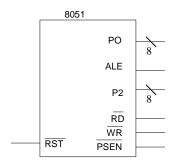
5. (10 Points) There are several reasons for adding assert statements to your VHDL code. Name the <u>most important</u> reason.

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1. (11 Points) The picture below shows an 8051 microcontroller. P0 can be either an input or an output (and hence may share the line with other drivers), ALE is an output, P2 is either an input or output, RD, WR, and PSEN are outputs, and RST is an input. P0 and P2 are 8 bits each. You may assume that any individual line/pin takes on a value of only 0 or 1. Write an entity declaration for the 8051.



2. (16 Points) Shown below is a signal assignment statement for a signal x, and a process which looks at values of x. Draw a timing diagram for signal x and variables a, b, c, d, e.

3. (23 Points) Write an entity/architecture pair for a simple, 4-bit ALU. The inputs to this ALU are a) a command line, which can take on values ADD, SUB, INC or DEC, and b) two 4-bit inputs A and B. The output is a 4-bit output C. When the command ADD is given, the output C = A + B. When the command SUB is given, C = A - B. When the command INC is given, C = B+1, and when the command DEC is given, C = B-1. Add assert statements to your code to make sure A, B, and C are within appropriate bounds. A result is calculated <u>any</u> time a command is put on the command line. Two points to make your life easier: a) If you need a special type definition for an entity port, just put it right above your entity declaration, b) A, B, and C can be of integer types.

