Instru	ction	j	k
ADDD	R5	R4	R2
SUBD	R3	R1	R2
MULTD	R3	R3	R 5

finishing times					
IS	RPO	EXE	WR		
1	1				

RS	RS Tag	Busy	Ор	Vj	Vk	Q	Qk
Add1	1	~	add	1000	\$ 0	0	٥
Add2	2						
Mult1	3						
Mult2	4						

Integer Reg#	Q	٧
1		
2		
3		
4		
5	1	
6		
7		

Figure 2: Clock cycle

Instru	ction	j	k
ADDD	R5	R4	R2
SUBD	R3	R1	R2
MULTD	R3	R3	R5

	finishing	2_====	
IS	RP0	EXE	WR
A	1		
1	1		
$\hat{}$	2		
<u>م</u>	•		

RS	RS Tag	Busy	Ор	Vj	Vk	Qj	Qk
Add1	1	~	odd	1000	8	٥	O
Add2	2	Y	<u> </u>	100	0	0	0
Mult1	3						
Mult2	4						

Integer Reg#	G	٧
1		
2		
3	a	
4		
5	1	
6		
7		

Figure 3: Clock cycle

Instruction		j	k
ADDD	R5	R4	R2
SUBD	R3	R1	R2
MULTD	R3	R3	R5

tinishing ames						
IS	RPO	EXE	WR			
1	1	3				
2	a					
3						

RS	RS Tag	Busy	Ор	Vj	Vk	Ö	Qk
Add1	1	7	odd	7020	0	0	0
Add2	2	Y	Sub	601	0	0	0
Mult1	3	~	mul			a	1
Mult2	4						

Integer Reg#	O	٧
1		
2		
3	3	
4		
5	1	-
6		
7		

Figure 4: Clock cycle . 3...

Instru	ction	j	k
ADDD	R5	R4	R2
SUBD	R3	R1.	R2
MULTD	R3	R3	R5

finishing times						
IS	RPO	EXE	WR			
1	ł	3	4			
2	2	4				
3						

RS	RS Tag	Busy	Ор	Vj	Vk	õ	Qk
Add1	1	7					
Add2	2	4	Sub	100	0	0	0
Mult1	3	4	mat		1000	a	0
Mult2	4						

Integer Reg#	O	٧
1		
2		
3	M	
4		
5	0	1000
6		
7		

Figure 5: Clock cycle

Instru	ict ion		}	k	
ADDD	R5	F	R	.2	
SUBD	R3	F	u	R	.2
MULTD	R3	R3		R3 R5	
L., ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,					
RS	RS	Busy	Ор	Vj	VA

finishing times					
IS	RPO	EXE	WR		
(ļ	3	4		
2	2	4	5		
3	5				

RS	RS Tag	Busy	Οp	Vj	Vk	Q	Qk
Add1	1	7					
Add2	2	2					
Mult1	3	Y	mut	loo	1000	٥	ð
Mult2	4						

Integer Reg#	Q	٧
1		
2		
3	3	_
4		
5		
6		
7		

Figure 6: Clock cycle . . 5..

finichina	timac

Instru	ction	j	k
ADDD	R5	R4	R2
SUBD	R3	R1	R2
MULTD	R3	R3	R5

mustaring unites					
IS	RPO	EXE	WR		
1	1	3	4		
2	Q	4	5		
3	5	15	16		

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	7					
Add2	2	7					
Mult1	3	11					
Mult2	4						

Integer Reg#	G	V
1		-
2		
3	0	10000
4		
5	·	
6		
7		

Figure 7: Clock cycle . . 1.6