CpE111 HW#5 Solutions

1
```
entity Gate-X is
  port( U, V : in bit; F : out bit);
end Gate-X;
architecture logic of Gate-X is
begin
   F <= U xor V;
end logic;
```

2.
```
g <= (a and b) or (not c and d);
```

3.
```
entity Function is
  port (a,b: in bit_vector(3 downto 0);
        G: out bit);
end Function;
architecture logic of Function is
begin
  g <= (a(3) xor b(3)) or (a(2) and b(2)) or
       (a(1) or b(1)) or (a(0) xor b(0));
end logic;
```

4.

```
entity Table is
  port( A,B,C : in bit; G : out bit);
end Table;
architecture logic of Table is
begin
  G <= '1' when (A='0' and B='1' and C='0') else
       '1' when (A='1' and B='1' and C='0') else
       '1' when (A='0' and B='0' and C='1') else
       '1' when (A='1' and B='0' and C='1') else
       '0';
end Logic;
```

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