CpE213 Sample Problems for Final Exam

The logic diagram in Figure 1 shows how you might use a 74HC373 octal latch (U2) and a 16k byte EPROM (U3) to expand an 8051 (U1) with a 16k external code memory space.

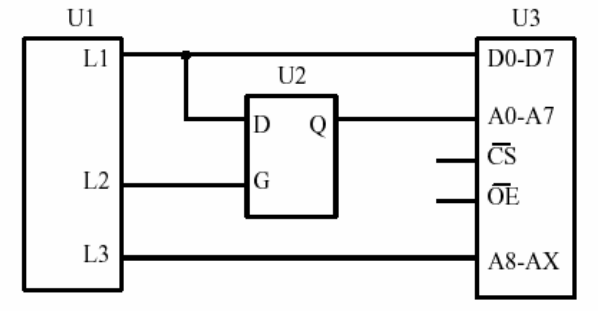

Figure 1

Answer questions 1 through 6 regarding the diagram.

1. Label AX is: a) A11 b) A12 c) A13
   d) A14 e) A15

2. Label L1 is: a) P0 b) P1 c) P2
   d) P3 e) any of the previous

3. Label L2 is: a) RD b) WR c) PSEN
   d) ALE e) any of the previous

4. Label L3 is: a) P0 b) P1 c)P2
   d) P3 e) any of the previous

   If a port is selected, bits ____ to ____ (for practice only, will be stated as a multiple choice question if appearing on the exam.)

5. OE should be connected to: a) RD b) WR
   c) PSEN d) ALE e) nothing

6. In order to recognize addresses in the range 0000H through 3FFFH, CS should be connected to a two-input gate of the type below:

   a) nand b) nor c) and
   d) or e) xor

   Fill in as practice:
   with inputs connected to P__.7 and P___.6

In the configuration of Figure 1, in order to use U3 for both external code and data, U3 can be replaced with a 16k static RAM with an additional write enable line (W). Assuming this replacement has been made, circle the most appropriate option for questions 7 though 9.

7. W should be connected which line of the 8051?
   a) RD b)WR c)RxD
   d) TxD e) any of the previous

8. This line is part of port:
   a) P0 b)P1 c) P2
   d) P3 e) not part of a port

9. OE will in turn need to be connected to a two-input gate of type:
   a) nand b) nor c) and d) or e) xor

   NOTE: QUESTIONS 1 to 9 ARE VERY COMPREHENSIVE QUESTIONS; THE MOST COMPLICATED ONES THAT I COULD COME UP WITH. A SIMILAR QUESTION ON THE EXAM WILL BE SIMPLER AND WILL HAVE FEWER PARTS.

10. The CJNE is a 3-byte, 2-cycle instruction, while the DJNZ is a 2-byte, 2-cycle instruction. Which version of the **for** loop below will be more efficient? Why?

```
i. for (i=0;i<20;i++);
ii. for (i=20; i>0; i--);
```

   a) Version i, as the resulting code utilizes DJNZ.
   b) Version ii, as the resulting code utilizes DJNZ.
   c) Version i, as the resulting code utilizes CJNE.
   d) Version ii, as the resulting code utilizes CJNE.
   e) They are equally efficient.

11. An SJMP instruction located at 0115H in code space is coded as

```
0115  80FE      SJMP LOOP
```

   The target address 'LOOP' is located at:

   a) 113H b) 115H c) 117H d) 213H e) 215H

12. The 8051 UART is similar to a:

a) timer b) shift register c) parallel port
d) counter e) power source

13. Which of the below is NOT a source of interrupts on the generic 8051:

a) INT0' b) INT1' c) WR' d) TF0 e) TF1

14. How many bits of the IE SFR must be set to enable one of the 8051's interrupts?

a) 0 b) 1 c) 2 d) 3 e) 4

15. How many levels of interrupt priority does the generic 8051 have?

a) 0 b) 1 c) 2 d) 3 e) 4

16. Assume that the following interrupts arrive simultaneously (far-fetched assumption):
serial (priority 0), T0 (priority 1), EX1 (priority 1), T1(priority 0)

Which interrupt will be serviced first? Note that we are defining "serviced" as the time when the first instruction corresponding to the interrupt service routine of an interrupt is executed.

NOTE: THIS DOCUMENT IS FOR PRACTICE ONLY. IT DOES NOT REFLECT THE ACTUAL DISTRIBUTION OF QUESTIONS PER TOPIC ON THE FINAL EXAM.