## **EE 2372 Test 2**

9 problems, 100 points.

November 24, 1998

## SOLUTIONS

## NAME

Closed book, closed notes, no calculators. Scratch paper will be provided, so do not use any of your own.

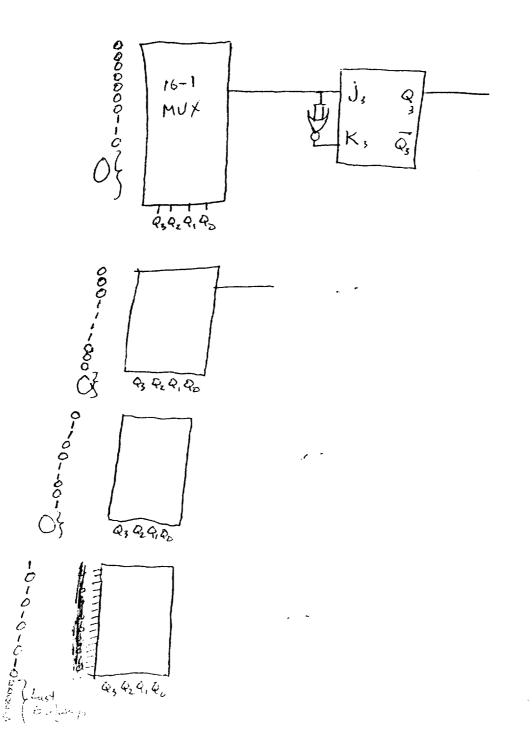
You are permitted pens or pencils, erasers, and a (non-calculator) watch. All other items are to be placed underneath your desk.

Please read the entire exam before beginning, and note point values. Some problems are more worthwhile than others.

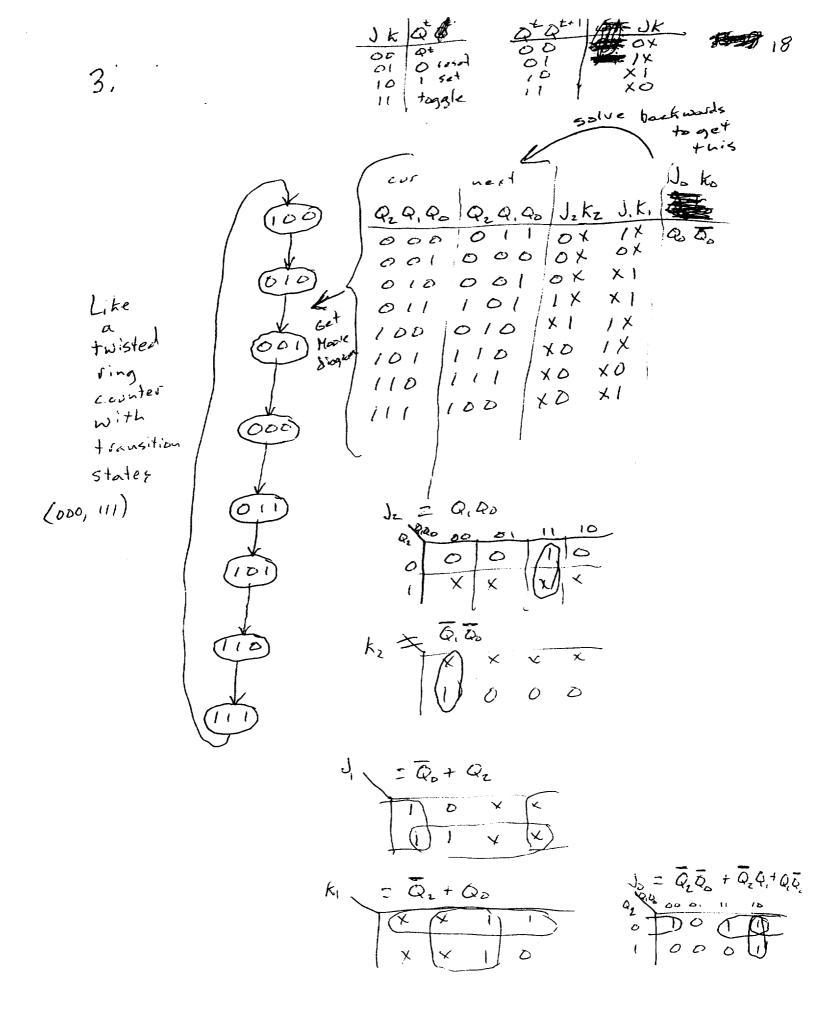
Do not turn this page until instructed to do so.

Good luck!

1. Design a synchronous decade (0-9) counter using four JK flip-flops, four NOR gates, and four 16-1 multiplexers. Any erroneous (glitch) state must be reset to zero on the next clock cycle. The states are QzQzQ, Qo. (MSB)

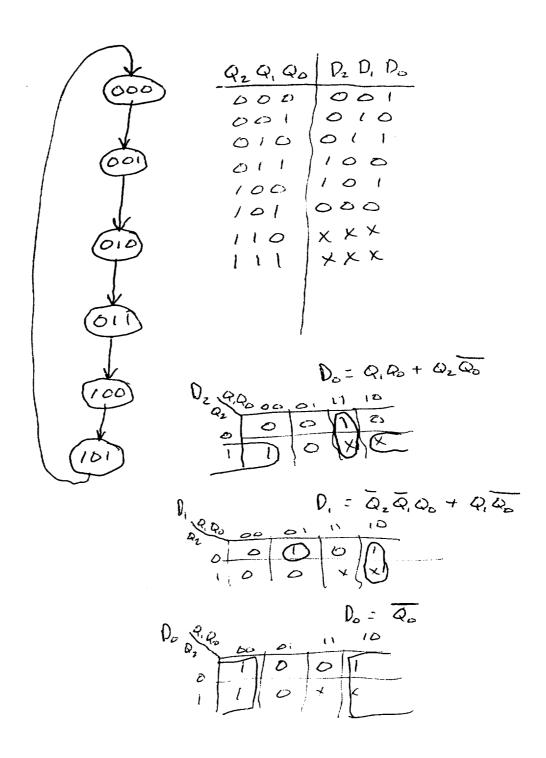


2. No, we can't make any gate we want, Using only XOR and inverters. If me could me could make an AND gote. ould look like this: Etase We dan see this is in possible by our dering A AND A We have these possibilities ABB = AB+ AB - ABB = AB+ AB  $\overline{A} \oplus \overline{B} = \overline{A} B + A \overline{B}$  $\overline{A \oplus B} = AB + \overline{AB}$ These all reduce to \$\overline{\to } \or \overline{\to } and we're stuck in a closed set of possibilities.



4. Design a 3-bit synchronous Medulo-6 counter, using Dflip flops: Oz D, Do. (It counts 0-5 and starts over.)

Use a Moore diagram



**3**2,4,6,8 even/

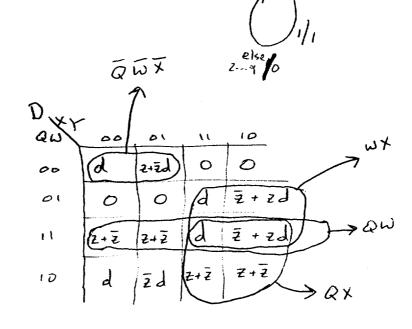
0/0

**A** 

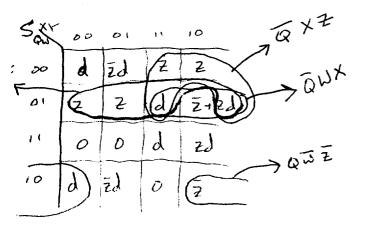


? WXYZ	FD S	0(z)	5(z)
2000	XX	d	·×
0001	× × × × × × 000	2+Ed	五
0011	1000	0	2
010	00	0	2
1000	0 0	0	E
1010	0 0	0	2
100	XX	弘	1 + 2d
1110	× × × ×	K	d
10000	XX	d	d
0010	XX	Ed	五人
0100	10	2002	Z
0110	10	2+2	0
1000	10	Z+ Z	0
1010	10	2+2	0
1100	10	シナノ	20
1101	× × × ×	d	1
in t		1 -,	1
;			
{			

5	•



0/0



D= QWX + WX+ QW+ QX S= QXZ + QWX + QWZ + QWZ

Minimal SOP, solved separately

D= QWX + QWX +QW + QX

Minimal gate count, by using term from 5 twice, re le-coing it in D.

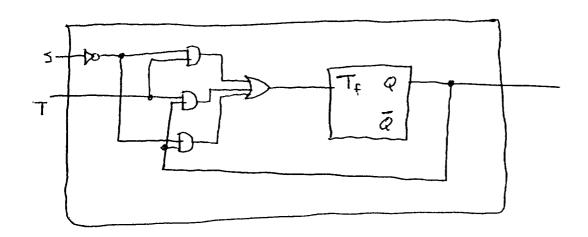
6. Make a Store-Toggle Flip flop with the following excitation table

ST	Qt+1	~
00	- T	To Jeset
00	विं वं	Toggle
11	0	leset

Q'ST	1 Qtri	<u></u>
000	0	0
001	1	1
010	0	0
011	<b>O</b> ,	0
100	0	1
•	0	1
101	( ,	0
110		4
( ( )	10	1

下57	00	0(	11	10	
3	0		0	8	
ı	(1	10	1	0	
1				ł	
76		5T +	Qt	<del>5</del> +	Q.

ANTE THE CAN BE CENTER OF



7. 2 bit of ideas and a Juffel X: 1 5 count of down Call CARA QREB AFR X AFRIT SA RA Alexand Carpina 外层 00101 0x 0.0000 1 21 / 13 /10 112 2 10 11,0000 AT SAI ME BOOK FRE FERT OF FREX OF THE STEEN 100 x 011 Reserved to the second Fr F

8. Design a 4-bit ring counter with initialize and error correction. The only inputs are the clock, and I, the initialize signal. The system outputs are:

1000

If the system enters any invalid state, it must return to 1000 on the next next clock eyele. The signal to do this is called E. Use D flip flops: D3 D2 D, D0.

Use D flip flops: D3 D2 D, D0.

Just write the equations for each D input - you don't need to draw them. Also write the equation for E.

E= You don't have an odd # of 1's + You have 3 1's

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E = \overline{Q_4 \oplus Q_3 \oplus Q_2 \oplus Q_1} + Q_3 Q_2 Q_1 + Q_4 Q_2 Q_1 + Q_4 Q_3 Q_1 + Q_4 Q_2 Q_1 + Q_4 Q_2 Q_1 + Q_4 Q_3 Q_1 + Q_4 Q_3 Q_1 + Q_4 Q_2 Q_1
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E = Q3 Q2 Q1 Q0 + Q3 Q2

9. F= ABZD + B+C

