EE213 Quiz 1 2/9/01
Closed Book, open crib sheet. Avg: 60
100pts 50 min

Score: 77

Name: Jesse Lan

Do not write on this sheet. Put all your answers on a separate sheet. You may put more than one answer on a page but use only one side of the page and do not mix up the answers. Put this sheet on top of your answers as a cover sheet. Do not staple or fold over the corner.

4 1. (5) Name and briefly describe the states, which make up a Gnome instruction cycle.

2. (10) Assume that the Gnome PC contains a 25 and that location 25 contains a 01000010 (binary code for a LDA 2 instruction) and that the previous instruction has just completed execution. The next instruction cycle will result in loading the Accumulator with the contents of register 2. Describe in as much detail as you can, the sequence of events (register transfers) during the instruction cycle which cause this to happen.

8

5 3. (5) If a computer's clock cycle has a period of 1 microsec (1 us), and each instruction takes four clock cycles, how long does it take to execute five instructions?

3 4. (10) Sketch a logic diagram showing how you would connect up a 64k byte ROM to an 8051 in order to implement 64k bytes of external code memory. Be sure to include and describe any additional components you might need.

10 5. (10) Name at least six of the 21 SFR's in the 8051.

5 6. (5) When will a MOV A,R0 instruction not produce the same result as a MOV A,0 instruction?

7. We can detect whether a single pole single throw (SPST) switch is open or closed by connecting it between an 8051 port bit and ground. No external memory or I/O is used.

7 a) (5) Would it be better, worse, or about the same to use P0.1 (port 0 bit 1) or P1.1 for this purpose?
(5) b) Why?
(5) c) What would be wrong with connecting the switch between P1.2 and Vcc? (vcc is the power supply)

10 8. (10) Sketch a timing diagram of the 8051 clock, PSEN, and ALE signals. Assume no external data accesses.

10 9. (5) a) What is the difference between a MOV A,0 and a MOV C,0 instruction?
(5) b) What is the difference between a MOV R1,0 and a MOV R1,#0 instruction?

0/5 10. (5) a) Why can't the instruction MOV @R0,#0 be used to clear location 100H?
(5) b) What is the location of the first instruction fetched by the 8051 after reset?

5 11. (5) What 8051 signals are used to select external data RAM?

5 12. (5) If the 8051 uses a 12 Mhz clock, how long is the active low pulse that is generated when the 8051 executes the three instructions setb p1.0, clr p1.0, setb p1.0? (these are all single cycle instructions)

Jesse Lee
CPE 213-Exam 1
2/9/01

1. Gnome Instruction cycle

Fetch - obtains an operation or data from memory

Decode - decides what to do with the current instruction (where to send it) + fetch data

Execute - The command in the IR is executed

2. Datapath = ~~IR~~, PC, ACC, ALU

Not yet. Only after Fetch cycle -2

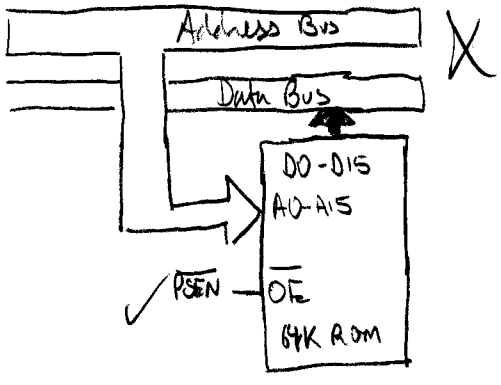
The IR will contain the LDA 2 instruction (01000010). Next, the IR puts this code on the abus. Next, rd_data is set to a 1 to allow the addr be set to 0010. This address is sent to the memory, and the memory responds by outputting the data stored there onto the data bus. Next, this data is sent to the ALU which does nothing and then it is sent to the accumulator. Now memory location 2 has been loaded into the ACC. ✓

3. T = 1 us for clock cycle
each instr 4 clock cycles
time for 5 instr

t = 5(4)(1 us) = 20 us

Time = 20 us

4.



5. SFR: Ports 0-3
Data Pointer DPH DPL
Stack Pointer
Accumulator
B Register
Program Status Word

6. If the Active Register bank is not Bank 0, then MOV A,R0 will not give the same result as MOV A,0.

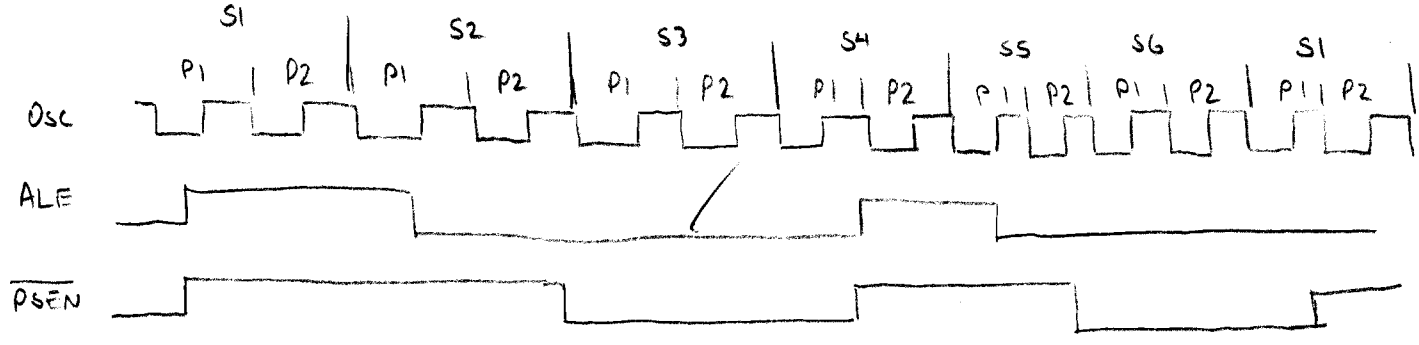
7. 0 a) If only data is being read, either port would suffice. X

2 b) Although P0 does not have a pullup resistor, the port is being driven externally. Therefore & input, they act similar

5 c) if the output is zero this could burn up the FET destroying the port.

How is it 'driven' if the switch is open?

8.



9. a) MOV A,0 moves byte address 00H into the accumulator.
MOV C,0 moves bit address 00H into the carry bit.

b) MOV R1,0 moves the data at memory location 0 into register 1.
MOV R1,#0 moves the hex number 0 into register 1.

10. a) This location is being indirectly accessed and is different from the actual location 100H. X

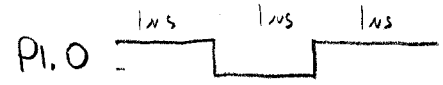
b) The PC is reset to zero after a system reset, therefore the first instruction fetched is from location 0 in memory.

3/3

11. The signals used to select external data RAM are:

ALE, $\overline{RD}$, $\overline{WR}$, ~~$\overline{EA}$~~

12. Uses 12MHz clock, each instr cycle is 1μs



~~1μs~~