CpE 213
Digital Systems Design
8051 Memory Map

Lecture 12

Monday 9/19/2005

UNIVERSITY OF MISSOURI-ROLLA
The Name. The Degree. The Difference.

8051 Memory Map

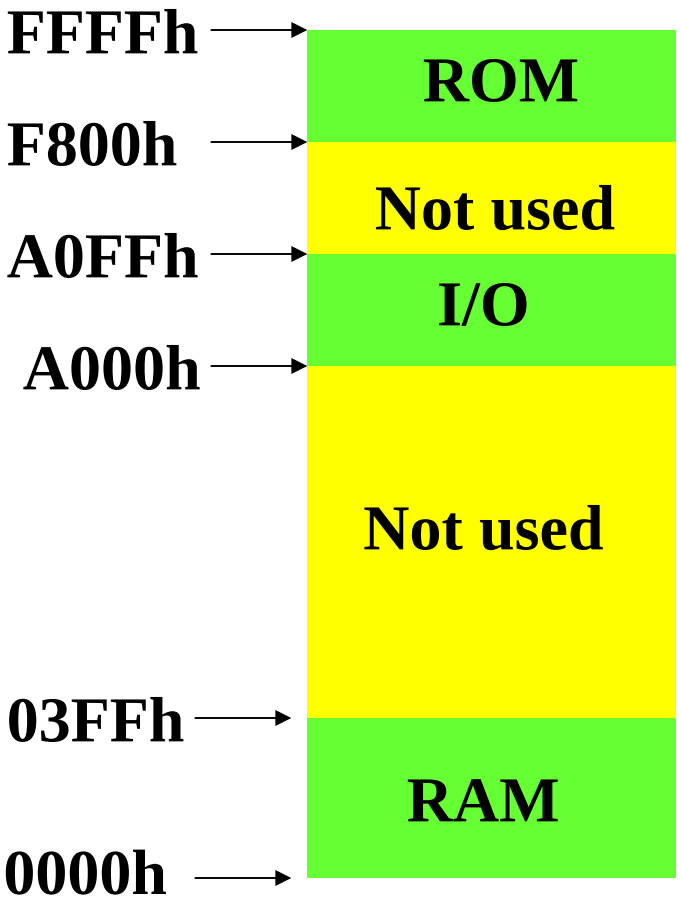
Overview

- 8051 memory map
  - Sections 2.1 and 2.4 of textbook
- 8051 flags and the program status word
  - Section 2.6
- 8051 register banks and stack
  - Section 2.7

Definitions

- When the CPU performs a READ or WRITE operation, it must first place an address on the address bus to select one and only one memory location or I/O device.
- Most 8-bit CPUs have a 16-bit address bus that can specify any of 64K = 65,536 different addresses.
- In hex, these addresses range from 0000H to FFFFH.
- The range of addresses that are available in a μC is called the .
- A diagram showing how the address space is allocated among RAM, ROM, and I/O is called the .

Memory map for a typical microcomputer



- We often refer to address 0000h as the of the address space, and as the top of the address space.

8051 memory organization

- In contrast to microprocessors such as the 8086, the 8051's memory is divided into four distinct areas:-
  - 256 × 8 RAM, memory.
  - 64K × 8 RAM, memory.
  - 4K × 8 ROM, memory.
  - 64K × 8 ROM, memory.
- The internal data memory is further divided into

- A given numeric address can refer to two logically and physically different memory locations, depending on the using the address.

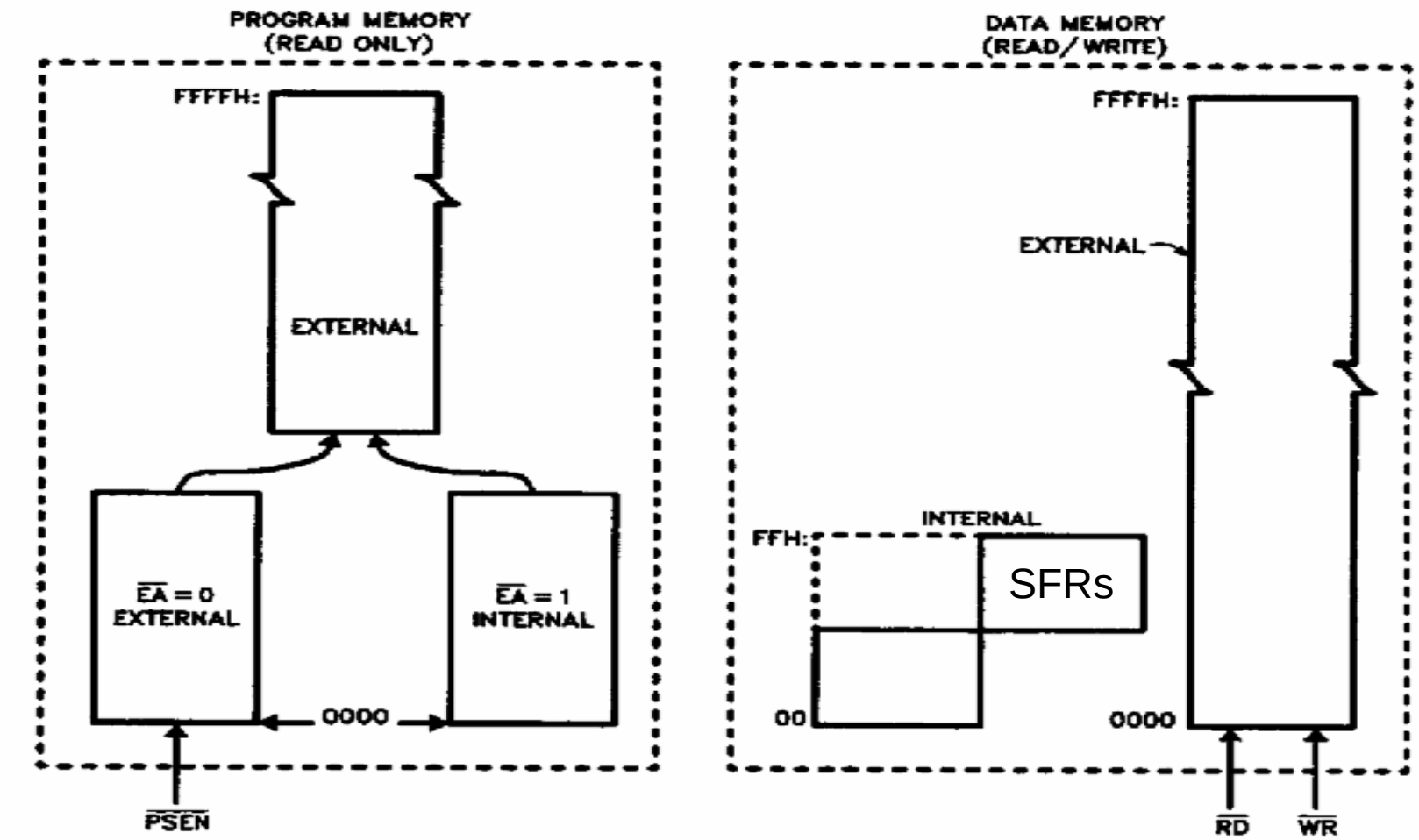
8051 memory organization

- As the 8051 has separate memory blocks, for and , and both blocks have the same address space.
  - This is called a architecture.
- Separating the program memory from the data memory:
  - improves , as we cannot inadvertently overwrite the program code
  - and allows us to use , or read only memory.

Code and data memory

- Code Memory
  - The 8051 accesses code memory when it executes an assembly language program or subroutine.
  - Code memory is read-only; you can't write to it.
  - The only instructions that access code memory are operations.
  - Code memory is intended for programs or subroutines that have been previously programmed into ROM or EPROM.
- Data memory
  - The data memory is the memory in which you can store and read data during the program execution.
  - It has to be RAM.

8051 memory organization



SFRs = Special Function Registers

8051 memory organization

- Program code memory:
  - When the 8051 is first reset, the program counter starts at . The physical location of address 0000h is either , depending on the 8051 pin
    -
    -
  - The CPU reads external code memory using the which is usually connected to pin on ROM.

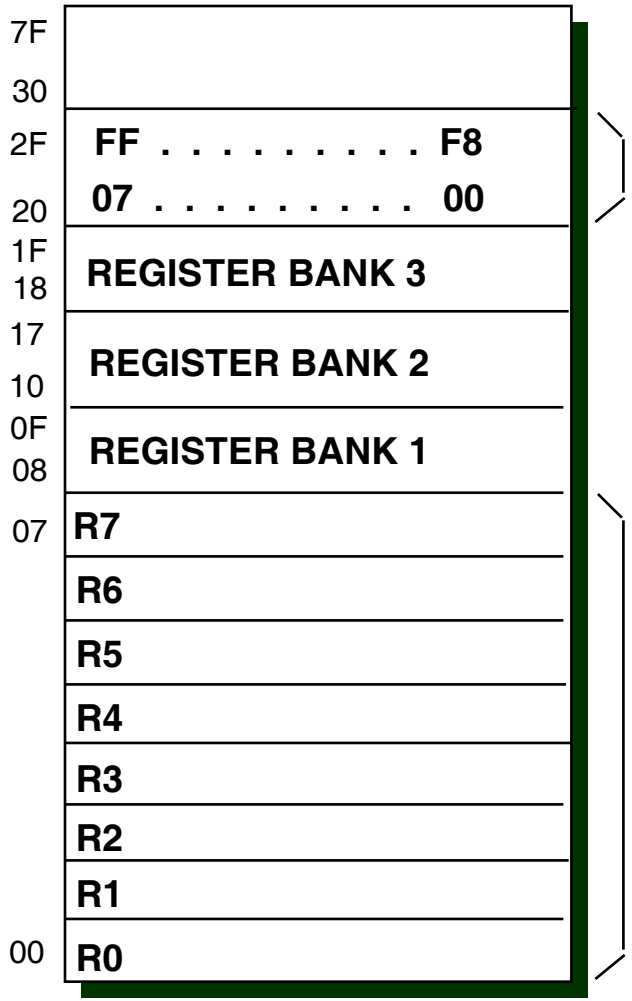
8051 memory organization

- External Data Memory:
  - If the application requires large amounts of data memory, then external data memory (RAM) can be used.
  - I/O to external RAM can only be made by using one of the instructions.
  - When executing a instruction, the 8051 issues the read signal using the pin (usually connected to on RAM) or the write signal using the pin (usually connected to on RAM).

Internal data memory

- 128 bytes of RAM
- addressable range: hexadecimal.
- addressable range: hexadecimal.
- bit-addressable space: hexadecimal.
- Four register banks: hexadecimal.
  - Direct addressing: the memory cell is referred to directly by its address.
  - Indirect addressing: referring to a register that, in turn, contains the address of the memory cell.
  - Addressing techniques will be discussed in a separate lecture.

Internal data memory



Register Banks

- The first 32 bytes of internal data storage are grouped into four banks of 8 bytes each, numbered from 0 to 3.
- Only one bank at a time can be in active use, and it is selected by means of 2 bits in the register, which can be programmed.
- The eight registers in the active bank are designated R0 through R7 and can be manipulated using software instructions.
- Bank is selected upon reset.
- Inactive register banks can be used as .

Instructions using registers

- Can use 1-byte or 2-byte instructions
  - MOV A, R5
  - MOV A, 05H
  - _____ version is shorter
  - Frequently accessed data should be stored in registers

Instruction	Bank 0	Bank 1	Bank 2
MOV A,	MOV A,	MOV A,	MOV A,

Bit-addressable and general-purpose RAM

- Bit-addressable RAM:
  - 16 bytes bit-addressable bytes in address range to ; total of 128 addressable bits.
  - The bits have individual addresses ranging from to , allowing a bit to be addressed directly.
- General-purpose RAM:
  - Ranges from to ;
  - is byte-addressable.

Special function registers

- Special Function Registers (SFRs) are memory locations that are used for special tasks. They should not be used for general purpose tasks.
- There are SFRs in the 8051, each is bits wide.
- SFRs occupy 128 bytes of address space, directly byte-addressable as .
  - Note that some addresses are empty!
- The SFR space contains:
  - Special purpose CPU registers.
  - I/O control registers.
  - I/O ports.
- 16 bytes are bit-addressable:
  - Set, Clear, AND, OR, MOV (addresses ending in 0 or 8).
- sets bit 0 of ACC.
- E0 is both byte address of whole ACC and bit address of LSB.
- Question: How to set MSB of B, leave others intact?

Special function register map

Bit addressable

F8								
F0	B							
E8								
E0	ACC							
D8								
D0	PSW							
C8								
C0								
B8	IP							
B0	P3							
A8	IE							
A0	P2							
98	SCON	SBUF						
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1		
80	P0	SP	DPH	DPL				PCON

Special function registers

- CPU registers:
  -
  -
  -
  -
  -
- Interrupt control:
  -
  -
- I/O Ports:
  -
  -
  -
  -

Special function registers

- Timers:
  -
  -
  -
  -
  -
  -
- Serial I/O:
  -
  -
- Other:
  -

Some commonly used SFRs

- Accumulator (ACC)
  - The accumulator is the primary SFR.
  - 8-bit register, usually referred to as A.
  - It is the source or destination address for most instructions.
  - Arithmetic, Boolean, and branching instructions use the accumulator.
- B register
  - This 8-bit register is used for operations.
  - For all other operations, the B register serves as a register.

Some commonly used SFRs

- Stack Pointer (SP) (8-bit register)
  - The 8051 uses for its stack.
  - The stack location is not fixed and user may assign any convenient value to SP (limited to addresses accessible through indirect addressing).
  - The SP defaults to on power up which causes the stack to commence at location .
  - The stack in the 8051 grows through memory.
  - The SP always points to the last location on the stack.
  - PUSH instruction increments the pointer and POP instruction decrements it.

Some commonly used SFRs

- Data Pointer (DPTR):
  - The DPTR is a 16-bit quantity held in two 8-bit parts:
    -
    -
  - The main purpose of the DPTR is to hold a 16-bit address for certain instructions.
  - It can be used as a single 16-bit register or as two 8-bit registers.
- Program Status Word (PSW):
  - The PSW is the most important of the SFRs. It is a one-byte register that holds 8 bits that can be addressed individually. Each bit is referred to as a flag.
  - Flags can be either set (1) or cleared (0). This is more efficient than using an entire byte memory location for a binary variable.

PSW: Program Status Word

CY	AC	F0	RS1	RS0	OV	---	P

CY : Carry Flag, set if addition causes carry or subtraction causes borrow

AC: Auxiliary Carry Flag, set if addition causes a carry to the high nibble or subtraction caused a borrow from the high nibble (BCD).

F0 : General purpose flag for user

RS1: Register bank Select 1

RS0: Register bank Select 0

OV: Arithmetic Overflow Flag, set when an operation causes a transition from 7Fh to a higher value, or from 80h to a lower value.

P : Accumulator Parity Flag, set/cleared for odd/even number of 1's in accumulator.

RS1	RS0	Register Bank	Address
0	0	0	00h - 07h
0	1	1	08h - 0Fh
1	0	2	10h - 17h
1	1	3	18h - 1Fh

Group Exercise

- PSW = 0000 0000 originally.
- What is PSW after executing:

Port Registers

- Port 0 at address 80H
- Port 1 at address 90H
- Port 2 at address A0H
- Port 3 at address B0H
- Ports 0,2,3 are not always available for I/O
- P1.2 through P1.7 are always available for I/O
- All ports are bit-addressable

For Wednesday

- Begin assignment 4.
- Review today's lecture notes and Sections 2.1, 2.4, 2.6, and 2.7 of your textbook.
- Read sections 2.2, 2.3 and 2.5.