CmpE213 – Digital Systems Design

Homework 3

The 8051 - internal and external memory

1. CLRC is a 1 byte instruction for the 8051 (an instruction using 1-byte of code-space) which requires 12 clock cycles. CLR 92 is a 2 byte instruction which also requires 12 clock cycles. Explain how these instructions can both be executed in 12 clock cycles while the number of bytes used to store each instruction is different.

2. Normally external code and data are stored on separate chips... code in ROM and data in RAM. However, this doesn't have to be the case. Adding simple logic gates (AND, OR, NOT, etc), show a circuit diagram with the 8051, an external RAM chip (the 6164 8k x 8 RAM), and an address latch, which reads both code and data from external RAM. Hint: the trick is in the control signals.

3. Suppose the 8051 performs the following instruction sequence:

Instruction	Meaning
MOV 2AH, #42H	Move the number #42H into internal mem location 2AH
SETB 54H	Set the bit at bit-mem location 54H
MOV A, 2AH	Move value in internal MEM(2AH) into Accumulator

   What value is in the accumulator (i.e. at memory location 2AH)?

4. Assume PSW = 0x10 before the following instruction sequence is executed

Instruction	Meaning
MOV A, #42H	#42H -> Acc
ADD A, #C0H	Acc + #C0H -> Acc

   What is the value of PSW after execution? (Show your work).

5. An 8051 with bank-switched EPROM is shown on pg 392 of your book. Labeling the EPROM in the upper right-hand corner of the illustration as EPROM 1, in the lower left-hand corner as EPROM 2, lower-middle as EPROM 3, and lower-right as EPROM 4. Note that P1.5, P1.6, and P1.7 are NOT address lines, just regular I/O ports.

   (a) What is the maximum number of memory locations that can be accessed by the 8051 using its 16 address lines (A0-A15)?

   (b) How many memory locations are stored in each EPROM?

   (c) So, how many memory locations do we have, total?

   (d) What? It can't be that many! Find the address space of each device (EPROM1 - EPROM4). Specify whether each is code-space or data-space.

(e) What? How can that be? This arrangement is a very common way of extending the maximum amount of internal memory, called Bank-Switching. EPROM1 constitutes 1 bank, EPROM2 constitutes another bank, etc. How does one choose which bank is accessed?

6. The timing of external signals needed to implement the instruction MOVX A, @DPTR and MOVX @DPTR, A (read and write an external memory location, respectively) are shown on pg 30 of your textbook. The figure below shows the 8051 hooked to external data memory and shows that the DPTR contains a value of 14A0H, the ACC contains a value of 2AH, and shows some locations inside of the external data memory. Show the steps that are taken to perform the instruction MOVX @DPTR,A, showing the values that are on or in each line/bus/register/memory location for each step (like we did in class for the code read instruction).

7. For the following timing diagram, find

   (a) What instructions were executed

   (b) For each instruction, where it was stored in memory

   (c) What data was read/written to memory, giving: a) its address, b) its value, c) whether it was READ or WRITTEN.