CpE318 – Digital Systems Modeling (with VHDL)
Winter Semester, 2001

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Office hours (tentative): Mon, Wed, Fri 1:30–2:30 PM
(Though I'm often available at other times)

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Prerequisites:
CpE111 or CS253

Textbook:
Peter J. Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann Publishers, 1996

Recommended supplements:
- Z. Navabi, *VHDL: Analysis and Modeling of Digital Systems*
- Other manuscripts/notes available electronically at **http://www.umr.edu/~daryl/classes/classes.html** and **http://www.ashenden.com.au/designers-guide/DG.html**.

Material covered (rough estimate):
Introduction to modeling (Chapter 1)
The VHDL modeling language (Chapters 2-5, 7-9)
CPU modeling (Chapters 6, 10)
Digital Systems modeling (Chapters 12-14, 16)
VHDL for synthesis/Rapid prototyping (Appendix A)
Verilog
Misc. advanced topics (TBA)

Grading: *(Tentative)*

20%	Test 1
20%	Test 2
23%	Final Exam
20%	Project
15%	Homework
2%	Evaluation (I can push your grade up or down by 1%)

Tests and Quizzes:

Tests will cover material from the lectures, text, and homework, with a slight emphasis on homework. Tests will generally be 45-60 minutes long and will primarily cover material presented since the last test. I am considering making one exam all or part take-home. The final exam will be comprehensive, though a slight emphasis will be placed on material that might not have been covered on the previous test. I may occasionally give small, in-class, quizzes.

Approximate dates:

Test 1	2/26/01
Test 2	4/09/01
Final Exam	05/15/01 (Tuesday), 4:00–6:00

Homework:

- You are expected to read appropriate sections of the textbook before presentation in class
- Homework problems will be assigned in class
- As a rule of thumb, no late homework is accepted.
- Homework will consist of answering questions from the book, solving problems, writing and simulating models, and, possibly, some laboratory work.
- While you are expected to complete all assigned problems, the grader may randomly pick only certain problems to grade. It is common in larger classes to compute your grade based on the accuracy of 1 or 2 problems and an evaluation of how hard you "tried" on the rest.
- Lowest homework grade is dropped
- Extra credit may occasionally be offered. You will not be penalized for not completing the extra credit, but if you have cause to be concerned about your grade I strongly encourage you to take advantage of this when available.
- Normally, I would strongly encourage you to work with others on homework assignments. However, for this class, we have two excellent GTAs to assist you with any problems. I strongly encourage you to work with them when possible. Working with others is still fine, to a point, but you must turn in original work. Multiple people turning in the same copy of a homework will be considered cheating and will be dealt

with accordingly. Expect especially harsh consequences if you cannot explain the answers in your homework.

- I recommend you complete all category 1 problems at the end of each chapter, whose answers are given in the back of the book.

Project:

You will be required to complete a "significant" digital systems modeling project. I have not decided yet if this project will be done individually or in teams. The project will most likely include modeling a system at both a high and low level and will require an appropriate level of testing to prove the model works. Most likely, testing will take place through a test-bench you design. In my evaluation of the project, I may subject your design to my own test-bench to ensure that testing was done correctly. I will give you specifics of the project near the middle of the semester. Your work will be documented through a formal report.

Approximate due dates:

Complete project specification (me)	2/23/01
Progress report	4/20/01
Formal report	5/02/01

Partial Credit:

Problems are rarely graded as all-or-none. Emphasis is placed first on proper understanding of the concepts, then on proper application of those concepts, and lastly on "the right answer". You will not be severely penalized for minor, non-conceptual errors. On the other hand, a simple answer with no work or explanation may not be given full credit.

If you feel you deserve more credit on a problem than was given, you may submit a written request for additional credit, clearly stating why you deserve additional credit. Such requests may not be made until 24 hours after the exam was handed back and should be in the form of a memo like you would use when communicating between professionals on the job. No requests will be accepted after 30 days.

Attendance:

Attendance to lectures is not required, however, I will not be sympathetic to problems caused by skipping class without a documented excuse. Excessive absence (in particular, failure to attend a quiz or exam without an excuse) may cause you to be dropped from the course.

Cheating:

Don't do it. Department policy is to fail you in the course on the first offense and to expel on the second.

Class Schedule: (tentative)

Lect.	Date	Topic	Read	Due
1	1/17	Semester outline and introduction	Ch 1	
2	1/19	Intro to Modeling	Ch 1	
3	1/22	Intro to Modeling	Ch 1	
4	1/24	Intro to VHDL; Entities and architectures	Ch 5.1, 5.2, 2	
5	1/26	Intro to VHDL	Ch 2	
6	1/29	Data types	Ch 2	
7	1/31	Sequential statements	Ch 3	
8	2/02	Sequential statements	Ch 3	
9	2/05	Composite data types	Ch 4	
10	2/07	Behavioral descriptions	Ch 5.3	
11	2/09	Behavioral descriptions	Ch 5.3	
12	2/12	Transport and inertial delays	Ch 5.3	
13	2/14	Structural descriptions	Ch 5.4	
14	2/16	Test benches		
15	2/19	Design processing	Ch 5.5	
16	2/21	Pipelined multiplier-accumulator	Ch 6.1	
17	2/23	Catch-up and review		Complete project spec.
18	2/26	**Test I**		
19	2/28	Pipelined multiplier-accumulator	Ch 6.2	
20	3/02	Pipelined multiplier-accumulator	Ch 6.3	
21	3/05	Procedures	Ch 7.1, 7.2	
22	3/07	Procedures and functions	Ch 7.3, 7.4	
23	3/09	Overloading and scope	Ch 7.5, 7.6	
24	3/12	Packages	Ch 8, Appendix C	
25	3/14	File I/O	Ch 18.1	
	3/16	Spring Recess		
26	3/19	Text I/O	Ch 18.2	
27	3/21	Resolved signals	Ch 11	
28	3/23	Resolved signals	Ch 11	
	3/26	Spring Break		
	3/28	Spring Break		
	3/30	Spring Break		
29	4/02	Aliases	Ch 9	
30	4/04	Bit-Vector Arithmetic package	Ch 10	
31	4/06	Catch-up and review		
32	4/09	**Test II**		
33	4/11	Bit-Vector Arithmetic package	Ch 10	
34	4/13	Generics	Ch 12	
35	4/16	Components and configuration	Ch 13	
36	4/18	Components and configuration	Ch 13	
37	4/20	Generate statements	Ch 14	Progress Report
38	4/23	Generate statements	Ch 14	
39	4/25	Guards and blocks	Ch 16	
40	4/27	Modeling for synthesis	Appendix A	
41	4/30	Modeling for synthesis	Appendix A	
42	5/02	Verilog	handout	Project
43	5/04	Verilog		
44	5/07	Advanced topic - tba		
45	5/09	Advanced topic - tba		
46	5/11	Catch-up and review; student assessment		
	5/15	**Final Exam** (at 4:00)		