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CpE 111 - Chapter 5 : HWas
5.2, 5.3, 5.6, 5.9, 5.12

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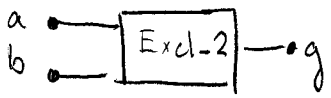
5.2 G: diagram & TT
F VHDL entity & architecture
S:



a	b	g
0	0	0
0	1	1
1	0	1
1	1	0

$a \oplus b$

```
entity  Excl_2 is
   port (a,b: in  bit;
         g: out bit);
end   Excl_2;

architecture Internal_d of Excl_2 is
begin
      g <= a xor b;
end  Internal_d;
```

5.3 G: $g = a \cdot b + c \cdot d$

F: VHDL statement using concurrent operators

S:

```
g <= (a and b) or (c and d);
```

5.6 G: `f <= (a and b) or (c and (w xor z));`

F: simplest boolean equation

S:

$f = a \cdot b + (c \cdot (w \oplus z))$

$w \oplus z = w \cdot \bar{z} + \bar{w} \cdot z$

$c \cdot w \oplus z = cw\bar{z} + c\bar{w}z$

$f = ab + cw\bar{z} + c\bar{w}z$

5.9 G: Diagram
F: VHDL listing that describes circuit
S:
```
entity Logic-circuit is
    port( a,b,c,d,e : in bit;
          Detect : out bit);
architecture Basic of Logic_circuit is
begin
    Detect <= ((a and b) or c ) nand ( d or e);
end Basic;
```

5.12 G: diagram
F: VHDL listing using vector statements

```
entity Logic-box is
   port( a, b : in bit_vector (3 downto 0);
         Out_1, Out-2 : out bit );
end Logic-box ;

architecture Basic of Logic-box is
begin
    Out_1 <= (a(3) xor b(3)) and (a(2) and b(2));
    Out_2 <= (a(1) or b(1)) or (a(0) and b(0));
end Basic;
```