200

Cp Eng 111, Section B
Fall 1999

Final Exam **Name:** Jenn Ku 12/14/99 fantastic!

Show all work on the exam papers. If you need additional space, use the reverse side of the paper. Closed book, closed notes, no calculator.

1. (a) Convert 101.01 from binary to decimal equivalent. (20)

$2^2\ 2^1\ 2^0\ .\ 2^{-1}\ 2^{-2}$

$4 + 1 + \frac{1}{2^2} = 5 + \frac{1}{4} =$ **5.25**

(b) Convert the decimal number 19.75 to binary.

$\frac{19}{2} = 9$	$r_0 = 1$	$.75 \cdot 2 = 1.5$ $r_{-1} = 1$
$\frac{9}{2} = 4$	$r_1 = 1$	$.5 \cdot 2 = 1$ $r_{-2} = 1$
$\frac{4}{2} = 2$	$r_2 = 0$	
$\frac{2}{2} = 1$	$r_3 = 0$	
$\frac{1}{2} = 0$	$r_4 = 1$	

10011.11

(c) Convert 0x 4F to decimal

$64 + 15 =$ **79**

2 | 16 | 4 | 64

(d) What is the 8-bit 1's complement of 10000010 ?

01111101

(e) What is the 8-bit 2's complement of 10100000 ?

01011111

01100000

$$\begin{array}{r} 01011111 \\ +\ 00000001 \\ \hline 01100000 \end{array}$$

01100000

01011111 ✓

01100000 -0

Name: Jesse Li

2. (24) Determine whether each of the following is True (T) or False (F). Circle the appropriate choice.

(a) NOT and AND form a complete logic set. (T) F

(b) AND and OR form a complete logic set. T (F)

(c) $A + \overline{A}\,B = A + B$ (T) F

(e) If a sequential network has a 4-state transition diagram, it will take 4 memory elements to implement its design. T (F)

(e) If a sequential network has a 7-state transition diagram, it will take 3 memory elements to implement its design. (T) F

(f) A 4:1 MUX has 2 select (input) lines. (T) F

3. (14) Given the truth table below,

(a) Complete the truth table, for the function $f(x,y,z) = (x + \overline{y}) \cdot z$

$x+\overline{y}$	$\overline{y}$	x	y	z	f(x,y,z)	g(x,y,z)
1	1	0	0	0	0	0
1	1	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	1	0	0
1	1	1	0	0	0	1
1	1	1	0	1	1	1
1	0	1	1	0	0	0
1	0	1	1	1	1	0

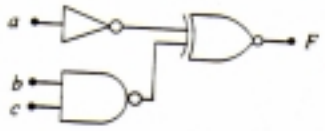
(b) Write g(x,y,z) as a canonical sum of products.

$g(x,y,z) = \overline{x}\,y\,\overline{z} + x\,\overline{y}\,\overline{z} + x\,\overline{y}\,z$

-0

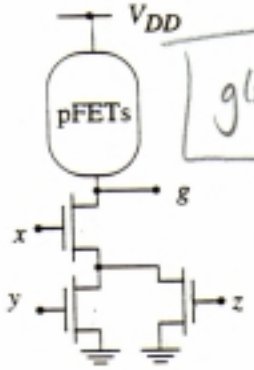
Name: Jesse Lee

4. (15) Construct the VHDL listing that describes the logic circuit shown below:




```
entity problem_4 is
port (a,b,c : in bit;
      F : out bit);
end problem_4;
architecture Logic of problem_4 is
begin
    F <= (b nand c) xnor not(a);
end Logic;
```

5. (15) Given the following CMOS circuit, determine the function g (x, y, z).



$g(x,y,z) = \overline{X \cdot (y+z)}$

nor

p fets in parallel NAND

$\overline{X \cdot y} + z$ $\quad X \cdot (y+z)$

p fet series

nfet parallel

$\overline{y+z} + \bar{x}$

$\overline{y+z \cdot x}$

x	y	z	g	y+z	(y+z)·x
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	1

1
1
1
1
1
1
0
0

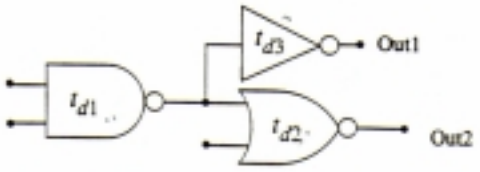
10

Name: Jesse Lin

6. (10) For the circuit below, calculate the propagation delay between the NAND gate and output 2, given the following parameters and assuming that both outputs drive an inverter.

$t_{p0,NOT}$ = 0.5 ns $t_{pL,NOT}$ = 0.4 ns $t_{p0,NAND}$ = 0.85 ns

$t_{pL,NAND}$ = 0.95 ns $t_{p0,NOR}$ = 0.8 ns $t_{pL,NOR}$ = 0.9 ns



tp inverter

$t_{p0,NAND} + t_{pL,NOT} + t_{pL,NOR} + t_{p0,NOR} + t_{pL,NOT}$ =

0.85 + 0.4 0.9 + 0.8 0.4 = 3.35ns

0.85
0.8
1.65
2.15
.4
3.05

1
1.6
1.75
3.35

7. (10) For each of the following, consider an 8-bit register whose initial value is 10001111. Assume this initial state for each operation below; determine the contents of the register after each operation.

(a) SHL 1 00011110 10001111

(b) ROR 2 11100011 10001111

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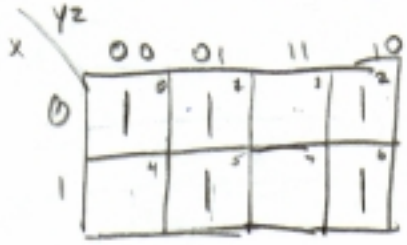
Name: Jesse Lin

8. (22) (a) Generate the Karnaugh map for $f(x,y,z) = \sum m(0, 1, 2, 5, 6)$



000
001
010
101
110

(b) Find the simplest form of the function g(w, x, y, z) which is described by the following K-map:

xy \ zw	11	10	00	01
01	1	1	0	1
11	1	1	0	0
10	1	0	0	0
00	0	1	0	1

$g(w,x,y,z) = yz + xzw + \bar{x}z\bar{w} + \bar{x}\bar{z}w$

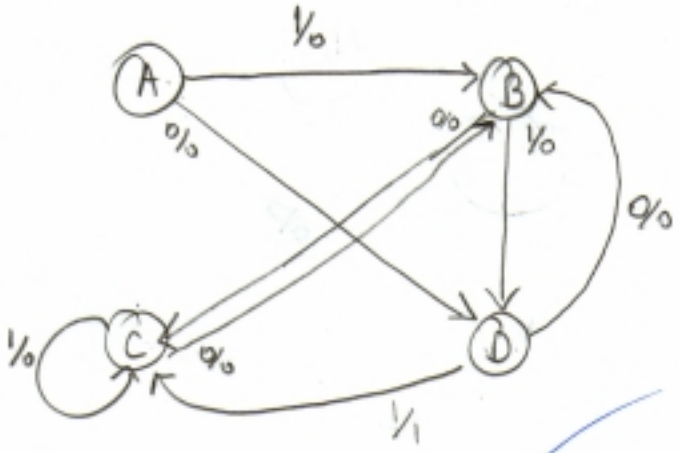
-0

Name: Jean Li

9. (20) Given the following state transition table,

	x = 0	x = 1
A	D/0	B/0
B	C/0	D/0
C	B/0	C/0
D	B/0	C/1

(a) Draw the corresponding state transition diagram



(b) Assuming you start at state A, determine the output sequence for the following input sequence: 00111101

1 2 3 4 5 6 7 8

00010000

at A

1 out 0 at D
2 out 0 at B
3 out 0 at D
4 out 1 at C
5 out 0 at C
6 out 0 at C
7 out 0 at B
8 out 0 at D

0001|0000

-0

Name: Jessa Li

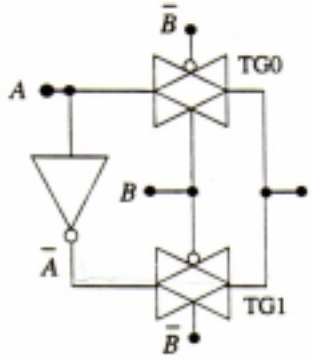
10. (10) Multiple choice (circle the correct answer):

(a) The transmission gate network below implements which of the following functions?

A OR B A OR NOT B A XOR B **A XNOR B**

A	B	
0	0	1
0	1	0
1	0	0
1	1	1

A xnor B



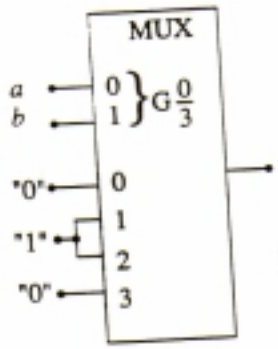
$ab + \bar{a}\bar{b}$

(b) The MUX below implements which of the following functions?

A OR B A OR NOT B **A XOR B** A XNOR B

b	a	
0	0	0
0	1	1
1	0	1
1	1	0

A xor B



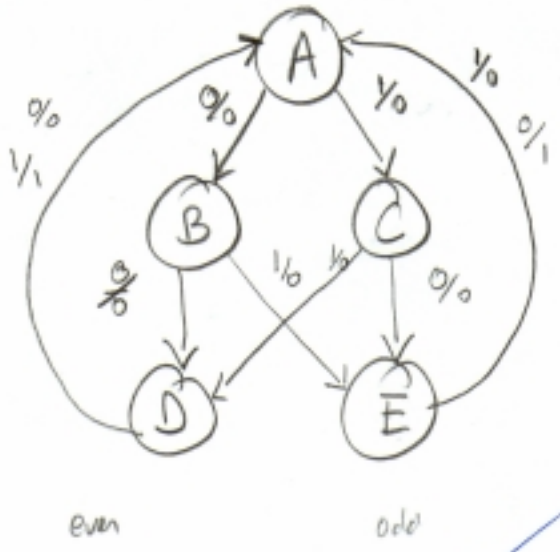
2

-0

Name: Jesse Le

11. (15) Draw the state transition diagram for a 3-bit odd parity network, that is, the output should be 0 unless the third input yields a 3-bit sequence with odd parity; in this case, the output should be 1. In all events, the system should return to its initial state after the third input bit.

3 bit odd parity check
out = 0



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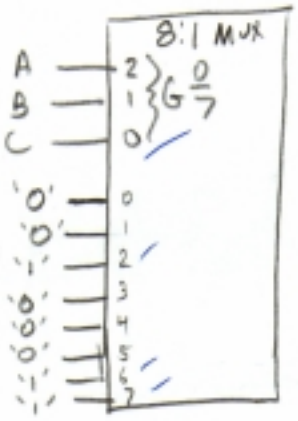
Name: _____

12. (10) Use an 8:1 MUX to implement the function $F(A, B, C) = A \cdot B \cdot C + B \cdot \bar{C}$

A	B	C	$\bar{C}$	$B \cdot \bar{C}$	ABC	F
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	1	0	1	1	0	1
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	1	0	1	1	0	1
1	1	1	0	0	1	1



A	B	C	$A \cdot B \cdot C$	$\bar{C}$	$B\bar{C}$	F
0	0	0	0	1	0	0
0	0	1	0	0	0	0
0	1	0	0	1	1	1
0	1	1	0	0	0	0
1	0	0	0	1	0	0
1	0	1	0	0	0	0
1	1	0	0	1	1	1
1	1	1	1	0	0	1

13. (15) Complete the timing diagram below for a positive edge-triggered D flip-flop, assuming an initial value of 0 for Q.