CpE 213
Digital Systems Design

Lecture 6

Thursday 9/11/2003

Before the next lecture

- Download assignment 2 (due tomorrow).
- Submit assignment to my office.
- Complete assignment 1 (due Tuesday).
- Review sections 1.11 and 2.1 to 2.4.3 of your textbook.
- Read the remainder of chapter 2.

Review: Complement Number (CN) Representation

- in CN, the negative of a number is equal to the so-called “complement” of the number
- there are two popular complements
  - radix complement of an n digit number D is given by $r^n - D$, where r is the radix (or base of the number)
  - diminished radix complement – we are not interested in this one for this course

2’s Complement Notation

- 2’s complement of a binary number, D
  - the complement equals $r^n - D = 2^n - D$
- alternative convenient way of finding 2’s complement
  - write the number in the binary form
  - flip all bits
  - add one
    - drop any carry out of MSB

8-bit Examples

	$17_{10} = 0010001_2$	$0_{10} = 0000000_2$	$1_{10} = 0000001_2$
flip bits	11101110_2	11111111_2	11111110_2
add 1	11101111_2	100000000_2	11111111_2

fact: a negative number will always have a 1 in the MSB

Conversions in 2's Complement

- 10111_2 = ?
  - $1\times(-2^4) + 0\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0$ $= -16+4+2+1 = -9$
- note that if we are not using unsigned numbers, $10111_2 = 1\times2^4 + 0\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0 = 16+4+2+1 = 23$
- given n bits, the range of representable numbers in 2's complement is -2^{n-1} to $(2^{n-1} - 1)$

2's Complement Addition/Subtraction

- add 2's complement numbers just as we would add positive numbers, and ignore the carry out of the "sign bit"
  - sign bit is the MSB

Calculate 3*5 with for loop

Code	Addr	Instr
		MOV A, #0
		MOV R0, A
		MOV A, #3
		MOV R1, A
	Loop:	MOV A, #5
		CLR C
		ADDC A, R0
		MOV R0, A
		MOV A, R1
		CLR C
		ADDC A, #FFh
		MOV R1, A
		JZ Stop
		SJMP Loop
	Stop:	SJMP Stop

Chapter 2
8051 Hardware

Gains and Losses

Microcontroller	Discrete Part
Slow	Fast
Programmable	No memory
More than one function	One specific task

Gains and Losses
NAND example

Microcontroller

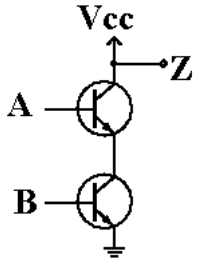
MOV C, P1.4

ANL C, P1.5

CPL C

MOV P1.7, C

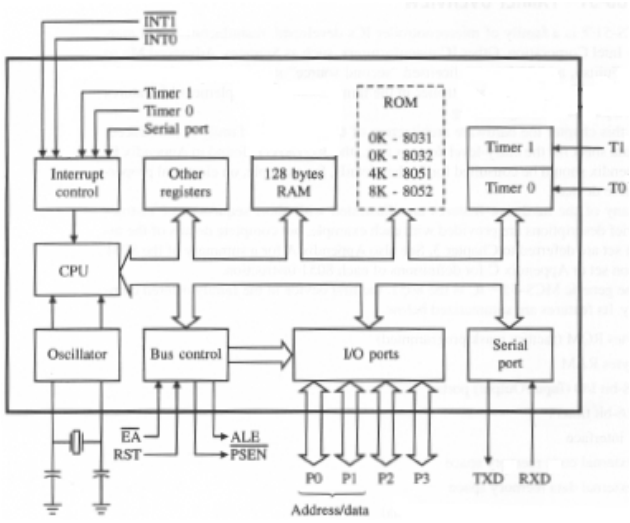
NAND2



8051 Family

- 8051 introduced in 1980 by Intel
- Second sourced by many vendors
- Competition from Motorola (6811) and Microchip (PIC)
- No such thing as '8051'
  - S87C751-1N24: OTP, 0-70°C, 24 pin PDIP
  - P89C51RD2BA: 64k Flash, 1k Ram, PLCC
  - See selection guide or ordering info for details

8051 Block Diagram

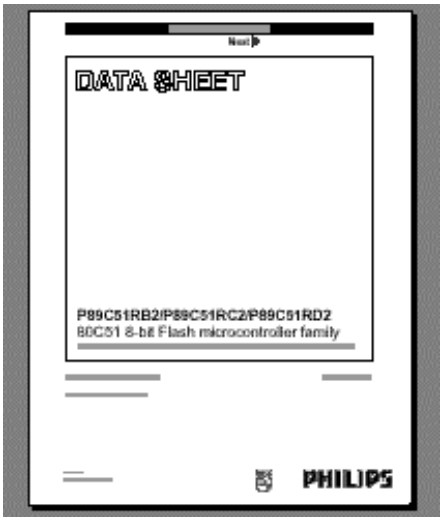


Generic 8051 Features

- 0-64kB internal code ROM, EPROM, Flash
- 64-256 bytes internal data RAM
- Four 8-bit I/O ports: P0, P1, P2, P3
- 1 to 3 16-bit counter/timers
- Bit addressable registers
- Serial interface
- 64k external code and data address space
- 12 MHz clock, 1 μsec cycle time

8051 Data Sheet

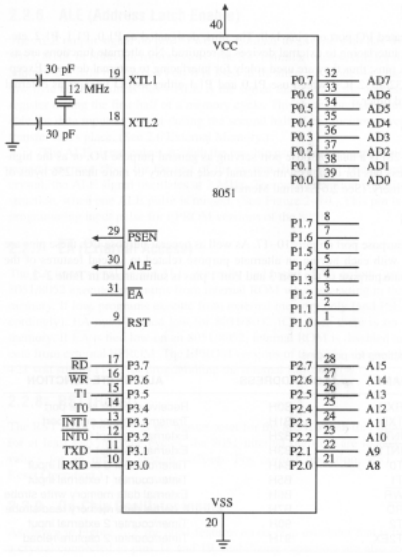
- Main source of microcontroller info
- Available in pdf at vendors' websites
- Selected datasheets on local CpE213 website
- Also in Appendix D
- Additional info in hdwr,pgmr,arch man



89C51Rx2 data sheet

- Features, Ordering Info, Packaging
- Block diagram,
- Logic diagram
- Pinouts [note different packages]
- Pin descriptions [summary of pin functions]
- Alternate functions for Port 3
- Oscillator characteristics: note Fig 2-3 difference
- DC characteristics

8051 Pinout (external perspective)



8051 pins

- 32 of 40 lines function as I/O port lines.
  - 24 of these lines are dual-purpose.
  - Can operate as I/O, control line, or part of data or address bus.
- Eight lines in each port can be treated as a unit for parallel interfaces (such as?)
- Each line can operate independently in interfacing to single-bit devices (such as?)

8051 I/O Ports

- P0: dual purpose
  - general I/O
  - data bus or lower byte of address bus
- P1: dedicated I/O port
- P2: dual purpose
  - general I/O
  - higher byte of address bus (for more than ___ memory)
- P3: dual purpose port
  - general I/O
  - each pin has alternate special features: serial, external interrupt, timer/counter, external data read and write.

8051 pins

- Four dedicated bus control signals
  - PSEN' (active low)
  - ALE
  - EA' (active low)
  - RST

Bus Control Signals

PSEN’

- Program Store Enable
- Enables external program (code) memory.
- Pulses low during instruction fetch state
- Usually connects to EPROM’s OE’ pin

ALE

- Address Latch Enable
- Used for de-muxing the address and data bus
- Pulses at 1/6th the oscillator frequency

More Bus Control Signals

EA’

- External Access
- Usually tied either high or low
- If high, program executes from internal memory
- If low program execute from external memory only. PSEN’ needs to be low.

RST

- Reset
- When high for 2 instruction/machine cycles, the micro-controller resets all internal registers, and begins a system reboot.
- Two methods for reset.

8051 Pins

XTL1 & 2

- On-chip oscillator inputs.
- Can be driven by a crystal or by a TTL clock source, providing the clock signal for the micro-controller.
- Stabilization capacitors are sometimes required.

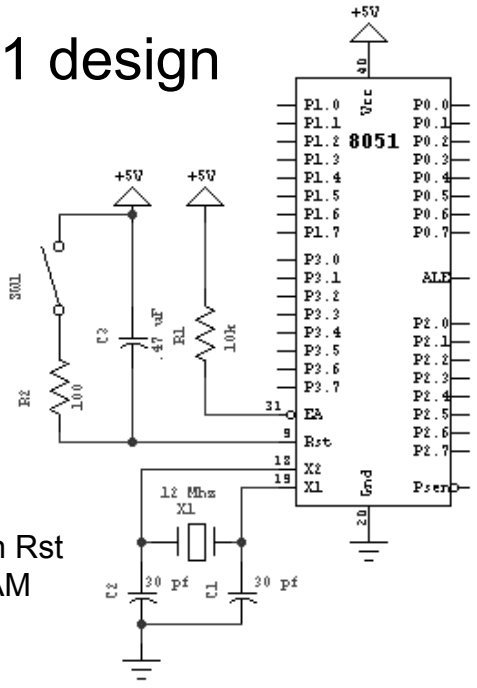
Vcc

- Power in pin
- +2.5V to +6V
- Usually +5V

GND/Vss

- Ground pin

A simple 8051 design



- 40 pin DIP package
- manual and power on Rst
- Internal ROM and RAM

More on I/O Ports

- 32 pins for 4 8-bit ports
- At power-on all are output ports by default
- To configure any port for input, write all 1's (how many bits?) to the port.