Cp Eng 213 – Digital Systems Design

Exam #2 (100pts) – Tuesday, Apr. 8, 2003
Open book and closed notes. One crib sheet/calculator allowed.
Show your work/derivation for full credit!

Name: Student ID:

1. Illustrate how the content of external memory address 101AH could be transferred to the accumulator, using INDIRECT ADDRESSING. Use a sequence of exactly two 8051 ASM instructions to do it. (5pts)

2. Illustrate how the content of code memory address, located by 16-bit base address of 1000H and 8-bit index of 1FH, could be transferred to the accumulator, using INDEXED ADDRESSING. Use a sequence of exactly three 8051 ASM instructions to do it. (5pts)

3. (10pts) The following is an 8051 instruction:

here: CJNE A, #10, here

a) What are the hexadecimal machine language bytes for this instruction?

b) Explain the purpose of each byte of this instruction.

c) How many machine cycles are required to execute this instruction?

d) In an 8051 is operating from a 12MHz crystal, how long does this instruction take to execute?

4. a) At a certain point in an 8051 ASM program, it is desired to jump to the label EXIT if the accumulator equals the ASCII code for ‘Q’ or ‘q’, or continue on otherwise. What instruction(s) would be used? (10pts)

b) What instruction(s) could be used to copy Flag0 in the PSW to the port pin P1.5? (5pts)

5. What are the hexadecimal bytes for the following instructions? (HINT: $ is the current content of PC.) (10pts)

a) MOVX @DPTR, A

b) SETB P1.1

c) CJNE A, #12H, $+6

d) POP DPL

e) JNB ACC.0, $+3

6. What is the content of accumulator A after the following instruction sequence executes? (10pts)

MOV A, #7FH
MOV 50H, #29H
MOV R0, #50H
XCHD A, @R0
RR A

7. (15pts) An 8051 subroutine is shown below:

```
SUB:    MOV R0, #20H
LOOP:   MOV @R0, #0
        INC R0
        CJNE R0, #80H, LOOP
        RET
```

a) What does this subroutine do?

b) In how many machine cycles does EACH instruction execute?

c) How many bytes long is EACH instruction?

d) How long does this subroutine take to execute? (Assume 12MHz operation.)

8. The following sequence of 8051 ASM lines makes an array of 8 different data and labels the beginning address of it as “TABLE”:

```
            CSEG AT 0
            LJMP START
TABLE:      DB 0, 1, 2, 3, 4, 5, 6, 7

            CSEG AT 100H
START:      NOP
```

Add more 8051 ASM lines to implement a program which outputs each data stored in the table to I/O port3, one by one, in reverse order (e.g., 7, 6, 5, 4, 3, 2, 1 and 0.) Note that a loop must be used to access the table. (20pts)

9. The 8051 internal memory is initialized as follows immediately prior to the execution of an RET instruction:

Internal Address	Contents	SFRs	Contents
0BH	9AH	SP (stack pointer)	0BH
0AH	78H	PC (pgm counter)	0200H
09H	56H	A	55H
08H	34H		
07H	12H		

What is the content of the PC and the content of the SP after the RET instruction executes? (10pts)