CpE 318 HW#6 (due 4/29/04) (20 points)

1) Design an IEEE single precision floating-point co-processor

* entity name: *FP_co*
* inputs: *F*: 2-bit std_logic_vector

F	operation
00	C = A + B
01	C = A × B
10	C = A ÷ B
11	C = $\sqrt{A}$

* inputs: *A*, *B*: 32-bit std_logic_vector (IEEE SP FP format)
* outputs: *C*: 32-bit std_logic_vector (IEEE SP FP format)

* name your file: lastname_student#_6.vhd
* include as comments: name and student number (-- precedes a comment line)

* email your main design and components as attachments from the PC (ftp to PC) to: cpe318@umr.edu
* your design will then be run on my testbench
* you should write your own testbench to test your design, however you should not turn this in
* make sure that all names and input/output order match those on this sheet, otherwise your design will not run on my testbench and you will receive 0 points
* the design must be synthesizable (i.e. no real or floating-point types)