PLEASE REGRADE ALL MISSED PROBLEMS

29, 30, 37, 38, 39, 41, 42

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CpE 213
Chapter 2 HW

1. Name 4 manufacturers of the 8051 microcontroller, besides Intel.

Siemens, AMD, Fujitsu, Philips list web address

www.fujitsu.com www.phillipssemiconductor.com www.siemenscan www.amd.com

2. Which device in the MCS-51 family would probably be used for a product that will be manufactured in large quantities with a large on-chip program

8052 - 8K ROM

3. What instruction could be used to set the Carry flag but at byte address 25H?

SETB 28H

4. What instruction sequence could be used to place the logical OR of the bits at bit address 00H and 01H into bit address 02H?

```
MOV  C, 00H
ORL  C, 01H
MOV  02H, C
```

5. What instruction sequence could be used to read bit 0 of Port 0 and write the state of the bit read to bit 0 of Port 3.

```
MOV   C P0.0
MOV   P3.0, C
```

6. Illustrate an instruction sequence to read bit 0 and bit 1 of Port 0 and write a status condition to bit 0 of Port 3 as follows: If both bits are 1, write 1 to output status, otherwise write a 0.

```
MOV   C, P0.0
ANL   C, P0.1
MOV   P3.0, C
```

7. Illustrate an instruction sequence to read bit 0 and bit 1 of Port 0 and write a status condition to bit 0 of Port 3 as follows: If either bit is 1, but not both, write a 1 to the output status bit, otherwise write a 0.

```
MOV   C, P0.0
XRL   C, P0.1
MOV   P3.0, C
```

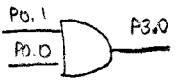
8. Illustrate an instruction sequence to read bit 0 and bit 1 of Port 0 and write a status condition to bit 0 of Port 3 as follows: If either bit is 1 write a 0 to output status bit, otherwise write a 1

```
MOV  C, P0.0
ORL  C, P0.1
MOV  P3.0, /C
```

00 1
01 0
10 0
11 0

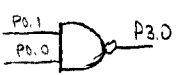
9. For the three preceeding questions, illustrate the operation using logic gates

a) 2.6



b) 2.7

c) 2.8



10. What bit addresses are set to a 1 as a result of the following operations

a) MOV 26H, #26H 00100110 — 35H, 32H, 31H

b) MOV R0, #26H 00100110
MOV @R0, #7AH 01111010 — 36H, 35H, 34H, 33H, 31H

c) MOV A, #13H 00010011

E4H, E1H, E0H ✓

d) MOV 30H, #65H
XRL 30H, #0AAH — ?

e) SET P1.1 91H ✓

f) MOV P3, #0CH 00001100

33H, 82H ✓

11. What one byte instruction has the same effect as the following 2-byte instruction? MOV 0E0H, #55H

MOV R6, #55H

12. Illustrate an instruction sequence to store the value 0ABH in external RAM at address 9A00H

```
MOV  A, #0ABH
MOV  DPTR, #9A00H
MOVX @DPTR, A
```

13. How many special function registers are defined on the 8052?

26 SFR

14. What is the value of the 8051's stack pointer immediately after a system reset?

✓ 07H

15. What instruction would be used to initialize the stack pointer to create a 64-byte stack at the top of internal memory (a) on the 8051 or (b) on the 8052?

✓ a) 128 bytes start 40H

MOV SP, #3FH

b) 256 bytes 80H

MOV SP #BFH

16. What instruction would be used to initialize the stack pointer to create a 32-byte stack at the top of memory on (a) 8051 or (b) 8052.

✓ a) 128 bytes 60H

MOV SP, #5FH

b) 256 bytes E0

MOV SP, #DFH

17. A certain subroutine makes extensive use of registers R0-R7. Illustrate how this subroutine could switch the active register bank to bank 3 upon entry & restore the previously active register upon exit.

✓

```
PUSH  PSW
SET B RS1
SET B RS0
POP   PSW
```

18. What is the active register bank after execution of each of the following instructions?

a) MOV PSW, #0FDH ? 11111101 Bank 3

b) MOV PSW, #18H ? 00011000 Bank 3

c) MOV PSW, #08H ? 00001000 Bank 1

19 What is the active register bank after execution of each of the following registers?

a) MOV PSW, #0C8H 11001000 Bank 1

b) MOV PSW, #30H ? 00110000 Bank 2

c) MOV PSW, #10H 00010000 Bank 2

20. The 80C31BH-1 can operate using a 16 MHz crystal to its XTAL1 and XTAL2 inputs. If MOVX instructions are not used, what is the frequency of the signal on ALE?

$\frac{8}{3}$ MHz

21. If an 8051 is operating from a 4MHz crystal, what is the duration of a machine cycle?

3 μs

22 If an 8051 is operating from a 15 MHz crystal, what is the frequency of the waveform on ALE? Assume the software is not accessing external RAM.

$\frac{5}{3}$ MHz

* 23. What is the duty cycle of ALE? Assume that software is not accessing external RAM. (Note: Duty cycle is defined as proportion of time a pulse waveform is high.)

$\frac{2}{6} = \frac{1}{3}$ 33⅓%

24. Section 2.8 states that the 8051 is reset if the RST pin is held high for a minimum of two machine cycles.

a) If an 8051 is operating from an 8MHz crystal, what is the minimum length of time for RST to be high to achieve a system reset? $\frac{8}{12} = \frac{2}{3}$

3 µs

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b) Figure 2-5 shows an RC circuit for a manual reset. While the reset button is depressed, RST = 5V and the system is held in a reset state. How long after the reset button is released will the 8051 remain in a reset state?

$V = Ve^{-t/RC} = 2.5\ V$

$\tau = RC = (8.2 \times 10^3)(1.0 \times 10^{-6})$

$t = 8.45\ s$

25. How many low-power Schottky loads can be driven by the port pins P1.7 or P3.8?

4 Low power Schottky loads

26. Name the 8051 control bus signals used to select external EPROMs and external RAMs?

EPROMS: $\overline{EA}$, $\overline{PSEN}$, ALE
RAM: $\overline{EA}$, $\overline{RD}$, $\overline{WR}$, ALE

27. What is the bit address of the most-sig bit of byte address 25H in the 8051's internal data memory.

2FH

28. What is the bit address of bit 3 in byte address 2FH in the 8051's internal data memory?

7BH

29. Some of the bit addressable locations in the 8031's on-chip data memory are brought out as signals on the 8031 IC. Which ones? What are their pin numbers + what are their bit addresses?

P0.0, 80H, Pin 39; P0.1, 81H, 38, P0.2, 82H, 37; P0.3, 83H, 36; P0.4, 84H, 35
P0.5, 85H, 34; P0.6, 86H, 33; P0.7, 87H, 32; P1.0, 90H, 1; P1.1, 91H, 2, P1.2, 92H 3
P1.3, 93H, 4; P1.4, 94H, 5, P1.5, 95H, 6; P1.6, 90H, 7; P1.7, 97H, 8; P2.0, A0H, 21,
P2.1, A1H, 22; P2.2, A2H, 23; P2.3, A3H, 24; P2.4, A4H, 25; P2.5, A5H, 26; P2.6, A6H, 27
P2.7, A7H, 28; P3.0, B0H, 10; P3.1, B1H, 11; P3.2, B2H, 12, P3.3, B3H, 13, P3.4, B4H, 14;
P3.5, B5H, 15; P3.6, B6H, 16; P3.7, B7H, 17

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30. Identify the bit position + byte address for each of the following SETB instructions.

a) SETB 37H — Byte Address 26H, Bit 7

b) SETB 77H — Byte Address 2EH, Bit 7

c) SETB 0F7H — Byte Address F0H, Bit 7

31. Identify bit position + byte address for each of following

a) SETB 0A8H — Byte Address A8H, Bit 0

b) SETB 84H — Byte Address 80H, Bit 4

c) SETB 63H — Byte Address 2CH, Bit 3

32. What instruction sets the least significant bit of the accumulator w/o affecting the other 7 bits?

SETB E0H

33. What is the state of the P bit in the PSW after execution of each of the following instructions?

a) MOV A, #55H — P = 0

b) MOV A, #0F8H — P = 1

c) MOV A, #0FFH — P = 0

34. What is the state of the P bit in the PSW after execution of each of the following instructions?

a) CLR A — P = 0
b) MOV A, #03H — P = 0
c) MOV A, #0ABH — P = 1

35. What instruction sequence could be used to copy the content of R7 to external RAM location 100H

```
MOV  A, R7
MOV  DPTR, #100H
MOVX @DPTR, A
```

36. Illustrate an instruction sequence to read external ram address 08F5H & place the byte read into the B accumulator?

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```
MOV DPTR, #08F5H
MOVX B,@DPTR
```

use acc

37. Assume the first instruction executed following a system reset is a subroutine call. At what address in internal RAM is the PC saved before branching to the subroutine?

✓ 07H

38. Consider the instruction MOV SP, #08-H. What is the effect of this instruction if executed on 8032?
(b) What is effect of on 8031?

3/4 a) create a 76 byte stack ✓

∝ b) not valid

39. If an 8031 program is designed to use only register bank zero, then the stack pointer need not be initialized. However, if an 8031 prog is designed to use all four register banks, then it is imperative that the stack pointer be explicitly initialized. Why?

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Y When switching between register banks, the PSW is pushed into the stack to retain what was the active stack.

40. What is the difference between the 8051's idle mode & powerdown mode?

In idle mode the clock is gated to the CPU but not to the interrupt, timer, & serial port. ALE and (PSEN) are held high.

In power down mode the oscillator is stopped, all functions are stopped, all on chip RAM contents remain, ports retain logic, ALE & (PSEN) are made low.

41. What instruction could force the 8051 into powerdown mode.

MOV 87H,#82H Y

42 Illustrate how two 32K-byte static RAM's could be interfaced to the 8051 so that they occupy the full 64 K external data space.