CmpE 111 – Introduction to Computer Engineering

a.k.a Digital Logic Design

Winter Semester, 1999

Instructor

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(Though I'm often available at other times)

Textbook

D. Gajski, *Principles of Digital Design*,
Prentice Hall, 1997

Homework

(Tentative) homework assignments and due dates are shown in the course outline. No late homework will be accepted.

Prerequisite

CSc 53, 73, or 74.

Lab

Students should be concurrently enrolled in CmpE 112.

Grading

(Tentative)

10%	Homework (Drop lowest)
20%	Test 1
20%	Test 2
20%	Test 3
25%	Final Exam
5%	Evaluation (Attendance, homework, progress, participation, etc)

CmpE 111 Course Outline

(tentative)

Lecture	Date	Topic	Covering	Homework
1	1/12	Introduction	Ch1	Ch1:2,6
2	1/14	Number Systems	Ch2	Ch2:1,4,5,11,14
3	1/19	Math, Codes	Ch2	Ch2:16,18b,19c,22c,27,29
4	1/21	Boolean Algebra	Ch3	Ch3:2ad,3,4ad,6c **Ch1 Due**
5	1/26	Forms, Operators, Gates	Ch3	Ch3:7b,8a,10c,11,14,15
6	1/28	Logic Gates	Ch3	Ch3:16a **Ch2 Due**
7	2/2	Logic Gates, Implementation	Ch3	Ch3:20a
8	2/4	Boolean Cubes, Karnaugh Maps	Ch4	Ch4:1c,2c,3a,5d,6bc **Ch3 Due**
9	2/9	Tabulation, Tech. Mapping	Ch4	Ch4:8c,P1 (see below)
10	2/11	**Test I**		
11	2/16	Mapping, Hazards	Ch4	Ch4:10a,11b,13b
12	2/18	Mapping, Hazards	Ch4	Ch4:18 **Ch4:1–8c,P1 Due**
13	2/23	Adders	Ch5	Ch5:1,5b,7b
14	2/25	ALU, Decoders, Selectors	Ch5	Ch5:8,10b,P2 **Ch4:10–18 Due**
15	3/2	Busses, Encoders, Comparators	Ch5	Ch5:12,14d,15
16	3/4	Shifters, ROMs, PLAs	Ch5	Ch5:18,22b
17	3/9	Latches, Flip-Flops	Ch6	Ch6:1b,2b,5b,6 **Ch5 Due**
	3/11	Spring Recess		
18	3/16	Flip-Flops, Sequential Logic Anal.	Ch6	Ch6:7,9
19	3/18	**Test II**		
	3/23	Spring Break		
	3/25	Spring Break		
20	3/30	Analysis, State-Machine, Synthesis	Ch6	Ch6:10
21	4/1	State Minimization, Encoding	Ch6	Ch6:12,14 **Ch6:1–9 Due**
22	4/6	Memory, Optimization	Ch6	Ch6:17,22
23	4/8	Registers, Counters	Ch7	Ch7:1,4
24	4/13	Counters, Reg. Files	Ch7	Ch7:9b,10b,15c **Ch6:10–22 Due**
25	4/15	RAM, Stacks	Ch7	Ch7:16b
26	4/20	Datapaths	Ch7	Ch7:22
27	4/22	Control Units	Ch7	**Ch7 Due**
28	4/27	FSMD, ASM charts	Ch8	Ch8:1,4,8
29	4/29	**Test III**		
30	5/4	ASM charts, Pipelining	Ch8	**Ch8 Due**
31	5/6	TBA, Review	Ch8	
	5/14	**Final Exam, Friday, 8:00-10:00 AM**		

P1. Develop K-Map and minimum SOP for BCD to 7-segment decoder.

P2. Develop gate realization of BCD to 7-segment decoder using gate library primitives.