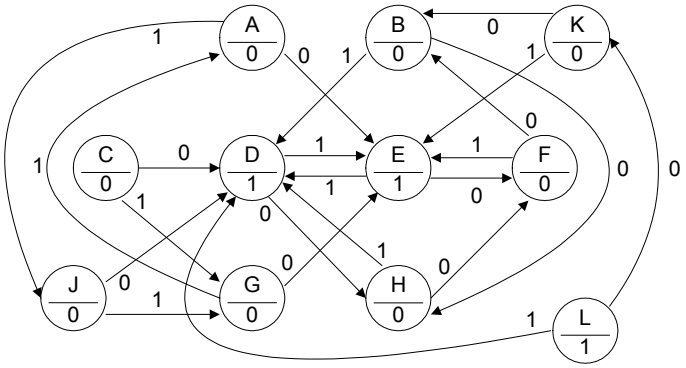
CpE 318 HW#3 (due 2/24/04) (20 points)

[3] 1) Reduce the following state diagram to the minimal number of states, and draw the optimized state diagram. Rename a combined state with the names of all states that were combined (i.e. if states A, B, and C are equivalent, then the new state name would be: A, B, C).



[2] 2a) Generate a minimal non-resetting state diagram for a Mealy machine that detects an active-high signal pulse, 010, or an active-low signal pulse, 101. The output, *Z*, is active-high.

Sample input/output sequence:
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X: 010101011011
Z: 001111110010
Time →
```

[1] b) Show the state table, and row reduction if possible.

[1] c) Show the implication table.

[1] d) Make a good state assignment.

[1] e) Draw the minimized logic diagram.

[2] f) Code this state machine as a dataflow model (inputs are clk, rst, and *X*, outputs are *Z* and current state).

[2] g) Code this state machine as a behavioral model (inputs are clk, rst, and *X*, outputs are *Z* and current state).

[1] h) Synthesize the models of 2f) and 2g) and turn in the synthesized code, not including the primitives.

[4] i) Write an exhaustive testbench and macro, showing clk, rst, *X*, *Z*, and the current state, for the behavioral, dataflow, and synthesized models; then simulate the models and turn in the waveforms. Write a brief explanation of the simulations.

[1] j) Compare the dataflow and behavioral synthesized models (i.e. area, speed, and state assignment). Which is better? Why?

[1] k) Add unused states to the minimized state diagram with dotted lines. Comment on robustness.

- use a synchronous reset, positive edge-triggered flip-flops, and a clock period of 50 ns
- change inputs on the falling edge of the clock