EE 2372 Test 2

9 problems, 100 points.

November 24, 1998

NAME

Closed book, closed notes, no calculators. Scratch paper will be provided, so do not use any of your own.

You are permitted pens or pencils, erasers, and a (non-calculator) watch. All other items are to be placed underneath your desk.

Please read the entire exam before beginning, and note point values. Some problems are more worthwhile than others.

Do not turn this page until instructed to do so.

Good luck!

8 points

1. Design a synchronous decade (0-9) counter using four JK flip-flops, four NOR gates, and four 16-1 multiplexers. Any erroneous (glitch) state must be reset to zero on the next clock cycle. The states are $Q_3 Q_2 Q_1 Q_0$. (MSB) (LSB)

4 points

2. Can you make any gate you want, using only XOR gates and inverters? (Circle your answer.)

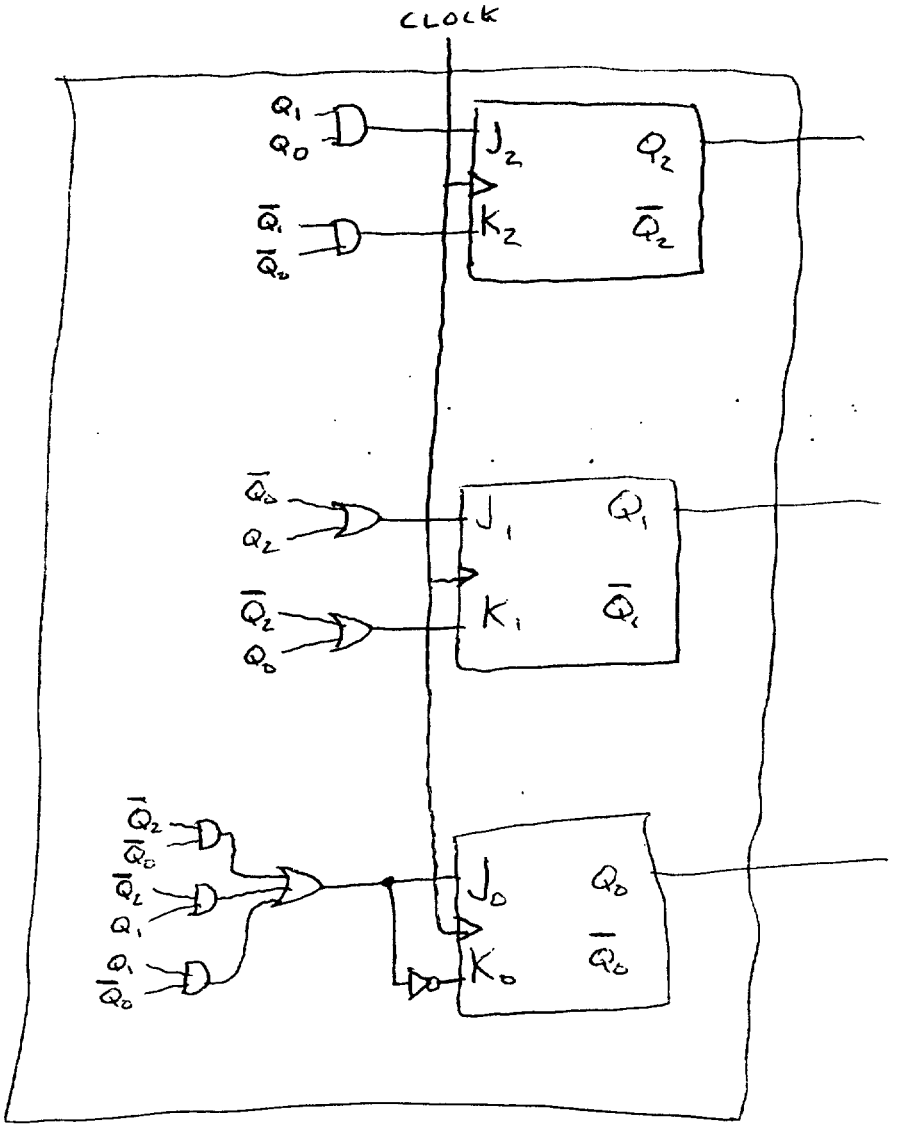
YES No

If you said yes, show how.

If you said no, why not?

18 points

3. What is this system doing?



Hint: Draw the Moore diagram.

12 points

4. Design a 3-bit synchronous Modulo-6 counter, using D flip flops: D_2 D_1 D_0.
(It counts 0-5 and starts over.)

Use a Moore diagram

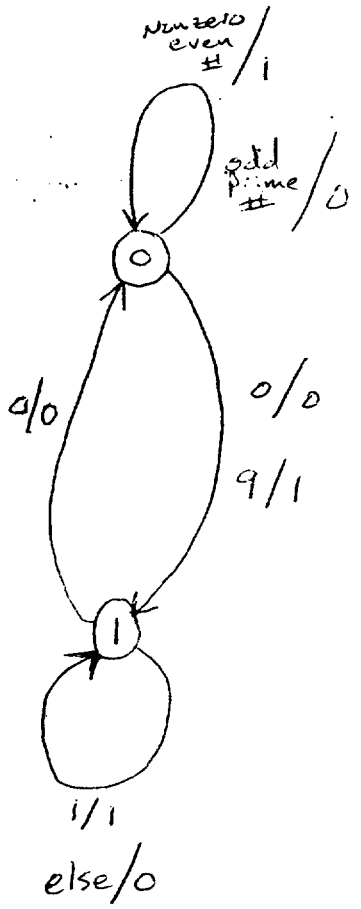
Write minimal SOP expressions for

D_2 D_1 D_0

You don't need to draw the devices.

17 points

5. Your input is in Excess-3, and your problem is specified by the Mealy Diagram below. Design the complete system in minimal SOP form. Use the variable-entered map technique. Don't draw the gates, just write the minimal SOP expressions. Now, can you further reduce the gate count by finding redundancies in the S and D expressions?



11 points

6. Make a Store-Toggle flip-flop with the following excitation table

S	T	Q^{t+1}	
0	0	0	reset
0	1	$\overline{Q^t}$	Toggle
1	0	Q^t	Store
1	1	0	reset

Implement this using a T flip-flop and additional logic. (We will call the T flip-flop's input T_f to distinguish it from the T above.)

Fill in the state transition table below:

Q^t	Q^{t+1}	S	T
0	0		
0	1		
1	0		
1	1		

(Hint: For two lines, the correct answer is not unique. Pick any correct answer for those lines.)

11 points

7. Design a two-bit up/down counter.

The control input is: $\begin{cases} X = 0 \Rightarrow \text{count down} \\ X = 1 \Rightarrow \text{count up} \end{cases}$

The states are

$Q_A = A \equiv$ Most Significant Bit

$Q_B = B \equiv$ Least significant Bit

You can only use SR flip flops, XOR gates, and inverters.

12 points

8. Design a 4-bit ring counter with initialize and error correction. The only inputs are the clock and I, the initialize signal. The system outputs are:

1000
0100
0010
0001
1000
⋮

If the system enters any invalid state, it must return to 1000 on the next clock cycle. The signal to do this is called E.

Use D flip flops: $D_3\ D_2\ D_1\ D_0$.

Just write the equations for each D input — you don't need to draw them. Also write the equation for E.

7 points

9. Configure a 74154 decoder (see following pages) to implement the function $F = A\bar{B}\bar{C}\bar{D} + B + C$.