CpE311 – Test I, F02

Name_____

Show all your work in the space provided. Answers with a simple "yes", "no", or a single number are typically incomplete and will not be given full credit. Answers in non-reduced form, like (a+sqrt(b))/c, are fine where appropriate. Good English on essay/short answer questions is required. ON MULTIPLE CHOICE QUESTIONS, IF YOU'RE NOT SURE GUESS CAREFULLY– you will get points off for wrong answers. If you know part of an answer, write what you know for partial credit.

1. (20 Points) Act I logic. Implement the following function using ACT1 logic modules. Use as many modules as you like. Show your work.

   $F = (A \oplus B) + \overline{B}C$

2. (10 Points) Software tools. *Briefly* describe the method used to determine the critical path using the Mentor Graphics and/or Leonardo synthesis and simulation tools (as you did in Lab 1). Keep your explanation within the space given below.

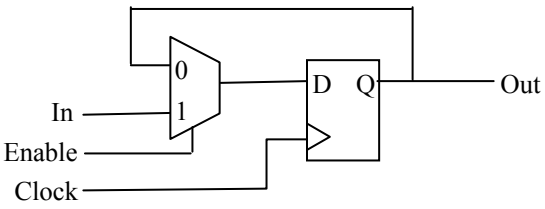
3. (20 Points) Choosing a chip technology. Say you are asked to design an ASIC for a high-tech product with a short lifespan and a small total production (i.e. 1000s of units, not 10,000s of units). It is expected that the ASIC will NOT contain a particularly large number of gates and will NOT have to be particularly fast. Explain what type of chip technology (custom, CBIC, MGA, FPGA, etc.) you believe would be best for this project. Defend your selection, such that you convince me your choice is right and that you thoroughly understand your options. Try to keep your explanation within the space given below.

4. (5 Points) Timing. In a typical design implemented in an ACT1 FPGA, interconnect probably accounts for about how much of the total delay along a circuits critical path (compared to logic):

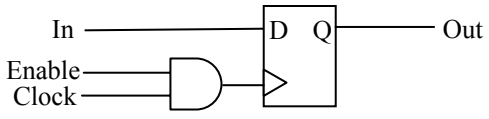
a) almost none	b) around 25%	c) around 50%
d) around 75%	e) around 100%	f) None of the above

5. (5 Points). Gated clock. Circle the better of the two following design choices:

a)



b)



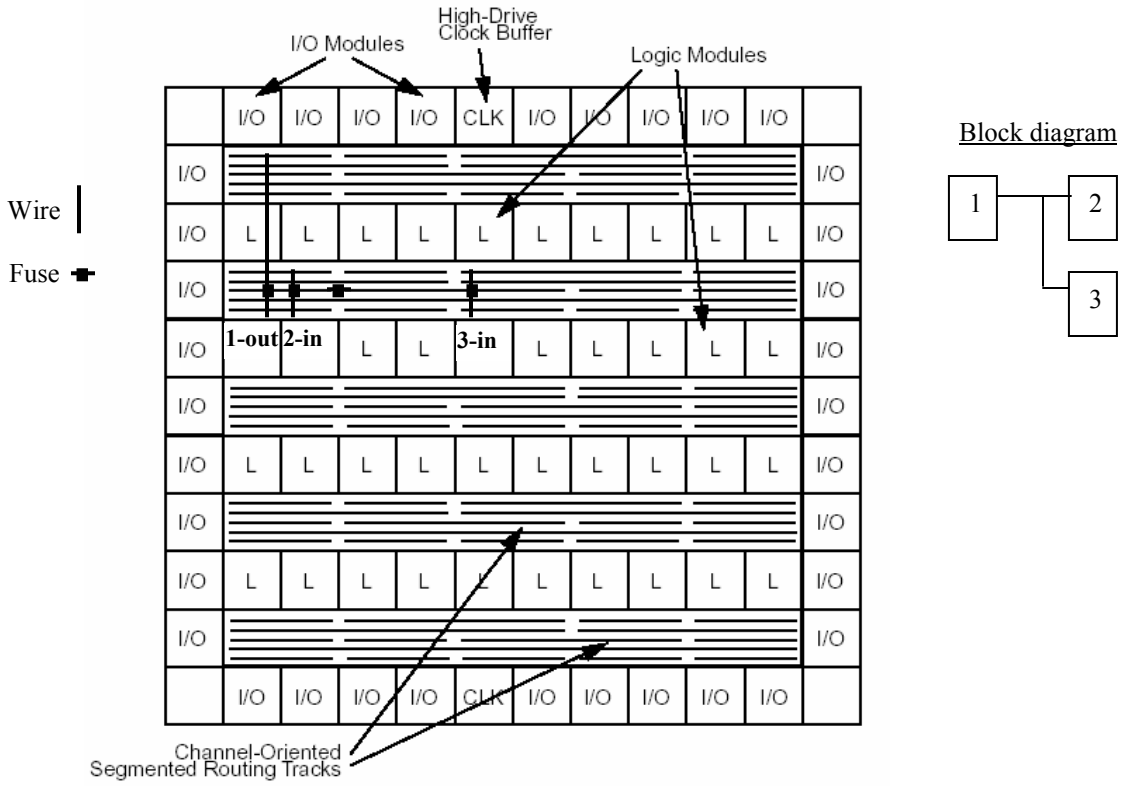
6. (15 Points) VHDL. Draw a block diagram for the circuit that would likely be synthesized for the following VHDL code. Clearly label any signals/wires appropriately, especially circuit inputs and outputs. Draw boxes around entities or "entity-like" structures. Label components appropriately if not obvious (e.g. "flip-flop", "OR-gate", "adder", etc).

```
library IEEE;
use IEEE.std_logic_1164.all;

entity e1 is
    port(a,clk: in std_logic;
        f:out std_logic);
end entity e1;

architecture a1 of e1 is
    signal b: std_logic;
begin
    p1: process (a,b) is
    begin
        f <= a AND b;
    end process;
    p2: process (clk) is
    begin
        if (clk = '1') then
            b <= a;
        end if;
    end process;
end;
```

7. (25 Points) Calculating time delays. A particular circuit was synthesized in an ACT1 logic module as shown below. Inputs and outputs are marked in the figure. Connecting wires are shown in bold, as are blown anti-fuses between interconnect. Note that one anti-fuse is used to connect two horizontal tracks.



a) (15 points) Draw an equivalent RC network between logic elements 1, 2, and 3 (1-out, 2-in, 3-in) that could be used to calculate delay. Mark the approximate size of resistors or capacitors where appropriate. Clearly label where the logic modules connect to the circuit in your diagram.

b) (10 points) Calculate the time delay constant from the output at logic element 1 (i.e. 1-out) to the input at logic element 3 (i.e. 3-in). Assume T_J=70 degrees C.