CpE 213 - Homework Set 1

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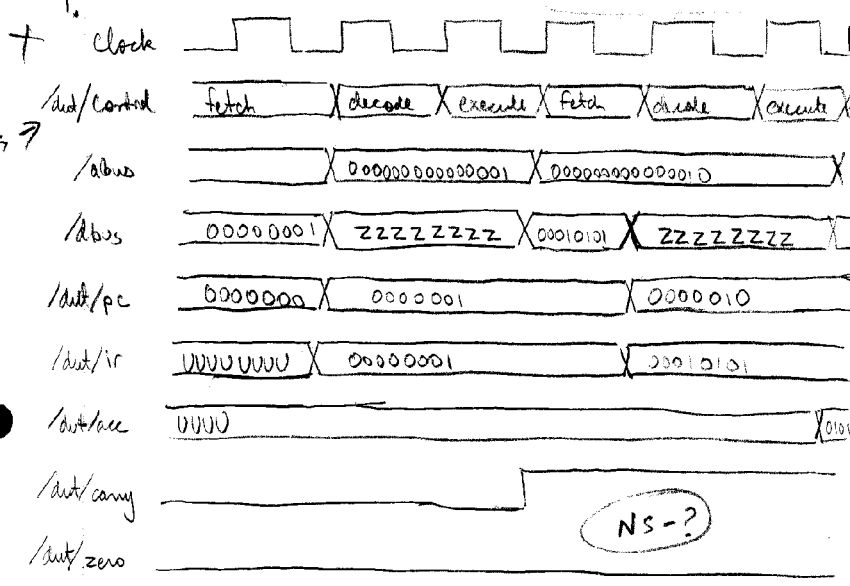
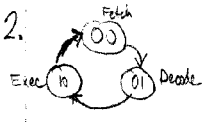
1/25/01

1.



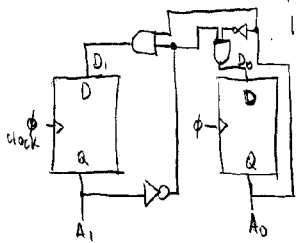
2.



Present $A_1 A_0$	Next A_1, A_0	Inputs $D_1 D_0$
00	01	01
01	10	10
10	00	00
11	00	00

$D_1 = \bar{A}_1 A_0$

$D_0 = \bar{A}_1 \bar{A}_0$



3. Range of code addresses: 0-127

4 Range of data addresses: 0-15

5 code: 7Fh
data: Fh

6. rd_data

7. There would be 11 ones concatenated to the abus: 11111111111

8. There is a control signal from the control unit to the IR that has combinational logic that only allows the IR to latch at the end of the fetch cycle.

9.

Inst Op	Code	Addr
Lda #1	11h	0001h
Sta 0	30h	0002h
Lda #2	12h	0003h
Clr C	00h	0004h
Add 0	50h	0005h
Sta 1	31h	0006h
Jump 6	86h	0007h

Instr	Op	Code	Addr
Lda	#F	1Fh	0001h
Sta	2	32h	0002h
Lda	#0	10h	0003h
Sta	0	30h	0004h
Lda	#3	13h	0005h
Sta	1	31h	0006h
Lda	#5	15h	0007h
Clr	C	00h	0008h
Add	0	50h	0009h
Sta	0	30h	000Ah
Lda	1	41h	000Bh
Clr	C	00h	000Ch
Add	#F	2Fh	000Dh
Sta	1	31h	000Fh
Tst	2	72h	000Fh
Skip z		03h	0010h
Jump	Loop (7)	87h	0011h
Jump	stop (18)	92h	0012h

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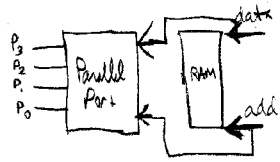

The parallel port could be connected in parallel with the memory. Then, the address decoder in the parallel port would be set to output data when a certain memory address is input. For example, if we set memory address 0h was input, this could correspond to parallel port output. Then the data sent on the data line to the memory would also be sent out on the parallel port