

CpE401 – Advanced VLSI Design

Fall Semester, 2003

Instructor:

Dr. Daryl Beetner

Email: daryl@ece.umn.edu (Best way to reach me)

Office: EECH 126

Web page: <http://www.umn.edu/~daryl>

Office hours (tentative): Tues. 3-5.

(though I'm often available at other times)

Prerequisites: CpE311 – I wouldn't attempt this class without it.
CpE318 can also be helpful but is not required.

Textbook: *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. J. Bowhill, F. Fox, IEEE Press, 2001.

NOTE CHANGE!

Recommended supplements:

- *Application-Specific Integrated Circuits*, M. J. S. Smith, Addison-Wesley, 1997.
- *Digital Integrated Circuits*, 2nd Ed. J. M. Rabaey, A. Chandrakasan, B. Nikolik, Prentice Hall, 2003.
- *CMOS Analog Circuit Design*, Allen and Holberg, Oxford University Press, 2002.
- A variety of in-class handouts occasionally available on the web at <http://www.umn.edu/~daryl>.

Material Covered: (*subject to change – watch for updates*).

Introduction (1 lect.) (Ch. 1.2.1, 1.5, 1.6, 1.7)

Deep-submicron design (2 lect.) (Ch. 2)

Device models – parasitics (1 lect.) (Possibly some Ch. 3)

Electrical wire models (2 lect.)

Crosstalk (2 lect) (Some Ch 16, 17)

Driving interconnect (1 lect.) (Ch. 7)

Analyzing interconnect (0.5 lect.) (Some Ch. 16)

High-speed electrical signaling (2 lect.) (Ch. 19)

Advanced packaging (1 lect.)

I/O models and ESD protection (1 lect.) (Ch. 18)

EMC issues in VLSI design (2 lect.)

Low voltage technologies (1 lect.) (Ch. 4)

Dynamic CMOS design (2 lect.) (Ch. 8)

Domino Circuits (1 lect.)

Essentials of Analog CMOS design (3 lect.)

Process variation (0.5 lect.) (Ch. 6)

Low power design (2 lect.) (Ch. 3)

Grading: (*tentative*)

- 30% Test 1
- 30% Final Exam
- 10% Presentation topic and questions
- 10% Homework
- 18% Project
- 2% Evaluation (I can push you up or down by 1%. Unusual to push you to an A if no test scores with an A)

Presentation: Each person in class will be asked to give a 10-15 minute presentation on the topic of his choice, relevant to advanced VLSI design. Basically anything not covered in this course or CpE311 in VLSI design is fair game. See my web-site for ideas if you have trouble. A sign-up sheet will be passed around soon. In addition to actually giving the presentation, you must:

- Turn in a rough outline of your presentation 2-weeks before talk.
- Turn in a homework question and 2-page explanation of topic 1-week before talk. Using slide “notes” is OK if adequate explanation is given.

You will be graded on the quality of your presentation, write-up and homework question. Warning: if you make question too hard to grade, you might grade ;-).

Project: To be announced.

Tests and Quizzes:

Tests will cover material from the lectures, text, homework and labs, with a slight emphasis on homework. Tests will primarily cover material presented since the last exam, though usually has *some* material from earlier tests. Final exams are comprehensive, though a slight emphasis will be placed on material that might not have been covered on the previous test. I reserve the right to give small, surprise, in-class quizzes and adjust grade distribution accordingly.

Test dates:

Test I: Approximately Oct. 14

Final: Friday, Dec. 19, 8-10 AM.

Homework:

- You are expected to read appropriate sections of the textbook before presentation in class.
- Homework problems will be assigned in class or possibly on the web.
- As a rule of thumb, no late homework is accepted.
- Homework may involve some lab work.
- While you are expected to complete all assigned problems, the grader may randomly pick only certain problems to grade. It is common in larger classes to compute your grade based on the accuracy of 1 or 2 problems and an evaluation of how hard you “tried” on the rest.
- Lowest homework grade is dropped.

- Extra credit may occasionally be offered. You will not be penalized for not completing the extra credit, but if you have cause to be concerned about your grade I strongly recommend you take advantage of it when available.
- I strongly encourage you to study with others, as this can be a powerful tool for learning. However, I insist that you must a) attempt to understand and solve each problem by yourself and b) thoroughly understand any solution you turn in. If you cannot adequately explain the basis for your solution at a later date, no credit will be given even if your solution is correct. Simply “copying someone else’s homework will be considered cheating and will not be accepted under any circumstances.
- Homework is due at the beginning of class. I probably will not prompt you for it.

Partial Credit:

Problems are rarely graded as all-or-none. Emphasis is placed first on proper understanding of the concepts, then on proper application of those concepts, and lastly on “the right answer”. You will not be severely penalized for minor, non-conceptual errors. On the other hand, a simple answer with no work or explanation may not be given full credit.

If you feel you deserve more credit on a problem than was given, you may submit a written request for additional credit, clearly stating why you deserve additional credit. Such requests may not be made until 24 hours after the exam was handed back and should be in the form of a memo like you would use when communicating between professionals on the job. No requests will be accepted after 30 days. Clear violation of this policy may result in a *reduction* of points.

Attendance:

Attendance to lectures is generally not required (except for me ;-), however, I will not be sympathetic to problems caused by skipping class without a documented excuse. Excessive absence (in particular, failure to attend a quiz or exam without an excuse) may cause you to be dropped from the course.

Cheating:

Don’t do it! Department policy is to fail you in the course for the first offense and to expel you from the school of engineering for the second.