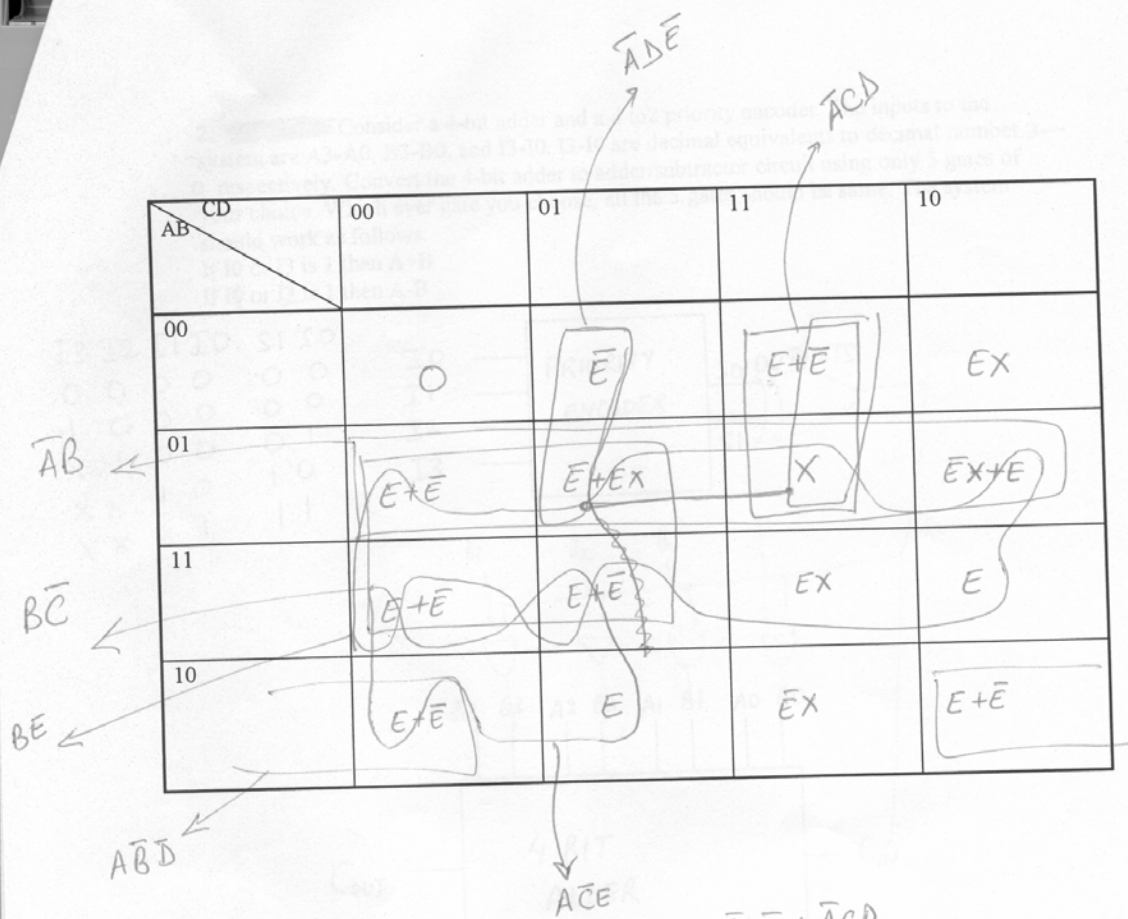1) Implement the function:

F= ΠM(0, 1, 3, 4, 18, 23, 28, 30) + ΠMx(5, 11, 12, 14, 15, 22, 31)

Fill in the truth table. Implement the function using 16:1 MUX and also get the minimal
SOP equation using the k-map on the next page.

Decimal	ABCDE	F	F(E)
0	00000	0	
1	00001	0	0
2	00010	1	
3	00011	0	$\overline{E}$
4	00100	0	
5	00101	X	EX
6	00110	1	
7	00111	1	$E+\overline{E}$
8	01000	1	
9	01001	1	$E+\overline{E}$
10	01010	1	
11	01011	X	$\overline{E}+EX$
12	01100	X	
13	01101	1	$\overline{E}X+E$
14	01110	X	
15	01111	X	X
16	10000	1	
17	10001	1	$E+\overline{E}$
18	10010	0	
19	10011	1	E
20	10100	1	
21	10101	1	$E+\overline{E}$
22	10110	X	
23	10111	0	$\overline{E}X$
24	11000	1	
25	11001	1	$E+\overline{E}$
26	11010	1	
27	11011	1	$E+\overline{E}$
28	11100	0	
29	11101	1	E
30	11110	0	
31	11111	X	EX

$$\overline{A}D\overline{E}$$

$$\overline{A}CD$$

AB \ CD	00	01	11	10
00	O	$\overline{E}$	$E+\overline{E}$	EX
01	$E+\overline{E}$	$\overline{E}+EX$	X	$\overline{E}X+E$
11	$E+\overline{E}$	$E+\overline{E}$	EX	E
10	$E+\overline{E}$	E	$\overline{E}X$	$E+\overline{E}$

$$\overline{A}B$$

$$B\overline{C}$$

$$BE$$

$$A\overline{B}\overline{D}$$

$$A\overline{C}E$$

$$SOP = A\overline{C}E + A\overline{B}\overline{D} + BE + B\overline{C} + \overline{A}B + \overline{A}D\overline{E} + \overline{A}CD$$

$$X = D$$

16:1
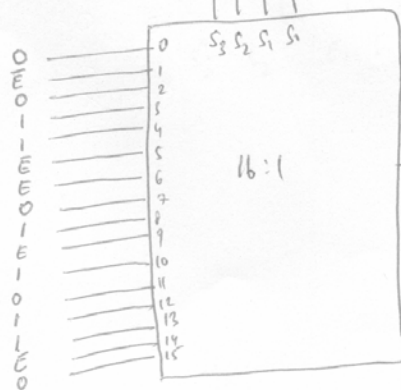
2. Consider a 4-bit adder and a 4 to2 priority encoder. The inputs to the system are A3-A0, B3-B0, and I3-I0. I3-I0 are decimal equivalents to decimal number 3 — 0 respectively. Convert the 4-bit adder to adder/subtractor circuit using only 5 gates of your choice. Which ever gate you choose, all the 5 gates should be same. The system should work as follows.

If I0 or I3 is 1 then A+B

If I0 or I3 is 1 then A-B

I3	I2	I1	I0	S1	S0
0	0	0	0	0	0
1	0	0	0	0	0
X	1	0	0	0	1
X	X	1	0	1	0
X	X	X	1	1	1
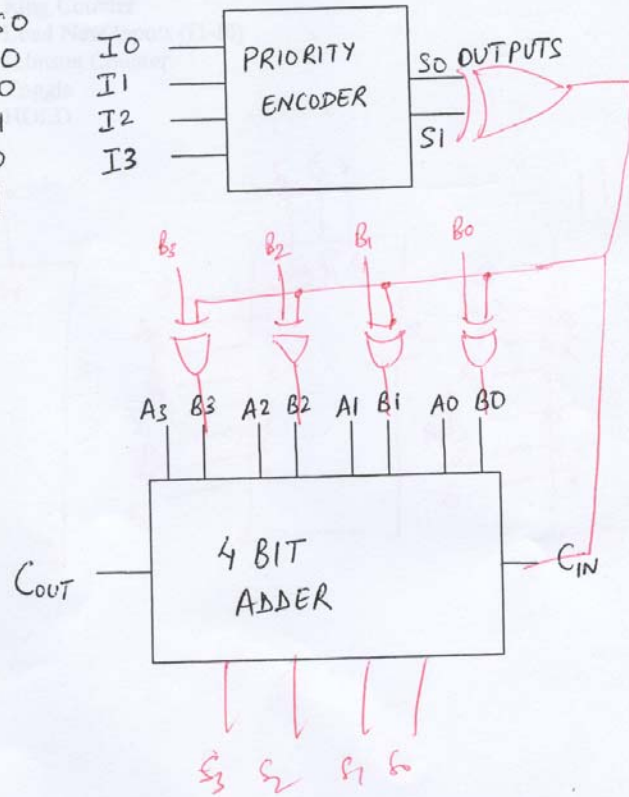
3) Design and draw a 4-bit universal shift register application using only multiplexers. The system should function according to the following function table. The outputs of the shift register is Q3-Q0

S2	S1	S0	Funtion
0	0	0	Shift Left
0	0	1	Shift Right
0	1	0	Set
0	1	1	Ring Counter
1	0	0	Load New Inputs (I3-I0)
1	0	1	Johnson Counter
1	1	0	Toggle
1	1	1	HOLD
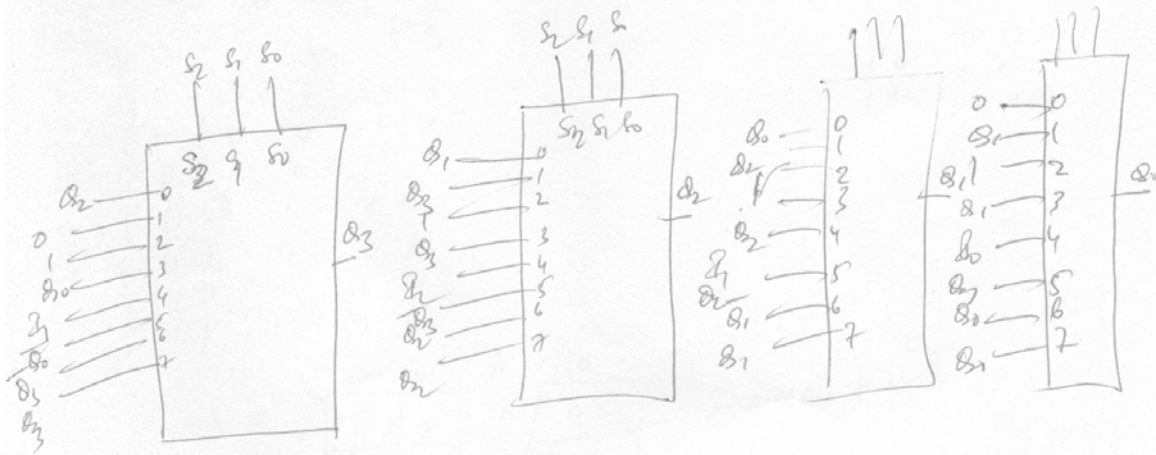
4) Design a flip-flop with the below given truth table using a S-R flip-flop.

U	V	Output
0	0	SET
0	1	RESET
1	0	TOGGLE
1	1	SET

S	R	Q_{t+1}	$\overline{Q}_{t+1}$
0	0	HOLD	
0	1	0	1
1	0	1	0
1	1	NOT USED	

U	V	Q_0	$\overline{Q}_0$	S	R
0	0	0	1	1	0
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	1	X	0

$$S = \overline{V}\overline{Q_0} + U\overline{Q_0}$$

$$R = U\overline{V}Q_0 + \overline{U}V$$