CpE 213
Digital Systems Design

Lecture 3

Tuesday 9/2/2003

Basic information

- Instructor: Sahra Sedigh-Ali
- Email: sedighali@ieee.org
- Phone: 341-7505
- Office: EECH 219
- Office Hours: TR 1:30-3:00, or by appointment.
- Email is the best way to reach me.

Prerequisites by Topic

- Familiarity with C programming.
- Knowledge of the functions of NAND, NOR, decoders, multiplexers, and similar combinational logic elements.
- Knowledge of the functions of D flip-flops, registers, counters, and similar sequential logic elements.

Important reminder

- The course syllabus is a legally binding agreement between you and your instructor.
- Portions have been skipped in class.
- Please read it in its entirety.

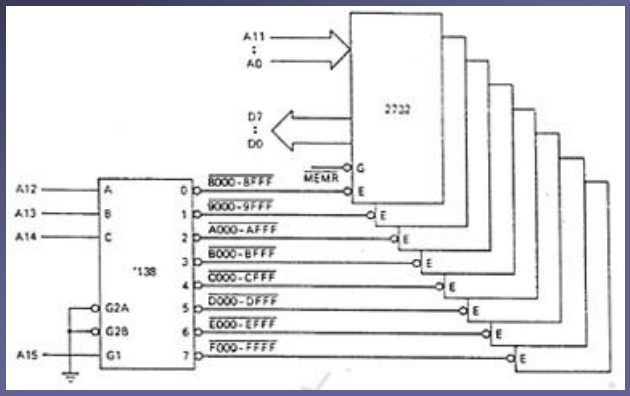
Documents you should have

- Syllabus
- Schedule
- Lecture 1 Notes
- Lecture 2 Notes
- ISM Errata
- WIMP 51 handout

Extra credit opportunity

- Get 5 (out of total 100 points)
- Come to my office (EECH219) during office hours to have your picture taken

32K memory system



Question 4

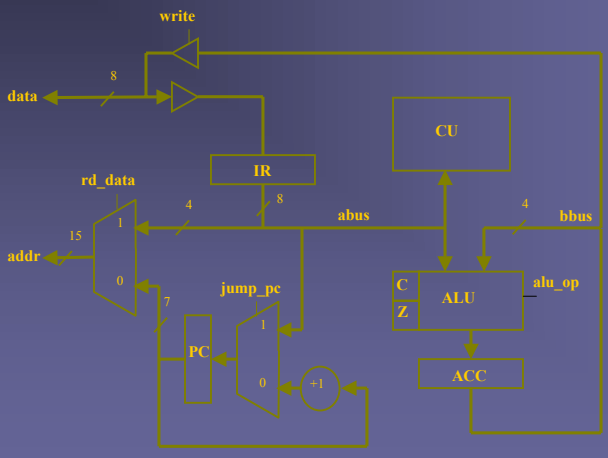
- What is the usual meaning of “16-bit” in the phrase “16-bit computer”?

  “16-bit computer” refers to the fact the size of the data bus of the CPU is 16 lines wide.

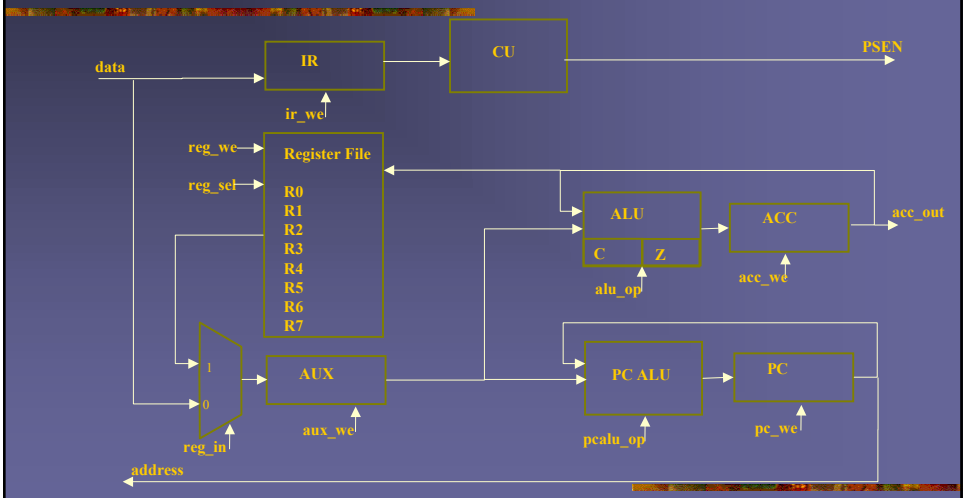
Intro to computer organization

- Most processors today are von Neuman
  - single locus of execution
  - program and data in same storage
- Use a non-commercial 4 bit machine- GNOME2
  - Simple instruction set - 16 vs 8051's 255
  - Accumulator based architecture - like 8051
  - No input/output subsystem
  - Easy to construct from scratch in an FPGA

GNOME2 Microprocessor

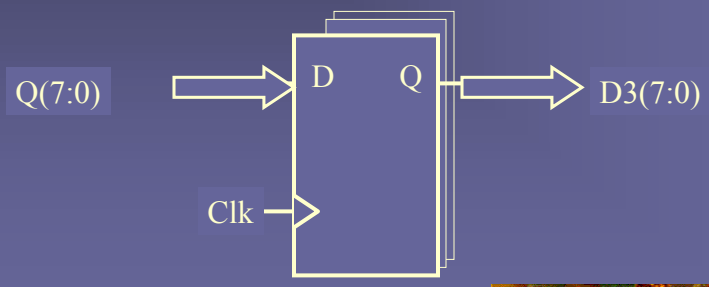


Wimp51 Microprocessor

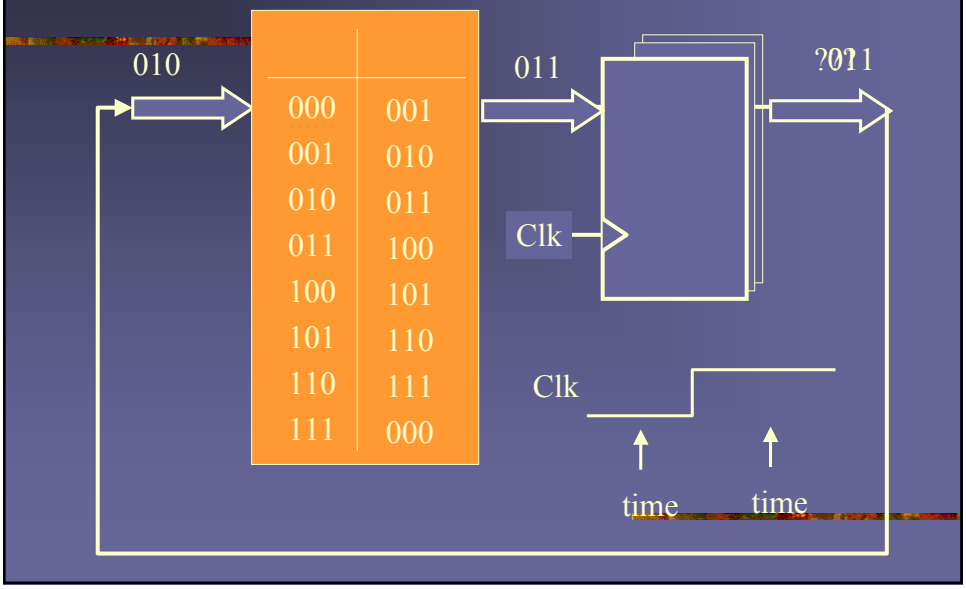


Register = array of flip flops

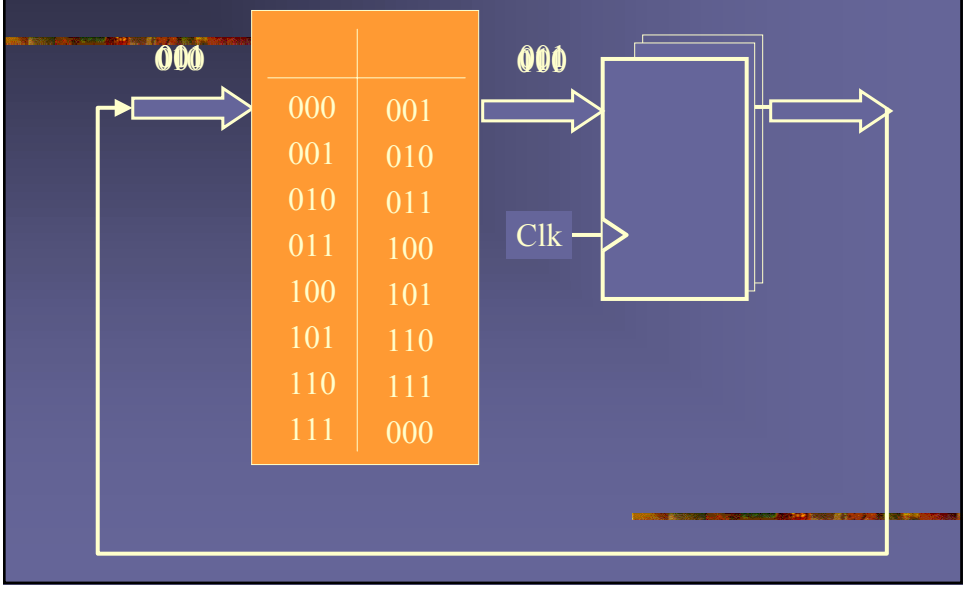
- Stack 8 flip flops to get 8 bit data register
- Strobe Clk to get D3 <= Q;



Register + Logic = State machine



A counter!

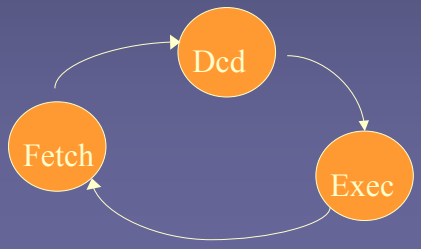


Wimp51 subsystems

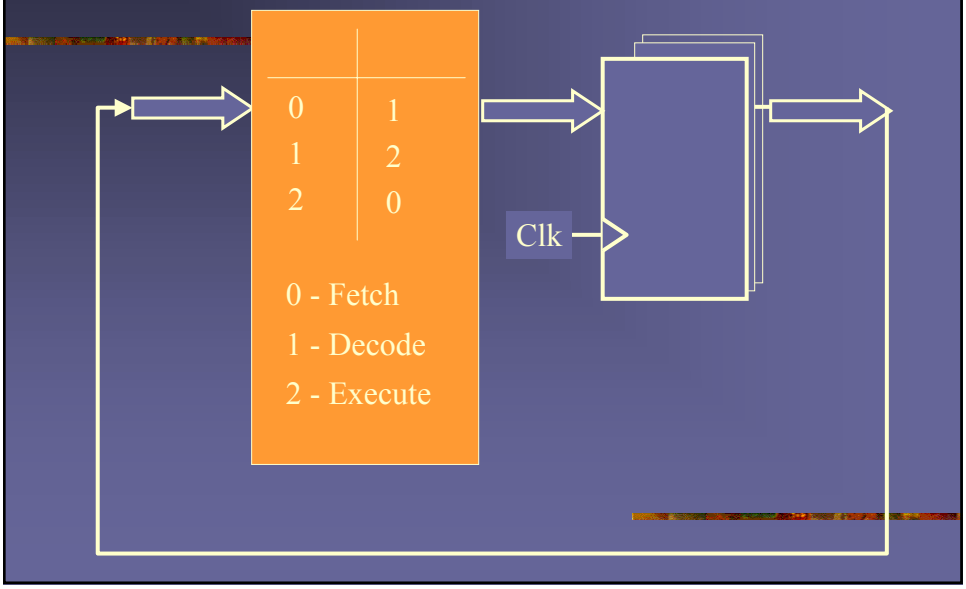
- PC is an eight bit counter, 0 to 255
- AUX reg can be added to PC for jump instr
- ACC and ALU form a ‘register with logic’ block
- IR and memory form a ‘register with logic’ block
- Control Unit (CU) is a 2 bit counter, 0 to 2
- Datapath = IR, AUX, PC, ACC, Regfile, ALU, PCALU
  - 12 registers plus Logic (ALU, PCALU)

Wimp51 control unit

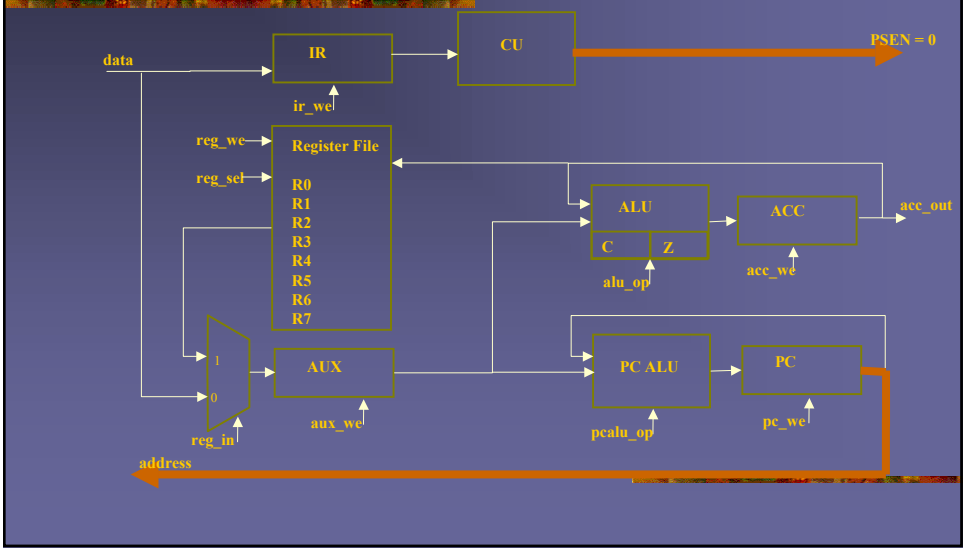
- Simple state machine
- Fetch/Decode/Execute states
- Each state takes one clock cycle
- A complete loop is an instruction cycle



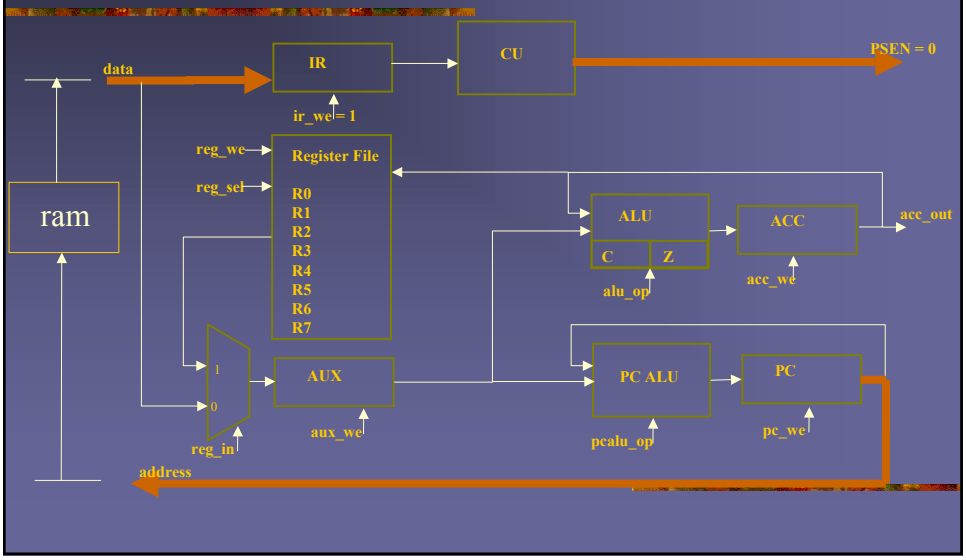
Wimp51 control unit



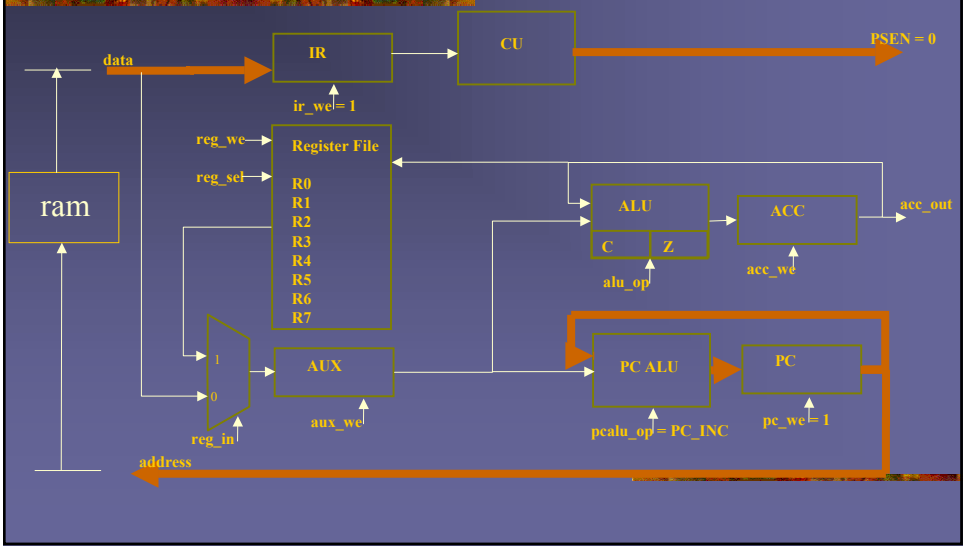
Fetch cycle step 1: addr <= PC



Fetch cycle step 2: IR<= data



Fetch cycle: PC<= PC+1



Before the next lecture

- Review WIMP handout
- Finalize four partners that you will work with for the rest of the semester
- Answer questions from WIMP handouts
- Bring your answers to class for discussion