CpE 111 -- Introduction to Computer Engineering

Section B, Fall 1999 **Class Hours:** MWF 1130-1220 **Class Room:** 101 EECH

Instructor: Dr. A. Miller

Office: 125 EECH
Office Hours: MWF 1000-1115
MW 1400-1500
Other times by appointment

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Prerequisites: CSc 53, CSc 73 or CSc 74. Students should enroll in CpE 111 and CpE 112 simultaneously. Prerequisites by topic: basic programming background and elementary circuit concepts as obtained in a physics course.

Text: Uyemura, A First Course in Digital Systems Design: An Integrated Approach, Brooks/Cole Publishing, 1999

Goals: To introduce: modern logic and state machine concepts, problem solving and design principles, vocabulary and philosophy of the digital world.

Schedule and Reading Assignments:

Introduction and Concepts in Digital Systems	Chapter 1
Boolean Algebra and Logic Gates	Chapter 2
Combinational Logic Design	Chapter 3
Exam 1	**FRI, 17 Sep 1999**
Digital Hardware	Chapter 4
First Concepts in VHDL	Chapter 5
CMOS Logic Circuits (selected topics)	Chapter 6: 6.1 through 6.5
Silicon Chips and VLSI (selected topics)	Chapter 7: 7.1, 7.2, 7.3, 7.6
Exam 2	**WED, 20 Oct 1999**
Logic Components	Chapter 8
Memory Elements and Arrays	Chapter 9
Exam 3	**FRI, 19 Nov 1999**
Sequential Logic Networks	Chapter 10
	Review
Final Exam	**TUES, 14 Dec 1999**

Grading:	3 exams @ 100 points each*	300 pts (50%)
	11 assignments @ 10 points each**	100 pts (16.7%)
	final exam	200 pts (33.3%)

* Attendance on the day of the exam is expected.

** Homework assignments will be due BY END OF CLASSTIME every Wednesday, except WK01, WK04 (exam#1), WK09 (exam#2),WK13 (exam#3), and WK14 (Thanksgiving), Lowest homework grade will be dropped. Homework will be selected problems from the text which will be announced no later than the Friday of the previous week and which will be posted outside of 125 EECH.

For both exams and homework problems, for partial credit to be awarded, work/derivation must be shown.