CpE311 – Test I, W03

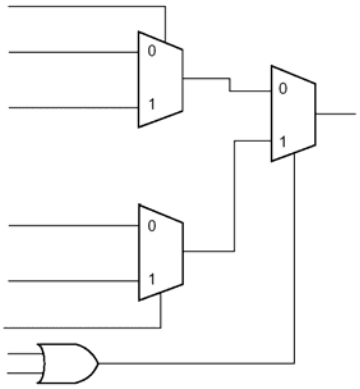
Name _____

Show all your work in the space provided. Answers with a simple "yes", "no", or a single number are typically incomplete and will not be given full credit. Answers in non-reduced form, like (a+sqrt(b))/c, are fine where appropriate. Good English on essay/short answer questions is required. ON MULTIPLE CHOICE QUESTIONS, IF YOU'RE NOT SURE GUESS CAREFULLY– you will get points off for wrong answers. If you know part of an answer, write what you know for partial credit.

1. (20 Points) Implement the following logic using ACT1 logic modules:

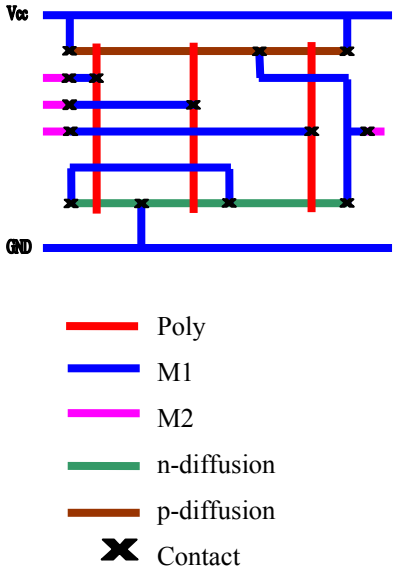
   Z <= not (A and (B or C));

   Only A, B, and C are available (not their complements). Try to use as few modules as possible. Show your work. One module is given for you. (Note: a bit tricky).



2. (15 Points) In a few sentences, explain whether one should use an NFET or a PFET as a pull-up or pull-down and explain why. Your explanation why is worth the most points and must be in your own words. Please use space provided.

3. (15 Points) A stick diagram is shown on the overhead projector for a CMOS logic gate. Draw the circuit diagram for the gate. Label all inputs and outputs… (I have not given them names). (The diagram is also shown below but is not in color)



4. (15 Points) What is the most significant factor in the cost of an IC design? Explain. If you think you might be wrong, point out other factors that are close. Please use space provided.

5. (15 Points) Following are some short segments of VHDL code. Mark each one as GOOD code or BAD code. Good code is code that is efficient (no un-necessary components, delays), will compile, synthesize, and work. Bad code is code that is not good. If code is bad, explain why completely. If you're not sure, assume it is probably bad and give your explanation.

a) Assume a, b, c, and clk are all signals of type bit:

```
process is
begin
     b <= a;
     wait until clk='1';
     b <= c;
     wait on a;
end process;
```

b)

Assume:

```
use IEEE.std_logic_arith.all;
signal d,e: unsigned(3 downto 0);
signal out1,out2: unsigned(7 downto 0);
```

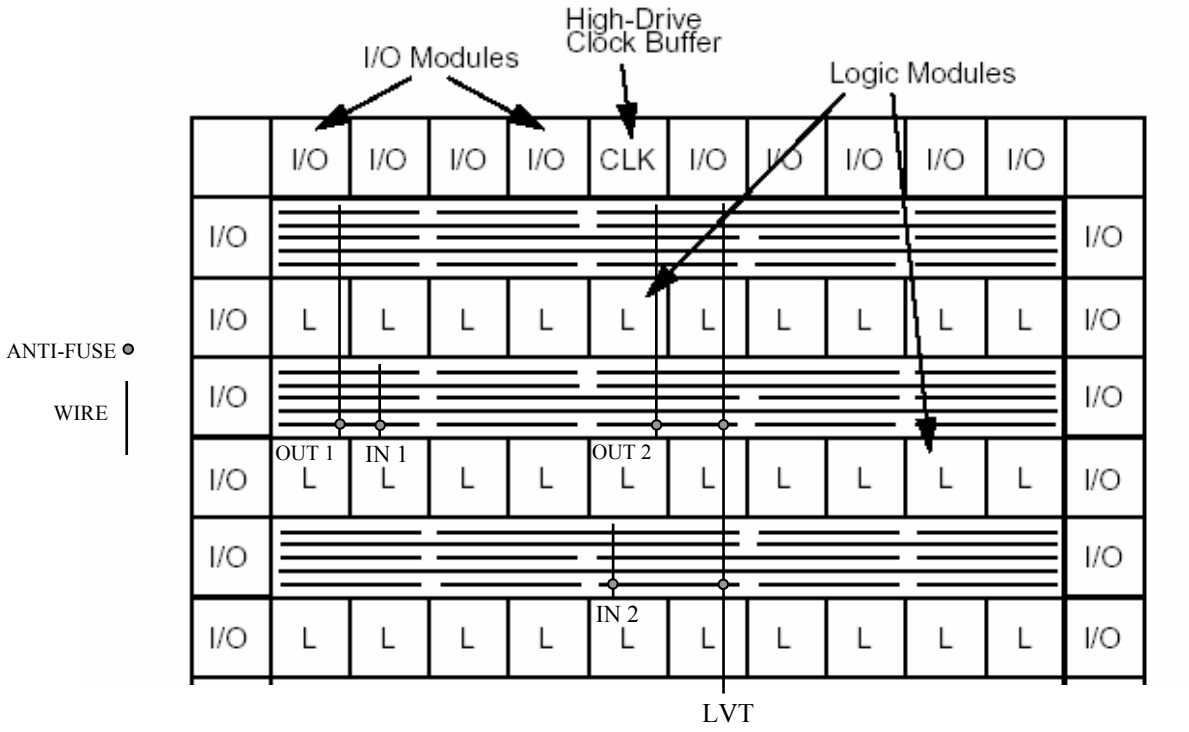
for this code segment:

```
process (d,e)
begin
    if (d*e > 42) then
        out1 <= d*e;
    else
        out2 <= d*e;
    end if;
end process;
```

c) Assume a and Q are of type std_logic and the following implements a D latch (not a flip-flop).

```
D_latch: process (clk) is
begin
    if (clk = '1') then
        Q <= a;
    end if;
end process;
```

6. (20 Points) Two different circuits were synthesized in an ACT1 logic module as shown below. Out1 connects to In1 through a minimum-length segment of horizontal interconnect. Out2 connects to In2 through two minimum-length segments of horizontal interconnect and a long vertical track. By what factor is circuit 1 (with out1 and In1) faster than circuit 2 (with out2 and in2).



a) (10 points) Draw an equivalent RC network between out1 and in1 and between out2 and in2. Mark the approximate size of resistors or capacitors where appropriate. Clearly label where the logic modules connect to the circuit in your diagram.

b) (10 points) Calculate the factor that circuit 1 is faster than circuit 2.