CpE 313 Spring 2004
Microprocessor System Design
Final Exam

May 12, 2004

Instructions

Read each individual problem appearing on this exam carefully and do only what is specifically stated.

This exam is designed to be completed by a well-prepared student in approximately **120 minutes**; most students are expected to finish it within the allotted time. On your initial pass through this exam, skip any problems that appear to be overly difficult.

IMPORTANT: Put down your initials at the TOP of EACH page. Also, be sure to read and sign the Academic Honesty Statement that follows:
"In signing this statement, I hereby certify that the work on this exam is my own and that I have not copied the work of any other student while completing this exam. I understand that, if I fail to honor this agreement, I will receive a score of ZERO for this exam and will be subject to possible disciplinary action."

Printed Name: ..... **Signature:** .....

Date: .....

DO NOT BEGIN UNTIL INSTRUCTED TO DO SO.

Problem 1 – Performance Measurement ..... 10 Points

The table below shows average instruction frequency for a benchmark when compiled for a particular microprocessor.

Table 1: Instruction frequency for the benchmark

instruction	frequency
load	10.4
store	36.2
add	16.7
sub	2.5
miscellanious ALU	17.5
cond branch	10.9
jump	3.6
call	1.1
return	1.1

Suppose we have made the following measurements about the CPI for instructions.

Table 2: The microprocessor's CPI's for different instructions

instruction	clock cycles			
all ALU instructions	1.0			
loads	4			
stores	1.8			
cond branches	3			
uncond branches	2			

1a) Calculate the average CPI for the benchmark. Use a blank column in Table 2 to put your results.

1b) Calculate the percentage of the benchmark execution time that is spent in each category shown in Table 2.

Problem 2 – Pipelining ..... 10 Points

A particular compiler has been charged with the task of producing an optimized version of the benchmark given in Problem 1.

2a) Write down a sequence of two or three assembly language instructions to demonstrate a RAW hazard that a compiler can avoid.

2b) Write down a sequence of two or three assembly language instructions to demonstrate a RAW hazard that a compiler *cannot* avoid.

Problem 3 – Caches ..... 10 Points

A microprocessor has a 64 KB 4-way virtually indexed physically tagged data cache. The page size for the system is 16KB, and block size is 32B. B stands for "bytes."

3a) Determine the number of page offset bits.

3b) Determine the number of block offset bits.

3c) Determine the number of cache index bits.

3d) Would this cache exhibit the synonym problem?

Problem 4 – Tomasulo's Algorithm ..... 10 Points

Consider the instruction sequence given below. These instructions are to be executed by a dynamically scheduled single-issue pipeline that is managed by Tomasulo's algorithm.

```
div F2, F1, F4
or F6, F2, F4
and F4, F3, F1
```

Assume that instruction `div F2, F1, F4` is already being executed during clock cycle x, and will finish execution at the end of clock cycle $x + 10$.

4a) Will `or` be fetched in clock cycle $x + 1$? If yes, will `or` be issued in clock cycle $x + 2$? *Explain* your answers.

4b) Describe the state of `and` at the end of clock cycles $x + 2$ to $x + 8$? Assume `and` takes 2 cycles of execution.

Problem 5 – Miscellaneous Part 1 ..... 20 Points

What is the purpose of:

5a) a re-order buffer?

5b) a page table?

5c) a translation look-aside buffer?

5d) the dual set of cache tags on some multiprocessor caches?

Problem 6 – Miscellaneous Part 2 ..... 20 Points

What is the purpose of:

6a) a write buffer?

6b) a write-back buffer?

6c) a branch prediction buffer?

6d) a branch target buffer?

Problem 7 – Miscellaneous Part 3 ..... 20 Points

What is the purpose of:

7a) synonym alignment?

7b) the PID or ASN field in some TLBs?

7c) the reservation stations in a dynamically scheduled single-issue pipeline that is managed by Tomasulo's algorithm?

7d) enforcing object alignment?