CpE 318 HW#4 (due 4/06/04) (13 points)

[1] 1) Calculate the TPC for the AVG_of_N module described and shown below (show TPC diagram).

The AVG_of_N module repeats the following indefinitely:
i) read a block of N+1 bytes from port X: N, B_1, B_2, …, B_N
ii) output the average of the bytes read, rounded to the nearest whole number

2) Redesign the AVG_of_N module such that it achieves optimal throughput.

[2] a) Show revised datapath.

[2] b) Show revised ASM.

[1] c) Calculate TPC for revised design (show TPC diagram).

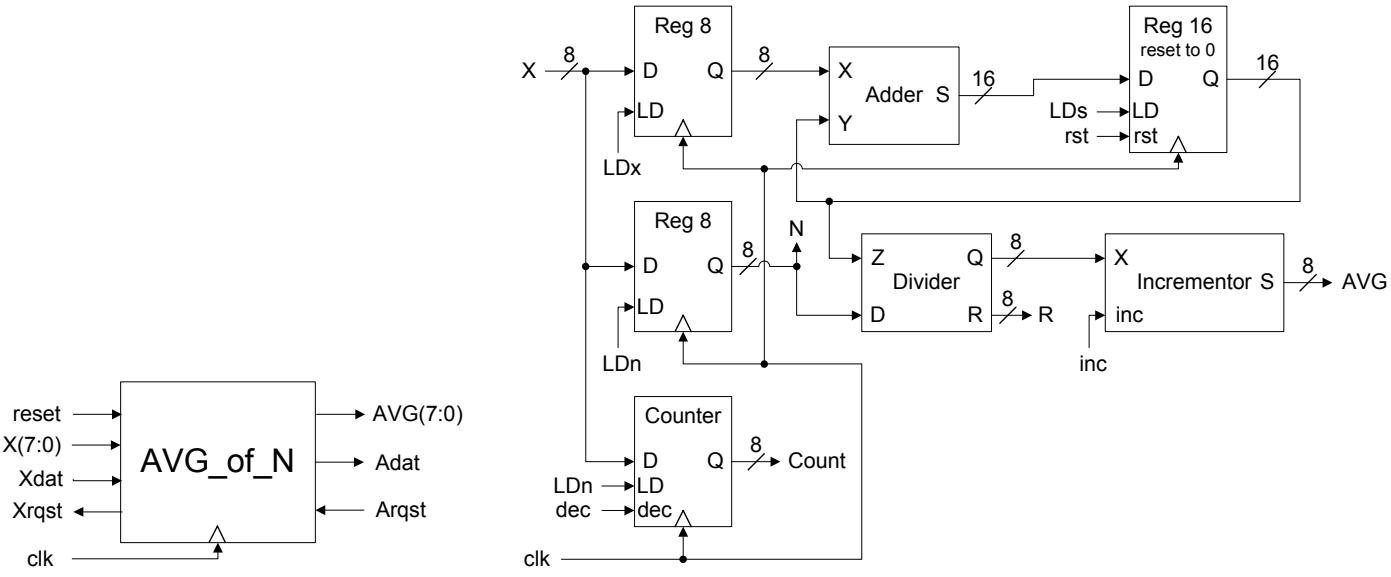
[2] d) Derive optimized next-state and output equations.

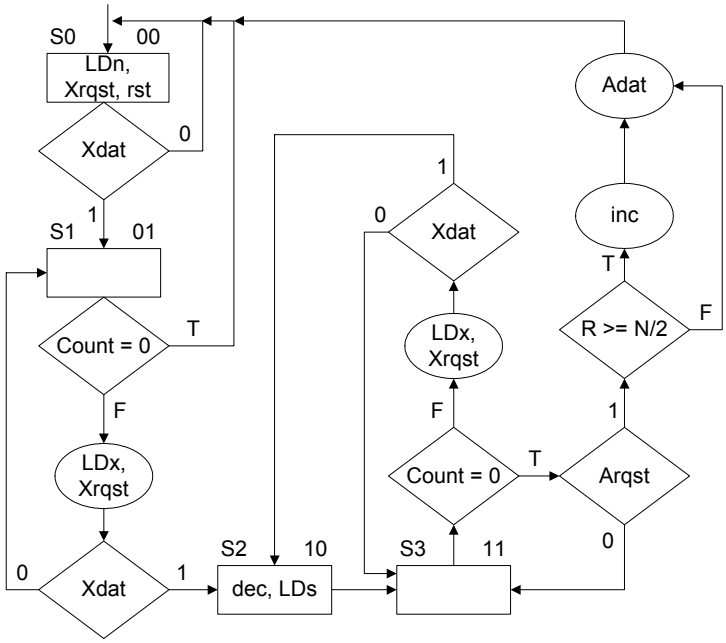
[2] e) Write synthesizable behavioral VHDL description (turn in VHDL code).

[2] f) Write exhaustive testbench and macro, then simulate and explain simulation (turn in VHDL testbench, macro, and simulation waveforms with explanation).

[1] g) Synthesize the VHDL model and simulate the synthesized design (turn in synthesized code, not including the primitives, and simulation waveforms with explanation).

- use a synchronous reset, positive edge-triggered flip-flops, and a clock period of 50 ns.
- change inputs on the falling edge of the clock




S0
00
LDn,
Xrqst, rst
Xdat
0
1
S1
01
Count = 0
T
F
LDx,
Xrqst
0
Xdat
1
S2
10
dec, LDs
S3
11
1
0
Xdat
LDx,
Xrqst
F
Count = 0
T
Arqst
1
0
R >= N/2
F
T
inc
Adat