Jesse Lu
12/6/99
Sec J

EE 112, Section J
Final Practical Exam

12 / 06 / 1999.
Points 100

103/100

Part 1: (60 Points)

A: Using Karnaugh maps, design a minimal circuit to implement the function described by the following truth table:

A	B	C	Output
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(~ represents inversion)

	~B~C	~BC	BC	B~C
~A	1		1	
A	1			1

$\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$

not a minimal function

-2

Design the circuit in Design Architect. Make sure your circuit has all the components necessary to compile a BIT file.

B: Simulate your design. Make sure to simulate all possible input states.
Print out your circuit(top level design and bottom level design), a waveform showing your simulation, and a list showing your simulation.

C: Place 'patgen' in your design and create a BIT file for your design. Print out the ".par" file associated with the design. The ".par" file will be in this directory "'your design name'/xproj/".

D: Verify your simulation results to match the equation given above.

Look at List sheet

Part 2: (40 Points)

A: Hook the scope up to watch the circuit function. Pins 3, 4, and 5 are probe points for the input to the logic function of the circuit in question. (These signals are generated on the board.) Pin 6 is the output of the logic function.

B: Download "final.bit" into the proto-board and adjust the scope to obtain a stable trace of the four signals. Label the signals appropriately.

C: From the output waveforms determine the logic function being implemented by the circuit in question.

D: Minimize the logic function using Karnaugh maps. (Bonus Points 5

		00 ~B~C	01 ~BC	11 BC	10 B~C
0	~A		1		1
1	A		1	1	

Part D

method 1

$O = \bar{B}C + AC + \bar{A}B\bar{C}$ ✓ +5

~~$O = BC + B(A+C)$~~ ~~method 2~~

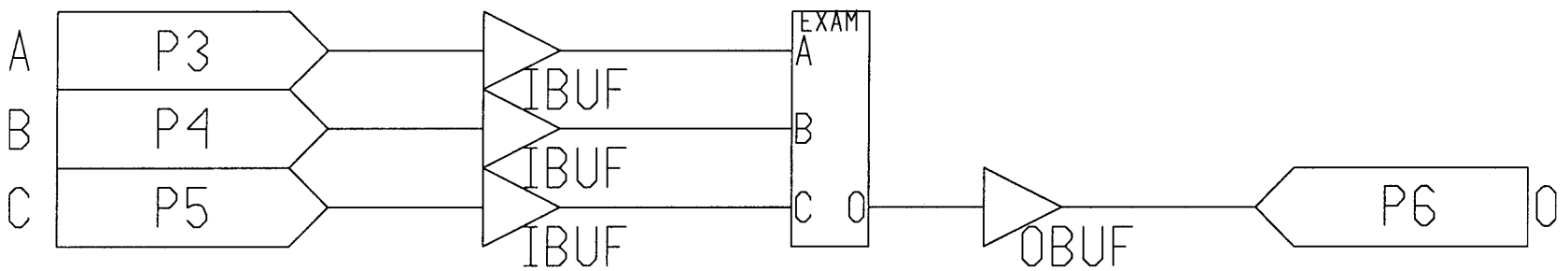
A B C	O	Check
0 0 0	0	0
0 0 1	1	1
0 1 0	1	1
0 1 1	0	0
1 0 0	0	0
1 0 1	1	1
1 1 0	0	0
1 1 1	1	1 ✓

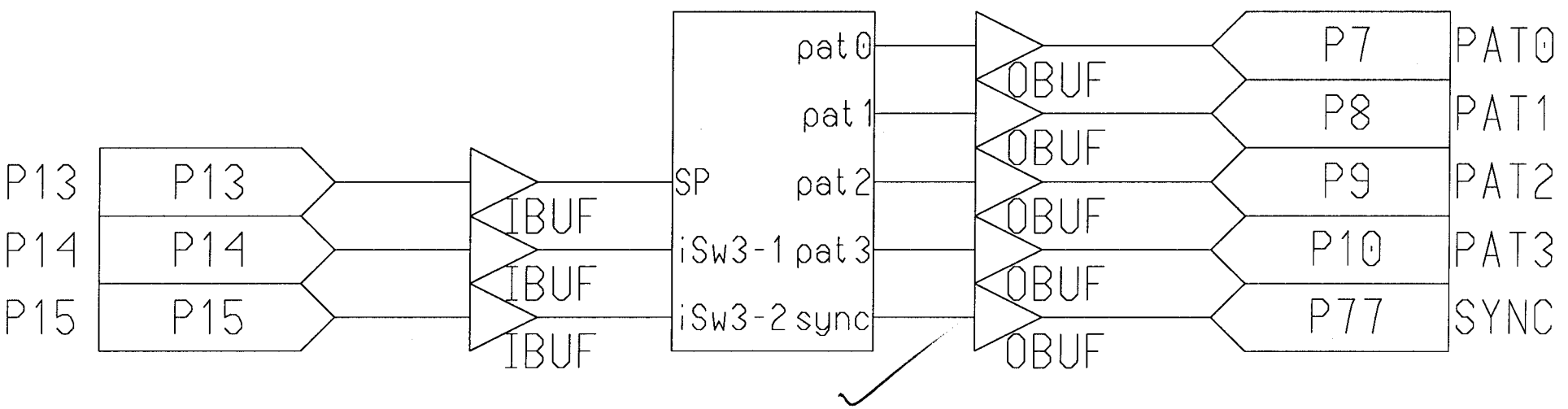
$\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + ABC$

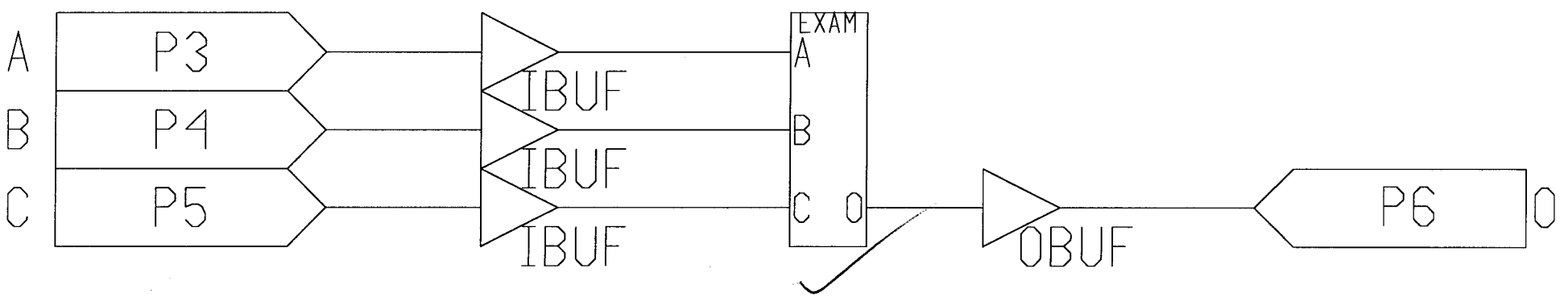
Part C

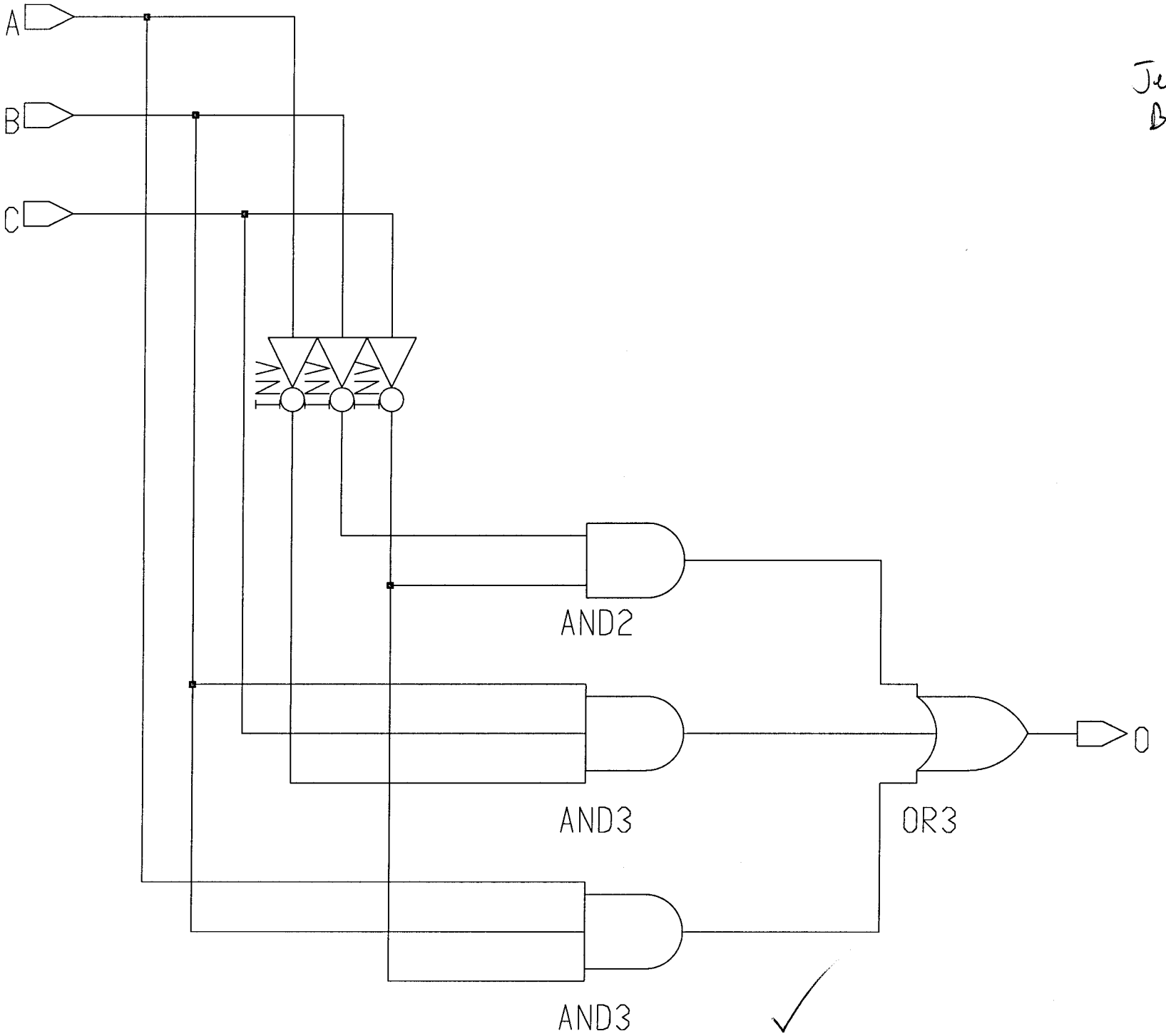
$O = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + ABC$ ✓

Jesse Lai


A
B
C
P3
P4
P5
IBUF
IBUF
IBUF
EXAM
A
B
C
O
OBUF
P6
O


P13
P14
P15
P13
P14
P15
IBUF
IBUF
IBUF
SP
iSw3-1
iSw3-2
pat 0
pat 1
pat 2
pat 3
sync
OBUF
OBUF
OBUF
OBUF
OBUF
P7
P8
P9
P10
P77
PAT0
PAT1
PAT2
PAT3
SYNC


A
B
C
P3
P4
P5
IBUF
IBUF
IBUF
EXAM
A
B
C
O
OBUF
P6
O



Jess Lai
Bottom Level Design

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List Output

```
      0.0 0   0   0   Xr
      0.1 0   0   0   X
      0.5 0   0   0   1  ->
    100.0 0   0   1   1
    100.5 0   0   1   0  ->
    200.0 0   1   0   0  ->
    300.0 0   1   1   0
    300.4 0   1   1   1  ->
    400.0 1   0   0   1
    400.4 1   0   0   0
    400.5 1   0   0   1  ->
    500.0 1   0   1   1
    500.5 1   0   1   0  ->
    600.0 1   1   0   0
    600.5 1   1   0   1  ->
    700.0 1   1   1   1
    700.5 1   1   1   0  ->
Time(ns) ^/A   ^/C
           ^/B   ^/O
```

I looked at this list output + compared it to the expected results

A	B	C	O
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

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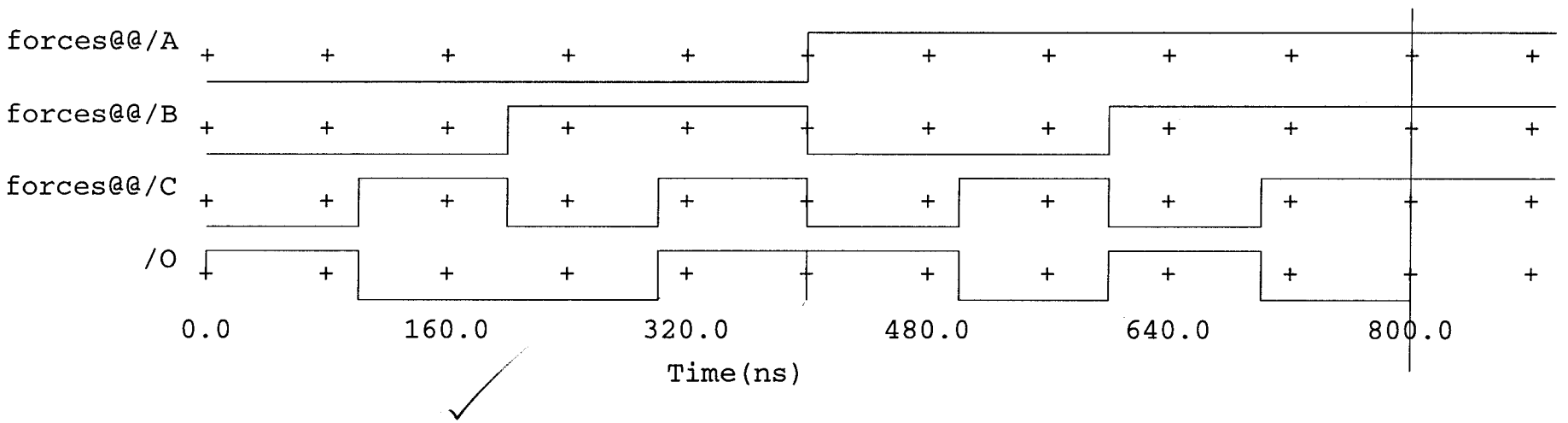
Trace Output



```
PAR: Xilinx Place And Route M1.5.25.
Copyright (c) 1995-1998 Xilinx, Inc.  All rights reserved.

Mon Dec  6 17:08:58 1999

/usr/local/xilinx.15i/bin/sol/par -w -ol 2 -d 0 map.ncd exam_2.ncd exam_2.pcf


Constraints file: exam_2.pcf

Loading device database for application par from file "map.ncd".
   "exam_2" is an NCD, version 2.27, device xc4005e, package pc84, speed -1
Loading device for application par from file '4005e.nph' in environment
/usr/local/xilinx.15i.
Device speed data version:  x1_0.96  PRELIMINARY.


Resolved that IOB <A> must be placed at site P3.
   Place IOB A in site P3.
Resolved that IOB <B> must be placed at site P4.
   Place IOB B in site P4.
Resolved that IOB <C> must be placed at site P5.
   Place IOB C in site P5.
Resolved that IOB <O> must be placed at site P6.
   Place IOB O in site P6.
Resolved that IOB <P13> must be placed at site P13.
   Place IOB P13 in site P13.
Resolved that IOB <P14> must be placed at site P14.
   Place IOB P14 in site P14.
Resolved that IOB <P15> must be placed at site P15.
   Place IOB P15 in site P15.
Resolved that IOB <PAT0> must be placed at site P7.
   Place IOB PAT0 in site P7.
Resolved that IOB <PAT1> must be placed at site P8.
   Place IOB PAT1 in site P8.
Resolved that IOB <PAT2> must be placed at site P9.
   Place IOB PAT2 in site P9.
Resolved that IOB <PAT3> must be placed at site P10.
   Place IOB PAT3 in site P10.
Resolved that IOB <SYNC> must be placed at site P77.
   Place IOB SYNC in site P77.


Device utilization summary:

   Number of External IOBs           12 out of 61     19%
      Flops:                          0
      Latches:                        0

   Number of CLBs                     5 out of 196     2%
      Total CLB Flops:                4 out of 392     1%
      4 input LUTs:                   8 out of 392     2%
      3 input LUTs:                   1 out of 196     1%

   Number of OSCILLATORs              1 out of 1     100%



Overall effort level (-ol):   2 (set by user)
Placer effort level (-pl):    2 (default)
```

```
Placer cost table entry (-t): 1
Router effort level (-rl):    2 (default)

Starting initial Placement phase.  REAL time: 23 secs
Finished initial Placement phase.  REAL time: 24 secs

Starting Constructive Placer.  REAL time: 25 secs
Finished Constructive Placer.  REAL time: 25 secs

Writing design to file "exam_2.ncd".

Starting Optimizing Placer.  REAL time: 25 secs
Optimizing
Swapped 79 comps.
Xilinx Placer [1]   5940   REAL time: 26 secs

Finished Optimizing Placer.  REAL time: 26 secs

Writing design to file "exam_2.ncd".

Total REAL time to Placer completion: 26 secs
Total CPU time to Placer completion: 19 secs

0 connection(s) routed; 38 unrouted.
Starting router resource preassignment
Completed router resource preassignment. REAL time: 27 secs
Starting iterative routing.
Routing active signals.
End of iteration 1
38 successful; 0 unrouted; (0) REAL time: 27 secs
Constraints are met.
Routing PWR/GND nets.
Power and ground nets completely routed.
Writing design to file "exam_2.ncd".
Starting cleanup
Improving routing.
End of cleanup iteration 1
38 successful; 0 unrouted; (0) REAL time: 31 secs
Writing design to file "exam_2.ncd".
Total REAL time: 32 secs
Total CPU  time: 23 secs
End of route.  38 routed (100.00%); 0 unrouted.
No errors found.
Completely routed.

This design was run without timing constraints.  It is likely that much better
circuit performance can be obtained by trying either or both of the following:

  - Enabling the Delay Based Cleanup router pass, if not already enabled
  - Supplying timing constraints in the input design


Total REAL time to Router completion: 32 secs
Total CPU time to Router completion: 24 secs

Generating PAR statistics.

   The Delay Summary Report

   The Score for this design is: 201
```

The Number of signals not completely routed for this design is: 0

The Average Connection Delay for this design is:	1.531 ns
The Average Connection Delay on critical nets is:	0.000 ns
The Average Clock Skew for this design is:	0.270 ns
The Maximum Pin Delay is:	3.621 ns
The Average Connection Delay on the 10 Worst Nets is:	2.424 ns

Listing Pin Delays by value: (ns)

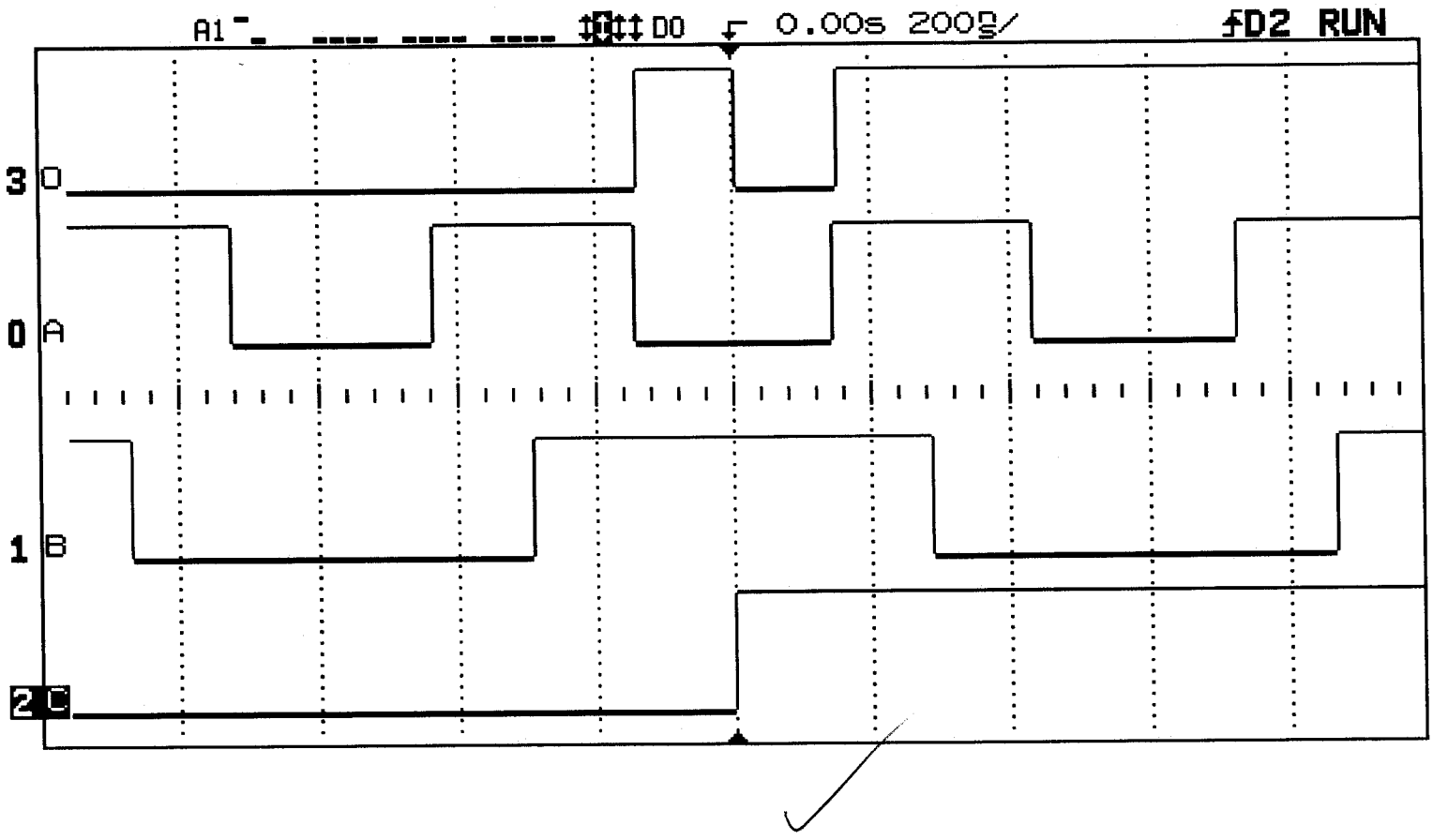
d <= 10	< d <= 20	< d <= 30	< d <= 40	< d <= 50	d > 50
38	0	0	0	0	0

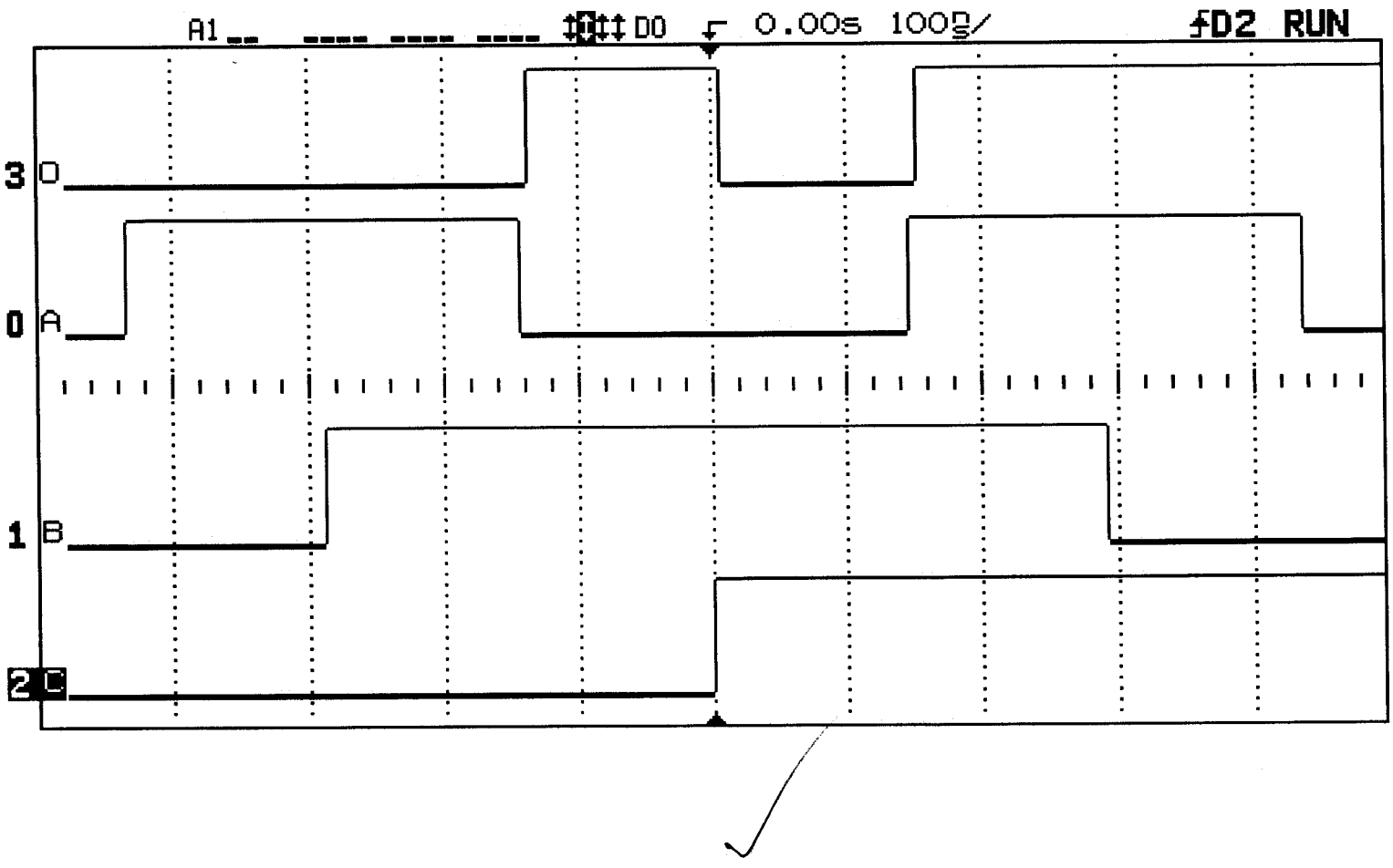
Writing design to file "exam_2.ncd".

All signals are completely routed.

Total REAL time to PAR completion: 35 secs
Total CPU time to PAR completion: 26 secs

PAR done.


A1
D0
0.00s 200g/
D2 RUN
3 D
0 A
1 B
2 C


A1
D0
0.00s
100
D2 RUN
3 D
0 A
1 B
2 C