CpE 318 HW#1 (due 1/29/04) (12 points)

For the following truth table:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

[1] A) Derive *F* in simplified SOP form.
[1] B) Draw the simplified logic diagram of *F* using only AND, OR, and INV gates.
[1] C) Write a dataflow VHDL description of *F*.
[1] D) Write a structural VHDL description of *F*.
[1] E) Write a behavioral VHDL description of *F*, including the case where if any input is 'U' then *F* = 'U'.
[1] F) Write an exhaustive testbench for *F*, including an *incorrect* signal, with a 10 ns time step between input vectors (include a testcase where all inputs are 'U').
[1] G) Write a macro to trace all inputs, the output, and *incorrect*, and run the simulation.
[3] H) Turn in 3 waveforms, one each for the dataflow, structural, and behavioral models.
[1] I) What is the difference in the output between the behavioral and the dataflow models? Explain why. (Hint: this occurs when some inputs are 'U', but not all).
[1] J) What would be the worse-case path delay of the structural description in terms of *ns* if the following components were used?

Entity Name	Input Names	Output Names	Description	Delay (ns)
INV	A	Z	inverter	1
OR2	A, B	Z	2-input OR	2
OR3	A, B, C	Z	3-input OR	3
OR4	A, B, C, D	Z	4-input OR	4
AND2	A, B	Z	2-input AND	2
AND3	A, B, C	Z	3-input AND	3
AND4	A, B, C, D	Z	4-input AND	4