Solution to Homework 10, CpE 313 – Fall 2004

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Solution to Homework 10 – Question 1

- Please complete the Tomasulo's algorithm work sheets in this handout for:
- 1) CC 1--CC 8,
  2) CC 10--CC11,
  3) CC15--CC16, and
  4) CC56--CC57.
- **This HW is due in class on Tuesday Nov 2, 2004.**

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Homework 10 – Question 1

- assume
  - floating point add/sub take 2 cycles of **execution**
  - floating point mult takes 10 cycles of **execution**
  - load takes 2 cycles of **execution**
  - floating point divide takes 40 cycles of **execution**
  - three FP adder units, two mult units (mult also does divide)
  - two load units (store units not discussed in this example)
- in following slides,
  - Vj = value of source operand 1
  - Vk = value of source operand 2
  - Qj = for a pending op, this is # of the RS which will produce Vj
  - Qk = for a pending op, this is # of the RS which will produce Vk

3

finishing times

Instruction	j	k
LD F6	34	R2
LD F2	45	R3
MULTD F0	F2	F4
SUBD F8	F6	F2
DIVD F10	F0	F6
ADDD F6	F8	F2

IS	RPO	EXE	WR
1	1		

Tag or Q is allocated to an instruction **and** reg file by the issue logic.

CC 1

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	No					
Load1	3	Yes	load	34	50	0	0
Load2	4	No					
Add3	5	No					
Mult1	6	No					
Mult2	7	No					

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	0	18
2	0	32
4	0	56
6	3	
8	0	98
10	0	66

4

finishing times

Instruction	j	k
LD F6	34	R2
LD F2	45	R3
MULTD F0	F2	F4
SUBD F8	F6	F2
DIVD F10	F0	F6
ADDD F6	F8	F2

IS	RPO	EXE	WR
1	1		
2	2		

CC 2

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	No					
Load1	3	Yes	load	34	50	0	0
Load2	4	Yes	load	45	100	0	0
Add3	5	No					
Mult1	6	No					
Mult2	7	No					

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	0	18
2	4	
4	0	56
6	3	
8	0	98
10	0	66

5

finishing times

Instruction	j	k
LD F6	34	R2
LD F2	45	R3
MULTD F0	F2	F4
SUBD F8	F6	F2
DIVD F10	F0	F6
ADDD F6	F8	F2

IS	RPO	EXE	WR
1	1	3	
2	2		
3			

CC 3

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	No					
Load1	3	Yes	load	34	50	0	0
Load2	4	Yes	load	45	100	0	0
Add3	5	No					
Mult1	6	Yes	mult		56	4	0
Mult2	7	No					

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	4	
4	0	56
6	3	
8	0	98
10	0	66

6

Instruction		j	k
LD	F6	34	R2
LD	F2	45	R3
MULTD	F0	F2	F4
SUBD	F8	F6	F2
DIVD	F10	F0	F6
ADDD	F6	F8	F2

finishing times

IS	RPO	EXE	WR
1	1	3	4
2	2	4	
3			
4			

Tag or Q is de-allocated when an instruction completes.

CC 4

assume mem[34+R2] = 84

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	Yes	sub	84		0	4
Add2	2	No					
Load1	3	No					
Load2	4	Yes	load	45	100	0	0
Add3	5	No					
Mult1	6	Yes	mult		56	4	0
Mult2	7	No					

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	4	
4	0	56
6	0	84
8	1	
10	0	66

7

Instruction		j	k
LD	F6	34	R2
LD	F2	45	R3
MULTD	F0	F2	F4
SUBD	F8	F6	F2
DIVD	F10	F0	F6
ADDD	F6	F8	F2

finishing times

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5		
4	5		
5			

CC 5

assume mem[45+R3] = 42

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	Yes	sub	84	42	0	0
Add2	2	No					
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	Yes	mult	42	56	0	0
Mult2	7	Yes	divd		84	6	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	0	42
4	0	56
6	0	84
8	1	
10	7	

8

finishing times

Instruction		j	k
LD	F6	34	R2
LD	F2	45	R3
MULTD	F0	F2	F4
SUBD	F8	F6	F2
DIVD	F10	F0	F6
ADDD	F6	F8	F2

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5		
4	5		
5			
6			

CC 6

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	Yes	sub	84	42	0	0
Add2	2	Yes	add		42	1	0
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	Yes	mult	42	56	0	0
Mult2	7	Yes	divd		84	6	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	0	42
4	0	56
6	2	
8	1	
10	7	

9

finishing times

Instruction		j	k
LD	F6	34	R2
LD	F2	45	R3
MULTD	F0	F2	F4
SUBD	F8	F6	F2
DIVD	F10	F0	F6
ADDD	F6	F8	F2

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5		
4	5	7	
5			
6			

CC 7

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	Yes	sub	84	42	0	0
Add2	2	Yes	add		42	1	0
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	Yes	mult	42	56	0	0
Mult2	7	Yes	divd		84	6	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	0	42
4	0	56
6	2	
8	1	
10	7	

10

finishing times

Instruction		j	k	IS	RPO	EXE	WR
LD	F6	34	R2	1	1	3	4
LD	F2	45	R3	2	2	4	5
MULTD	F0	F2	F4	3	5		
SUBD	F8	F6	F2	4	5	7	8
DIVD	F10	F0	F6	5			
ADDD	F6	F8	F2	6	8		

CC 8

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	Yes	add	42	42	0	0
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	Yes	mult	42	56	0	0
Mult2	7	Yes	divd		84	6	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	0	42
4	0	56
6	2	
8	0	42
10	7	

11

finishing times

Instruction		j	k	IS	RPO	EXE	WR
LD	F6	34	R2	1	1	3	4
LD	F2	45	R3	2	2	4	5
MULTD	F0	F2	F4	3	5		
SUBD	F8	F6	F2	4	5	7	8
DIVD	F10	F0	F6	5			
ADDD	F6	F8	F2	6	8	10	

CC 10

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	Yes	add	42	42	0	0
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	Yes	mult	42	56	0	0
Mult2	7	Yes	divd		84	6	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	0	42
4	0	56
6	2	
8	0	42
10	7	

12

finishing times

Instruction		j	k	IS	RPO	EXE	WR
LD	F6	34	R2	1	1	3	4
LD	F2	45	R3	2	2	4	5
MULTD	F0	F2	F4	3	5		
SUBD	F8	F6	F2	4	5	7	8
DIVD	F10	F0	F6	5			
ADDD	F6	F8	F2	6	8	10	11

CC 11

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	No					
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	Yes	mult	42	56	0	0
Mult2	7	Yes	divd		84	6	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	0	42
4	0	56
6	0	84
8	0	42
10	7	

13

finishing times

Instruction		j	k	IS	RPO	EXE	WR
LD	F6	34	R2	1	1	3	4
LD	F2	45	R3	2	2	4	5
MULTD	F0	F2	F4	3	5	15	
SUBD	F8	F6	F2	4	5	7	8
DIVD	F10	F0	F6	5			
ADDD	F6	F8	F2	6	8	10	11

CC 15

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	No					
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	Yes	mult	42	56	0	0
Mult2	7	Yes	divd		84	6	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	6	
2	0	42
4	0	56
6	0	84
8	0	42
10	7	

14

finishing times

Instruction		j	k
LD	F6	34	R2
LD	F2	45	R3
MULTD	F0	F2	F4
SUBD	F8	F6	F2
DIVD	F10	F0	F6
ADDD	F6	F8	F2

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5	15	16
4	5	7	8
5	16		
6	8	10	11

CC 16

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	No					
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	No					
Mult2	7	Yes	divd	23 52	84	0	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	0	2352
2	0	42
4	0	56
6	0	84
8	0	42
10	7	

15

finishing times

Instruction		j	k
LD	F6	34	R2
LD	F2	45	R3
MULTD	F0	F2	F4
SUBD	F8	F6	F2
DIVD	F10	F0	F6
ADDD	F6	F8	F2

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5	15	16
4	5	7	8
5	16	56	
6	8	10	11

CC 56

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk
Add1	1	No					
Add2	2	No					
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	No					
Mult2	7	Yes	divd	23 52	84	0	0

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	0	2352
2	0	42
4	0	56
6	0	84
8	0	42
10	7	

16

finishing times

Instruction	j	k	IS	RPO	EXE	WR
LD F6	34	R2	1	1	3	4
LD F2	45	R3	2	2	4	5
MULTD F0	F2	F4	3	5	15	16
SUBD F8	F6	F2	4	5	7	8
DIVD F10	F0	F6	5	16	56	57
ADDD F6	F8	F2	6	8	10	11

CC 57

RS	*RS Tag*	*Busy*	*Op*	*Vj*	*Vk*	*Qj*	*Qk*
Add1	1	No					
Add2	2	No					
Load1	3	No					
Load2	4	No					
Add3	5	No					
Mult1	6	No					
Mult2	7	No					

Integer Reg #	Q	V
1	0	213
2	0	50
3	0	100
4	0	417
5	0	87

FP Reg #	Q	V
0	0	2352
2	0	42
4	0	56
6	0	84
8	0	42
10	0	28

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Solution to Homework 10 – Question 2

- assume
  - add/sub take 2 cycles of **execution**
  - mult takes 10 cycles of **execution**
  - load takes 2 cycles of **execution**
  - store takes 2 cycles of **execution**
  - two adder units, two mult units
  - two load units, one store unit
- assume
  - mem[34+R2] = 4
  - mem[45+R2] = 5

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Tomasulo Example – Notation

- in following slides,
  - Vj = value of source operand 1
  - Vk = value of source operand 2
  - Qj = for a pending op, this is # of the RS which will produce Vj
  - Qk = for a pending op, this is # of the RS which will produce Vk

19

Instruction	j	k
LD R3	34	R2
LD R7	45	R2
MULTD R7	R7	R3
SUBD R1	R1	1
SD R7	21	R2
ADDD R2	R2	8

finishing times

IS	RPO	EXE	WR

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	n							
Add1	2	n							
Add2	3	n							
Mult1	4	n							
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	100
2	0	0
3	0	31
4	0	1000
5	0	2000
6	0	3000
7	0	49

20

finishing times

Instruction	j	k
LD R3	34	R2
LD R7	45	R2
MULTD R7	R7	R3
SUBD R1	R1	1
SD R7	21	R2
ADDD R2	R2	8

IS	RPO	EXE	WR
1	1		

CC 01

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	n							
Add1	2	n							
Add2	3	n							
Mult1	4	n							
Mult2	5	n							
Load1	6	y	ld	34	0	0	0		
Load2	7	n							

Integer Reg #	Q	V
1	0	100
2	0	0
3	6	
4	0	1000
5	0	2000
6	0	3000
7	0	49

21

finishing times

Instruction	j	k
LD R3	34	R2
LD R7	45	R2
MULTD R7	R7	R3
SUBD R1	R1	1
SD R7	21	R2
ADDD R2	R2	8

IS	RPO	EXE	WR
1	1		
2	2		

CC 02

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	n							
Add1	2	n							
Add2	3	n							
Mult1	4	n							
Mult2	5	n							
Load1	6	y	ld	34	0	0	0		
Load2	7	y	ld	45	0	0	0		

Integer Reg #	Q	V
1	0	100
2	0	0
3	6	
4	0	1000
5	0	2000
6	0	3000
7	7	

22

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	
2	2		
3			

CC 03

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	n							
Add1	2	n							
Add2	3	n							
Mult1	4	y	mul			7	6		
Mult2	5	n							
Load1	6	y	ld	34	0	0	0		
Load2	7	y	ld	45	0	0	0		

Integer Reg #	Q	V
1	0	100
2	0	0
3	6	
4	0	1000
5	0	2000
6	0	3000
7	4	

23

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	4
2	2	4	
3			
4	4		

CC 04

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	n							
Add1	2	y	sub	100	1	0	0		
Add2	3	n							
Mult1	4	y	mul		4	7	0		
Mult2	5	n							
Load1	6	n							
Load2	7	y	ld	45	0	0	0		

Integer Reg #	Q	V
1	2	
2	0	0
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	4	

24

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5		
4	4		
5			

CC 05

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0		4
Add1	2	y	sub	100	1	0	0		
Add2	3	n							
Mult1	4	y	mul	5	4	0	0		
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	2	
2	0	0
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	4	

25

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5		
4	4	6	
5			
6	6		

CC 06

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0		4
Add1	2	y	sub	100	1	0	0		
Add2	3	y	add	0	8	0	0		
Mult1	4	y	mul	5	4	0	0		
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	2	
2	3	
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	4	

26

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5		
4	4	6	7
5			
6	6		

CC 07

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0		4
Add1	2	n							
Add2	3	y	add	0	8	0	0		
Mult1	4	y	mul	5	4	0	0		
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	99
2	3	
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	4	

27

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5		
4	4	6	7
5			
6	6	8	

CC 08

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0		4
Add1	2	n							
Add2	3	y	add	0	8	0	0		
Mult1	4	y	mul	5	4	0	0		
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	99
2	3	
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	4	

28

finishing times

Instruction		j	k	IS	RPO	EXE	WR
LD	R3	34	R2	1	1	3	4
LD	R7	45	R2	2	2	4	5
MULTD	R7	R7	R3	3	5		
SUBD	R1	R1	1	4	4	6	7
SD	R7	21	R2	5			
ADDD	R2	R2	8	6	6	8	9

CC 09

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0		4
Add1	2	n							
Add2	3	n							
Mult1	4	y	mul	5	4	0	0		
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	99
2	0	8
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	4	

29

finishing times

Instruction		j	k	IS	RPO	EXE	WR
LD	R3	34	R2	1	1	3	4
LD	R7	45	R2	2	2	4	5
MULTD	R7	R7	R3	3	5	15	
SUBD	R1	R1	1	4	4	6	7
SD	R7	21	R2	5			
ADDD	R2	R2	8	6	6	8	9

CC 15

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0		4
Add1	2	n							
Add2	3	n							
Mult1	4	y	mul	5	4	0	0		
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	99
2	0	8
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	4	

30

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5	15	16
4	4	6	7
5	16		
6	6	8	9

CC 16

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0	20	0
Add1	2	n							
Add2	3	n							
Mult1	4	n							
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	99
2	0	8
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	0	20

31

finishing times

Instruction		j	k
LD	R3	34	R2
LD	R7	45	R2
MULTD	R7	R7	R3
SUBD	R1	R1	1
SD	R7	21	R2
ADDD	R2	R2	8

IS	RPO	EXE	WR
1	1	3	4
2	2	4	5
3	5	15	16
4	4	6	7
5	16	18	
6	6	8	9

CC 18

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	y	sd	21	0	0	0	20	0
Add1	2	n							
Add2	3	n							
Mult1	4	n							
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	99
2	0	8
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	0	20

32

finishing times

Instruction		j	k	IS	RPO	EXE	WR
LD	R3	34	R2	1	1	3	4
LD	R7	45	R2	2	2	4	5
MULTD	R7	R7	R3	3	5	15	16
SUBD	R1	R1	1	4	4	6	7
SD	R7	21	R2	5	16	18	19
ADDD	R2	R2	8	6	6	8	9

CC 19

RS	RS Tag	Busy	Op	Vj	Vk	Qj	Qk	V_{dst}	Q_{dst}
Store1	1	n							
Add1	2	n							
Add2	3	n							
Mult1	4	n							
Mult2	5	n							
Load1	6	n							
Load2	7	n							

Integer Reg #	Q	V
1	0	99
2	0	8
3	0	4
4	0	1000
5	0	2000
6	0	3000
7	0	20

33