CpE 213
Digital Systems Design

Lecture 7

Thursday 9/16/2003

Before the next lecture

- Review Chapter 2.
- Read Chapter 3.

Calculate 3*5 with for loop

Code	Addr	Instr
		MOV A, #0
		MOV R0, A
		MOV A, #3
		MOV R1, A
	Loop:	MOV A, #5
		CLR C
		ADDC A, R0
		MOV R0, A
		MOV A, R1
		CLR C
		ADDC A, #0FFh
		MOV R1, A
		JZ Stop
		SJMP Loop
	Stop:	SJMP Stop

Code for previous program

Mnemonic	**Code**		
MOV A, #0	74 00		
MOV R0, A	F8		
MOV A, #3	74 03		
MOV R1, A	F9		
MOV A, #5	74 05		
CLR C	C3		
ADDC A, R0	38		
MOV R0, A	F8		
MOV A, R1	E9		
CLR C	C3		
ADDC A, #FF	34 ??		
MOV R1, A	F9		
JZ Stop	60 ??		
SJMP Loop	80 ??		
SJMP Stop	80 FE		

Register contents

Code executed:	PC	R0	R1	ACC	C
MOV A, #0	00	xx	xx	xx	x
MOV R0, A	02	xx	xx	00	x
MOV A, #3	03	00	xx	00	x
MOV R1, A	05	00	xx	03	x
MOV A, #5	06	00	03	03	x
CLR C	08	00	03	05	x
ADDC A, R0	09	00	03	05	0
MOV R0, A	0A	00	03	05	0
MOV A, R1	0B	05	03	05	0
CLR C	0C	05	03	03	0
ADDC A, #FF	0D	05	03	03	0
MOV R1, A	0F	05	03	02	1
JZ Stop	10	05	02	02	1
SJMP Loop	12	05	02	02	1
MOV A, #5	06	05	02	02	1
CLR C	08	05	02	05	1
ADDC A, R0	09	05	02	05	0
MOV R0, A	0A	05	02	0A	0
MOV A, R1	0B	0A	02	0A	0
CLR C	0C	0A	02	02	0
ADDC A, #FF	0D	0A	02	02	0
MOV R1, A	0F	0A	02	01	1
JZ Stop	10	0A	01	01	1
SJMP Loop	12	0A	01	01	1
MOV A, #5	06	0A	01	01	1
CLR C	08	0A	01	05	1
ADDC A, R0	09	0A	01	05	0
MOV R0, A	0A	0A	01	0F	0
MOV A, R1	0B	0F	01	0F	0
CLR C	0C	0F	01	01	0
ADDC A, #FF	0D	0F	01	01	0
MOV R1, A	0F	0F	01	00	1
JZ Stop	10	0F	00	00	1
SJMP Stop	14	0F	00	00	1
Total instructions	**34**	0F	00	00	1
Total clock cycles	**102**				

Modification required for 21*60

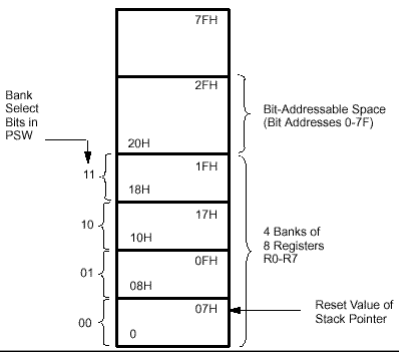
Quiz – Fill in the table below

Note: numbers in first column are in decimal

	Mnemonic	Code	PC	R0	R1	ACC	C
	MOV A, #11	74 ??	00	xx	xx	xx	x
	MOV R0,A	1111 1???					
	MOV A, #04	74 ??					
	CLR C	C3					
	ADDC A, R0	0011 1???					
	MOV R1, A	1111 1???					
	MOV A, #04	74 ??					
	ADDC A, R1	0011 1???					
Stop	SJMP Stop	80 ??					

8051 HW Continued - Internal RAM

- Low 128 bytes contains:
  - 16x8 bits of bit addressable RAM
    - cpl 0 is same as xrl 20h,#1
  - Four banks of 8 registers (R0 through R7)
    - PSW(4:3) selects
    - good for context switching
    - What is the address of register 5 in bank 3?

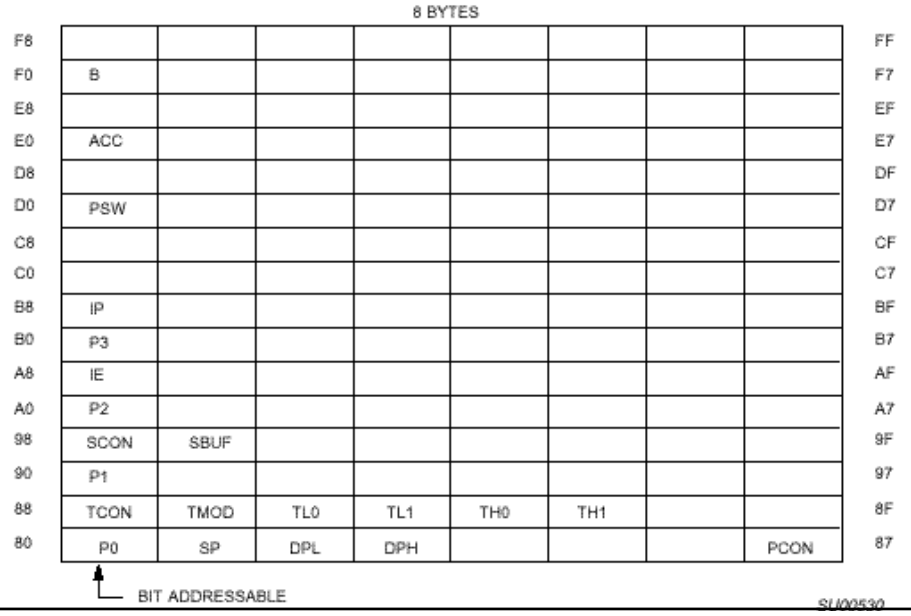


Instructions using registers

- Can use 1-byte or 2-byte instructions
  - MOV A, R5
  - MOV A,05H
  - _____ version is shorter
  - Frequently accessed data should be stored in registers

Instruction	Bank 0	Bank 1	Bank 2
MOV A,R0	MOV A, 00H	MOV A, 08H	MOV A, 10H

Special Function Regs



Special Function Registers (SFRs)

- Are not just memory locations – are registers serving special functions
- SFRs ending in 8 or 0 are both byte and bit addressable (includes ACC)
- Mostly accessed by indirect addressing
- SETB 0E0H sets bit 0 of ACC
- E0 is both byte address of whole ACC and bit address of LSB
- Question: How to set MSB of B, leave others intact?

Program Status Word (PSW)

- SFR at address D0H

MSB LSB

CY	AC	F0	RS1	RS0	OV	—	P

BIT	SYMBOL	FUNCTION
PSW.7	CY	Carry flag.
PSW.6	AC	Auxilliary Carry flag. (For BCD operations.)
PSW.5	F0	Flag 0. (Available to the user for general purposes.)
PSW.4	RS1	Register bank select control bit 1. Set/cleared by software to determine working register bank. (See Note.)
PSW.3	RS0	Register bank select control bit 0. Set/cleared by software todetermine working register bank. (See Note.)
PSW.2	OV	Overflow flag.
PSW.1	—	User-definable flag.
PSW.0	P	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the Accumulator, i.e., even parity.

NOTE: The contents of (RS1, RS0) enable the working register banks as follows:
(0,0)— Bank 0 (00H–07H)
(0,1)— Bank 1 (08H–0fH)
(1,0)— Bank 2 (10H–17H)
(1,1)— Bank 3 (18H–17H)

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