CpE111
Introduction to Computer Engineering

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CH 4: Digital Hardware

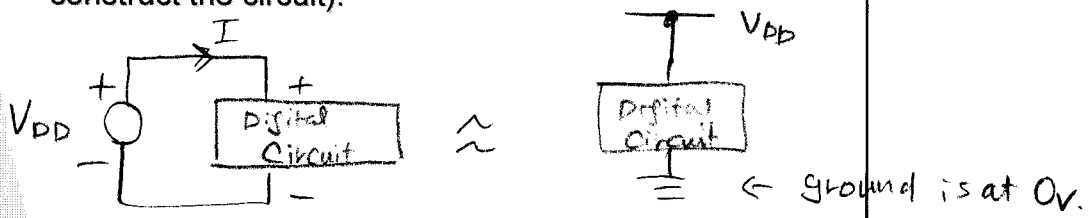
UMR UNIVERSITY OF MISSOURI-ROLLA
The Name. The Degree. The Difference.

Hardware?

- The physical realization of a digital element or system.
- How to represent logic 0 and logic 1 states?
  1. Voltage V, which has units of volts (v).
  2. Electrical current I, which has units of ampres (A or amps).
- Two are related: a voltage causes electrical current to flow.
- Most digital logic chips use two different voltage ranges to define logic 0 and logic 1 conditions.

Power Supply

- All electronic networks require a power supply to operate.
- In digital circuits, the power supply is usually modeled as a voltage source with a value that we will denote by V_{DD} (usually 5v, 3.3v or 2.5v).
- Ex) schematic diagram of a digital system with a power supply (since the drawing shows the "scheme" used to construct the circuit).

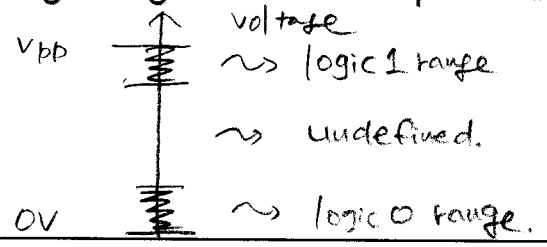


positive side voltage is higher as much as V_{DD} volts

Logic Levels

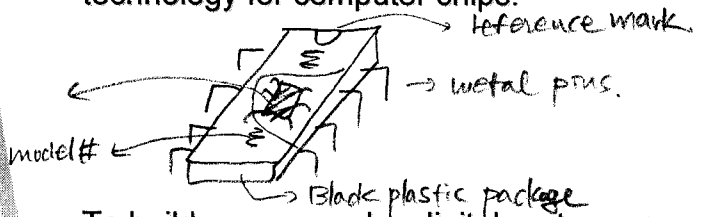
- Logic 0 -> 0v and Logic 1 -> V_{DD} (ex., 5v), in general.
  - Low voltage represents logic 0 & high voltage represents 1 -> called positive logic.
  - High voltage represents logic 0 & low voltage represents 1 -> called negative logic.
- Two voltage ranges are used in practice.

ex)



Digital Integrated Circuits

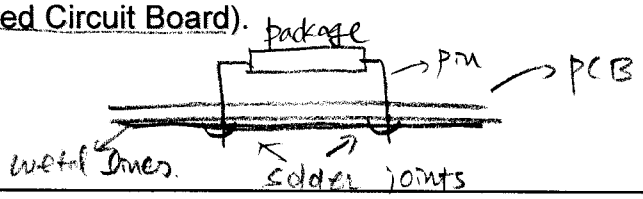
- ICs (Integrated Circuits) = Computer chips.
- Dual inline package (DIP) is very common packaging technology for computer chips.



Silicon chip inside

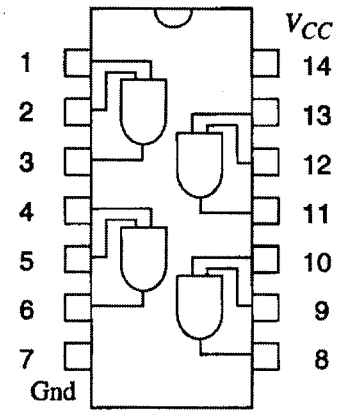
=) complex circuit is fabricated on a Silicon chip by optical lithography.

- To build more complex digital systems -> use PCB (Printed Circuit Board).



Pin-Out Diagram

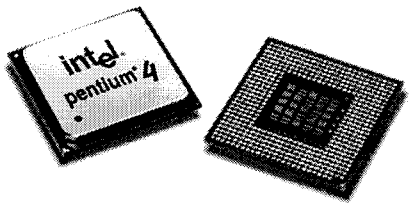
- The logic functions that a particular chip implements are usually shown by embedding equivalent logic diagrams in package outline drawings.
- Ex) Quad-AND chip. V_{CC} is an alternative notation for the power supply voltage.



ex) pin3 = pin1 • pin2.

Different Packaging Technologies?

- PGA (Pin Grid Array) is used for most microprocessor chips, since larger chip can be embedded and larger # of pins can be allocated.
- There are different variations – INTEL's LGA775 and AMD's Socket939.



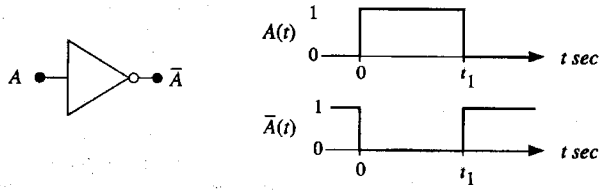
ICs can be categorized with respect to the # of gates inside

IC Integration Levels

- SSI (Small-Scale Integration): ICs with a few gates.
- MSI (Medium-Scale Integration): ICs with a few hundred gates.
- LSI (Large-Scale Integration): 1K – 100K gates.
- VLSI (Very Large-Scale Integration): a few million gates.
- ULSI (Ultra Large-Scale Integration): around one billion gates.
- Ex) INTEL Pentium 4 processor has about 125 million gates.

Logic Delay Times

- Waveform (a plot of a variable as a function of time) is used to measure the behavior of a gate.
- Ex)



(a) Logic gate (b) Ideal waveforms

→ input waveform

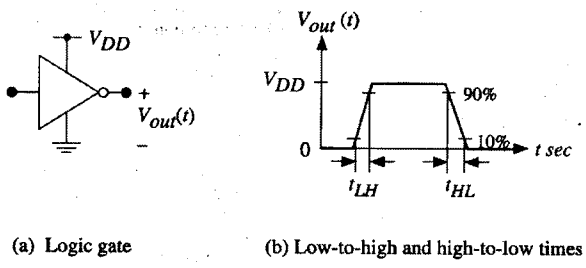
→ output waveform.

- In the real world, a voltage cannot chance instantaneously.

⇒ There should be some delays for 0→1 & 1→0 transitions

Output Switching Times

- Two time intervals must be considered:
  - t_{LH}, the output low-to-high time, also called the rise time, t_r.
  - t_{HL}, the output high-to-low time, also called the fall time, t_f.
  - By convention, these time intervals are not measured between 0v to VDD, but represent the transition required between 10% to 90% voltage levels, as shown below.



(a) Logic gate (b) Low-to-high and high-to-low times

Continued,

- The minimum amount of time needed for the gate to switch from 0 to 1 then back again is given by:

$$t_{min} = t_{LH} + t_{HL}$$

- The maximum switching frequency is:

$$f_{MAX} = \frac{1}{(t_{LH} + t_{HL})} \quad [\text{in Hz}]$$

- =max # of logic transitions that the gate can make in 1 sec.
- Ex) $t_{LH} = 7.2\,ns$ & $t_{HL} = 3.9\,ns$, f_{max}?

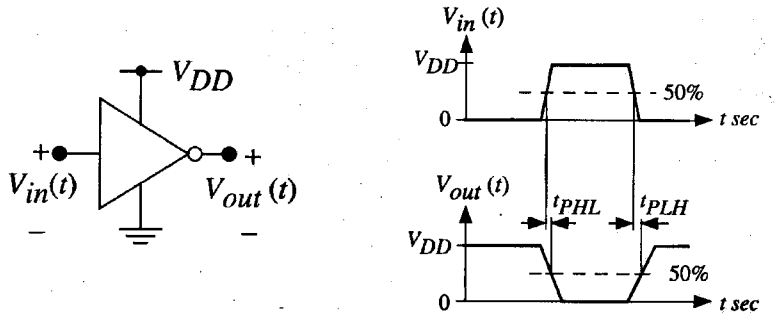
$$f_{max} = \frac{1}{7.2 \times 10^{-9} + 3.9 \times 10^{-9}} = 90.09\ MHz$$

(≈ 90.09 million transitions per sec max.

Propagation Delay

- It can be hard to keep track of both delay times for every logic gate.
- At the logic design level, it is simpler to introduce a single delay time that represents an average switching time, called "propagation delay", from the input to the output.
- This is to include the physical delay of a logic signal as it "propagates" through a chain of gates.

Inverter Gate Example



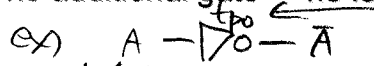
- Then, t_P (=propagation delay) = 1/2 (t_{PHL} + t_{PLH}) or =max(t_{PHL}, t_{PLH}), alternatively.

Fan-In & Fan-Out

- The fan-in of a digital logic gate refers to the number of inputs.
- Ex) inverter has fan-in of 1 and NAND2 has fan-in of 2.
- The fan-in provides information about intrinsic speed of the gate -> the propagation delay increases with the fan-in.
- Ex) OR2 is faster than OR3.

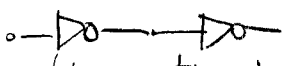
Continued,

- The switching time of an electronic gate depends on the number of gates that are driven (or connected) at the output.
- The fan-out of a gate is the number of gates that are driven by the output, and it depends how the gate is used in the logic chain -> increasing the fan-out slows down the logic flow through the gate.
- If no additional gate -> no load (fan-out=0)



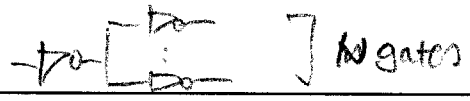
t_{PO} ← no load propagation delay.

- Fan-out=1 ->



$t_{P1} = t_{PO} + 1 \cdot t_{PL}$ ← additional delay time needed to drive the load (next inverter).

- Fan-out=N ->



$$t_{PN} = t_{PO} + N \cdot t_{PL}$$

Logic Cascades and Delays

- Ex) linear chain of 4 inverters.

$t_d = t_{d1} + t_{d2} + t_{d3} + t_{d4}$

Fan-in & fan-out delays must be considered.

$t_{d4} = t_{to,NOT} + t_L$

$t_{to,NOT}$: no-load P.D.

t_L: The load at the forth gate is not specified. So, t_L is used

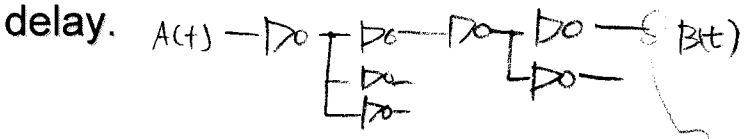
$t_d = 4 \cdot t_{to,NOT} + 3\, t_{PL,NOT} + t_L$

$4 \cdot t_{to,NOT}$: no-load prop delay

$3\, t_{PL,NOT}$: fan-out delay

Continued,

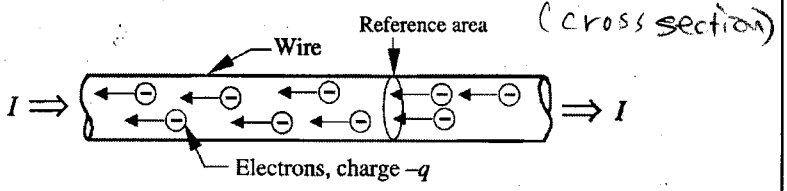
- Ex) Inverter chain with increased internal delay.



$$t'_d = \underbrace{4 \cdot t_{p0,NOT}}_{\text{no-load prop delay}} + \underbrace{6 \cdot t_{pL,NOT}}_{\text{6 fan-outs driven}} + t_L$$

⇒ takes more time because of more fan-outs!

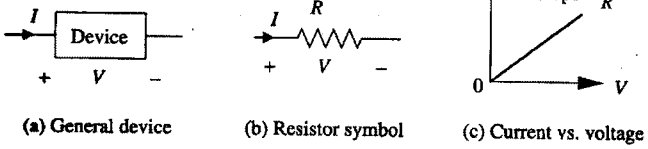
Basic Electric Circuits



- Let's consider electric current flowing through a wire.
- The current I (measured in ampares, A) represents the flow of charge (denoted by Q, measured in units of coulombs, C) across a reference area shown.
- So, the current is the time rate of change of the charge across the area, as given by the derivative; I = dQ/dt.
- 1A = 1C/sec crossing the reference plane.
- Electrons flow right to left and current flows in the direction of positive charge (left to right).
- The voltage on the left side is higher than the right side.

Resistance

- Every electronic device has a natural tendency to "resist" the flow of charge -> Resistance (parameter R is used).
- R = V/I (V: voltage, I: current)
- The unit of resistance is the ohm (Ω).
- Ex) 1Ω resistor admits 1A of current with 1v applied across it -> Ohm's law.



(a) General device (b) Resistor symbol (c) Current vs. voltage

$V = IR \Rightarrow I = V/R = (1/R) \cdot V$

slope.

⇒ Linear relationship between I & V.

Power Dissipation (P) of Resistor

- The power dissipation of a resistor in units of watts (W) is given by:
- P = VI = (IR)I = I^2R (since V = IR, Ohm's law).
- Ex) Power dissipation of a resistor at 15v and 5A.

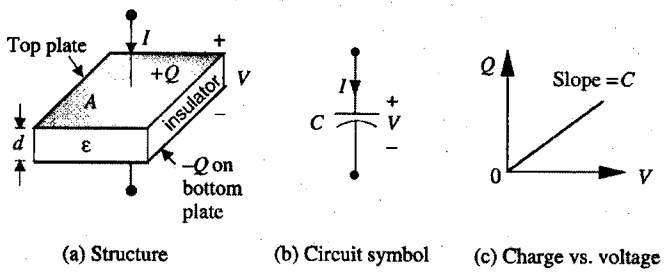
$R = V/I = 15/5 = 3\Omega$

So, $P = (5A)^2 \cdot 3\Omega$

$= 25 \times 3 = 75$ watts.

Capacitance

- A parameter that describes how a particular device can store electric charge.
- Ex) Parallel-place capacitor.



(a) Structure (b) Circuit symbol (c) Charge vs. voltage

Continued,

- The device consists of two metal plates that are separated from each other by an insulating layer such as glass.
  1. A voltage V is applied to the plates as shown.
  2. A charge of +Q is induced on the top plate and a charge of –Q is induced on the bottom plate.
  3. Then, the amount of charge Q stored is Q = CV.
- The unit of capacitance is the farad (F) such that C = Q/V.

charge
unit : coulomb.
voltage
capacitance

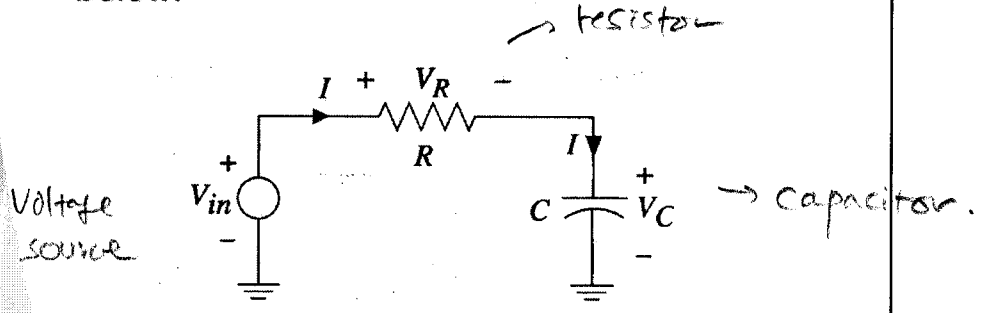
ex) charge 10C & 5V, capacitance?

$C = \frac{10C}{5V} = 2F$

Examples

The RC (Resistor-Capacitor) Circuit

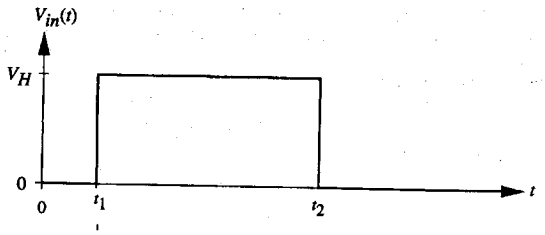
- Digital switching networks are often modeled by using the series-connected RC circuit shown below.



Continued,

1. Three components carry the same current I, since they are connected in series.
2. But three different voltages are shown; V_{in} (input voltage), V_R (resistor voltage) and V_C (capacitor voltage).
3. The relationship among these voltages is from Kirchhoff's voltage law (KVL);
   - Sum of voltage rises = sum of voltage drops.
   - $V_{in} = V_R + V_C$
   - So, V_R & V_C respond to changes in the input voltage V_{in}.

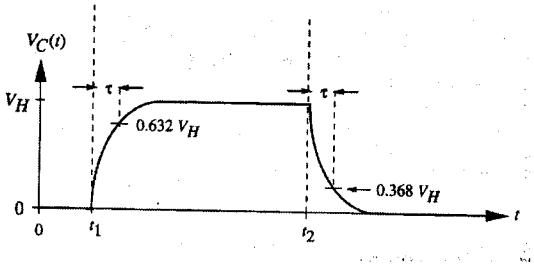
RC Circuit Behavior



- Input voltage $V_{in}(t)$ from 0v to a high voltage V_H at time t_1 and then back to 0v at time t_2.
- Then, capacitor voltage $V_C(t)$?

Continued,

- When V_{in} is charged to a high voltage V_H, current starts flowing. The current is given by; $I = dQ/dt$ (current is the time rate of change of the charge).
- So, the current "charges the capacitor" and the capacitor charge Q_C increases with time; $V_C = Q_C/C$.
- When input voltage switches back down to 0v, V_C decays to 0v.
- -> Q_C goes up, then V_C goes up; Q_C goes down, then V_C goes down with time.



derivative

Capacitor charge (increase with time).

$$V_C = \frac{Q_C}{C}$$

stays

Detailed Analysis

- The time delay as the capacitor voltage changes from 0 to V_H is due to the resistance R in the circuit, which impedes the current flow.
  - -> $V_R = IR$
  - -> $V_R = V_{in} - V_C$ (by KVL)
  - So, $I = (V_{in} - V_C)/R$
- When the capacitor is charged, the voltage increases according to the formula:

$$V_C(t) = V_H[1 - e^{-(t-t_1)/\tau}] \qquad t \geq t_1$$

"tau"

- -> exponential dependence formula: (e is "Euler e" and e = 2.71828... and τ (tau) is called the time constant and $\tau = RC$ seconds).

Continued,

- τ represents the delay for the capacitor voltage to change from 0v to a certain high level that is chosen at time τ seconds from t_1.
- -> The voltage at this time is...

$$V_C(t = t_1 + \tau) = V_H[1 - e^{-1}] = 0.632V_H \approx (2/3)V_H$$

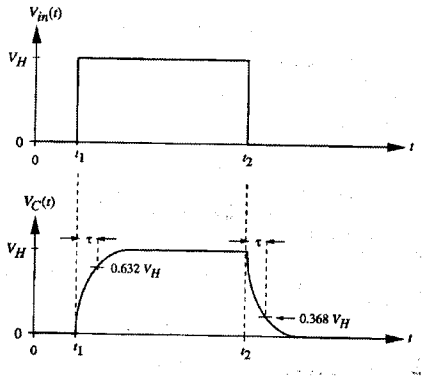
- Small τ means fast transition.
- Large τ means slow transition.

Continued,

- The discharge event is similar:

$$V_C(t) = V_H e^{-(t-t_2)/\tau} \qquad t \geq t_2$$

$$V_C(t = t_2 + \tau) = V_H e^{-1} = 0.368V_H \approx (1/3)V_H$$



$V_{H} \rightarrow V_C = (0.368) \cdot 5V = 1.84V$
also takes 1ns.

Example

- Consider an RC circuit with values of R=1000Ω and C=10^{-12}F.

  So, $\tau = RC = 10^3 \times 10^{-12} = 10^{-9}$ sec = 1ns.

  If $V_H = 5V$, then a low → high transition from 0V to V_C = $(0.632) \cdot 5V = 3.16V$ takes $\tau = 1ns$.
- What if we reduce R= R=1000Ω to 500Ω and C=5-[illegible]F?

  $\tau = 500 \times 5 \times 10^{-13} = 0.25ns$

  ⇒ 4 times faster transitions.
- Keeping R=1000Ω, how can we achieve τ=0.25ns?

  $RC = 0.25ns$

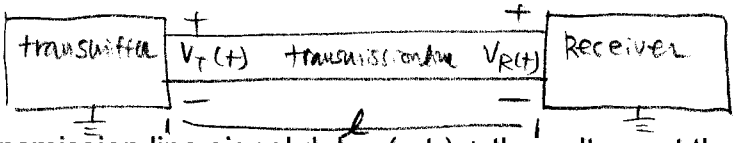
  $\Rightarrow 1000C = 0.25ns \Rightarrow C = 2.5 \times 10^{-13} F.$

Application to Digital Circuits

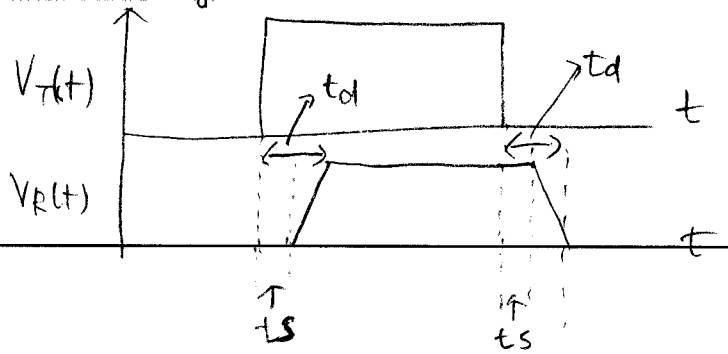
- Transitions 0->1 and 1->0 take time.
- The switching time of every digital electronic network is governed by any resistance and capacitance in the network.
- Parasitic elements: unwanted resistance and capacitance contributions that cannot be eliminated and that act to slow down the network response.
- So, keeping R and C as small as possible is desired!

Transmission Lines

- Another type of logic delay arises when we analyze the physics of transmitting a voltage along a wire.



- Transmission line signal delay (= t_s) + the voltage at the end of transmission line takes time to "build up" to the final value = t_d.



Program Completed

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The Name. The Degree. The Difference.