ADS Assignment 1 Session 2 (Spring) 2019

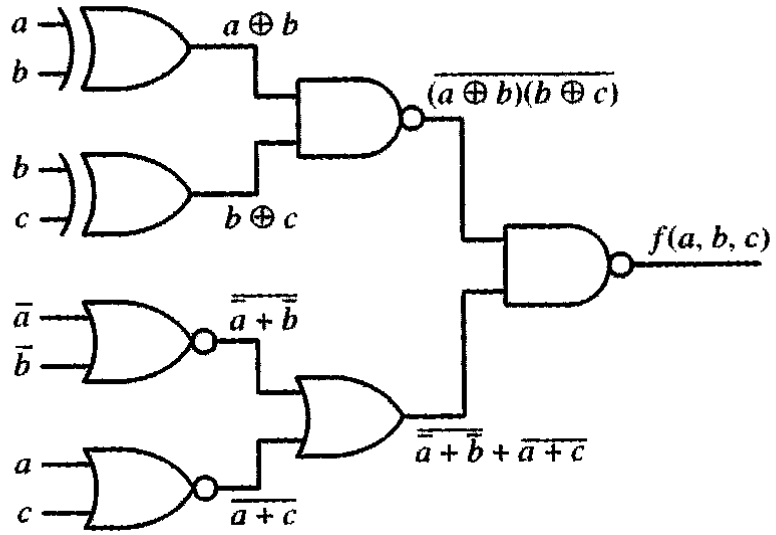
This assignment 1 is an *individual* VHDL assignment. Through discussion among students is encouraged, plagiarism is not tolerated. Therefore, it is in your interest to protect your work. Please be warned that any student found to hand in a report "similar" to another will be awarded a zero mark.

Late assignments will attract a penalty of 20% per day, and will not be accepted after five days.
No submission will automatically lead to zero marks.

The due date for this assignment is 6 pm Wednesday, 28 August 2019.
On the deadline, submit (upload) the soft copy of your report to TurnItIn (through UtsOnline).

Part 1 Combinational circuit modeling

Using VHDL, implement this circuit, either using a structural model or a behavioral model.



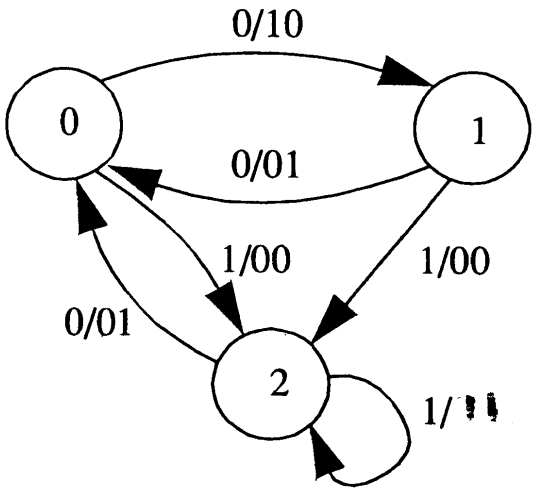
Test the model by performing simulations to show that the outputs of the model match the output of the circuit.
Test: Use these values to test (in your simulation): a=0, b=1, c=1

This question in the tutorial (1-9) asked you to find a simplified Boolean expression and logic circuit. You also need to implement an either structural or behavioral model of your answer, then synthesize and simulate to compare with your results from above.

Hints:
-This part of the assignment is the question in the tutorial (1-9) where you asked to find a simplified Boolean expression and logic circuit.
-The behavioral model simplifies your work!

Part 2 Sequential circuit modeling

Implement and test a VHDL model for the state machine for a traffic-light controller shown below.



Add a synchronous reset input to the first state 0.

Simulate the performance of the state machines by showing its clock, present state, and output when the input sequence is 100101. Make the synchronous reset and state transitions effective on **the falling edge** of your clock.

Display all inputs, outputs, and states in your simulation timing diagram.

What to hand in:
A report that is containing source codes of all the VHDL programs you have written, printouts of your simulation outputs, as well as your detailed assumptions, comment/interpretation of the results; Soft copy to TURNITIN (UTS on Line.

Marking scheme:
Eight marks for VHDL work:

	Code	Simulation
Combinational Circuit	3 marks	1 mark
Sequential Circuit	3 marks	1 mark

Two marks for the report:
Your report can be brief but make sure you include assumptions, discussions, and interpretation of the various simulation results.

Assumptions	0.5 mark
Discussion, observation and conclusion	0.5 mark
Interpretation of simulation	1 mark