

# A Review of Charge-Coupled Device Image Sensors

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## Introduction

Invented in 1969 at AT&T Bell Labs by Willard Boyle and George E. Smith [1, 2, 3], a charge-coupled device (CCD) is a planar array of metal–oxide–semiconductor (MOS) capacitors (MOSCAP) etched into a semiconductor surface (typically silicon), forming an integrated circuit (IC) with light sensitive elements, with each element representing a picture component, or a pixel. In a more technical sense, a CCD IC is a serial device where charge packets are generated, transferred and read one after another. The charge packets, which are stored in the depletion region of the MOSCAPs, are transferred within the IC by controlling individual MOSCAP gate voltages so as to allow the charges to flow from one MOSCAP to the next, and hence the name “charge-coupled” devices. An amplifier at the output stage of the imaging sensor provides a voltage reading that can be digitally processed [4, 5]. Figure 1 shows a CCD developed for ultraviolet (UV) light imaging applications. Figure 2 demonstrates how light quanta are detected and processed in a CCD, where generated charges are transformed into electrical energy, represented by voltages, one pixel after another as they are received using a horizontal shift register [6, 7].

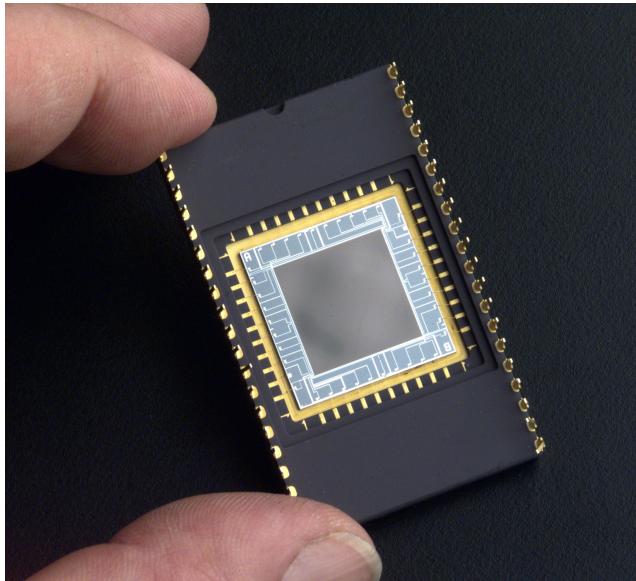


Figure 1: An application-specific CCD for ultraviolet (UV) imaging in a wire-bonded package. Adapted from [4].

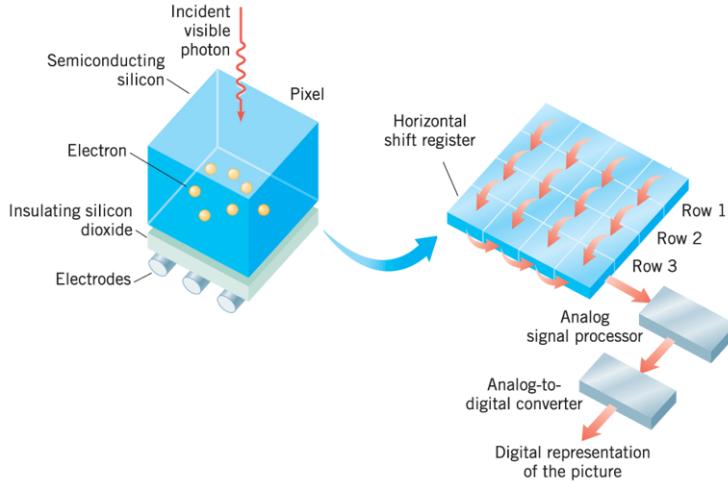


Figure 2: Image detection and processing in a CCD using metallic electrodes. Adapted from [6].

## Theory

### Physical principles

A MOSCAP is made up of a metal electrode (i.e. a gate) and an insulator thin film (i.e. gate dielectric), such as silicon dioxide ( $\text{SiO}_2$ ), placed on top of a semiconductor substrate. The insulator film can be as thin as 1.5 nm. Before 1970, metals (e.g., aluminum (Al)) were usually used as gate metal electrodes, thus the *M* in *MOS*. Due to its ability to withstand high thermal budgets without reacting with  $\text{SiO}_2$ , heavily doped polycrystalline silicon (poly-Si) replaced Al and other metals as the standard gate material after 1970. However, MOSCAP persisted as a term. MOSCAP structures with *p*-type silicon substrates are referred to as nMOS capacitors, whereas structures with *n*-type substrates are referred to as pMOS capacitors [8]. *In a CCD image sensor, each pixel corresponds to an nMOS capacitor.*

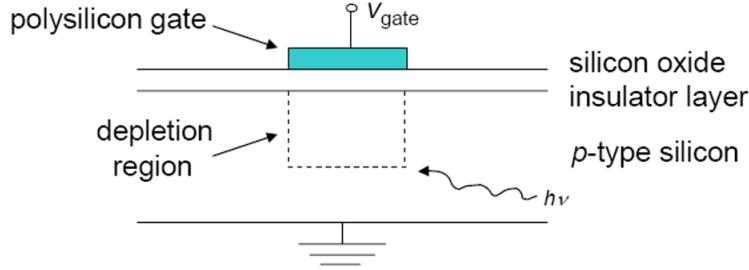


Figure 3: Basic metal–oxide–semiconductor capacitor (MOSCAP). Adapted from [5].

Figure 4 shows three regions of operation of the pMOS capacitor: a) accumulation, b) depletion, and c) inversion because the capacitance changes with respect to the applied direct-current (DC) voltage.

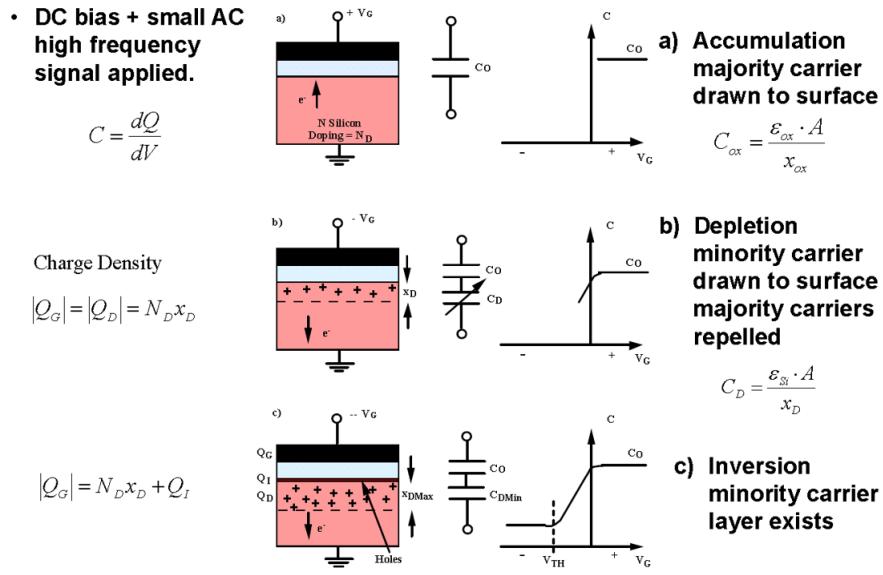


Figure 4: pMOS capacitor structure and resulting CV plot; (a) corresponds to accumulation, (b) to depletion, and (c) to inversion. Adapted from [9].

Assuming that the charges linked to the  $\text{SiO}_2/\text{Si}$  system are not present and the system has come to a final, steady state condition, we consider the following [9]:

1. A DC voltage of  $+V_G$  on the gate (Figure 4[a]): Positive gate voltages attract the majority carrier electrons in the  $n$ -type substrate to the silicon surface (i.e. majority carrier accumulation). The capacitance in this case is basically the oxide capacitance ( $C_{ox}$ ) and is measured using a small high-frequency AC signal (typically between 100 kHz and 1 MHz). No depletion layers will be created. Instead, the silicon substrate will form a resistance along with  $C_{ox}$ . Only the capacitive part of the impedance is extracted, and it is independent of  $V_G$ , as illustrated in the first equation in the right-hand part of Figure 4[a].
2. A DC voltage of  $-V_G$  on the gate (Figure 4[b]): A depletion region is formed as negative voltages diffuse the majority of carrier electrons away from the silicon surface. Positive charges from the substrate donor atoms (they have a net positive charge because mobile electrons were diffused away) will balance any net negative charge placed on the gate and maintain charge neutrality. As a result

$$|Q_G| = |Q_D| = N_D x_D, \quad (1)$$

where  $N_D$  is the doping in the silicon substrate (assumed to be uniform);  $Q_D$  and  $Q_G$  are depletion region and gate net charges, respectively, with units of number of charges per  $\text{cm}^2$ ; and  $x_D$  is the depletion region depth, which is a function of the gate voltage (increasing as  $V_G$  increases). By definition, the depletion region has a capacitance-per-unit area given by

$$C_D = \frac{\epsilon_{Si}}{x_D} \quad (2)$$

where  $\epsilon_{Si}$  is the relative permittivity of silicon. The extracted capacitance of MOSCAP's structure is now a varying depletion region oxide ( $C_D$ ) in series with  $C_{ox}$ , as illustrated in the plot on the right-hand side of Figure 4[b].  $C_D$  decreases as  $V_G$  becomes more negative because  $x_D$  increases.

3. Larger values of negative DC gate voltage ( $V_G$ ) on the gate (Figure 4[c]): If the applied negative DC voltage is high enough, an inversion layer is formed because the silicon surface will essentially invert from an  $n$ -type to a  $p$ -type material. As the negative voltage on the gate

attracts the minority carrier holes in the substrate to the surface—and if enough of them are present there—they can form the inversion layer of *p*-type carriers. The gate voltage at which this inversion takes place is called the threshold voltage. Once the inversion layer is created,  $x_D$  stops growing and reaches a saturation value of  $x_{D\text{Max}}$ .

A *pn* junction is a junction dividing a *p*-type semiconductor and an *n*-type semiconductor. In a *pn* junction, excess electrons diffuse into the *p*-type material and, similarly, excess holes diffuse into the *n*-type material. As can be seen in Figure 5, a resulting electric field will eventually stop the diffusion process, creating a depletion layer, where the charge distribution is electrically equivalent to a two-plate capacitor [5].

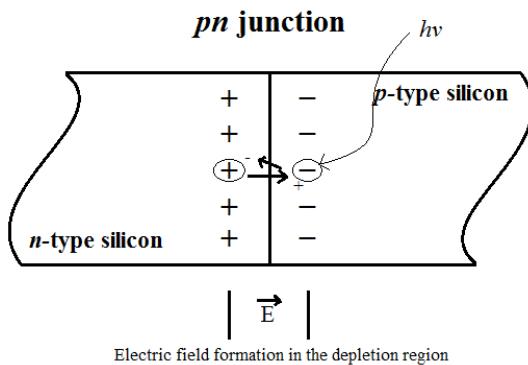


Figure 5: Illustration of the *pn* junction [5].

When a photon interacts with the semiconductor, it creates an electron-hole pair ( $e-h$ ), given that the incident photo energy is equal to or higher than the band gap energy of the semiconductor material. The incident photon energy is given by

$$E_{inc.} = \frac{hc}{\lambda} \quad (3)$$

where  $h$  is Plank's constant and  $c$  is the speed of light in vacuum.  $\lambda$  is the wavelength of incident light. Since silicon has an energy band gap of approximately 1.124 eV at 300 K, photons in the visible range (wavelengths in the range of 400 to 700 nm, corresponding to about 1.77 to 3.1 eV) have enough energy to create  $e-h$  pairs. A dislodged electron will be attracted to

the most positively charged zone in the *pn*-junction, located in the depletion region in the *n*-type material, as illustrated in Figure 5. In the visible range, dielectric layers in an IC are transparent to incident light whereas metal layers are generally reflective with a loss of some incoming photons [10, 11].

*In relation to the above discussion, MOSCAPs in a typical operational *n*-channel CCD IC (i.e. *p*-doped silicon, not *n*-doped silicon as discussed above) are biased into the depletion region before they are being exposed to incident light. Therefore, the gate needs to be biased at a positive voltage ( $+V_G$ ), above the threshold voltage for strong inversion, since this will result in the formation of the *n*-channel underneath the gate as in a MOS transistor.[12] The threshold voltage is the voltage at which the surface potential of the device inverts the underlying channel. The channel can be weakly inverted or strongly inverted with surface potentials of  $\phi_B$  or  $2\phi_B$ , respectively, where  $\phi_B$  is the carrier potential barrier [4].*

Figure 6 shows an nMOS photogate, which is essentially a typical MOSCAP system for collecting and transferring generated e-h pairs, and is used in time-delay-and-integration CCDs (TDI-CCDs) and frame transfer CCD (FT-CCDs) [11].

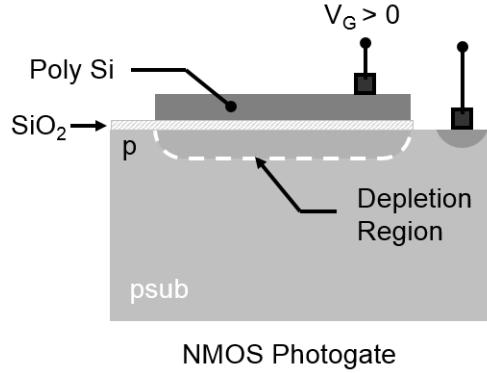


Figure 6: nMOS photogate. Adapted from [11].

## Device operation and enhancements

CCDs operate in state referred to as the *deep depletion* since, after initial biasing, the holes are forced to move farther into the substrate, and no free electrons are at or close to the silicon surface. Operation in the deep depletion region is necessary since it might take up to one hour in some devices (such

as CCDs in high-end scientific cameras) to reach the thermal equilibrium required for strong inversion [4, 13]. Furthermore, due to discontinuous charge distribution boundaries at the edges of the MOSCAP [14], fringing electric fields are introduced and therefore widen the potential well that contains the local minimum of potential energy and therefore facilitates the charge packet transfer process [11]. A comparison between an ideal and non-ideal nMOS photogates is provided in Figure 7, whereas the effect of the gap between gate electrodes on the charge transfer process is illustrated in Figure 8. The physical distance between gate electrodes should be small relative to the dielectric thickness in order to enable effective charge coupling through the fringing electric fields from adjacent electrodes [11].

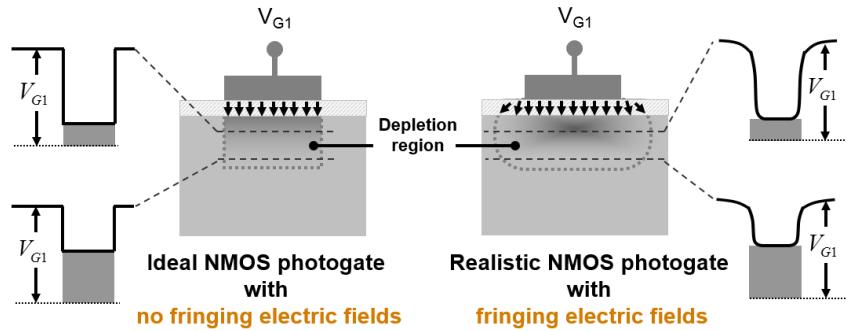


Figure 7: Fringing electric fields in nMOS photogates. Adapted from [11].

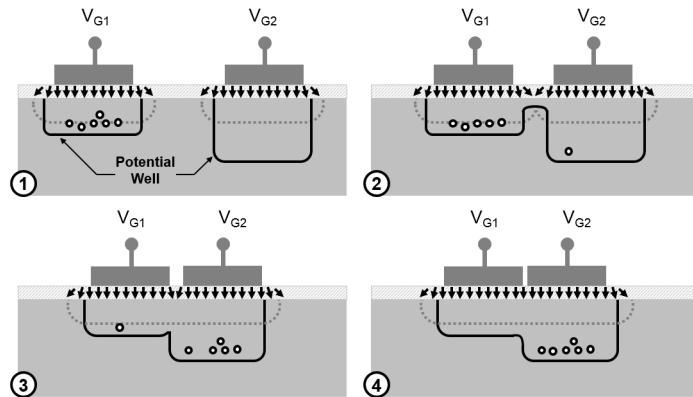


Figure 8: Illustration of the effect of shortening the gap between two adjacent gate electrodes. Adapted from [11].

### Buried channel CCD:

The surface channel/thin oxide interface layer usually suffers from crystal defects that may trap charges, resulting in charge losses and image smearing effects when charge packets are transferred along this interface. In buried channel CCDs, a layer of *n*-doped silicon over the *p*-doped silicon layer with a voltage bias applied between them, as illustrated in Figure 9, the charge storage region is “buried” within the depletion region. Buried channel CCDs hence suffer considerably less from trapped interface charges [5, ?, 15].

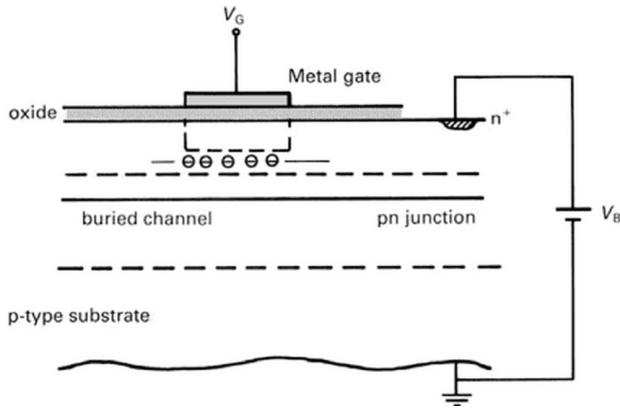


Figure 9: A cross-sectional view of a storage site in a buried channel CCD. Adapted from [?].

### Backside-illuminated CCD:

Illuminating the CCD from its back side will allow light to strike the photocathode layer without passing through the electrodes and wiring layer, and therefore avoid losses. Although electrodes are semi-transparent, non-uniform losses occur. This causes variation in the sensitivity within an individual pixel. Backside illumination involves thinning the CCD, either by dry or wet etching, to about 15 micron. In a back-illuminated CCD (Figure 10), the wiring is oriented behind the photocathode layer by performing backside etching of the silicon wafer during the fabrication process so that incident light can strike the photocathode layer without passing across the electrodes and wiring layer [5, 16, 17, 18].

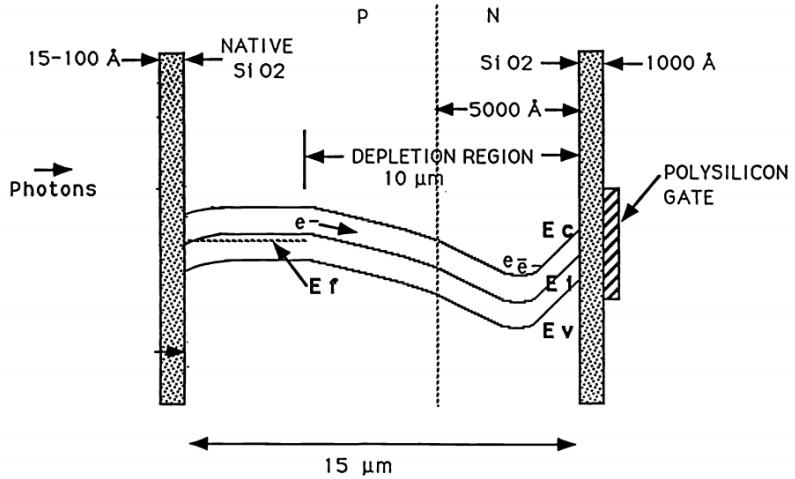


Figure 10: A cross-sectional view of a backside-illuminated thinned CCD. Adapted from [19].

## Performance

### Charge generation:

Image sensors are often characterized by their quantum efficiency (QE), which measures the portion of photon flux that leads to photocurrent in a photodetector. QE is often referred to as the spectral response to emphasize its dependence on incident light wavelength. It is defined as the number of signal electrons generated per striking photons and it may be greater than 100% if more than one electron is generated per striking photon [20, 21]. Figure 11 shows an example of spectral response of a CCD chip.

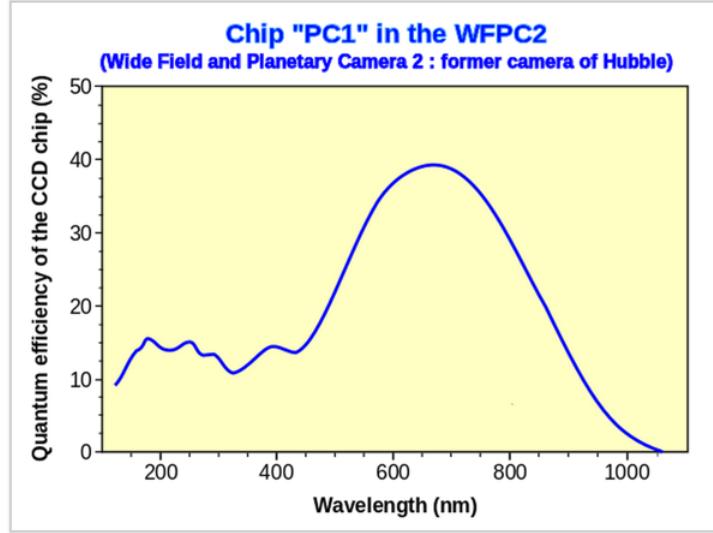


Figure 11: Spectral response of a CCD chip in the Hubble Space Telescope’s Wide Field and Planetary Camera 2. Adapted from [20].

### Charge collection:

Image sensors are also characterized by their well capacity, which is the maximum amount of charge a pixel can accumulate. In modern image sensors, a “full well” capacity can reach a few hundred thousand electrons per pixel with a typical areal density of about 10,000 electrons/ $\mu\text{m}^2$  [5, 3]. The well capacity areal density can be determined as follows

$$\frac{Q}{A} = \frac{C_{ox}}{A}V \quad (4)$$

Blooming is a phenomenon that takes place in CCD image sensors when the finite charge capacity of individual photodetectors is reached [22]. Figure 12 shows an example of blooming artifacts in CCD images.

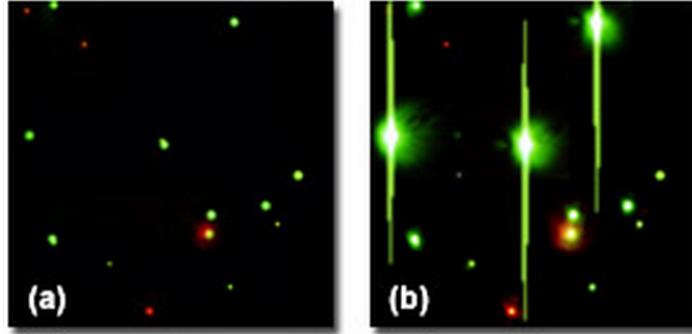


Figure 12: Blooming artifacts in a CCD image. Adapted from [22].

#### Charge transfer:

Defects in the silicon crystal lattice traps charges that would eventually be released. This causes some inefficiency in the charge transfer process. The charge transfer efficiency (CTE) quantifies the charge transfer process. CTE measures the portion of electrons shifted from pixel to the next [23]. Advanced CCDs can have a CTE/transfer of about 99.99995%. Figure 13 demonstrates the difference between good and bad CTE CCD images, where the weak image has vertical tails.

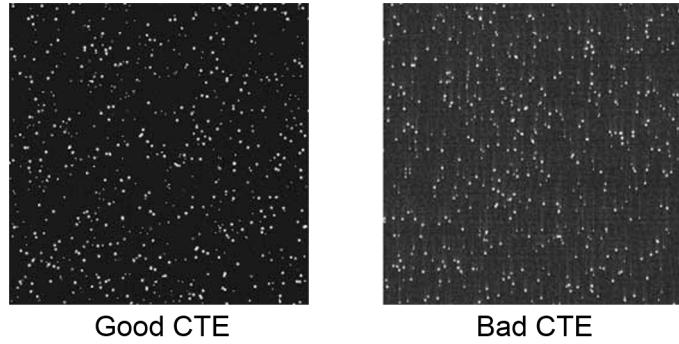


Figure 13: Good and bad CTE CCD images. Adapted from [5].

Furthermore, undesired thermal secondary effects can cause electrons to move from the valence band to the conduction band, which creates “dark current” noise. Dark current is created near the surface channel/thin oxide

interface layer [24, 25]. To reduce the undesired thermal effects, CCD chips can be operated at temperatures of approximately 140 K [5].

### Charge detection:

Figure 14 shows a schematic of the output circuitry of a CCD, where the reset transistor effectively connects the output photodiode to the power supply, VR, in order to clear all charges accumulated during light exposure. The output transistor is a buffer amplifier that permits for pixel voltage reading.  $C_O$  is an output storage capacitor.

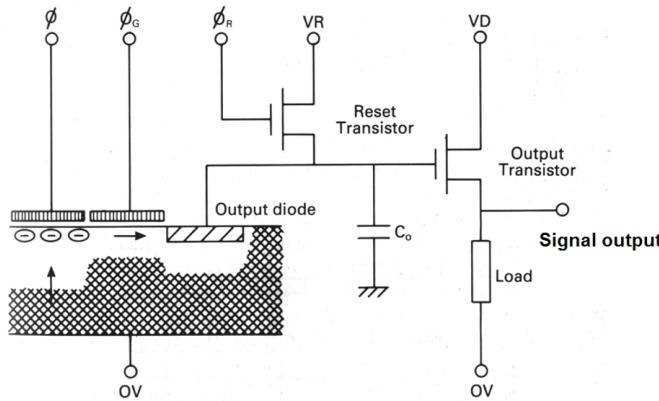


Figure 14: CDD output circuit. Adapted from [5].

The noise associated with recharging  $C_O$  is referred to as the reset noise and is given by

$$\sigma = \sqrt{kTC_O} \quad (5)$$

This type of noise can be removed by subtracting the reset voltage from the voltage reading after readout. The final value of the readout noise is determined after adding the noise from the output transistor. CCD readout noise lowers the sensor signal-to-noise ratio [5, 26]. Moreover, in order to ensure CCD output linearity, electrons should not fill more than 80% of the CCD well capacity [5].

### **Comparison between CCD and CMOS image sensors:**

CCD image sensors have very wide dynamic range (DR )since MOSCAPs can hold large signals (more information per pixel), while they exhibit very low read noise and dark current. CMOS components exhibit relatively higher read noise with pixels that are smaller in size compared to that of CCDs and therefore they have lower DR. On the other hand, CMOS sensors can access a silicon array more rapidly than CCD sensor, but at the expense of higher read noise [27, 28, 29]. The following table shows a comparison between CCD and CMOS image sensor technologies [30]:

	<b>CCD</b>	<b>CMOS</b>
<b>Dynamic range</b>	>10,000	>5,000
<b>Detection speed</b>	Slow	Fast
<b>Quantum efficiency</b>	25-95%	15-35%
<b>Multi-channel</b>	Yes	
<b>Real-time</b>	Yes	
<b>Spectral sensitivity</b>	300-1,100	400-1,100
<b>Read noise</b>	Excellent	

Table 1: Comparison between CCD and CMOS image sensors.

## Modern Examples of CCDs

Figure 14 shows a digital photograph of a CCD linear image sensor for industrial application manufactured by Hamamatsu Photonics.

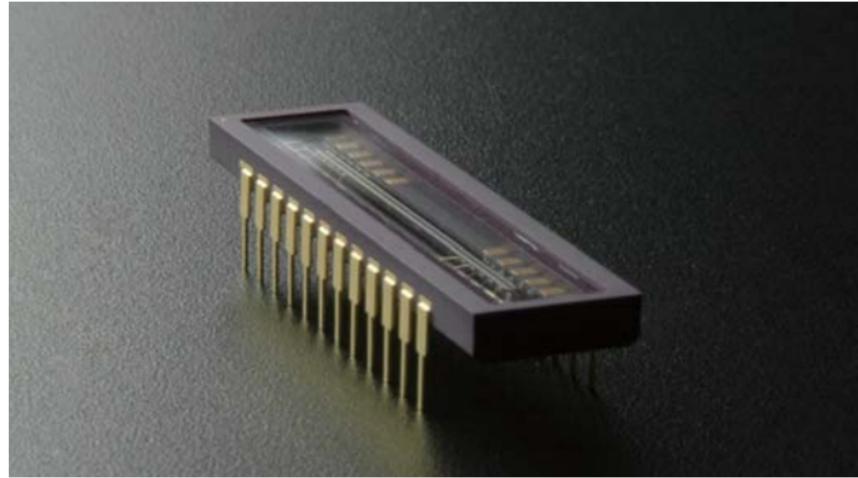


Figure 15: Modern CCD linear sensor. Adapted from S10201-04-01 datasheet.

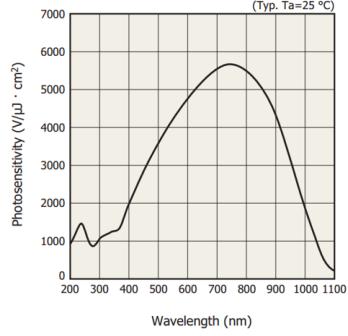
The sensor has the following features:

1.  $12\mu\text{m}$  (H)  $\times 12\mu\text{m}$  (V) pixel size
2. Up to  $4096 \times 128$  number of effective pixels
3. Up to 16 ports
4. 30 MHz/port pixel size
5. 50 kHz line rate (net bit rate)

Figure 14 shows the spectra response and device configuration of the sensor.

#### Spectral response (without window)

The back-thinned (back-illuminated) structure ensures higher sensitivity than front-illuminated types in the UV through the near IR region (200 to 1100 nm).



#### Configuration (S10201-04-01)

Using multiple amplifiers (multiple output ports) permits parallel image readout at a fast line rate.

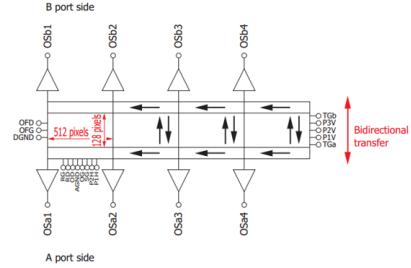


Figure 16: S10201-04-01 spectral response and device configuration. Adapted from S10201-04-01 datasheet.

## Concluding Remarks

A CCD is an arrangement of tiny light sensitive detectors with each pixel corresponding to *p*-doped MOS capacitors. Compared to other technologies, CCDs have higher dynamic ranges and quantum efficiencies, but slower detection speed. Because of their output linearity, high quantum efficiencies and ease of use, CCDs were quickly adopted by physicists and engineers for almost all UV-to-IR applications. The major disadvantage of CCDs is that they are expensive compared to other image sensors.

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