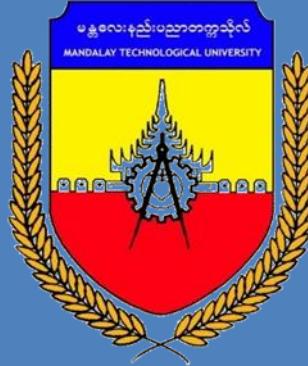


MANDALAY TECHNOLOGICAL UNIVERSITY

DEPARTMENT OF MECHATRONIC ENGINEERING



POWER ELECTRONICS II

McE 42036

Motto: Creative, Innovative, Mechatronics

Commonly used Power and Converter Equations

Instantaneous power: $p(t) = v(t)i(t)$

Energy: $W = \int_{t_1}^{t_2} p(t) dt$

Average power: $P = \frac{W}{T} = \frac{1}{T} \int_{t_0}^{t_0+T} p(t) dt = \frac{1}{T} \int_{t_0}^{t_0+T} v(t)i(t) dt$

Average power for a dc voltage source: $P_{dc} = V_{dc} I_{avg}$

rms voltage: $V_{rms} = \sqrt{\frac{1}{T} \int_0^T v^2(t) dt}$

rms for $v = v_1 + v_2 + v_3 + \dots$: $V_{rms} = \sqrt{V_{1,rms}^2 + V_{2,rms}^2 + V_{3,rms}^2 + \dots}$

rms current for a triangular wave: $I_{rms} = \frac{I_m}{\sqrt{3}}$

rms current for an offset triangular wave: $I_{rms} = \sqrt{\left(\frac{I_m}{\sqrt{3}}\right)^2 + I_{dc}^2}$

rms voltage for a sine wave or a full-wave rectified sine wave: $V_{rms} = \frac{V_m}{\sqrt{2}}$

rms voltage for a half-wave rectified sine wave: $V_{\text{rms}} = \frac{V_m}{2}$

Power factor: $\text{pf} = \frac{P}{S} = \frac{P}{V_{\text{rms}} I_{\text{rms}}}$

Total harmonic distortion: $\text{THD} = \sqrt{\sum_{n=2}^{\infty} I_n^2}$

Distortion factor: $\text{DF} = \sqrt{\frac{1}{1 + (\text{THD})^2}}$

Form factor = $\frac{I_{\text{rms}}}{I_{\text{avg}}}$

Crest factor = $\frac{I_{\text{peak}}}{I_{\text{rms}}}$

Buck converter: $V_o = V_s D$

Boost converter: $V_o = \frac{V_s}{1 - D}$

Buck-boost and Ćuk converters: $V_o = -V_s \left(\frac{D}{1 - D} \right)$

SEPIC: $V_o = V_s \left(\frac{D}{1 - D} \right)$

Flyback converter: $V_o = V_s \left(\frac{D}{1 - D} \right) \left(\frac{N_2}{N_1} \right)$

Forward converter: $V_o = V_s D \left(\frac{N_2}{N_1} \right)$

BRIEF CONTENTS

Chapter 1

Introduction 1

Chapter 2

Power Computations 21

Chapter 3

Half-Wave Rectifiers 65

Chapter 4

Full-Wave Rectifiers 111

Chapter 5

AC Voltage Controllers 171

Chapter 6

DC-DC Converters 196

Chapter 7

DC Power Supplies 265

Chapter 8

Inverters 331

Chapter 9

Resonant Converters 387

Chapter 10

**Drive Circuits, Snubber Circuits,
and Heat Sinks** 431

**Appendix A Fourier Series for Some
Common Waveforms** 461

Appendix B State-Space Averaging 467

Index 473

AC Voltage Controllers

AC to ac Converters

5.1 INTRODUCTION

An ac voltage controller is a converter that controls the voltage, current, and average power delivered to an ac load from an ac source. Electronic switches connect and disconnect the source and the load at regular intervals. In a switching scheme called phase control, switching takes place during every cycle of the source, in effect removing some of the source waveform before it reaches the load. Another type of control is integral-cycle control, whereby the source is connected and disconnected for several cycles at a time.

The phase-controlled ac voltage controller has several practical uses including light-dimmer circuits and speed control of induction motors. The input voltage source is ac, and the output is ac (although not sinusoidal), so the circuit is classified as an ac-ac converter.

5.2 THE SINGLE-PHASE AC VOLTAGE CONTROLLER

Basic Operation

A basic single-phase voltage controller is shown in Fig. 5-1a. The electronic switches are shown as parallel thyristors (SCRs). This SCR arrangement makes it possible to have current in either direction in the load. This SCR connection is called antiparallel or inverse parallel because the SCRs carry current in opposite directions. A triac is equivalent to the antiparallel SCRs. Other controlled switching devices can be used instead of SCRs.

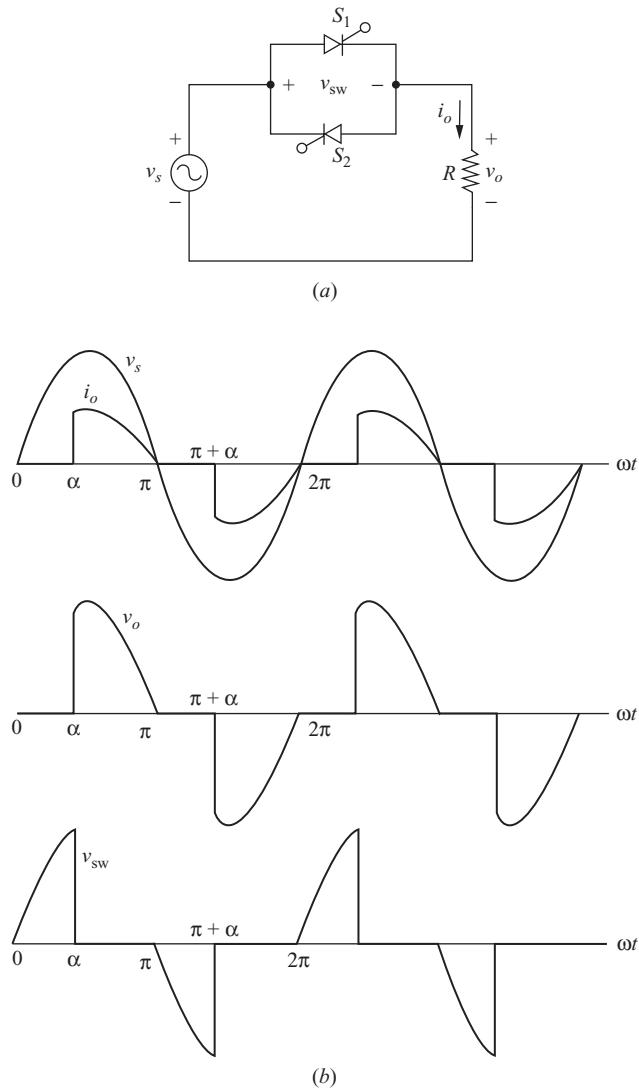


Figure 5-1 (a) Single-phase ac voltage controller with a resistive load; (b) Waveforms.

The principle of operation for a single-phase ac voltage controller using phase control is quite similar to that of the controlled half-wave rectifier of Sec. 3.9. Here, load current contains both positive and negative half-cycles. An analysis identical to that done for the controlled half-wave rectifier can be done on a half-cycle for the voltage controller. Then, by symmetry, the result can be extrapolated to describe the operation for the entire period.

Some basic observations about the circuit of Fig. 5-1a are as follows:

1. The SCRs cannot conduct simultaneously.
2. The load voltage is the same as the source voltage when either SCR is on. The load voltage is zero when both SCRs are off.
3. The switch voltage v_{sw} is zero when either SCR is on and is equal to the source voltage when neither is on.
4. The average current in the source and load is zero if the SCRs are on for equal time intervals. The average current in each SCR is not zero because of unidirectional SCR current.
5. The rms current in each SCR is $1/\sqrt{2}$ times the rms load current if the SCRs are on for equal time intervals. (Refer to Chap. 2.)

For the circuit of Fig. 5-1a, S_1 conducts if a gate signal is applied during the positive half-cycle of the source. Just as in the case of the SCR in the controlled half-wave rectifier, S_1 conducts until the current in it reaches zero. Where this circuit differs from the controlled half-wave rectifier is when the source is in its negative half-cycle. A gate signal is applied to S_2 during the negative half-cycle of the source, providing a path for negative load current. If the gate signal for S_2 is a half period later than that of S_1 , analysis for the negative half-cycle is identical to that for the positive half, except for algebraic sign for the voltage and current.

Single-Phase Controller with a Resistive Load

Figure 5-1b shows the voltage waveforms for a single-phase phase-controlled voltage controller with a resistive load. These are the types of waveforms that exist in a common incandescent light-dimmer circuit. Let the source voltage be

$$v_s(\omega t) = V_m \sin \omega t \quad (5-1)$$

Output voltage is

$$v_o(\omega t) = \begin{cases} V_m \sin \omega t & \text{for } \alpha < \omega t < \pi \text{ and } \alpha + \pi < \omega t < 2\pi \\ 0 & \text{otherwise} \end{cases} \quad (5-2)$$

The rms load voltage is determined by taking advantage of positive and negative symmetry of the voltage waveform, necessitating evaluation of only a half-period of the waveform:

$$V_{o,\text{rms}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\pi} [V_m \sin(\omega t)]^2 d(\omega t)} = \frac{V_m}{\sqrt{2}} \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}} \quad (5-3)$$

Note that for $\alpha = 0$, the load voltage is a sinusoid that has the same rms value as the source. Normalized rms load voltage is plotted as a function of α in Fig. 5-2.

The rms current in the load and the source is

$$I_{o,\text{rms}} = \frac{V_{o,\text{rms}}}{R} \quad (5-4)$$

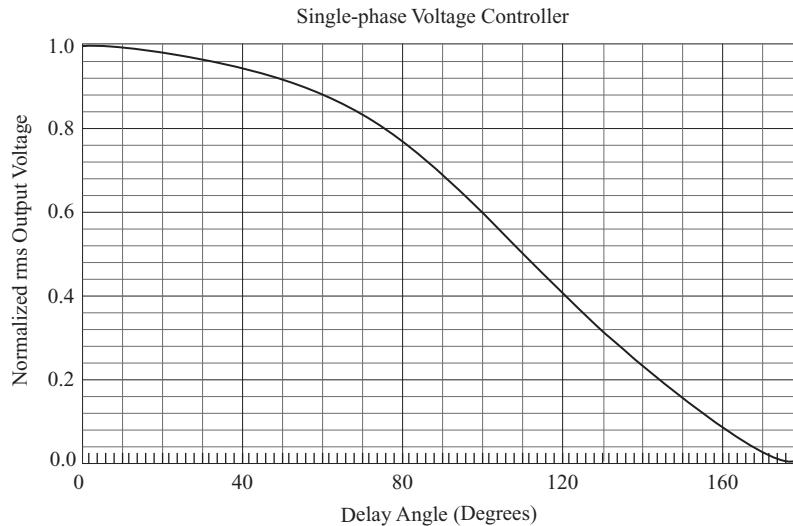


Figure 5-2 Normalized rms load voltage vs. delay angle for a single-phase ac voltage controller with a resistive load.

and the power factor of the load is

$$\begin{aligned}
 \text{pf} &= \frac{P}{S} = \frac{P}{V_{s,\text{rms}} I_{s,\text{rms}}} = \frac{V_{o,\text{rms}}^2 / R}{V_{s,\text{rms}} (V_{o,\text{rms}} / R)} = \frac{V_{o,\text{rms}}}{V_{s,\text{rms}}} \\
 &= \frac{\frac{V_m}{\sqrt{2}} \sqrt{1 - \frac{\alpha}{\pi} + \frac{(\sin 2\alpha)}{2\pi}}}{V_m / \sqrt{2}}
 \end{aligned}$$

$$\boxed{\text{pf} = \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}}} \quad (5-5)$$

Note that $\text{pf} = 1$ for $\alpha = 0$, which is the same as for an uncontrolled resistive load, and the power factor for $\alpha > 0$ is less than 1.

The average source current is zero because of half-wave symmetry. The average SCR current is

$$I_{\text{SCR, avg}} = \frac{1}{2\pi} \int_{\alpha}^{\pi} \frac{V_m \sin(\omega t)}{R} d(\omega t) = \frac{V_m}{2\pi R} (1 + \cos \alpha) \quad (5-6)$$

Since each SCR carries one-half of the line current, the rms current in each SCR is

$$I_{\text{SCR, rms}} = \frac{I_{o,\text{rms}}}{\sqrt{2}} \quad (5-7)$$

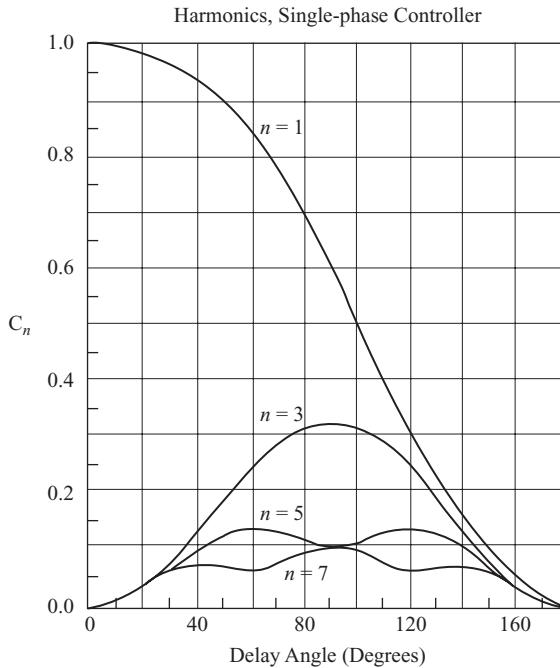


Figure 5-3 Normalized harmonic content vs. delay angle for a single-phase ac voltage controller with a resistive load; C_n is the normalized amplitude. (See Chap. 2.)

Since the source and load current is nonsinusoidal, harmonic distortion is a consideration when designing and applying ac voltage controllers. Only odd harmonics exist in the line current because the waveform has half-wave symmetry. Harmonic currents are derived from the defining Fourier equations in Chap. 2. Normalized harmonic content of the line currents vs. α is shown in Fig. 5-3. Base current is source voltage divided by resistance, which is the current for $\alpha = 0$.

EXAMPLE 5-1

Single-Phase Controller with a Resistive Load

The single-phase ac voltage controller of Fig. 5-1a has a 120-V rms 60-Hz source. The load resistance is $15\ \Omega$. Determine (a) the delay angle required to deliver 500 W to the load, (b) the rms source current, (c) the rms and average currents in the SCRs, (d) the power factor, and (e) the total harmonic distortion (THD) of the source current.

■ Solution

- (a) The required rms voltage to deliver 500 W to a $15\ \Omega$ load is

$$P = \frac{V_{o,\text{rms}}^2}{R}$$

$$V_{o,\text{rms}} = \sqrt{PR} = \sqrt{(500)(15)} = 86.6\ \text{V}$$

The relationship between output voltage and delay angle is described by Eq. (5-3) and Fig. 5-2. From Fig. 5-2, the delay angle required to obtain a normalized output of $86.6/120 = 0.72$ is approximately 90° . A more precise solution is obtained from the numerical solution for α in Eq. (5-3), expressed as

$$86.6 - 120\sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}} = 0$$

which yields

$$\alpha = 1.54 \text{ rad} = 88.1^\circ$$

(b) Source rms current is

$$I_{o,\text{rms}} = \frac{V_{o,\text{rms}}}{R} = \frac{86.6}{15} = 5.77 \text{ A}$$

(c) SCR currents are determined from Eqs. (5-6) and (5-7),

$$I_{\text{SCR,rms}} = \frac{I_{\text{rms}}}{\sqrt{2}} = \frac{5.77}{\sqrt{2}} = 4.08 \text{ A}$$

$$I_{\text{SCR,avg}} = \frac{\sqrt{2}(120)}{2\pi(15)} [1 + \cos(88.1^\circ)] = 1.86 \text{ A}$$

(d) The power factor is

$$\text{pf} = \frac{P}{S} = \frac{500}{(120)(5.77)} = 0.72$$

which could also be computed from Eq. (5-5).

(e) Base rms current is

$$I_{\text{base}} = \frac{V_{s,\text{rms}}}{R} = \frac{120}{15} = 8.0 \text{ A}$$

The rms value of the current's fundamental frequency is determined from C_1 in the graph of Fig. 5-3.

$$C_1 \approx 0.61 \Rightarrow I_{1,\text{rms}} = C_1 I_{\text{base}} = (0.61)(8.0) = 4.9 \text{ A}$$

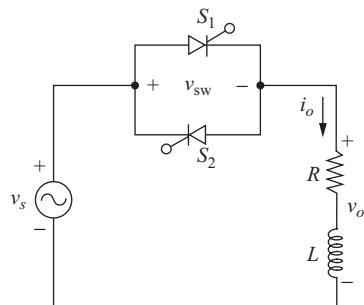
The THD is computed from Eq. (2-68),

$$\text{THD} = \frac{\sqrt{I_{\text{rms}}^2 - I_{1,\text{rms}}^2}}{I_{1,\text{rms}}} = \frac{\sqrt{5.77^2 - 4.9^2}}{4.9} = 0.63 = 63\%$$

Single-Phase Controller with an *RL* Load

Figure 5-4a shows a single-phase ac voltage controller with an *RL* load. When a gate signal is applied to S_1 at $\omega t = \alpha$, Kirchhoff's voltage law for the circuit is expressed as

$$V_m \sin(\omega t) = R i_o(t) + L \frac{di_o(t)}{dt} \quad (5-8)$$



(a)

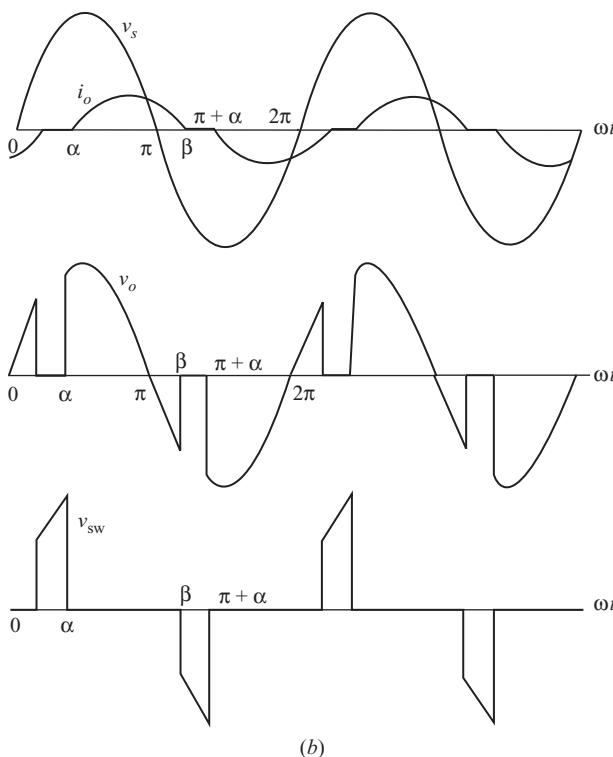


Figure 5-4 (a) Single-phase ac voltage controller with an *RL* load; (b) Typical waveforms.

The solution for current in this equation, outlined in Sec. 3.9, is

$$i_o(\omega t) = \begin{cases} \frac{V_m}{Z} \left[\sin(\omega t - \theta) - \sin(\alpha - \theta) e^{(\alpha - \omega t)/\omega\tau} \right] & \text{for } \alpha \leq \omega t \leq \beta \\ 0 & \text{otherwise} \end{cases} \quad (5-9)$$

where

$$Z = \sqrt{R^2 + (\omega L)^2}, \quad \text{and} \quad \theta = \tan^{-1}\left(\frac{\omega L}{R}\right)$$

The extinction angle β is the angle at which the current returns to zero, when $\omega t = \beta$,

$$i_o(\beta) = 0 = \frac{V_m}{Z} \left[\sin(\beta - \theta) - \sin(\alpha - \theta) e^{(\alpha - \beta)/\omega\tau} \right] \quad (5-10)$$

which must be solved numerically for β .

A gate signal is applied to S_2 at $\omega t = \pi + \alpha$, and the load current is negative but has a form identical to that of the positive half-cycle. Figure 5-4b shows typical waveforms for a single-phase ac voltage controller with an RL load.

The conduction angle γ is defined as

$$\gamma = \beta - \alpha \quad (5-11)$$

In the interval between π and β when the source voltage is negative and the load current is still positive, S_2 cannot be turned on because it is not forward-biased. The gate signal to S_2 must be delayed at least until the current in S_1 reaches zero, at $\omega t = \beta$. The delay angle is therefore at least $\beta - \pi$.

$$\alpha \geq \beta - \pi \quad (5-12)$$

The limiting condition when $\beta - \alpha = \pi$ is determined from an examination of Eq. (5-10). When $\alpha = \theta$, Eq. (5-10) becomes

$$\sin(\beta - \alpha) = 0$$

which has a solution

$$\beta - \alpha = \pi$$

Therefore,

$$\gamma = \pi \quad \text{when } \alpha = \theta \quad (5-13)$$

If $\alpha < \theta$, $\gamma = \pi$, provided that the gate signal is maintained beyond $\omega t = \theta$.

In the limit, when $\gamma = \pi$, one SCR is always conducting, and the voltage across the load is the same as the voltage of the source. The load voltage and current are sinusoids for this case, and the circuit is analyzed using phasor analysis for ac circuits. *The power delivered to the load is continuously controllable between the two extremes corresponding to full source voltage and zero.*

This SCR combination can act as a *solid-state relay*, connecting or disconnecting the load from the ac source by gate control of the SCRs. The load is disconnected from the source when no gate signal is applied, and the load has the same voltage as the source when a gate signal is continuously applied. In practice, the gate signal may be a high-frequency series of pulses rather than a continuous dc signal.

An expression for rms load current is determined by recognizing that the square of the current waveform repeats every π rad. Using the definition of rms,

$$I_{o,\text{rms}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\beta} i_o^2(\omega t) d(\omega t)} \quad (5-14)$$

where $i_o(\omega t)$ is described in Eq. (5-9).

Power absorbed by the load is determined from

$$P = I_{o,\text{rms}}^2 R \quad (5-15)$$

The rms current in each SCR is

$$I_{\text{SCR},\text{rms}} = \frac{I_{o,\text{rms}}}{\sqrt{2}} \quad (5-16)$$

The average load current is zero, but each SCR carries one-half of the current waveform, making the average SCR current

$$I_{\text{SCR},\text{avg}} = \frac{1}{2\pi} \int_{\alpha}^{\beta} i_o(\omega t) d(\omega t) \quad (5-17)$$

EXAMPLE 5-2

Single-Phase Voltage Controller with RL Load

For the single-phase voltage controller of Fig. 5-4a, the source is 120 V rms at 60 Hz, and the load is a series RL combination with $R = 20 \Omega$ and $L = 50 \text{ mH}$. The delay angle α is 90° . Determine (a) an expression for load current for the first half-period, (b) the rms load current, (c) the rms SCR current, (d) the average SCR current, (e) the power delivered to the load, and (f) the power factor.

■ Solution

(a) The current is expressed as in Eq. (5-9). From the parameters given,

$$Z = \sqrt{R^2 + (\omega L)^2} = \sqrt{(20)^2 + [(377)(0.05)]^2} = 27.5 \Omega$$

$$\theta = \tan^{-1}\left(\frac{\omega L}{R}\right) = \tan^{-1}\frac{(377)(0.05)}{20} = 0.756 \text{ rad}$$

$$\omega\tau = \omega\left(\frac{L}{R}\right) = 377\left(\frac{0.05}{20}\right) = 0.943 \text{ rad}$$

$$\frac{V_m}{Z} = \frac{120\sqrt{2}}{27.5} = 6.18 \text{ A}$$

$$\alpha = 90^\circ = 1.57 \text{ rad}$$

$$\frac{V_m}{Z} \sin(\alpha - \theta) e^{\alpha/\omega\tau} = 23.8 \text{ A}$$

The current is then expressed in Eq. (5-9) as

$$i_o(\omega t) = 6.18 \sin(\omega t - 0.756) - 23.8e^{-\omega t/0.943} \text{ A} \quad \text{for } \alpha \leq \omega t \leq \beta$$

The extinction angle β is determined from the numerical solution of $i(\beta) = 0$ in the above equation, yielding

$$\beta = 3.83 \text{ rad} = 220^\circ$$

Note that the conduction angle $\gamma = \beta - \alpha = 2.26 \text{ rad} = 130^\circ$, which is less than the limit of 180° .

(b) The rms load current is determined from Eq. (5-14).

$$I_{o,\text{rms}} = \sqrt{\frac{1}{\pi} \int_{1.57}^{3.83} [6.18 \sin(\omega t - 0.756) - 23.8e^{-\omega t/0.943}] d(\omega t)} = 2.71 \text{ A}$$

(c) The rms current in each SCR is determined from Eq. (5-16).

$$I_{\text{SCR},\text{rms}} = \frac{I_{o,\text{rms}}}{\sqrt{2}} = \frac{2.71}{\sqrt{2}} = 1.92 \text{ A}$$

(d) Average SCR current is obtained from Eq. (5-17).

$$I_{\text{SCR, avg}} = \frac{1}{2\pi} \int_{1.57}^{3.83} [6.18 \sin(\omega t - 0.756) - 23.8e^{-\omega t/0.943}] d(\omega t) = 1.04 \text{ A}$$

(e) Power absorbed by the load is

$$P = I_{o,\text{rms}}^2 R = (2.71)^2 (20) = 147 \text{ W}$$

(f) Power factor is determined from P/S .

$$\text{pf} = \frac{P}{S} = \frac{P}{V_{s,\text{rms}} I_{s,\text{rms}}} = \frac{147}{(120)(2.71)} = 0.45 = 45\%$$

PSpice Simulation of Single-Phase AC Voltage Controllers

The PSpice simulation of single-phase voltage controllers is very similar to the simulation of the controlled half-wave rectifier. The SCR is modeled with a diode and voltage-controlled switch. The diodes limit the currents to positive values, thus duplicating SCR behavior. The two switches are complementary, each closed for one-half the period.

The Schematic Capture circuit requires the full version, whereas the text CIR file will run on the PSpice A/D Demo version.

EXAMPLE 5-3

PSpice Simulation of a Single-Phase Voltage Controller

Use PSpice to simulate the circuit of Example 5-2. Determine the rms load current, the rms and average SCR currents, load power, and total harmonic distortion in the source current. Use the default diode model in the SCR.

Solution

The circuit for the simulation is shown in Fig. 5-5. This requires the full version of Schematic Capture.

The PSpice circuit file for the A/D Demo version is as follows:

```
SINGLE-PHASE VOLTAGE CONTROLLER (voltcont.cir)
*** OUTPUT VOLTAGE IS V(3) , OUTPUT CURRENT IS I(R) ***
***** INPUT PARAMETERS *****
.PARAM VS = 120 ;source rms voltage
.PARAM ALPHA = 90 ;delay angle in degrees
.PARAM R = 20 ;load resistance
.PARAM L = 50mH ;load inductance
.PARAM F = 60 ;frequency
.PARAM TALPHA = {ALPHA/(360*F)} PW 5 {0.5/F} ;converts angle to time delay

***** CIRCUIT DESCRIPTION *****
VS 1 0 SIN(0 {VS*SQRT(2)} {F})
S1 1 2 11 0 SMOD
D1 2 3 DMOD ; FORWARD SCR
S2 3 5 0 11 SMOD
```

AC VOLTAGE CONTROLLER

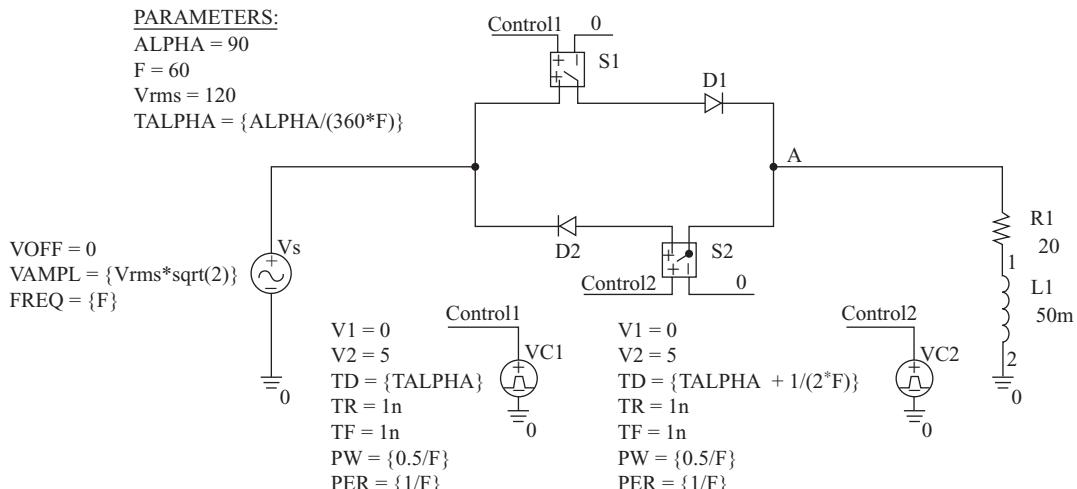


Figure 5-5 The circuit schematic for a single-phase ac voltage controller. The full version of Schematic Capture is required for this circuit.

```

D2 5 1 DMOD ; REVERSE SCR
R 3 4 {R}
L 4 0 {L}

***** MODELS AND COMMANDS *****
.MODEL DMOD D
.MODEL SMOD VSWITCH (RON=.01)
VCONTROL 11 0 PULSE(-10 10 {TALPHA} 0 0 {PW} {1/F}) ;control for both
switches
.TRAN .1MS 33.33MS 16.67MS .1MS UIC ;one period of output
.FOUR 60 I(R) ;Fourier Analysis to get THD
.PROBE
.END

```

Using the PSpice A/D input file for the simulation, the Probe output of load current and related quantities is shown in Fig. 5-6. From Probe, the following quantities are obtained:

Quantity	Expression	Result
RMS load current	RMS(I(R))	2.59 A
RMS SCR current	RMS(I(S1))	1.87 A
Average SCR current	AVG(I(S1))	1.01 A
Load power	AVG(W(R))	134 W
Total harmonic distortion	(from the output file)	31.7%

Note that the nonideal SCRs (using the default diode) result in smaller currents and load power than for the analysis in Example 5-2 which assumed ideal SCRs. A model for the particular SCR that will be used to implement the circuit will give a more accurate prediction of actual circuit performance.

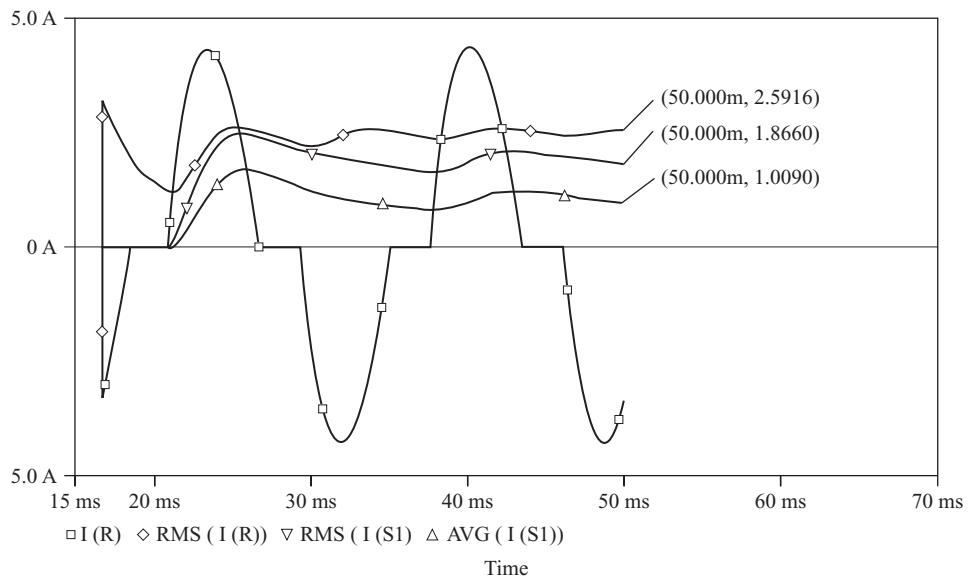
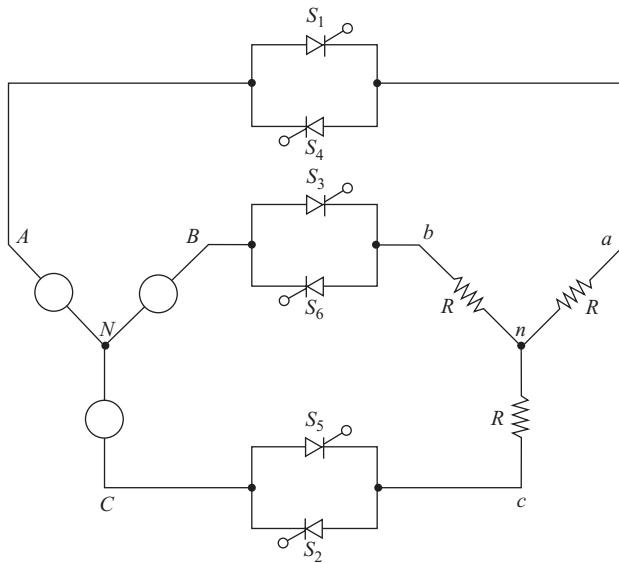


Figure 5-6 Probe output for Example 5-3.

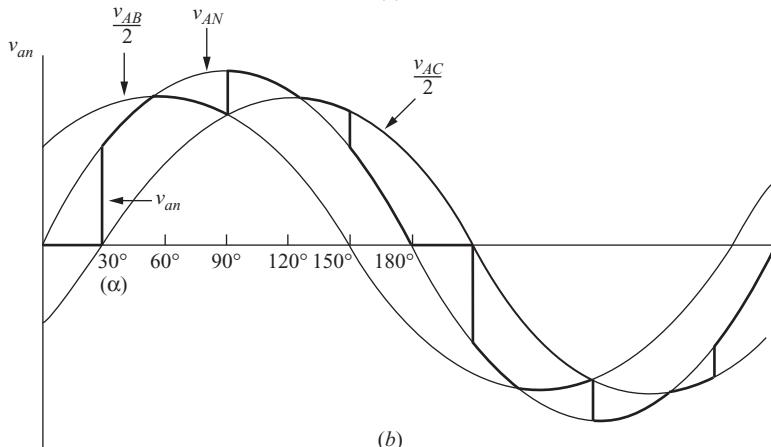
5.3 THREE-PHASE VOLTAGE CONTROLLERS

Y-Connected Resistive Load

A three-phase voltage controller with a *Y*-connected resistive load is shown in Fig. 5-7a. The power delivered to the load is controlled by the delay angle α on each SCR. The six SCRs are turned on in the sequence 1-2-3-4-5-6, at 60° intervals. Gate signals are maintained throughout the possible conduction angle.



(a)



(b)

Figure 5-7 (a) Three-phase ac voltage controller with a *Y*-connected resistive load; (b) Load voltage v_{an} for $\alpha = 30^\circ$; (c) Load voltages and switch currents for a three-phase resistive load for $\alpha = 30^\circ$; (d) Load voltage v_{an} for $\alpha = 75^\circ$; (e) Load voltage v_{an} for $\alpha = 120^\circ$.

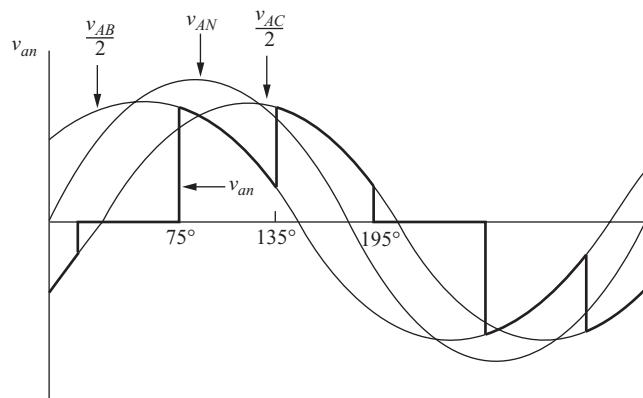
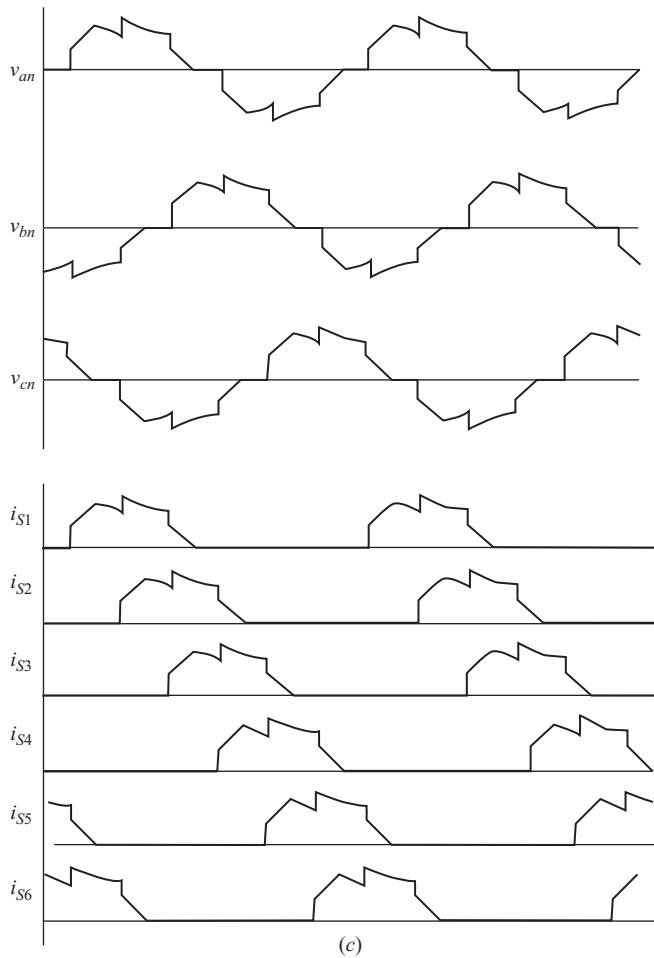


Figure 5-7 (continued)

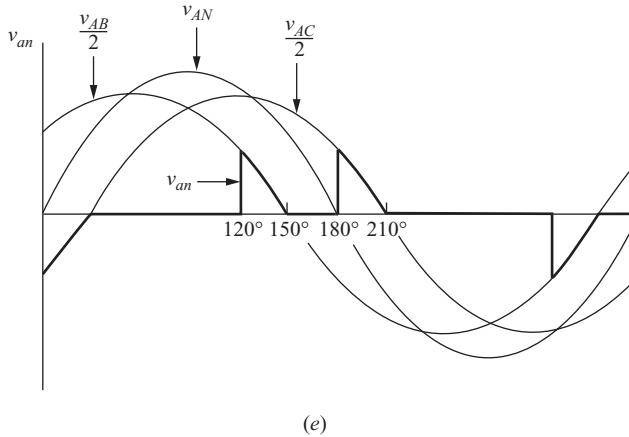


Figure 5-7 (continued)

The instantaneous voltage across each phase of the load is determined by which SCRs are conducting. At any instant, three SCRs, two SCRs, or no SCRs are on. The instantaneous load voltages are either a line-to-neutral voltage (three on), one-half of a line-to-line voltage (two on), or zero (none on).

When three SCRs are on (one in each phase), all three phase voltages are connected to the source, corresponding to a balanced three-phase source connected to a balanced three-phase load. The voltage across each phase of the load is the corresponding line-to-neutral voltage. For example, if S_1 , S_2 , and S_6 are on, $v_{an} = v_{AN}$, $v_{bn} = v_{BN}$, and $v_{cn} = v_{CN}$. When two SCRs are on, the line-to-line voltage of those two phases is equally divided between the two load resistors that are connected. For example, if only S_1 and S_2 are on, $v_{an} = v_{AC}/2$, $v_{cn} = v_{CA}/2$, and $v_{bn} = 0$.

Which SCRs are conducting depends on the delay angle α and on the source voltages at a particular instant. The following are the ranges of α that produce particular types of load voltages with an example for each:

For $0 < \alpha < 60^\circ$:

Two or three SCRs conduct at any one time for this range of α . Figure 5-7b shows the load line-to-neutral voltage v_{an} for $\alpha = 30^\circ$. At $\omega t = 0$, S_5 and S_6 are conducting and there is no current in R_a , making $v_{an} = 0$. At $\omega t = \pi/6 (30^\circ)$, S_1 receives a gate signal and begins to conduct; S_5 and S_6 remain on, and $v_{an} = v_{AN}$. The current in S_5 reaches zero at 60° , turning S_5 off. With S_1 and S_6 remaining on, $v_{an} = v_{AB}/2$. At 90° , S_2 is turned on; the three SCRs S_1 , S_2 , and S_6 are then on; and $v_{an} = v_{AN}$. At 120° , S_6 turns off, leaving S_1 and S_2 on, so $v_{an} = v_{AC}/2$. As the firing sequence for the SCRs proceeds, the number of SCRs on at a particular instant alternates between 2 and 3. All three phase-to-neutral load voltages and switch currents are shown in Fig. 5-7c. For intervals to exist when three SCRs are on, the delay angle must be less than 60° .

For $60^\circ < \alpha < 90^\circ$:

Only two SCRs conduct at any one time when the delay angle is between 60 and 90° . Load = voltage v_{an} for $\alpha = 75^\circ$ is shown in Fig. 5-7d. Just

prior to 75° , S_5 and S_6 are conducting, and $v_{an} = 0$. When S_1 is turned on at 75° , S_6 continues to conduct, but S_5 must turn off because v_{CN} is negative. Voltage v_{an} is then $v_{AB}/2$. When S_2 is turned on at 135° , S_6 is forced off, and $v_{an} = v_{AC}/2$. The next SCR to turn on is S_3 , which forces S_1 off, and $v_{an} = 0$. One SCR is always forced off when an SCR is turned on for α in this range. Load voltages are one-half line-to-line voltages or zero.

For $90^\circ < \alpha < 150^\circ$:

Only two SCRs can conduct at any one time in this mode. Additionally, there are intervals when no SCRs conduct. Figure 5-7e shows the load voltage v_{an} for $\alpha = 120^\circ$. In the interval just prior to 120° , no SCRs are on, and $v_{an} = 0$. At $\alpha = 120^\circ$, S_1 is given a gate signal, and S_6 still has a gate signal applied. Since v_{AB} is positive, both S_1 and S_6 are forward-biased and begin to conduct, and $v_{an} = v_{AB}/2$. Both S_1 and S_6 turn off when v_{AB} becomes negative. When a gate signal is applied to S_2 , it turns on, and S_1 turns on again.

For $\alpha > 150^\circ$, there is no time interval when an SCR is forward-biased while a gate signal is applied. Output voltage is zero for this condition.

Normalized output voltage vs. delay angle is shown in Fig. 5-8. Note that a delay angle of zero corresponds to the load being connected directly to the

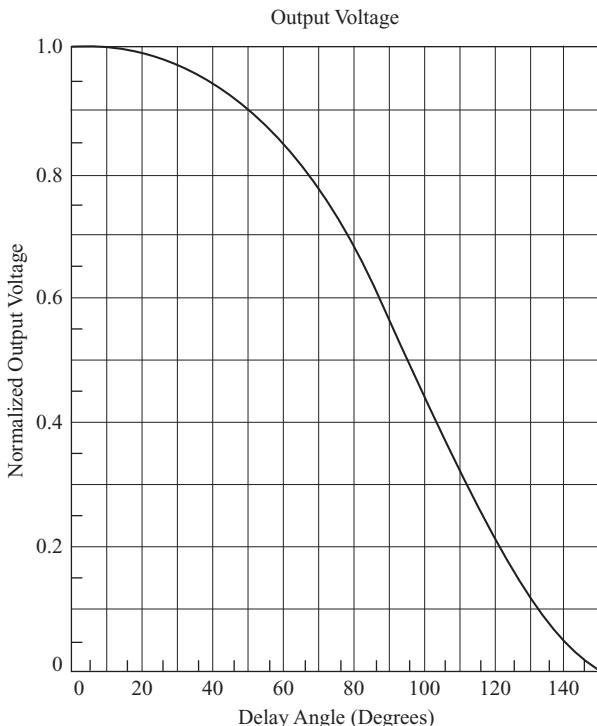


Figure 5-8 Normalized rms output voltage for a three-phase ac voltage controller with a resistive load.

three-phase source. The range of output voltage for the three-phase voltage controller is between full source voltage and zero.

Harmonic currents in the load and line for the three-phase ac voltage controller are the odd harmonics of order $6n \pm 1$, $n = 1, 2, 3, \dots$ (that is, 5th, 7th, 11th, 13th). . . . Harmonic filters may be required in some applications to prevent harmonic currents from propagating into the ac system.

Since analysis of the three-phase ac voltage controller is cumbersome, simulation is a practical means of obtaining rms output voltages and power delivered to a load. PSpice simulation is presented in Example 5-4.

Y-Connected *RL* Load

The load voltages for a three-phase voltage controller with an *RL* load are again characterized by being a line-to-neutral voltage, one-half of a line-to-line voltage, or zero. The analysis is much more difficult for an *RL* load than for a resistive load, and simulation provides results that would be extremely difficult to obtain analytically. Example 5-4 illustrates the use of PSpice for a three-phase ac voltage controller.

EXAMPLE 5-4

PSpice Simulation of a Three-Phase Voltage Controller

Use PSpice to obtain the power delivered to a *Y*-connected three-phase load. Each phase of the load is a series *RL* combination with $R = 10 \Omega$ and $L = 30 \text{ mH}$. The three-phase source is 480 V rms line-to-line at 60 Hz, and the delay angle α is 75° . Determine the rms value of the line currents, the power absorbed by the load, the power absorbed by the SCRs, and the total harmonic distortion (THD) of the source currents.

■ Solution

A PSpice A/D input file for the *Y*-connected three-phase voltage controller with an *RL* load is as follows:

```
THREE-PHASE VOLTAGE CONTROLLER-R-L LOAD (3phvc.cir)
*SOURCE AND LOAD ARE Y-CONNECTED (UNGROUNDED)
***** INPUT PARAMETERS *****
.PARAM Vs = 480
; rms line-to-line voltage
.PARAM ALPHA = 75
; delay angle in degrees
.PARAM R = 10
; load resistance (y-connected)
.PARAM L = 30mH
; load inductance
.PARAM F = 60
; source frequency

***** COMPUTED PARAMETERS *****
.PARAM Vm = {Vs*SQRT(2)/SQRT(3)} ; convert to peak line-neutral volts
.PARAM DLAY = {1/(6*F)} ; switching interval is 1/6 period
.PARAM PW = {.5/F} TALPHA={ALPHA/(F*360)}
.PARAM TRF = 10US ; rise and fall time for pulse switch control
```

```
*****
THREE-PHASE SOURCE *****
VAN 1 0 SIN(0 {VM} 60)
VBN 2 0 SIN(0 {VM} 60 0 0 -120)
VCN 3 0 SIN(0 {VM} 60 0 0 -240)

*****
SWITCHES *****
S1 1 8 18 0 SMOD ; A-phase
D1 8 4 DMOD
S4 4 9 19 0 SMOD
D4 9 1 DMOD

S3 2 10 20 0 SMOD ; B-phase
D3 10 5 DMOD
S6 5 11 21 0 SMOD
D6 11 2 DMOD

S5 3 12 22 0 SMOD ; C-phase
D5 12 6 DMOD
S2 6 13 23 0 SMOD
D2 13 3 DMOD

*****
LOAD *****
RA 4 4A {R} ; van = v(4,7)
LA 4A 7 {L}

RB 5 5A {R} ; vbn = v(5,7)
LB 5A 7 {L}

RC 6 6A {R} ; vcn = v(6,7)
LC 6A 7 {L}

*****
SWITCH CONTROL *****
V1 18 0 PULSE(-10 10 {TALPHA} {TRF} {TRF} {PW} {1/F})
V4 19 0 PULSE(-10 10 {TALPHA+3*DLAY} {TRF} {TRF} {PW} {1/F})
V3 20 0 PULSE(-10 10 {TALPHA+2*DLAY} {TRF} {TRF} {PW} {1/F})
V6 21 0 PULSE(-10 10 {TALPHA+5*DLAY} {TRF} {TRF} {PW} {1/F})
V5 22 0 PULSE(-10 10 {TALPHA+4*DLAY} {TRF} {TRF} {PW} {1/F})
V2 23 0 PULSE(-10 10 {TALPHA+DLAY} {TRF} {TRF} {PW} {1/F})

*****
MODELS AND COMMANDS *****
.MODEL SMOD VSWITCH(RON=0.01)
.MODEL DMOD D
.TRAN .1MS 50MS 16.67ms .05MS UIC
.FOUR 60 I(RA) ; Fourier analysis of line current
.PROBE
.OPTIONS NOPAGE ITL5=0
.END
```

Probe output of the steady-state current in one of the phases is shown in Fig. 5-9. The rms line current, load power, and power absorbed by the SCRs are obtained by entering the appropriate expression in Probe. The THD in the source current is determined from the Fourier analysis in the output file. The results are summarized in the following table.

Quantity	Expression	Result
RMS line current	RMS(I(RA))	12.86 A
Load power	3*AVG(V(4,7)*I(RA))	4960 W
Total SCR power absorbed	6*AVG(V(1,4)*I(S1))	35.1 W
THD of source current	(from the output file)	13.1%

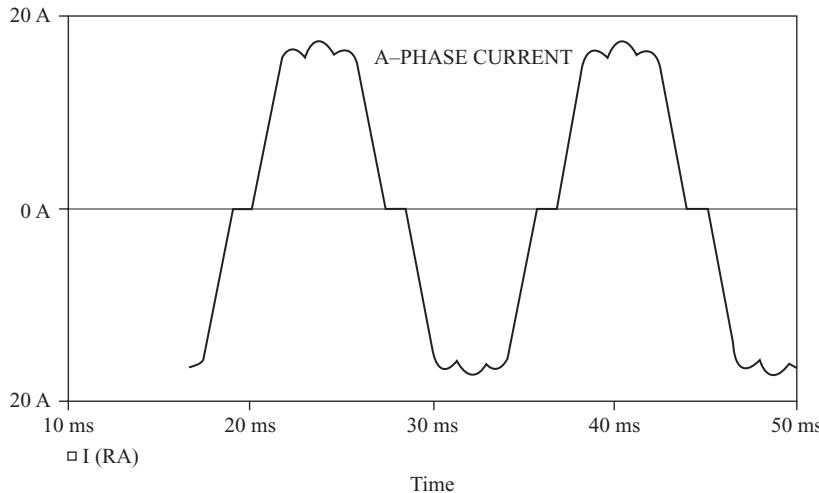


Figure 5-9 Probe output for Example 5-4.

Delta-Connected Resistive Load

A three-phase ac voltage controller with a delta-connected resistive load is shown in Fig. 5-10a. The voltage across a load resistor is the corresponding line-to-line voltage when a SCR in the phase is on. The delay angle is referenced to the zero crossing of the line-to-line voltage. SCRs are turned on in the sequence 1-2-3-4-5-6.

The line current in each phase is the sum of two of the delta currents:

$$\begin{aligned} i_a &= i_{ab} - i_{ca} \\ i_b &= i_{bc} - i_{ab} \\ i_c &= i_{ca} - i_{bc} \end{aligned} \quad (5-18)$$

The relationship between rms line and delta currents depends on the conduction angle of the SCRs. For small conduction angles (large α), the delta currents do not overlap (Fig. 5-10b), and the rms line currents are

$$I_{L,\text{rms}} = \sqrt{2} I_{\Delta,\text{rms}} \quad (5-19)$$

For large conduction angles (small α), the delta currents overlap (Fig. 5-10c), and the rms line current is larger than $\sqrt{2} I_{\Delta,\text{rms}}$. In the limit when $\gamma = \pi$ ($\alpha = 0$), the delta currents and line currents are sinusoids. The rms line current is determined from ordinary three-phase analysis.

$$I_{L,\text{rms}} = \sqrt{3} I_{\Delta,\text{rms}} \quad (5-20)$$

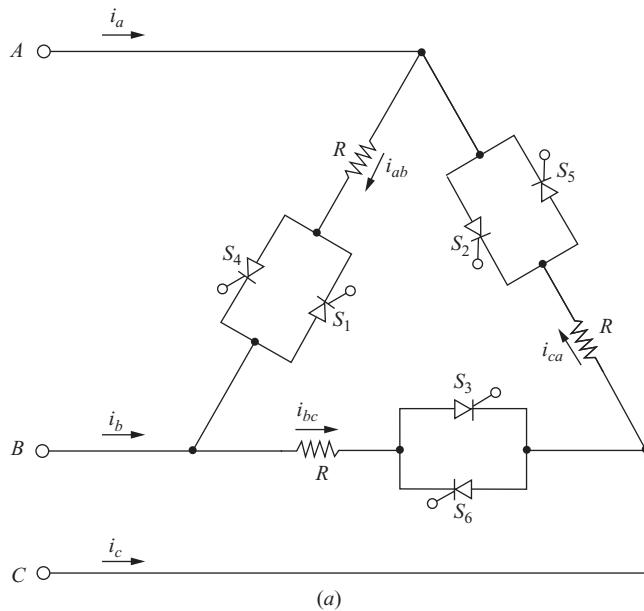
The range of rms line current is therefore

$$\sqrt{2} I_{\Delta,\text{rms}} \leq I_{L,\text{rms}} \leq \sqrt{3} I_{\Delta,\text{rms}} \quad (5-21)$$

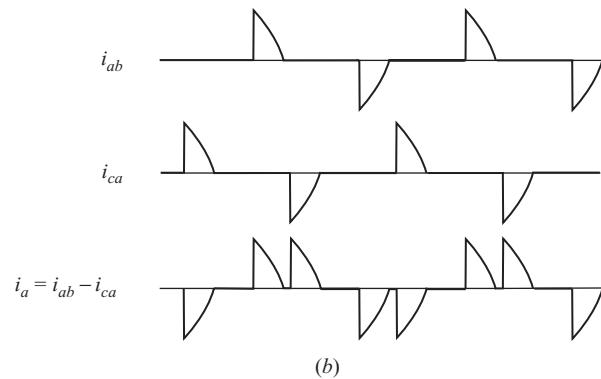
depending on α .

Figure 5-10

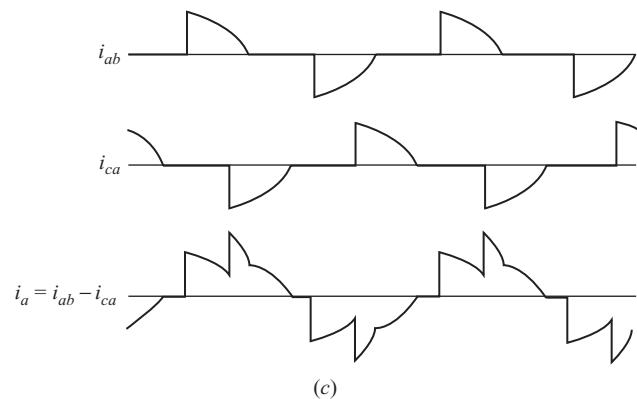
(a) Three-phase ac voltage controller with a delta-connected resistive load;
 (b) Current waveforms for $\alpha = 130^\circ$;
 (c) Current waveforms for $\alpha = 90^\circ$.



(a)



(b)



(c)

Use of the delta-connected three-phase voltage controller requires the load to be broken to allow thyristors to be inserted in each phase, which is often not feasible.

5.4 INDUCTION MOTOR SPEED CONTROL

Squirrel-cage induction motor speed can be controlled by varying the voltage and/or frequency. The ac voltage controller is suitable for some speed control applications. The torque produced by an induction motor is proportional to the square of the applied voltage. Typical torque-speed curves for an induction motor are shown in Fig. 5-11. If a load has a torque-speed characteristic like that also shown in Fig. 5-11, speed can be controlled by adjusting the motor voltage. Operating speed corresponds to the intersection of the torque-speed curves of the motor and the load. A fan or pump is a suitable load for this type of speed control, where the torque requirement is approximately proportional to the square of the speed.

Single-phase induction motors are controlled with the circuit of Fig. 5-4a, and three-phase motors are controlled with the circuit of Fig. 5-7a. Energy efficiency is poor when using this type of control, especially at low speeds. The large slip at low speeds results in large rotor losses. Typical applications exist where the load is small, such as single-phase fractional-horsepower motors, or where the time of low-speed operation is short. Motor speed control using a variable-frequency source from an inverter circuit (Chap. 8) is usually a preferred method.

5.5 STATIC VAR CONTROL

Capacitors are routinely placed in parallel with inductive loads for power factor improvement. If a load has a constant reactive voltampere (VAR) requirement, a fixed capacitor can be selected to correct the power factor to unity. However, if a

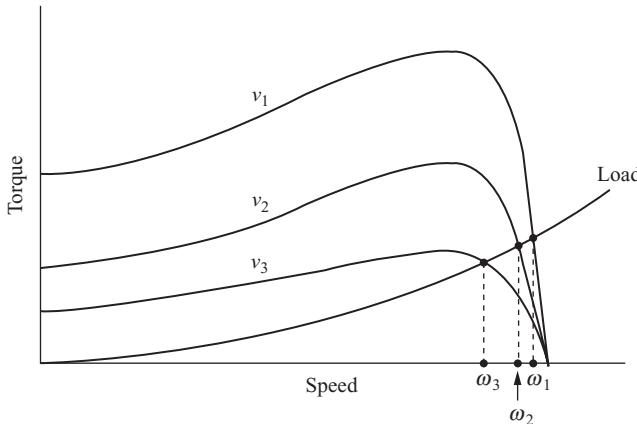


Figure 5-11 Torque-speed curves for an induction motor.

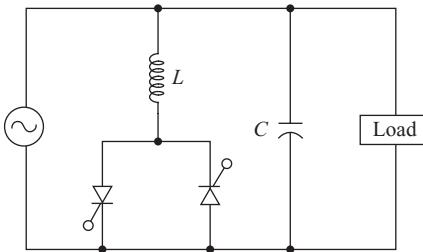


Figure 5-12 Static VAR control.

load has a varying VAR requirement, the fixed-capacitor arrangement results in a changing power factor.

The circuit of Fig. 5-12 represents an application of an ac voltage controller to maintain a unity power factor for varying load VAR requirements. The power factor correction capacitance supplies a fixed amount of reactive power, generally greater than required by the load. The parallel inductance absorbs a variable amount of reactive power, depending on the delay angle of the SCRs. The net reactive power supplied by the inductor-capacitor combination is controlled to match that absorbed by the load. As the VAR requirement of the load changes, the delay angle is adjusted to maintain unity power factor. This type of power factor correction is known as *static VAR control*.

The SCRs are placed in the inductor branch rather than in the capacitor branch because very high currents could result from switching a capacitor with a SCR.

Static VAR control has the advantage of being able to adjust to changing load requirements very quickly. Reactive power is continuously adjustable with static VAR control, rather than having discrete levels as with capacitor banks which are switched in and out with circuit breakers. Static VAR control is becoming increasingly prevalent in installations with rapidly varying reactive power requirements, such as electric arc furnaces. Filters are generally required to remove the harmonic currents generated by the switched inductance.

5.6 Summary

- Voltage controllers use electronic switches to connect and disconnect a load to an ac source at regular intervals. This type of circuit is classified as an ac-ac converter.
- Voltage controllers are used in applications such as single-phase light-dimmer circuits, single-phase or three-phase induction motor control, and static VAR control.
- The delay angle for the thyristors controls the time interval for the switch being on and thereby controls the effective value of voltage at the load. The range of control for load voltage is between full ac source voltage and zero.
- An ac voltage controller can be designed to function in either the fully on or fully off mode. This application is used as a solid-state relay.
- The load and source current and voltage in ac voltage controller circuits may contain significant harmonics. For equal delay angles in the positive and negative half-cycles, the average source current is zero, and only odd harmonics exist.

- Three-phase voltage controllers can have Y - or Δ -connected loads.
- Simulation of single-phase or three-phase voltage controllers provides an efficient analysis method.

5.7 Bibliography

- B. K. Bose, *Power Electronics and Motor Drives: Advances and Trends*, Academic Press, New York, 2006.
- A. K. Chattopadhyay, *Power Electronics Handbook*, edited by M. H. Rashid, Academic Press, New York, 2001, Chapter 16.
- M. A. El-Sharkawi, *Fundamentals of Electric Drives*, Brooks/Cole, Pacific Grove, Calif., 2000.
- B. M. Han and S. I. Moon, "Static Reactive-Power Compensator Using Soft-Switching Current-Source Inverter," *IEEE Transactions on Power Electronics*, vol. 48, no. 6, December 2001.
- N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3d ed., Wiley, New York, 2003.
- M. H. Rashid, *Power Electronics: Circuits, Devices, and Systems*, 3d ed., Prentice-Hall, Upper Saddle River, N. J., 2004.
- R. Valentine, *Motor Control Electronics Handbook*, McGraw-Hill, New York, 1996.
- B. Wu, *High-Power Converters and AC Drives*, Wiley, New York, 2006.

Problems

Single-phase Voltage Controllers

- 5-1.** The single-phase ac voltage controller of Fig. 5-1a has a 480-V rms 60-Hz source and a load resistance of $50\ \Omega$. The delay angle α is 60° . Determine (a) the rms load voltage, (b) the power absorbed by the load, (c) the power factor, (e) the average and rms currents in the SCRs, and (f) the THD of the source current.
- 5-2.** The single-phase ac voltage controller of Fig. 5-1a has a 120-V rms 60-Hz source and a load resistance of $20\ \Omega$. The delay angle α is 45° . Determine (a) the rms load voltage, (b) the power absorbed by the load, (c) the power factor, (d) the average and rms currents in the SCRs, and (e) the THD of the source current.
- 5-3.** The single-phase ac voltage controller of Fig. 5-1a has a 240-V rms source and a load resistance of $35\ \Omega$. (a) Determine the delay angle required to deliver 800 W to the load. (b) Determine the rms current in each SCR. (c) Determine the power factor.
- 5-4.** A resistive load absorbs 200 W when connected to a 120-V rms 60-Hz ac voltage source. Design a circuit which will result in 200 W absorbed by the same resistance when the source is 240 V rms at 60 Hz. What is the peak load voltage in each case?
- 5-5.** The single-phase ac voltage controller of Fig. 5-1a has a 120-V rms source at 60 Hz and a load resistance of $40\ \Omega$. Determine the range of α so that the output power can be controlled from 200 to 400 W. Determine the range of power factor that will result.
- 5-6.** Design a circuit to deliver power in the range of 750 to 1500 W to a $32\text{-}\Omega$ resistor from a 240-V rms 60-Hz source. Determine the maximum rms and average currents in the switching devices, and determine the maximum voltage across the devices.

- 5-7.** Design a circuit to deliver a constant 1200 W of power to a load that varies in resistance from 20 to 40 Ω . The ac source is 240 V rms, 60 Hz. Determine the maximum rms and average currents in the devices, and determine the maximum voltage across the devices.
- 5-8.** Design a light-dimmer for a 120-V, 100-W incandescent lightbulb. The source is 120 V rms, 60 Hz. Specify the delay angle for the triac to produce an output power of (a) 75 W (b) 25 W. Assume that the bulb is a load of constant resistance.
- 5-9.** A single-phase ac voltage controller is similar to Fig. 5-1a except that S_2 is replaced with a diode. S_1 operates at a delay angle α . Determine (a) an expression for rms load voltage as a function of α and V_m and (b) the range of rms voltage across a resistive load for this circuit.
- 5-10.** The single-phase ac voltage controller of Fig. 5-1a is operated with unequal delays on the two SCRs ($\alpha_1 \neq \alpha_2$). Derive expressions for the rms load voltage and average load voltage in terms of V_m , α_1 , and α_2 .
- 5-11.** The single-phase ac voltage controller of Fig. 5-4a has a 120-V rms 60-Hz source. The series RL load has $R = 18 \Omega$ and $L = 30 \text{ mH}$. The delay angle $\alpha = 60^\circ$. Determine (a) an expression for current, (b) rms load current, (c) rms current in each of the SCRs, and (d) power absorbed by the load. (e) Sketch the waveforms of output voltage and voltage across the SCRs.
- 5-12.** The single-phase ac voltage controller of Fig. 5-4a has a 120-V rms 60-Hz source. The RL load has $R = 22 \Omega$ and $L = 40 \text{ mH}$. The delay angle $\alpha = 50^\circ$. Determine (a) an expression for current, (b) rms load current, (c) rms current in each of the SCRs, and (d) power absorbed by the load. (e) Sketch the waveforms of output voltage and voltage across the SCRs.
- 5-13.** The single-phase ac voltage controller of Fig. 5-4a has a 120-V rms 60-Hz source. The RL load has $R = 12 \Omega$ and $L = 24 \text{ mH}$. The delay angle α is 115° . Determine the rms load current.
- 5-14.** The single-phase ac voltage controller of Fig. 5-4a has a 120-V rms 60-Hz source. The RL load has $R = 12 \Omega$ and $L = 20 \text{ mH}$. The delay angle α is 70° . (a) Determine the power absorbed by the load for ideal SCRs. (b) Determine the power in the load from a PSpice simulation. Use the default diode and $R_{on} = 0.1 \Omega$ in the SCR model. (c) Determine the THD of the source current from the PSpice output.
- 5-15.** Use PSpice to determine the delay angle required in the voltage controller of Fig. 5-4a to deliver (a) 400 W, and (b) 700 W to an RL load with $R = 15 \Omega$ and $L = 15 \text{ mH}$ from a 120-V rms 60-Hz source.
- 5-16.** Use PSpice to determine the delay angle required in the voltage controller of Fig. 5-4a to deliver (a) 600 W, and (b) 1000 W to an RL load with $R = 25 \Omega$ and $L = 60 \text{ mH}$ from a 240-V rms 60-Hz source.
- 5-17.** Design a circuit to deliver 250 W to an RL series load, where $R = 24 \Omega$ and $L = 35 \text{ mH}$. The source is 120 V rms at 60 Hz. Specify the rms and average currents in the devices. Specify the maximum voltage across the devices.

Three-phase Voltage Controllers

- 5-18.** The three-phase voltage controller of Fig. 5-7a has a 480-V rms line-to-line source and a resistive load with 35Ω in each phase. Simulate the circuit in PSpice to determine the power absorbed by the load if the delay angle α is (a) 20° , (b) 80° , and (c) 115° .

- 5-19.** The three-phase Y -connected voltage controller has a 240-V rms, 60-Hz line-to-line source. The load in each phase is a series RL combination with $R = 16 \Omega$ and $L = 50 \text{ mH}$. The delay angle α is 90° . Simulate the circuit in PSpice to determine the power absorbed by the load. On a graph of one period of A -phase current, indicate the intervals when each SCR conducts. Do your analysis for steady-state current.
- 5-20.** For the delta-connected resistive load in the three-phase voltage controller of Fig. 5-10, determine the smallest delay angle such that the rms line current is described by $I_{\text{line rms}} = \sqrt{2}I_{\Delta \text{rms}}$.
- 5-21.** Modify the PSpice circuit file for the three-phase controller for analysis of a delta-connected load. Determine the rms values of the delta currents and the line currents for a 480-V rms source, a resistive load of $R = 25 \Omega$ in each phase, and a delay angle of 45° . Hand in a Probe output showing i_{ab} and i_a .
- 5-22.** A three-phase ac voltage controller has a 480-V rms, 60-Hz source. The load is Y -connected, and each phase has series RLC combination with $R = 14 \Omega$, $L = 10 \text{ mH}$, and $C = 1 \mu\text{F}$. The delay angle is 70° . Use PSpice to determine (a) the rms load current, (b) the power absorbed by the load, and (c) the THD of the line current. Also hand in a graph of one period of A -phase current, indicating which SCRs are conducting at each time. Do your analysis for steady-state current.
- 5-23.** For a three-phase ac voltage controller with a Y -connected load, the voltage across the S_1-S_4 SCR pair is zero when either is on. In terms of the three-phase source voltages, what is the voltage across the S_1-S_4 pair when both are off?

DC-DC Converters

Dc-dc converters are power electronic circuits that convert a dc voltage to a different dc voltage level, often providing a regulated output. The circuits described in this chapter are classified as switched-mode dc-dc converters, also called switching power supplies or switchers. This chapter describes some basic dc-dc converter circuits. Chapter 7 describes some common variations of these circuits that are used in many dc power supply designs.

6.1 LINEAR VOLTAGE REGULATORS

Before we discuss switched-mode converters, it is useful to review the motivation for an alternative to linear dc-dc converters that was introduced in Chapt. 1. One method of converting a dc voltage to a lower dc voltage is a simple circuit as shown in Fig. 6-1. The output voltage is

$$V_o = I_L R_L$$

where the load current is controlled by the transistor. By adjusting the transistor base current, the output voltage may be controlled over a range of 0 to roughly V_s . The base current can be adjusted to compensate for variations in the supply voltage or the load, thus regulating the output. This type of circuit is called a linear dc-dc converter or a linear regulator because the transistor operates in the linear region, rather than in the saturation or cutoff regions. The transistor in effect operates as a variable resistance.

While this may be a simple way of converting a dc supply voltage to a lower dc voltage and regulating the output, the low efficiency of this circuit is a serious drawback for power applications. The power absorbed by the load is $V_o I_L$, and

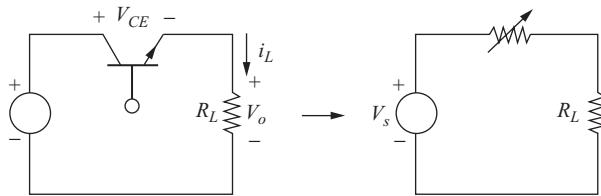


Figure 6-1 A basic linear regulator.

the power absorbed by the transistor is $V_{CE}I_L$, assuming a small base current. The power loss in the transistor makes this circuit inefficient. For example, if the output voltage is one-quarter of the input voltage, the load resistor absorbs one-quarter of the source power, which is an efficiency of 25 percent. The transistor absorbs the other 75 percent of the power supplied by the source. Lower output voltages result in even lower efficiencies. Therefore, the linear voltage regulator is suitable only for low-power applications.

6.2 A BASIC SWITCHING CONVERTER

An efficient alternative to the linear regulator is the switching converter. In a switching converter circuit, the transistor operates as an electronic switch by being completely on or completely off (saturation or cutoff for a BJT or the triode and cutoff regions of a MOSFET). This circuit is also known as a dc chopper.

Assuming the switch is ideal in Fig. 6-2, the output is the same as the input when the switch is closed, and the output is zero when the switch is open. Periodic

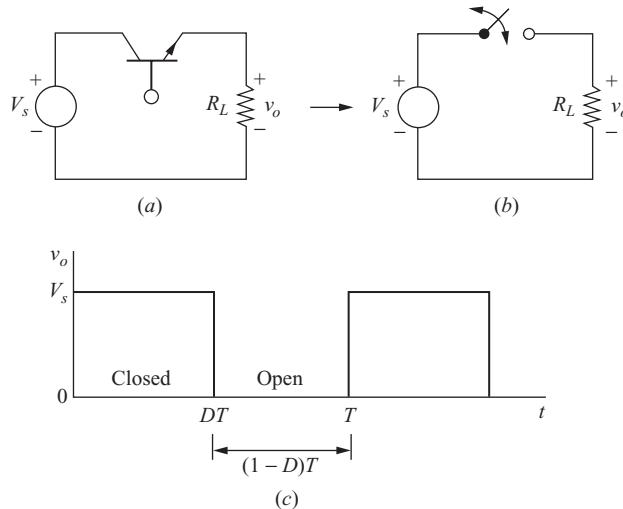


Figure 6-2 (a) A basic dc-dc switching converter; (b) Switching equivalent; (c) Output voltage.

opening and closing of the switch results in the pulse output shown in Fig. 6-2c. The average or dc component of the output voltage is

$$V_o = \frac{1}{T} \int_0^T v_o(t) dt = \frac{1}{T} \int_0^{DT} V_s dt = V_s D \quad (6-1)$$

The dc component of the output voltage is controlled by adjusting the duty ratio D , which is the fraction of the switching period that the switch is closed

$$D \equiv \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}} = \frac{t_{\text{on}}}{T} = t_{\text{on}} f \quad (6-2)$$

where f is the switching frequency. The dc component of the output voltage will be less than or equal to the input voltage for this circuit.

The power absorbed by the ideal switch is zero. When the switch is open, there is no current in it; when the switch is closed, there is no voltage across it. Therefore, all power is absorbed by the load, and the energy efficiency is 100 percent. Losses will occur in a real switch because the voltage across it will not be zero when it is on, and the switch must pass through the linear region when making a transition from one state to the other.

6.3 THE BUCK (STEP-DOWN) CONVERTER

Controlling the dc component of a pulsed output voltage of the type in Fig. 6-2c may be sufficient for some applications, such as controlling the speed of a dc motor, but often the objective is to produce an output that is purely dc. One way of obtaining a dc output from the circuit of Fig. 6-2a is to insert a low-pass filter after the switch. Figure 6-3a shows an *LC* low-pass filter added to the basic converter. The diode provides a path for the inductor current when the switch is opened and is reverse-biased when the switch is closed. This circuit is called a *buck converter* or a *step-down converter* because the output voltage is less than the input.

Voltage and Current Relationships

If the low-pass filter is ideal, the output voltage is the average of the input voltage to the filter. The input to the filter, v_x in Fig. 6-3a, is V_s when the switch is closed and is zero when the switch is open, provided that the inductor current remains positive, keeping the diode on. If the switch is closed periodically at a duty ratio D , the average voltage at the filter input is $V_s D$, as in Eq. (6-1).

This analysis assumes that the diode remains forward-biased for the entire time when the switch is open, implying that the inductor current remains positive. An inductor current that remains positive throughout the switching period is known as *continuous current*. Conversely, discontinuous current is characterized by the inductor current's returning to zero during each period.

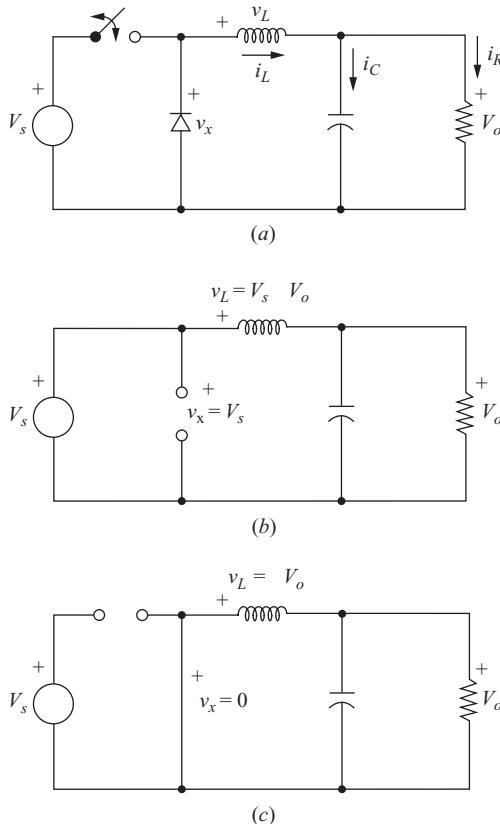


Figure 6-3 (a) Buck dc-dc converter; (b) Equivalent circuit for the switch closed; (c) Equivalent circuit for the switch open.

Another way of analyzing the operation of the buck converter of Fig. 6-3a is to examine the inductor voltage and current. This analysis method will prove useful for designing the filter and for analyzing circuits that are presented later in this chapter.

Buck converters and dc-dc converters in general, have the following properties when operating in the steady state:

1. The inductor current is periodic.

$$i_L(t + T) = i_L(t) \quad (6-3)$$

2. The average inductor voltage is zero (see Sec. 2.3).

$$V_L = \frac{1}{T} \int_t^{t+T} v_L(\lambda) d\lambda = 0 \quad (6-4)$$

3. The average capacitor current is zero (see Sec. 2.3).

$$I_C = \frac{1}{T} \int_t^{t+T} i_C(\lambda) d\lambda = 0 \quad (6-5)$$

4. The power supplied by the source is the same as the power delivered to the load. For nonideal components, the source also supplies the losses.

$$\begin{aligned} P_s &= P_o && \text{ideal} \\ P_s &= P_o + \text{losses} && \text{nonideal} \end{aligned} \quad (6-6)$$

Analysis of the buck converter of Fig. 6-3a begins by making these assumptions:

1. The circuit is operating in the steady state.
2. The inductor current is continuous (always positive).
3. The capacitor is very large, and the output voltage is held constant at voltage V_o . This restriction will be relaxed later to show the effects of finite capacitance.
4. The switching period is T ; the switch is closed for time DT and open for time $(1-D)T$.
5. The components are ideal.

The key to the analysis for determining the output V_o is to examine the inductor current and inductor voltage first for the switch closed and then for the switch open. The net change in inductor current over one period must be zero for steady-state operation. The average inductor voltage is zero.

Analysis for the Switch Closed When the switch is closed in the buck converter circuit of Fig. 6-3a, the diode is reverse-biased and Fig. 6-3b is an equivalent circuit. The voltage across the inductor is

$$v_L = V_s - V_o = L \frac{di_L}{dt}$$

Rearranging,

$$\frac{di_L}{dt} = \frac{V_s - V_o}{L} \quad \text{switch closed}$$

Since the derivative of the current is a positive constant, the current increases linearly as shown in Fig. 6-4b. The change in current while the switch is closed is computed by modifying the preceding equation.

$$\begin{aligned} \frac{di_L}{dt} &= \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{V_s - V_o}{L} \\ (\Delta i_L)_{\text{closed}} &= \left(\frac{V_s - V_o}{L} \right) DT \end{aligned} \quad (6-7)$$

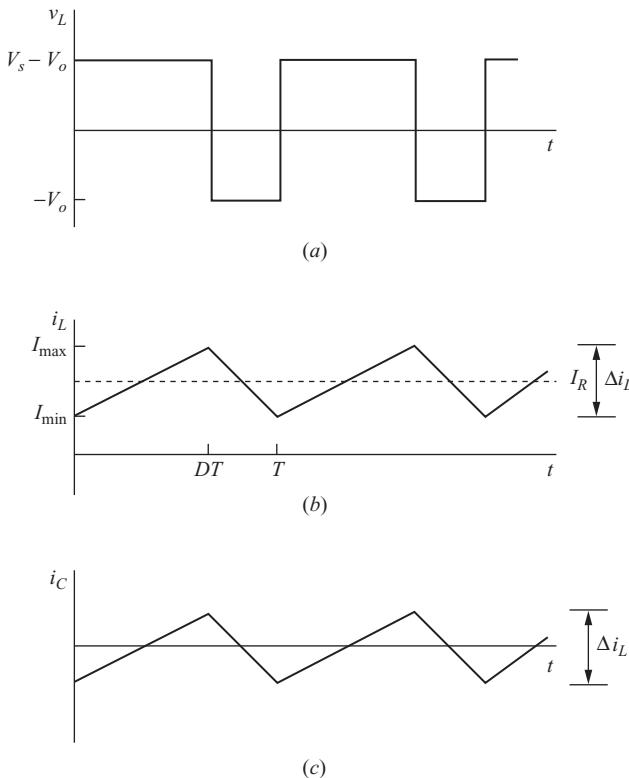


Figure 6-4 Buck converter waveforms: (a) Inductor voltage; (b) Inductor current; (c) Capacitor current.

Analysis for the Switch Open When the switch is open, the diode becomes forward-biased to carry the inductor current and the equivalent circuit of Fig. 6-3c applies. The voltage across the inductor when the switch is open is

$$v_L = -V_o = L \frac{di_L}{dt}$$

Rearranging,

$$\frac{di_L}{dt} = \frac{-V_o}{L} \quad \text{switch open}$$

The derivative of current in the inductor is a negative constant, and the current decreases linearly as shown in Fig. 6-4b. The change in inductor current when the switch is open is

$$\begin{aligned} \frac{\Delta i_L}{\Delta t} &= \frac{\Delta i_L}{(1-D)T} = -\frac{V_o}{L} \\ (\Delta i_L)_{\text{open}} &= -\left(\frac{V_o}{L}\right)(1-D)T \end{aligned} \tag{6-8}$$

Steady-state operation requires that the inductor current at the end of the switching cycle be the same as that at the beginning, meaning that the net change in inductor current over one period is zero. This requires

$$(\Delta i_L)_{\text{closed}} + (\Delta i_L)_{\text{open}} = 0$$

Using Eqs. (6-7) and (6-8),

$$\left(\frac{V_s - V_o}{L}\right)(DT) - \left(\frac{V_o}{L}\right)(1 - D)T = 0$$

Solving for V_o ,

$$V_o = V_s D \quad (6-9)$$

which is the same result as Eq. (6-1). *The buck converter produces an output voltage that is less than or equal to the input.*

An alternative derivation of the output voltage is based on the inductor voltage, as shown in Fig. 6-4a. Since the average inductor voltage is zero for periodic operation,

$$V_L = (V_s - V_o)DT + (-V_o)(1 - D)T = 0$$

Solving the preceding equation for V_o yields the same result as Eq. (6-9), $V_o = V_s D$.

Note that the output voltage depends on only the input and the duty ratio D . If the input voltage fluctuates, the output voltage can be regulated by adjusting the duty ratio appropriately. A feedback loop is required to sample the output voltage, compare it to a reference, and set the duty ratio of the switch accordingly. Regulation techniques are discussed in Chap. 7.

The average inductor current must be the same as the average current in the load resistor, since the average capacitor current must be zero for steady-state operation:

$$I_L = I_R = \frac{V_o}{R} \quad (6-10)$$

Since the change in inductor current is known from Eqs. (6-7) and (6-8), the maximum and minimum values of the inductor current are computed as

$$\begin{aligned} I_{\max} &= I_L + \frac{\Delta i_L}{2} \\ &= \frac{V_o}{R} + \frac{1}{2} \left[\frac{V_o}{L} (1 - D)T \right] = V_o \left(\frac{1}{R} + \frac{1 - D}{2Lf} \right) \end{aligned} \quad (6-11)$$

$$\begin{aligned} I_{\min} &= I_L - \frac{\Delta i_L}{2} \\ &= \frac{V_o}{R} - \frac{1}{2} \left[\frac{V_o}{L} (1 - D)T \right] = V_o \left(\frac{1}{R} - \frac{1 - D}{2Lf} \right) \end{aligned} \quad (6-12)$$

where $f = 1/T$ is the switching frequency.

For the preceding analysis to be valid, continuous current in the inductor must be verified. An easy check for continuous current is to calculate the minimum inductor current from Eq. (6-12). Since the minimum value of inductor current must be positive for continuous current, a negative minimum calculated from Eq. (6-12) is not allowed due to the diode and indicates discontinuous current. The circuit will operate for discontinuous inductor current, but the preceding analysis is not valid. Discontinuous-current operation is discussed later in this chapter.

Equation (6-12) can be used to determine the combination of L and f that will result in continuous current. Since $I_{\min} = 0$ is the boundary between continuous and discontinuous current,

$$\begin{aligned} I_{\min} = 0 &= V_o \left(\frac{1}{R} - \frac{1-D}{2Lf} \right) \\ (Lf)_{\min} &= \frac{(1-D)R}{2} \end{aligned} \quad (6-13)$$

If the desired switching frequency is established,

$$L_{\min} = \frac{(1-D)R}{2f} \quad \text{for continuous current} \quad (6-14)$$

where L_{\min} is the minimum inductance required for continuous current. In practice, a value of inductance greater than L_{\min} is desirable to ensure continuous current.

In the design of a buck converter, the peak-to-peak variation in the inductor current is often used as a design criterion. Equation (6-7) can be combined with Eq. (6-9) to determine the value of inductance for a specified peak-to-peak inductor current for continuous-current operation:

$$\Delta i_L = \left(\frac{V_s - V_o}{L} \right) DT = \left(\frac{V_s - V_o}{Lf} \right) D = \frac{V_o(1-D)}{Lf} \quad (6-15)$$

or

$$L = \left(\frac{V_s - V_o}{\Delta i_L f} \right) D = \frac{V_o(1-D)}{\Delta i_L f} \quad (6-16)$$

Since the converter components are assumed to be ideal, the power supplied by the source must be the same as the power absorbed by the load resistor.

$$\begin{aligned} P_s &= P_o \\ V_s I_s &= V_o I_o \end{aligned} \quad (6-17)$$

or

$$\frac{V_o}{V_s} = \frac{I_s}{I_o}$$

Note that the preceding relationship is similar to the voltage-current relationship for a transformer in ac applications. Therefore, the buck converter circuit is equivalent to a dc transformer.

Output Voltage Ripple

In the preceding analysis, the capacitor was assumed to be very large to keep the output voltage constant. In practice, the output voltage cannot be kept perfectly constant with a finite capacitance. The variation in output voltage, or ripple, is computed from the voltage-current relationship of the capacitor. The current in the capacitor is

$$i_C = i_L - i_R$$

shown in Fig. 6-5a.

While the capacitor current is positive, the capacitor is charging. From the definition of capacitance,

$$Q = CV_o$$

$$\Delta Q = C \Delta V_o$$

$$\Delta V_o = \frac{\Delta Q}{C}$$

The change in charge ΔQ is the area of the triangle above the time axis

$$\Delta Q = \frac{1}{2} \left(\frac{T}{2} \right) \left(\frac{\Delta i_L}{2} \right) = \frac{T \Delta i_L}{8}$$

resulting in

$$\Delta V_o = \frac{T \Delta i_L}{8C}$$

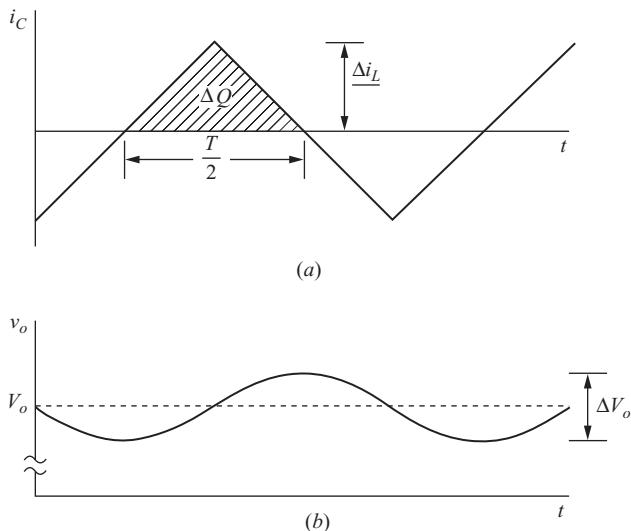


Figure 6-5 Buck converter waveforms. (a) Capacitor current; (b) Capacitor ripple voltage.

Using Eq. (6-8) for Δi_L ,

$$\Delta V_o = \frac{TV_o}{8CL}(1-D)T = \frac{V_o(1-D)}{8LCf^2} \quad (6-18)$$

In this equation, ΔV_o is the peak-to-peak ripple voltage at the output, as shown in Fig. 6-5b. It is also useful to express the ripple as a fraction of the output voltage,

$$\boxed{\frac{\Delta V_o}{V_o} = \frac{1-D}{8LCf^2}} \quad (6-19)$$

In design, it is useful to rearrange the preceding equation to express required capacitance in terms of specified voltage ripple:

$$\boxed{C = \frac{1-D}{8L(\Delta V_o/V_o)f^2}} \quad (6-20)$$

If the ripple is not large, the assumption of a constant output voltage is reasonable and the preceding analysis is essentially valid.

EXAMPLE 6-1

Buck Converter

The buck dc-dc converter of Fig. 6-3a has the following parameters:

$$\begin{aligned} V_s &= 50 \text{ V} \\ D &= 0.4 \\ L &= 400 \mu\text{H} \\ C &= 100 \mu\text{F} \\ f &= 20 \text{ kHz} \\ R &= 20 \Omega \end{aligned}$$

Assuming ideal components, calculate (a) the output voltage V_o , (b) the maximum and minimum inductor current, and (c) the output voltage ripple.

Solution

- (a) The inductor current is assumed to be continuous, and the output voltage is computed from Eq. (6-9),

$$V_o = V_sD = (50)(0.4) = 20 \text{ V}$$

- (b) Maximum and minimum inductor currents are computed from Eqs. (6-11) and (6-12).

$$\begin{aligned} I_{\max} &= V_o \left(\frac{1}{R} + \frac{1-D}{2Lf} \right) \\ &= 20 \left[\frac{1}{20} + \frac{1-0.4}{2(400)(10)^{-6}(20)(10)^3} \right] \\ &= 1 + \frac{1.5}{2} = 1.75 \text{ A} \end{aligned}$$

$$I_{\min} = V_o \left(\frac{1}{R} - \frac{1-D}{2Lf} \right)$$

$$= 1 - \frac{1.5}{2} = 0.25 \text{ A}$$

The average inductor current is 1 A, and $\Delta i_L = 1.5$ A. Note that the minimum inductor current is positive, verifying that the assumption of continuous current was valid.

- (c) The output voltage ripple is computed from Eq. (6-19).

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8LCf^2} = \frac{1-0.4}{8(400)(10)^{-6}(100)(10)^{-6}(20,000)^2}$$

$$= 0.00469 = 0.469\%$$

Since the output ripple is sufficiently small, the assumption of a constant output voltage was reasonable.

Capacitor Resistance—The Effect on Ripple Voltage

The output voltage ripple in Eqs. (6-18) and (6-19) is based on an ideal capacitor. A real capacitor can be modeled as a capacitance with an equivalent series resistance (ESR) and an equivalent series inductance (ESL). The ESR may have a significant effect on the output voltage ripple, often producing a ripple voltage greater than that of the ideal capacitance. The inductance in the capacitor is usually not a significant factor at typical switching frequencies. Figure 6.6 shows a capacitor model that is appropriate for most applications.

The ripple due to the ESR can be approximated by first determining the current in the capacitor, assuming the capacitor to be ideal. For the buck converter in the continuous-current mode, capacitor current is the triangular current waveform of Fig. 6-4c. The voltage variation across the capacitor resistance is

$$\Delta V_{o, \text{ESR}} = \Delta i_C r_C = \Delta i_L r_C \quad (6-21)$$

To estimate a worst-case condition, one could assume that the peak-to-peak ripple voltage due to the ESR algebraically adds to the ripple due to the capacitance. However, the peaks of the capacitor and the ESR ripple voltages will not coincide, so

$$\Delta V_o < \Delta V_{o,C} + \Delta V_{o, \text{ESR}} \quad (6-22)$$

where $\Delta V_{o,C}$ is ΔV_o in Eq. (6-18). The ripple voltage due to the ESR can be much larger than the ripple due to the pure capacitance. In that case, the output capacitor is chosen on the basis of the equivalent series resistance rather than capacitance only.

$$\Delta V_o \approx \Delta V_{o, \text{ESR}} = \Delta i_C r_C \quad (6-23)$$



Figure 6-6 A model for the capacitor including the equivalent series resistance (ESR).

Capacitor ESR is inversely proportional to the capacitance value—a larger capacitance results in a lower ESR. Manufacturers provide what are known as *low-ESR capacitors* for power supply applications.

In Example 6-1, the 100- μF capacitor may have an ESR of $r_C = 0.1 \Omega$. The ripple voltage due to the ESR is calculated as

$$\Delta V_{o,\text{ESR}} = \Delta i_C r_C = \Delta i_L r_C = (1.5 \text{ A})(0.1 \Omega) = 0.15 \text{ V}$$

Expressed as a percent, $\Delta V_o/V_o$ is $0.15/20 = 0.75$ percent. The total ripple can then be approximated as 0.75 percent.

Synchronous Rectification for the Buck Converter

Many buck converters use a second MOSFET in place of the diode. When S_2 is on and S_1 is off, current flows upward out of the drain of S_2 . The advantage of this configuration is that the second MOSFET will have a much lower voltage drop across it compared to a diode, resulting in higher circuit efficiency. This is especially important in low-voltage, high-current applications. A Shottky diode would have a voltage of 0.3 to 0.4 V across it while conducting, whereas a MOSFET will have an extremely low voltage drop due to an $R_{DS\text{on}}$ as low as single-digit milliohms. This circuit has a control scheme known as *synchronous switching*, or *synchronous rectification*. The second MOSFET is known as a *synchronous rectifier*. The two MOSFETs must not be on at the same time to prevent a short circuit across the source, so a “dead time” is built into the switching control—one MOSFET is turned off before the other is turned on. A diode is placed in parallel with the second MOSFET to provide a conducting path for inductor current during the dead time when both MOSFETs are off. This diode may be the MOSFET body diode, or it may be an extra diode, most likely a Shottky diode, for improved switching. The synchronous buck converter should be operated in the continuous-current mode because the MOSFET would allow the inductor current to go negative.

Other converter topologies presented in this chapter and in Chap. 7 can utilize MOSFETs in place of diodes.

6.4 DESIGN CONSIDERATIONS

Most buck converters are designed for continuous-current operation. The choice of switching frequency and inductance to give continuous current is given by Eq. (6-13), and the output voltage ripple is described by Eqs. (6-16) and (6-21). Note that as the switching frequency increases, the minimum size of the inductor to produce continuous current and the minimum size of the capacitor to limit output ripple both decrease. Therefore, high switching frequencies are desirable to reduce the size of both the inductor and the capacitor.

The tradeoff for high switching frequencies is increased power loss in the switches, which is discussed later in this chapter and in Chap. 10. Increased power loss in the switches means that heat is produced. This decreases the converter’s efficiency and may require a large heat sink, offsetting the reduction in size of the inductor and capacitor. Typical switching frequencies are above 20 kHz to avoid audio noise, and they extend well into the 100s of kilohertz and into the megahertz range. Some designers consider about 500 kHz to be the best compromise

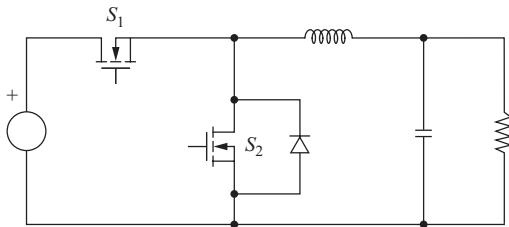


Figure 6-7 A synchronous buck converter. The MOSFET S_2 carries the inductor current when S_1 is off to provide a lower voltage drop than a diode.

between small component size and efficiency. Other designers prefer to use lower switching frequencies of about 50 kHz to keep switching losses small, while still others prefer frequencies larger than 1 MHz. As switching devices improve, switching frequencies will increase.

For low-voltage, high-current applications, the synchronous rectification scheme of Fig. 6-7 is preferred over using a diode for the second switch. The voltage across the conducting MOSFET will be much less than that across a diode, resulting in lower losses.

The inductor value should be larger than L_{\min} in Eq. (6-14) to ensure continuous-current operation. Some designers select a value 25 percent larger than L_{\min} . Other designers use different criteria, such as setting the inductor current variation, Δi_L in Eq. (6-15), to a desired value, such as 40 percent of the average inductor current. A smaller Δi_L results in lower peak and rms inductor currents and a lower rms capacitor current but requires a larger inductor.

The inductor wire must be rated at the rms current, and the core should not saturate for peak inductor current. The capacitor must be selected to limit the output ripple to the design specifications, to withstand peak output voltage, and to carry the required rms current.

The switch (usually a MOSFET with a low R_{DSon}) and diode (or second MOSFET for synchronous rectification) must withstand maximum voltage stress when off and maximum current when on. The temperature ratings must not be exceeded, often requiring a heat sink.

Assuming ideal switches and an ideal inductor in the initial design is usually reasonable. However, the ESR of the capacitor should be included because it typically gives a more significant output voltage ripple than the ideal device and greatly influences the choice of capacitor size.

EXAMPLE 6-2

Buck Converter Design 1

Design a buck converter to produce an output voltage of 18 V across a $10\text{-}\Omega$ load resistor. The output voltage ripple must not exceed 0.5 percent. The dc supply is 48 V. Design for continuous inductor current. Specify the duty ratio, the switching frequency, the values of the inductor and capacitor, the peak voltage rating of each device, and the rms current in the inductor and capacitor. Assume ideal components.

■ Solution

Using the buck converter circuit in Fig. 6-3a, the duty ratio for continuous-current operation is determined from Eq. (6-9):

$$D = \frac{V_o}{V_s} = \frac{18}{48} = 0.375$$

The switching frequency and inductor size must be selected for continuous-current operation. Let the switching frequency arbitrarily be 40 kHz, which is well above the audio range and is low enough to keep switching losses small. The minimum inductor size is determined from Eq. (6-14).

$$L_{\min} = \frac{(1 - D)(R)}{2f} = \frac{(1 - 0.375)(10)}{2(40,000)} = 78 \mu\text{H}$$

Let the inductor be 25 percent larger than the minimum to ensure that inductor current is continuous.

$$L = 1.25L_{\min} = (1.25)(78 \mu\text{H}) = 97.5 \mu\text{H}$$

Average inductor current and the change in current are determined from Eqs. (6-10) and (6-17).

$$I_L = \frac{V_o}{R} = \frac{18}{10} = 1.8 \text{ A}$$

$$\Delta i_L = \left(\frac{V_s - V_o}{L} \right) DT = \frac{48 - 18}{97.5(10)^{-6}} (0.375) \left(\frac{1}{40,000} \right) = 2.88 \text{ A}$$

The maximum and minimum inductor currents are determined from Eqs. (6-11) and (6-12).

$$I_{\max} = I_L + \frac{\Delta i_L}{2} = 1.8 + 1.44 = 3.24 \text{ A}$$

$$I_{\min} = I_L - \frac{\Delta i_L}{2} = 1.8 - 1.44 = 0.36 \text{ A}$$

The inductor must be rated for rms current, which is computed as in Chap. 2 (see Example 2-8). For the offset triangular wave,

$$I_{L,\text{rms}} = \sqrt{I_L^2 + \left(\frac{\Delta i_L/2}{\sqrt{3}} \right)^2} = \sqrt{(1.8)^2 + \left(\frac{1.44}{\sqrt{3}} \right)^2} = 1.98 \text{ A}$$

The capacitor is selected using Eq. (6-20).

$$C = \frac{1 - D}{8L(\Delta V_o/V_o)f^2} = \frac{1 - 0.375}{8(97.5)(10)^{-6}(0.005)(40,000)^2} = 100 \mu\text{F}$$

Peak capacitor current is $\Delta i_L/2 = 1.44 \text{ A}$, and rms capacitor current for the triangular waveform is $1.44/\sqrt{3} = 0.83 \text{ A}$. The maximum voltage across the switch and diode is V_s , or 48 V. The inductor voltage when the switch is closed is $V_s - V_o = 48 - 18 = 30 \text{ V}$. The inductor voltage when the switch is open is $V_o = 18 \text{ V}$. Therefore, the inductor must withstand 30 V. The capacitor must be rated for the 18-V output.

EXAMPLE 6-3

Buck Converter Design 2

Power supplies for telecommunications applications may require high currents at low voltages. Design a buck converter that has an input voltage of 3.3 V and an output voltage of 1.2 V. The output current varies between 4 and 6 A. The output voltage ripple must not exceed 2 percent. Specify the inductor value such that the peak-to-peak variation in inductor current does not exceed 40 percent of the average value. Determine the required rms current rating of the inductor and of the capacitor. Determine the maximum equivalent series resistance of the capacitor.

Solution

Because of the low voltage and high output current in this application, the synchronous rectification buck converter of Fig. 6-7 is used. The duty ratio is determined from Eq. (6-9).

$$D = \frac{V_o}{V_s} = \frac{1.2}{3.3} = 0.364$$

The switching frequency and inductor size must be selected for continuous-current operation. Let the switching frequency arbitrarily be 500 kHz to give a good tradeoff between small component size and low switching losses.

The average inductor current is the same as the output current. Analyzing the circuit for an output current of 4 A,

$$I_L = I_o = 4 \text{ A}$$

$$\Delta i_L = (40\%)(4) = 1.6 \text{ A}$$

Using Eq. (6-16),

$$L = \left(\frac{V_s - V_o}{\Delta i_L f} \right) D = \frac{3.3 - 1.2}{(1.6)(500,000)} (0.364) = 0.955 \mu\text{H}$$

Analyzing the circuit for an output current of 6 A,

$$I_L = I_o = 6 \text{ A}$$

$$\Delta i_L = (40\%)(6) = 2.4 \text{ A}$$

resulting in

$$L = \left(\frac{V_s - V_o}{\Delta i_L f} \right) D = \frac{3.3 - 1.2}{(2.4)(500,000)} (0.364) = 0.636 \mu\text{H}$$

Since 0.636 μH would be too small for the 4-A output, use $L = 0.955 \mu\text{H}$, which would be rounded to 1 μH .

Inductor rms current is determined from

$$I_{L,\text{rms}} = \sqrt{I_L^2 + \left(\frac{\Delta i_L / 2}{\sqrt{3}} \right)^2}$$

(see Chap. 2). From Eq. (6-15), the variation in inductor current is 1.6 A for each output current. Using the 6-A output current, the inductor must be rated for an rms current of

$$I_{L,\text{rms}} = \sqrt{6^2 + \left(\frac{0.8}{\sqrt{3}}\right)^2} = 6.02 \text{ A}$$

Note that the average inductor current would be a good approximation to the rms current since the variation is relatively small.

Using $L = 1 \mu\text{H}$ in Eq. (6-20), the minimum capacitance is determined as

$$C = \frac{1 - D}{8L(\Delta V_o/V_o)f^2} = \frac{1 - 0.364}{8(1)(10)^{-6}(0.02)(500,000)^2} = 0.16 \mu\text{F}$$

The allowable output voltage ripple of 2 percent is $(0.02)(1.2) = 24 \text{ mV}$. The maximum ESR is computed from Eq. (6-23).

$$\Delta V_o \approx r_C \Delta i_C = r_C \Delta i_L$$

or

$$r_C = \frac{\Delta V_o}{\Delta i_C} = \frac{24 \text{ mV}}{1.6 \text{ A}} = 15 \text{ m}\Omega$$

At this point, the designer would search manufacturer's specifications for a capacitor having $15\text{-m}\Omega$ ESR. The capacitor may have to be much larger than the calculated value of $0.16 \mu\text{F}$ to meet the ESR requirement. Peak capacitor current is $\Delta i_L/2 = 0.8 \text{ A}$, and rms capacitor current for the triangular waveform is $0.8/\sqrt{3} = 0.46 \text{ A}$.

6.5 THE BOOST CONVERTER

The boost converter is shown in Fig. 6-8. This is another switching converter that operates by periodically opening and closing an electronic switch. It is called a boost converter because the output voltage is larger than the input.

Voltage and Current Relationships

The analysis assumes the following:

1. Steady-state conditions exist.
2. The switching period is T , and the switch is closed for time DT and open for $(1-D)T$.
3. The inductor current is continuous (always positive).
4. The capacitor is very large, and the output voltage is held constant at voltage V_o .
5. The components are ideal.

The analysis proceeds by examining the inductor voltage and current for the switch closed and again for the switch open.

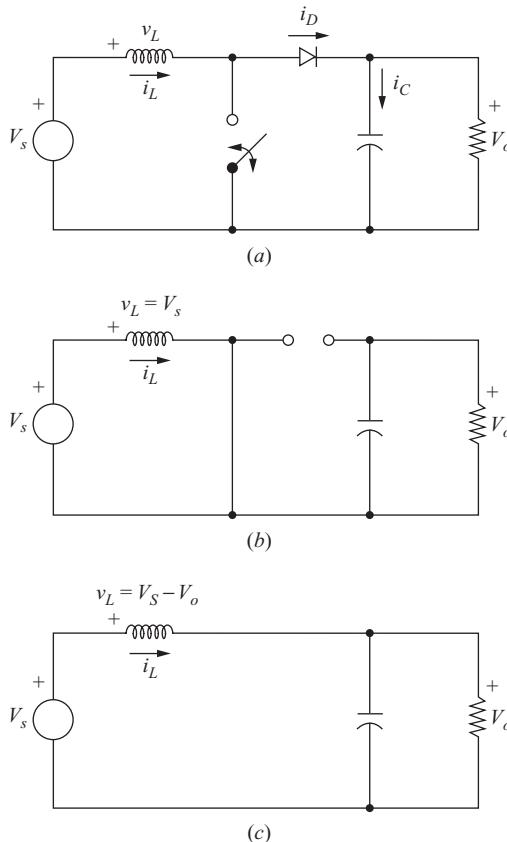


Figure 6-8 The boost converter. (a) Circuit; (b) Equivalent circuit for the switch closed; (c) Equivalent circuit for the switch open.

Analysis for the Switch Closed When the switch is closed, the diode is reverse-biased. Kirchhoff's voltage law around the path containing the source, inductor, and closed switch is

$$v_L = V_s = L \frac{di_L}{dt} \quad \text{or} \quad \frac{di_L}{dt} = \frac{V_s}{L} \quad (6-24)$$

The rate of change of current is a constant, so the current increases linearly while the switch is closed, as shown in Fig. 6-9b. The change in inductor current is computed from

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{V_s}{L}$$

Solving for \$\Delta i_L\$ for the switch closed,

$$(\Delta i_L)_{\text{closed}} = \frac{V_s DT}{L} \quad (6-25)$$

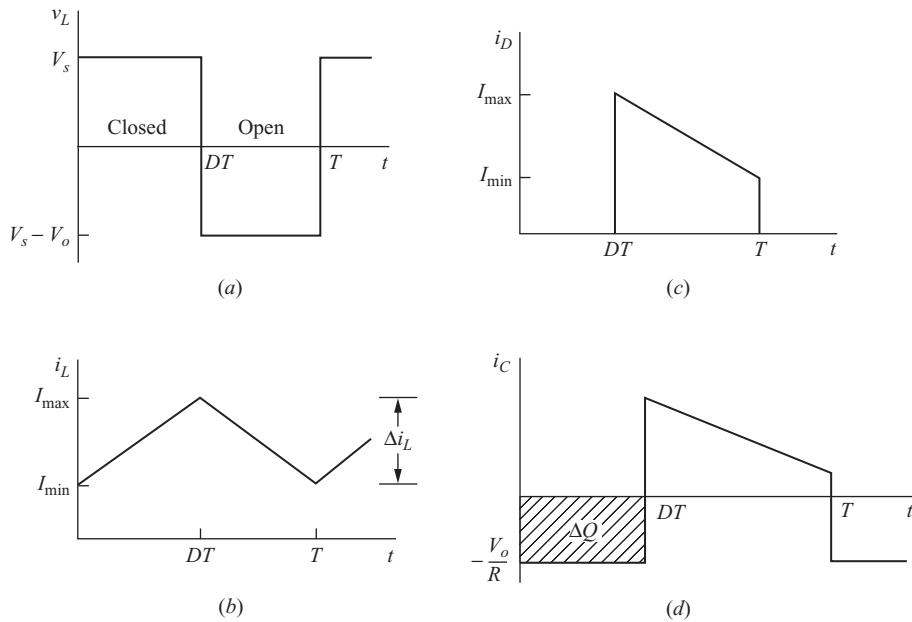


Figure 6-9 Boost converter waveforms. (a) Inductor voltage; (b) Inductor current; (c) Diode current; (d) Capacitor current.

Analysis for the Switch Open When the switch is opened, the inductor current cannot change instantaneously, so the diode becomes forward-biased to provide a path for inductor current. Assuming that the output voltage V_o is a constant, the voltage across the inductor is

$$v_L = V_s - V_o = L \frac{di_L}{dt}$$

$$\frac{di_L}{dt} = \frac{V_s - V_o}{L}$$

The rate of change of inductor current is a constant, so the current must change linearly while the switch is open. The change in inductor current while the switch is open is

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{V_s - V_o}{L}$$

Solving for Δi_L ,

$$(\Delta i_L)_{\text{open}} = \frac{(V_s - V_o)(1 - D)T}{L} \quad (6-26)$$

For steady-state operation, the net change in inductor current must be zero. Using Eqs. (6-25) and (6-26),

$$\begin{aligned}(\Delta i_L)_{\text{closed}} + (\Delta i_L)_{\text{open}} &= 0 \\ \frac{V_s DT}{L} + \frac{(V_s - V_o)(1 - D)T}{L} &= 0\end{aligned}$$

Solving for V_o ,

$$V_s(D + 1 - D) - V_o(1 - D) = 0$$

$$V_o = \frac{V_s}{1 - D}$$

(6-27)

Also, the average inductor voltage must be zero for periodic operation. Expressing the average inductor voltage over one switching period,

$$V_L = V_s D + (V_s - V_o)(1 - D) = 0$$

Solving for V_o yields the same result as in Eq. (6-27).

Equation (6-27) shows that if the switch is always open and D is zero, the output voltage is the same as the input. As the duty ratio is increased, the denominator of Eq. (6-27) becomes smaller, resulting in a larger output voltage. *The boost converter produces an output voltage that is greater than or equal to the input voltage.* However, the output voltage cannot be less than the input, as was the case with the buck converter.

As the duty ratio of the switch approaches 1, the output voltage goes to infinity according to Eq. (6-27). However, Eq. (6-27) is based on ideal components. Real components that have losses will prevent such an occurrence, as shown later in this section. Figure 6-9 shows the voltage and current waveforms for the boost converter.

The average current in the inductor is determined by recognizing that the average power supplied by the source must be the same as the average power absorbed by the load resistor. Output power is

$$P_o = \frac{V_o^2}{R} = V_o I_o$$

and input power is $V_s I_s = V_s I_L$. Equating input and output powers and using Eq. (6-27),

$$V_s I_L = \frac{V_o^2}{R} = \frac{[V_s/(1 - D)]^2}{R} = \frac{V_s^2}{(1 - D)^2 R}$$

By solving for average inductor current and making various substitutions, I_L can be expressed as

$$I_L = \frac{V_s}{(1-D)^2 R} = \frac{V_o^2}{V_s R} = \frac{V_o I_o}{V_s} \quad (6-28)$$

Maximum and minimum inductor currents are determined by using the average value and the change in current from Eq. (6-25).

$$I_{\max} = I_L + \frac{\Delta i_L}{2} = \frac{V_s}{(1-D)^2 R} + \frac{V_s D T}{2L} \quad (6-29)$$

$$I_{\min} = I_L - \frac{\Delta i_L}{2} = \frac{V_s}{(1-D)^2 R} - \frac{V_s D T}{2L} \quad (6-30)$$

Equation (6-27) was developed with the assumption that the inductor current is continuous, meaning that it is always positive. A condition necessary for continuous inductor current is for I_{\min} to be positive. Therefore, the boundary between continuous and discontinuous inductor current is determined from

$$I_{\min} = 0 = \frac{V_s}{(1-D)^2 R} - \frac{V_s D T}{2L}$$

$$\text{or } \frac{V_s}{(1-D)^2 R} = \frac{V_s D T}{2L} = \frac{V_s D}{2L f} \quad (6-31)$$

The minimum combination of inductance and switching frequency for continuous current in the boost converter is therefore

$$(L f)_{\min} = \frac{D(1-D)^2 R}{2} \quad (6-32)$$

A boost converter designed for continuous-current operation will have an inductor value greater than L_{\min} .

From a design perspective, it is useful to express L in terms of a desired Δi_L ,

$$L = \frac{V_s D T}{\Delta i_L} = \frac{V_s D}{\Delta i_L f} \quad (6-33)$$

Output Voltage Ripple

The preceding equations were developed on the assumption that the output voltage was a constant, implying an infinite capacitance. In practice, a finite capacitance will result in some fluctuation in output voltage, or ripple.

The peak-to-peak output voltage ripple can be calculated from the capacitor current waveform, shown in Fig. 6-9d. The change in capacitor charge can be calculated from

$$|\Delta Q| = \left(\frac{V_o}{R} \right) DT = C \Delta V_o$$

An expression for ripple voltage is then

$$\Delta V_o = \frac{V_o DT}{RC} = \frac{V_o D}{RCf}$$

or

$$\boxed{\frac{\Delta V_o}{V_o} = \frac{D}{RCf}} \quad (6-34)$$

where f is the switching frequency. Alternatively, expressing capacitance in terms of output voltage ripple yields

$$C = \frac{D}{R(\Delta V_o/V_o)f} \quad (6-35)$$

As with the buck converter, equivalent series resistance of the capacitor can contribute significantly to the output voltage ripple. The peak-to-peak variation in capacitor current (Fig. 6-9) is the same as the maximum current in the inductor. The voltage ripple due to the ESR is

$$\Delta V_{o,\text{ESR}} = \Delta i_C r_C = I_{L,\text{max}} r_C \quad (6-36)$$

EXAMPLE 6-4

Boost Converter Design 1

Design a boost converter that will have an output of 30 V from a 12-V source. Design for continuous inductor current and an output ripple voltage of less than one percent. The load is a resistance of 50 Ω. Assume ideal components for this design.

■ Solution

First, determine the duty ratio from Eq. (6-27),

$$D = 1 - \frac{V_s}{V_o} = 1 - \frac{12}{30} = 0.6$$

If the switching frequency is selected at 25 kHz to be above the audio range, then the minimum inductance for continuous current is determined from Eq. (6-32).

$$L_{\min} = \frac{D(1-D)^2(R)}{2f} = \frac{0.6(1-0.6)^2(50)}{2(25,000)} = 96 \mu\text{H}$$

To provide a margin to ensure continuous current, let $L = 120 \mu\text{H}$. Note that L and f are selected somewhat arbitrarily and that other combinations will also give continuous current.

Using Eqs. (6-28) and (6-25),

$$I_L = \frac{V_s}{(1-D)^2(R)} = \frac{12}{(1-0.6)^2(50)} = 1.5 \text{ A}$$

$$\frac{\Delta i_L}{2} = \frac{V_s DT}{2L} = \frac{(12)(0.6)}{(2)(120)(10)^{-6}(25,000)} = 1.2 \text{ A}$$

$$I_{\max} = 1.5 + 1.2 = 2.7 \text{ A}$$

$$I_{\min} = 1.5 - 1.2 = 0.3 \text{ A}$$

The minimum capacitance required to limit the output ripple voltage to 1 percent is determined from Eq. (6-35).

$$C \geq \frac{D}{R(\Delta V_o/V_o)f} = \frac{0.6}{(50)(0.01)(25,000)} = 48 \mu\text{F}$$

EXAMPLE 6-5

Boost Converter Design 2

A boost converter is required to have an output voltage of 8 V and supply a load current of 1 A. The input voltage varies from 2.7 to 4.2 V. A control circuit adjusts the duty ratio to keep the output voltage constant. Select the switching frequency. Determine a value for the inductor such that the variation in inductor current is no more than 40 percent of the average inductor current for all operating conditions. Determine a value of an ideal capacitor such that the output voltage ripple is no more than 2 percent. Determine the maximum capacitor equivalent series resistance for a 2 percent ripple.

■ Solution

Somewhat arbitrarily, choose 200 kHz for the switching frequency. The circuit must be analyzed for both input voltage extremes to determine the worst-case condition. For $V_s = 2.7 \text{ V}$, the duty ratio is determined from Eq. (6-27).

$$D = 1 - \frac{V_s}{V_o} = 1 - \frac{2.7}{8} = 0.663$$

Average inductor current is determined from Eq. (6-28).

$$I_L = \frac{V_o I_o}{V_s} = \frac{8(1)}{2.7} = 2.96 \text{ A}$$

The variation in inductor current to meet the 40 percent specification is then $\Delta i_L = 0.4(2.96) = 1.19 \text{ A}$. The inductance is then determined from Eq. (6-33).

$$L = \frac{V_s D}{\Delta i_L f} = \frac{2.7(0.663)}{1.19(200,000)} = 7.5 \mu\text{H}$$

Repeating the calculations for $V_s = 4.2 \text{ V}$,

$$D = 1 - \frac{V_s}{V_o} = 1 - \frac{4.2}{8} = 0.475$$

$$I_L = \frac{V_o I_o}{V_s} = \frac{8(1)}{4.2} = 1.90 \text{ A}$$

The variation in inductor current for this case is $\Delta i_L = 0.4(1.90) = 0.762 \text{ A}$, and

$$L = \frac{V_s D}{\Delta i_L f} = \frac{4.2(0.475)}{0.762(200,000)} = 13.1 \mu\text{H}$$

The inductor must be 13.1 μH to satisfy the specifications for the total range of input voltages.

Equation (6-35), using the maximum value of D , gives the minimum capacitance as

$$C = \frac{D}{R(\Delta V_o/V_o)f} = \frac{D}{(V_o/I_o)(\Delta V_o/V_o)f} = \frac{0.663}{(8/1)(0.02)(200,000)} = 20.7 \mu\text{F}$$

The maximum ESR is determined from Eq. (6-36), using the maximum peak-to-peak variation in capacitor current. The peak-to-peak variation in capacitor current is the same as maximum inductor current. The average inductor current varies from 2.96 A at $V_s = 2.7$ V to 1.90 A at $V_s = 4.2$ V. The variation in inductor current is 0.762 A for $V_s = 4.2$ A, but it must be recalculated for $V_s = 2.7$ V using the 13.1- μH value selected, yielding

$$\Delta i_L = \frac{V_s D}{L f} = \frac{2.7(0.663)}{13.1(10)^{-6}(200,000)} = 0.683 \text{ A}$$

Maximum inductor current for each case is then computed as

$$I_{L,\max,2.7\text{V}} = I_L + \frac{\Delta i_L}{2} = 2.96 + \frac{0.683}{2} = 3.30 \text{ A}$$

$$I_{L,\max,4.2\text{V}} = I_L + \frac{\Delta i_L}{2} = 1.90 + \frac{0.762}{2} = 2.28 \text{ A}$$

This shows that the largest peak-to-peak current variation in the capacitor will be 3.30 A. The output voltage ripple due to the capacitor ESR must be no more than $(0.02)(8) = 0.16$ V. Using Eq. (6-36),

$$\Delta V_{o,\text{ESR}} = \Delta i_C r_C = I_{L,\max} r_C = 3.3 r_C = 0.16 \text{ V}$$

which gives

$$r_C = \frac{0.16 \text{ V}}{3.3 \text{ A}} = 48 \text{ m}\Omega$$

In practice, a capacitor that has an ESR of 48 m Ω or less could have a capacitance value much larger than the 20.7 μF calculated.

Inductor Resistance

Inductors should be designed to have small resistance to minimize power loss and maximize efficiency. The existence of a small inductor resistance does not substantially change the analysis of the buck converter as presented previously in this chapter. However, inductor resistance affects performance of the boost converter, especially at high duty ratios.

For the boost converter, recall that the output voltage for the ideal case is

$$V_o = \frac{V_s}{1 - D} \quad (6-37)$$

To investigate the effect of inductor resistance on the output voltage, assume that the inductor current is approximately constant. The source current is the same as the inductor current, and average diode current is the same as average load current. The power supplied by the source must be the same as the power absorbed by the load and the inductor resistance, neglecting other losses.

$$\begin{aligned} P_s &= P_o + P_{r_L} \\ V_s I_L &= V_o I_D + I_L^2 r_L \end{aligned} \quad (6-38)$$

where r_L is the series resistance of the inductor. The diode current is equal to the inductor current when the switch is off and is zero when the switch is on. Therefore, the average diode current is

$$I_D = I_L(1 - D) \quad (6-39)$$

Substituting for I_D into Eq. (6-38),

$$V_s I_L = V_o I_L(1 - D) + I_L^2 r_L$$

which becomes

$$V_s = V_o(1 - D) + I_L r_L \quad (6-40)$$

In terms of V_o from Eq. (6-39), I_L is

$$I_L = \frac{I_D}{1 - D} = \frac{V_o / R}{1 - D} \quad (6-41)$$

Substituting for I_L into Eq. (6-40),

$$V_s = \frac{V_o r_L}{R(1 - D)} + V_o(1 - D)$$

Solving for V_o ,

$$V_o = \left(\frac{V_s}{1 - D} \right) \left(\frac{1}{1 + r_L / [R(1 - D)^2]} \right) \quad (6-42)$$

The preceding equation is similar to that for an ideal converter but includes a correction factor to account for the inductor resistance. Figure 6-10a shows the output voltage of the boost converter with and without inductor resistance.

The inductor resistance also has an effect on the power efficiency of converters. Efficiency is the ratio of output power to output power plus losses. For the boost converter

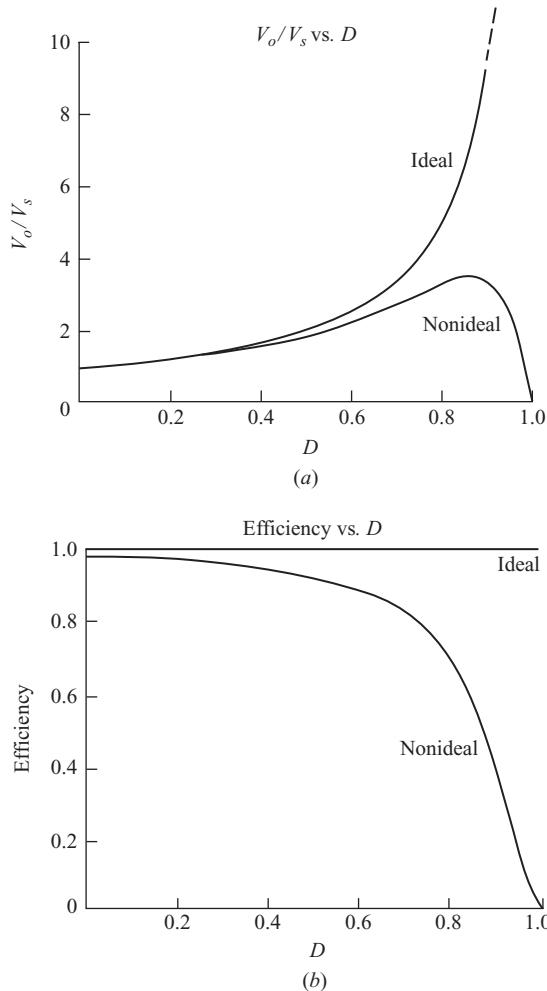


Figure 6-10 Boost converter for a nonideal inductor.
(a) Output voltage; (b) Boost converter efficiency.

$$\eta = \frac{P_o}{P_o + P_{\text{loss}}} = \frac{V_o^2/R}{V_o^2/R + I_L^2 r_L} \quad (6-43)$$

Using Eq. (6-41) for I_L ,

$$\eta = \frac{V_o^2/R}{V_o^2/R + (V_o/R)^2/(1-D)r_L} = \frac{1}{1 + r_L[R(1-D)^2]} \quad (6-44)$$

As the duty ratio increases, the efficiency of the boost converter decreases, as indicated in Fig. 6-10b.

6.6 THE BUCK-BOOST CONVERTER

Another basic switched-mode converter is the buck-boost converter shown in Fig. 6-11. The output voltage of the buck-boost converter can be either higher or lower than the input voltage.

Voltage and Current Relationships

Assumptions made about the operation of the converter are as follows:

1. The circuit is operating in the steady state.
2. The inductor current is continuous.
3. The capacitor is large enough to assume a constant output voltage.
4. The switch is closed for time DT and open for $(1-D)T$.
5. The components are ideal.

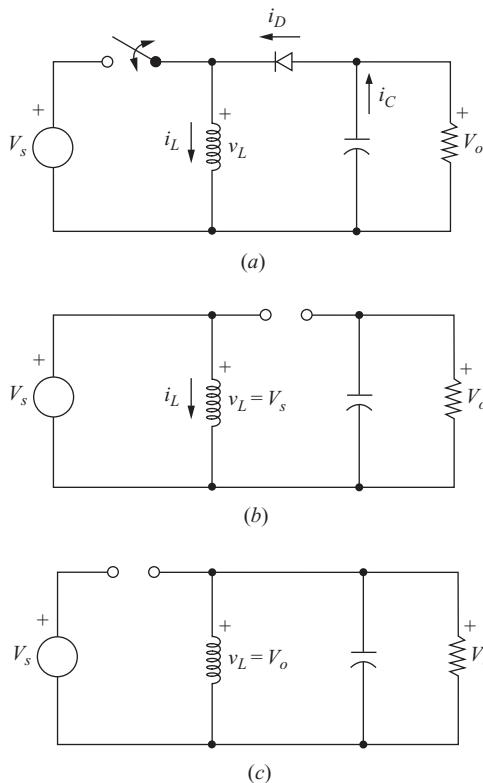


Figure 6-11 Buck-boost converter. (a) Circuit;
(b) Equivalent circuit for the switch closed;
(c) Equivalent circuit for the switch open.

Analysis for the Switch Closed When the switch is closed, the voltage across the inductor is

$$v_L = V_s = L \frac{di_L}{dt}$$

$$\frac{di_L}{dt} = \frac{V_s}{L}$$

The rate of change of inductor current is a constant, indicating a linearly increasing inductor current. The preceding equation can be expressed as

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{V_s}{L}$$

Solving for Δi_L when the switch is closed gives

$$(\Delta i_L)_{\text{closed}} = \frac{V_s DT}{L} \quad (6-45)$$

Analysis for the Switch Open When the switch is open, the current in the inductor cannot change instantaneously, resulting in a forward-biased diode and current into the resistor and capacitor. In this condition, the voltage across the inductor is

$$v_L = V_o = L \frac{di_L}{dt}$$

$$\frac{di_L}{dt} = \frac{V_o}{L}$$

Again, the rate of change of inductor current is constant, and the change in current is

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{V_o}{L}$$

Solving for Δi_L ,

$$(\Delta i_L)_{\text{open}} = \frac{V_o(1-D)T}{L} \quad (6-46)$$

For steady-state operation, the net change in inductor current must be zero over one period. Using Eqs. (6-45) and (6-46),

$$(\Delta i_L)_{\text{closed}} + (\Delta i_L)_{\text{open}} = 0$$

$$\frac{V_s DT}{L} + \frac{V_o(1-D)T}{L} = 0$$

Solving for V_o ,

$$V_o = -V_s \left(\frac{D}{1-D} \right)$$

(6-47)

The required duty ratio for specified input and output voltages can be expressed as

$$D = \frac{|V_o|}{V_s + |V_o|} \quad (6-48)$$

The average inductor voltage is zero for periodic operation, resulting in

$$V_L = V_s D + V_o(1 - D) = 0$$

Solving for V_o yields the same result as Eq. (6-47).

Equation (6-47) shows that the output voltage has opposite polarity from the source voltage. *Output voltage magnitude of the buck-boost converter can be less than that of the source or greater than the source, depending on the duty ratio of the switch.* If $D > 0.5$, the output voltage is larger than the input; and if $D < 0.5$, the output is smaller than the input. Therefore, this circuit combines the capabilities of the buck and boost converters. Polarity reversal on the output may be a disadvantage in some applications, however. Voltage and current waveforms are shown in Fig. 6-12.

Note that the source is never connected directly to the load in the buck-boost converter. Energy is stored in the inductor when the switch is closed and transferred to the load when the switch is open. Hence, the buck-boost converter is also referred to as an *indirect* converter.

Power absorbed by the load must be the same as that supplied by the source, where

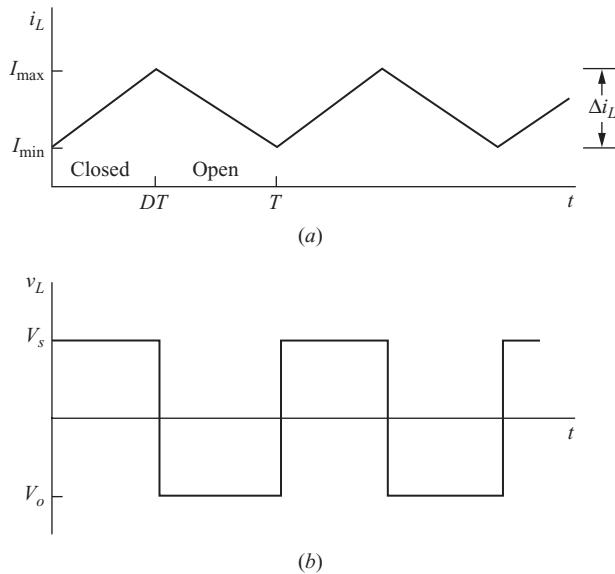


Figure 6-12 Buck-boost converter waveforms.
(a) Inductor current; (b) Inductor voltage; (c) Diode current; (d) Capacitor current.

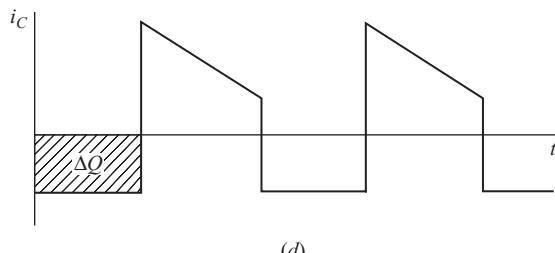
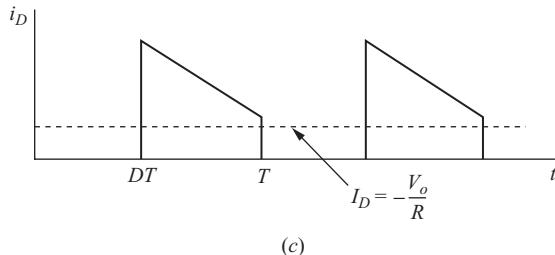


Figure 6-12 (continued)

$$P_o = \frac{V_o^2}{R}$$

$$P_s = V_s I_s$$

$$\frac{V_o^2}{R} = V_s I_s$$

Average source current is related to average inductor current by

$$I_s = I_L D$$

resulting in

$$\frac{V_o^2}{R} = V_s I_L D$$

Substituting for V_o using Eq. (6-47) and solving for I_L , we find

$$I_L = \frac{V_o^2}{V_s R D} = \frac{P_o}{V_s D} = \frac{V_s D}{R(1 - D)^2} \quad (6-49)$$

Maximum and minimum inductor currents are determined using Eqs. (6-45) and (6-49).

$$I_{\max} = I_L + \frac{\Delta i_L}{2} = \frac{V_s D}{R(1 - D)^2} + \frac{V_s D T}{2L} \quad (6-50)$$

$$I_{\min} = I_L - \frac{\Delta i_L}{2} = \frac{V_s D}{R(1 - D)^2} - \frac{V_s D T}{2L} \quad (6-51)$$

For continuous current, the inductor current must remain positive. To determine the boundary between continuous and discontinuous current, I_{\min} is set to zero in Eq. (6-51), resulting in

$$(Lf)_{\min} = \frac{(1 - D)^2 R}{2} \quad (6-52)$$

or

$$L_{\min} = \frac{(1 - D)^2 R}{2f} \quad (6-53)$$

where f is the switching frequency.

Output Voltage Ripple

The output voltage ripple for the buck-boost converter is computed from the capacitor current waveform of Fig. 6-12d.

$$|\Delta Q| = \left(\frac{V_o}{R} \right) DT = C \Delta V_o$$

Solving for ΔV_o ,

$$\Delta V_o = \frac{V_o DT}{RC} = \frac{V_o D}{RCf}$$

or

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} \quad (6-54)$$

As is the case with other converters, the equivalent series resistance of the capacitor can contribute significantly to the output ripple voltage. The peak-to-peak variation in capacitor current is the same as the maximum inductor current. Using the capacitor model shown in Fig. 6-6, where $I_{L,\max}$ is determined from Eq. (6-50),

$$\Delta V_{o,ESR} = \Delta i_C r_C = I_{L,\max} r_C \quad (6-55)$$

EXAMPLE 6-6

Buck-Boost Converter

The buck-boost circuit of Fig. 6-11 has these parameters:

$$V_s = 24 \text{ V}$$

$$D = 0.4$$

$$R = 5 \Omega$$

$$L = 20 \mu\text{H}$$

$$C = 80 \mu\text{F}$$

$$f = 100 \text{ kHz}$$

Determine the output voltage, inductor current average, maximum and minimum values, and the output voltage ripple.

■ Solution

Output voltage is determined from Eq. (6-47).

$$V_o = -V_s \left(\frac{D}{1-D} \right) = -24 \left(\frac{0.4}{1-0.4} \right) = -16 \text{ V}$$

Inductor current is described by Eqs. (6-49) to (6-51).

$$I_L = \frac{V_s D}{R(1-D)^2} = \frac{24(0.4)}{5(1-0.4)^2} = 5.33 \text{ A}$$

$$\Delta i_L = \frac{V_s D T}{L} = \frac{24(0.4)}{20(10)^{-6}(100,000)} = 4.8 \text{ A}$$

$$I_{L,\max} = I_L + \frac{\Delta i_L}{2} = 5.33 + \frac{4.8}{2} = 7.33 \text{ A}$$

$$I_{L,\min} = I_L - \frac{\Delta i_L}{2} = 5.33 - \frac{4.8}{2} = 2.93 \text{ A}$$

Continuous current is verified by $I_{\min} > 0$.

Output voltage ripple is determined from Eq. (6-54).

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} = \frac{0.4}{(5)(80)(10)^{-6}(100,000)} = 0.01 = 1\%$$

6.7 THE ĆUK CONVERTER

The Ćuk switching topology is shown in Fig. 6-13a. Output voltage magnitude can be either larger or smaller than that of the input, and there is a polarity reversal on the output.

The inductor on the input acts as a filter for the dc supply to prevent large harmonic content. Unlike the previous converter topologies where energy transfer is associated with the inductor, energy transfer for the Ćuk converter depends on the capacitor C_1 .

The analysis begins with these assumptions:

1. Both inductors are very large and the currents in them are constant.
2. Both capacitors are very large and the voltages across them are constant.
3. The circuit is operating in steady state, meaning that voltage and current waveforms are periodic.
4. For a duty ratio of D , the switch is closed for time DT and open for $(1-D)T$.
5. The switch and the diode are ideal.

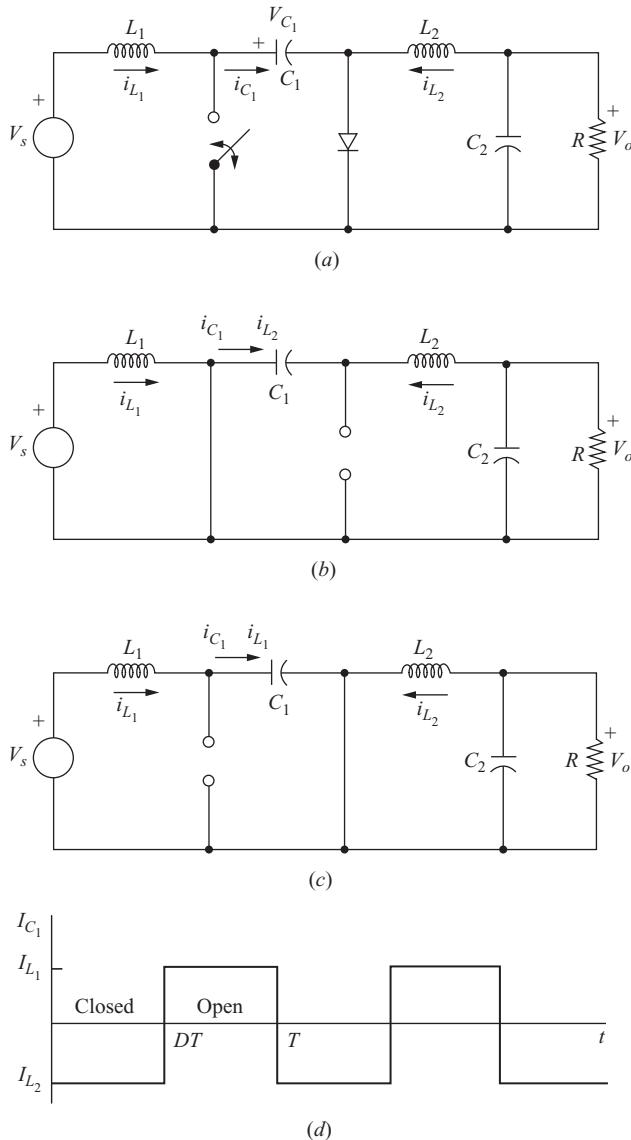


Figure 6-13 The Ćuk converter. (a) Circuit; (b) Equivalent circuit for the switch closed; (c) Equivalent circuit for the switch open; (d) Current in L_1 for a large inductance.

The average voltage across C_1 is computed from Kirchhoff's voltage law around the outermost loop. The average voltage across the inductors is zero for steady-state operation, resulting in

$$V_{C_1} = V_s - V_o$$

With the switch closed, the diode is off and the current in capacitor C_1 is

$$(i_{C_1})_{\text{closed}} = -I_{L_2} \quad (6-56)$$

With the switch open, the currents in L_1 and L_2 force the diode on. The current in capacitor C_1 is

$$(i_{C_1})_{\text{open}} = I_{L_1} \quad (6-57)$$

The power absorbed by the load is equal to the power supplied by the source:

$$-V_o I_{L_2} = V_s I_{L_1} \quad (6-58)$$

For periodic operation, the average capacitor current is zero. With the switch on for time DT and off for $(1-D)T$,

$$[(i_{C_1})_{\text{closed}}]DT + [(i_{C_1})_{\text{open}}](1-D)T = 0$$

Substituting using Eqs. (6-56) and (6-57),

$$\begin{aligned} & -I_{L_2}DT + I_{L_1}(1-D)T = 0 \\ \text{or } & \frac{I_{L_1}}{I_{L_2}} = \frac{D}{1-D} \end{aligned} \quad (6-59)$$

Next, the average power supplied by the source must be the same as the average power absorbed by the load,

$$P_s = P_o$$

$$V_s I_{L_1} = -V_o I_{L_2} \quad (6-60)$$

$$\frac{I_{L_1}}{I_{L_2}} = -\frac{V_o}{V_s}$$

Combining Eqs. (6-59) and (6-60), the relationship between the output and input voltages is

$$V_o = -V_s \left(\frac{D}{1-D} \right) \quad (6-61)$$

The negative sign indicates a polarity reversal between output and input.

Note that the components on the output (L_2 , C_2 , and R) are in the same configuration as the buck converter and that the inductor current has the same form as for the buck converter. Therefore, the ripple, or variation in output voltage, is the same as for the buck converter:

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8L_2C_2f^2} \quad (6-62)$$

The output ripple voltage will be affected by the equivalence series resistance of the capacitor as it was in the converters discussed previously.

The ripple in C_1 can be estimated by computing the change in v_{C1} in the interval when the switch is open and the currents i_{L_1} and i_{C_1} are the same. Assuming the current in L_1 to be constant at a level I_{L_1} and using Eqs. (6-60) and (6-61), we have

$$\Delta v_{C1} \approx \frac{1}{C_1} \int_{DT}^T I_{L_1} d(t) = \frac{I_{L_1}}{C_1} (1 - D) T = \frac{V_s}{RC_{1,f}} \left(\frac{D^2}{1 - D} \right)$$

or

$$\boxed{\Delta v_{C1} \approx \frac{V_o D}{RC_{1,f}}} \quad (6-63)$$

The fluctuations in inductor currents can be computed by examining the inductor voltages while the switch is closed. The voltage across L_1 with the switch closed is

$$v_{L_1} = V_s = L_1 \frac{di_{L_1}}{dt} \quad (6-64)$$

In the time interval DT when the switch is closed, the change in inductor current is

$$\frac{\Delta i_{L_1}}{DT} = \frac{V_s}{L_1}$$

or

$$\boxed{\Delta i_{L_1} = \frac{V_s DT}{L_1} = \frac{V_s D}{L_{1,f}}} \quad (6-65)$$

For inductor L_2 , the voltage across it when the switch is closed is

$$v_{L_2} = V_o + (V_s - V_o) = V_s = L_2 \frac{di_{L_2}}{dt} \quad (6-66)$$

The change in i_{L_2} is then

$$\boxed{\Delta i_{L_2} = \frac{V_s DT}{L_2} = \frac{V_s D}{L_{2,f}}} \quad (6-67)$$

For continuous current in the inductors, the average current must be greater than one-half the change in current. Minimum inductor sizes for continuous current are

$$\boxed{\begin{aligned} L_{1,\min} &= \frac{(1 - D)^2 R}{2 D f} \\ L_{2,\min} &= \frac{(1 - D) R}{2 f} \end{aligned}} \quad (6-68)$$

EXAMPLE 6-7

Cuk Converter Design

A Cuk converter has an input of 12 V and is to have an output of -18 V supplying a 40-W load. Select the duty ratio, the switching frequency, the inductor sizes such that the change in inductor currents is no more than 10 percent of the average inductor current, the output ripple voltage is no more than 1 percent, and the ripple voltage across C_1 is no more than 5 percent.

Solution

The duty ratio is obtained from Eq. (6-61),

$$\frac{V_o}{V_s} = -\frac{D}{1-D} = \frac{-18}{12} = -1.5$$

or

$$D = 0.6$$

Next, the switching frequency needs to be selected. Higher switching frequencies result in smaller current variations in the inductors. Let $f = 50$ kHz. The average inductor currents are determined from the power and voltage specifications.

$$I_{L2} = \frac{P_o}{-V_o} = \frac{40 \text{ W}}{18 \text{ V}} = 2.22 \text{ A}$$

$$I_{L1} = \frac{P_s}{V_s} = \frac{40 \text{ W}}{12 \text{ V}} = 3.33 \text{ A}$$

The change in inductor currents is computed from Eqs. (6-65) and (6-67).

$$\Delta i_L = \frac{V_s D}{L f}$$

The 10 percent limit in changes in inductor currents requires

$$L_2 \geq \frac{V_s D}{f \Delta i_{L2}} = \frac{(12)(0.6)}{(50,000)(0.222)} = 649 \mu\text{H}$$

$$L_1 \geq \frac{V_s D}{f \Delta i_{L1}} = \frac{(12)(0.6)}{(50,000)(0.333)} = 432 \mu\text{H}$$

From Eq. (6-62), the output ripple specification requires

$$C_2 \geq \frac{1-D}{(\Delta V_o/V_o)8L_2 f^2} = \frac{1-0.6}{(0.01)(8)(649)(10)^{-6}(50,000)^2} = 3.08 \mu\text{F}$$

Average voltage across C_1 is $V_s - V_o = 12 - (-18) = 30$ V, so the maximum change in v_{C_1} is $(30)(0.05) = 1.5$ V.

The equivalent load resistance is

$$R = \frac{V_o^2}{P} = \frac{(18)^2}{40} = 8.1 \Omega$$

Now C_1 is computed from the ripple specification and Eq. (6-63).

$$C_1 \geq \frac{V_o D}{R f \Delta v_{C_1}} = \frac{(18)(0.6)}{(8.1)(50,000)(1.5)} = 17.8 \mu\text{F}$$

6.8 THE SINGLE-ENDED PRIMARY INDUCTANCE CONVERTER (SEPIC)

A converter similar to the Ćuk is the single-ended primary inductance converter (SEPIC), as shown in Fig. 6-14. The SEPIC can produce an output voltage that is either greater or less than the input but with no polarity reversal.

To derive the relationship between input and output voltages, these initial assumptions are made:

1. Both inductors are very large and the currents in them are constant.
2. Both capacitors are very large and the voltages across them are constant.
3. The circuit is operating in the steady state, meaning that voltage and current waveforms are periodic.
4. For a duty ratio of D , the switch is closed for time DT and open for $(1 - D)T$.
5. The switch and the diode are ideal.

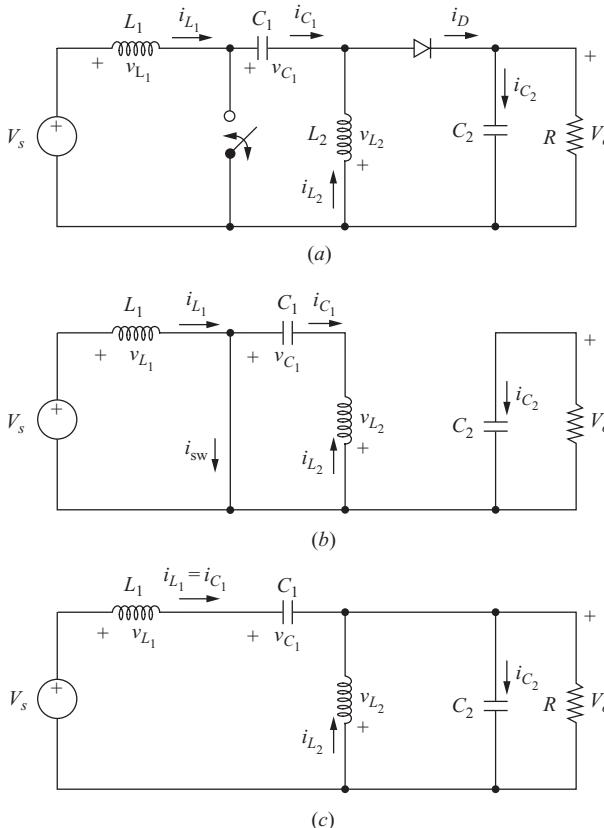


Figure 6-14 (a) SEPIC circuit; (b) Circuit with the switch closed and the diode off; (c) Circuit with the switch open and the diode on.

The inductor current and capacitor voltage restrictions will be removed later to investigate the fluctuations in currents and voltages. The inductor currents are assumed to be continuous in this analysis. Other observations are that the average inductor voltages are zero and that the average capacitor currents are zero for steady-state operation.

Kirchhoff's voltage law around the path containing V_s , L_1 , C_1 , and L_2 gives

$$-V_s + v_{L_1} + v_{C_1} - v_{L_2} = 0$$

Using the average of these voltages,

$$-V_s + 0 + V_{C_1} - 0 = 0$$

showing that the average voltage across the capacitor C_1 is

$$V_{C_1} = V_s \quad (6-69)$$

When the switch is closed, the diode is off, and the circuit is as shown in Fig. 6-14b. The voltage across L_1 for the interval DT is

$$v_{L_1} = V_s \quad (6-70)$$

When the switch is open, the diode is on, and the circuit is as shown in Fig. 6-14c. Kirchhoff's voltage law around the outermost path gives

$$-V_s + v_{L_1} + v_{C_1} + V_o = 0 \quad (6-71)$$

Assuming that the voltage across C_1 remains constant at its average value of V_s [Eq. (6-69)],

$$-V_s + v_{L_1} + V_s + V_o = 0 \quad (6-72)$$

or $v_{L_1} = -V_o \quad (6-73)$

for the interval $(1 - D)T$. Since the average voltage across an inductor is zero for periodic operation, Eqs. (6-70) and (6-73) are combined to get

$$(v_{L_1, \text{sw closed}})(DT) + (v_{L_1, \text{sw open}})(1 - D)T = 0$$

$$V_s(DT) - V_o(1 - D)T = 0$$

where D is the duty ratio of the switch. The result is

$$V_o = V_s \left(\frac{D}{1 - D} \right) \quad (6-74)$$

which can be expressed as

$$D = \frac{V_o}{V_o + V_s} \quad (6-75)$$

This result is similar to that of the buck-boost and Cuk converter equations, with the important distinction that there is no polarity reversal between input and output voltages. The ability to have an output voltage greater or less than the input with no polarity reversal makes this converter suitable for many applications.

Assuming no losses in the converter, the power supplied by the source is the same as the power absorbed by the load.

$$P_s = P_o$$

Power supplied by the dc source is voltage times the average current, and the source current is the same as the current in L_1 .

$$P_s = V_s I_s = V_s I_{L_1}$$

Output power can be expressed as

$$P_o = V_o I_o$$

resulting in

$$V_s I_{L_1} = V_o I_o$$

Solving for average inductor current, which is also the average source current,

$$I_{L_1} = I_s = \frac{V_o I_o}{V_s} = \frac{V_o^2}{V_s R} \quad (6-76)$$

The variation in i_{L_1} when the switch is closed is found from

$$v_{L_1} = V_s = L_1 \left(\frac{di_{L_1}}{dt} \right) = L_1 \left(\frac{\Delta i_{L_1}}{\Delta t} \right) = L_1 \left(\frac{\Delta i_{L_1}}{DT} \right) \quad (6-77)$$

Solving for Δi_{L_1} ,

$$\Delta i_{L_1} = \frac{V_s DT}{L_1} = \frac{V_s D}{L_1 f} \quad (6-78)$$

For L_2 , the average current is determined from Kirchhoff's current law at the node where C_1 , L_2 , and the diode are connected.

$$i_{L_2} = i_D - i_{C_1}$$

Diode current is

$$i_D = i_{C_2} + I_o$$

which makes

$$i_{L_2} = i_{C_2} + I_o - i_{C_1}$$

The average current in each capacitor is zero, so the average current in L_2 is

$$I_{L_2} = I_o \quad (6-79)$$

The variation in i_{L_2} is determined from the circuit when the switch is closed. Using Kirchhoff's voltage law around the path of the closed switch, C_1 , and L_2 with the voltage across C_1 assumed to be a constant V_s , gives

$$v_{L_2} = v_{C_1} = V_s = L_2 \left(\frac{di_{L_2}}{dt} \right) = L_2 \left(\frac{\Delta i_{L_2}}{\Delta t} \right) = L_2 \left(\frac{\Delta i_{L_2}}{DT} \right)$$

Solving for Δi_{L_2}

$$\Delta i_{L_2} = \frac{V_s DT}{L_2} = \frac{V_s D}{L_2 f} \quad (6-80)$$

Applications of Kirchhoff's current law show that the diode and switch currents are

$$i_D = \begin{cases} 0 & \text{when switch is closed} \\ i_{L_1} + i_{L_2} & \text{when switch is open} \end{cases} \quad (6-81)$$

$$i_{sw} = \begin{cases} i_{L_1} + i_{L_2} & \text{when switch is closed} \\ 0 & \text{when switch is open} \end{cases}$$

Current waveforms are shown in Fig. 6-15.

Kirchhoff's voltage law applied to the circuit of Fig. 6-14c, assuming no voltage ripple across the capacitors, shows that the voltage across the switch when it is open is $V_s + V_o$. From Fig. 6-14b, the maximum reverse bias voltage across the diode when it is off is also $V_s + V_o$.

The output stage consisting of the diode, C_2 , and the load resistor is the same as in the boost converter, so the output ripple voltage is

$$\boxed{\Delta V_o = \Delta V_{C_2} = \frac{V_o D}{R C_2 f}} \quad (6-82)$$

Solving for C_2 ,

$$\boxed{C_2 = \frac{D}{R(\Delta V_o/V_o)f}} \quad (6-83)$$

The voltage variation in C_1 is determined from the circuit with the switch closed (Fig. 6-14b). Capacitor current i_{C_1} is the opposite of i_{L_2} , which has previously been determined to have an average value of I_o . From the definition of capacitance and considering the magnitude of charge,

$$\Delta V_{C_1} = \frac{\Delta Q_{C_1}}{C} = \frac{I_o \Delta t}{C} = \frac{I_o D T}{C}$$

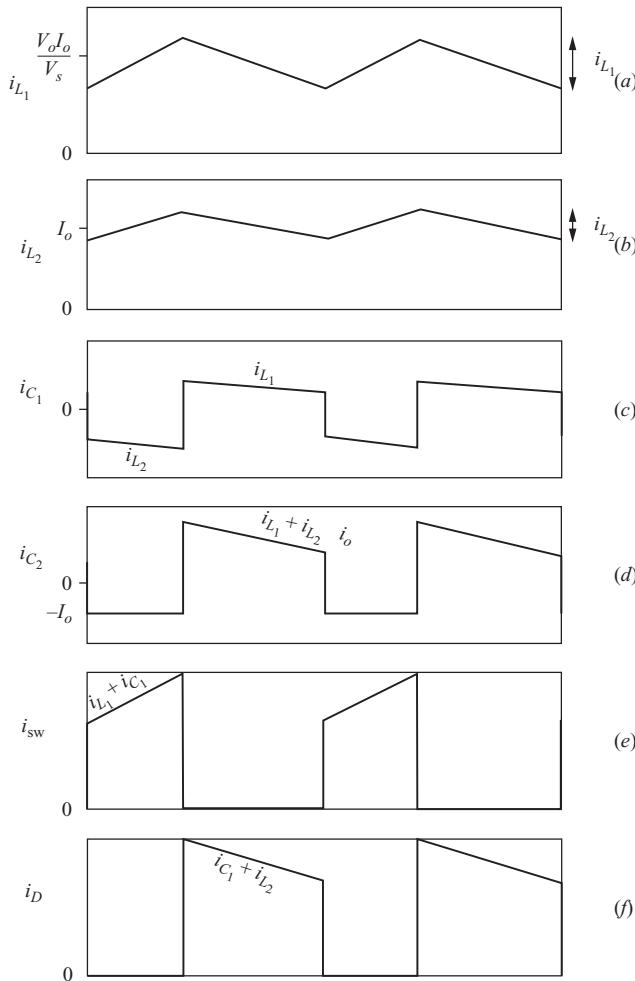


Figure 6-15 Currents in the SEPIC converter. (a) L_1 ; (b) L_2 ; (c) C_1 ; (d) C_2 ; (e) switch; (f) diode.

Replacing I_o with V_o/R ,

$$\Delta V_{C_1} = \frac{V_o D}{R C_1 f} \quad (6-84)$$

Solving for C_1 ,

$$C_1 = \frac{D}{R(\Delta V_{C_1}/V_o)f} \quad (6-85)$$

The effect of equivalent series resistance of the capacitors on voltage variation is usually significant, and the treatment is the same as with the converters discussed previously.

EXAMPLE 6-8

SEPIC Circuit

The SEPIC circuit of Fig. 6-14a has the following parameters:

$$\begin{aligned}V_s &= 9 \text{ V} \\D &= 0.4 \\f &= 100 \text{ kHz} \\L_1 = L_2 &= 90 \mu\text{H} \\C_1 = C_2 &= 80 \mu\text{F} \\I_o &= 2 \text{ A}\end{aligned}$$

Determine the output voltage; the average, maximum, and minimum inductor currents; and the variation in voltage across each capacitor.

Solution

The output voltage is determined from Eq. (6-74).

$$V_o = V_s \left(\frac{D}{1 - D} \right) = 9 \left(\frac{0.4}{1 - 0.4} \right) = 6 \text{ V}$$

The average current in L_1 is determined from Eq. (6-76).

$$I_{L1} = \frac{V_o I_o}{V_s} = \frac{6(2)}{9} = 1.33 \text{ A}$$

From Eq. (6-78)

$$\Delta i_{L1} = \frac{V_s D}{L_1 f} = \frac{9(0.4)}{90(10)^{-6}(100,000)} = 0.4 \text{ A}$$

Maximum and minimum currents in L_1 are then

$$\begin{aligned}I_{L1,\max} &= I_{L1} + \frac{\Delta i_{L1}}{2} = 1.33 + \frac{0.4}{2} = 1.53 \text{ A} \\I_{L1,\min} &= I_{L1} - \frac{\Delta i_{L1}}{2} = 1.33 - \frac{0.4}{2} = 1.13 \text{ A}\end{aligned}$$

For the current in L_2 , the average is the same as the output current $I_o = 2 \text{ A}$. The variation in I_{L2} is determined from Eq. (6-80)

$$\Delta i_{L2} = \frac{V_s D}{L_2 f} = \frac{9(0.4)}{90(10)^{-6}(100,000)} = 0.4 \text{ A}$$

resulting in maximum and minimum current magnitudes of

$$\begin{aligned}I_{L2,\max} &= 2 + \frac{0.4}{2} = 2.2 \text{ A} \\I_{L2,\min} &= 2 - \frac{0.4}{2} = 1.8 \text{ A}\end{aligned}$$

Using an equivalent load resistance of $6 \text{ V}/2 \text{ A} = 3 \Omega$, the ripple voltages in the capacitors are determined from Eqs. (6-82) and (6-84).

$$\Delta V_o = \Delta V_{C_2} = \frac{V_o D}{R C_2 f} = \frac{6(0.4)}{(3)80(10)^{-6}(100,000)} = 0.1 \text{ V}$$

$$\Delta V_{C_1} = \frac{V_o D}{R C_1 f} = \frac{6(0.4)}{(3)80(10)^{-6}(100,000)} = 0.1 \text{ V}$$

In Example 6-8, the values of L_1 and L_2 are equal, which is not a requirement. However, when they are equal, the rates of change in the inductor currents are identical [Eqs. (6-78) and (6-80)]. The two inductors may then be wound on the same core, making a 1:1 transformer. Figure 6-16 shows an alternative representation of the SEPIC converter.

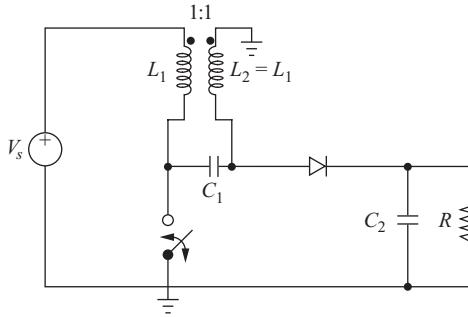
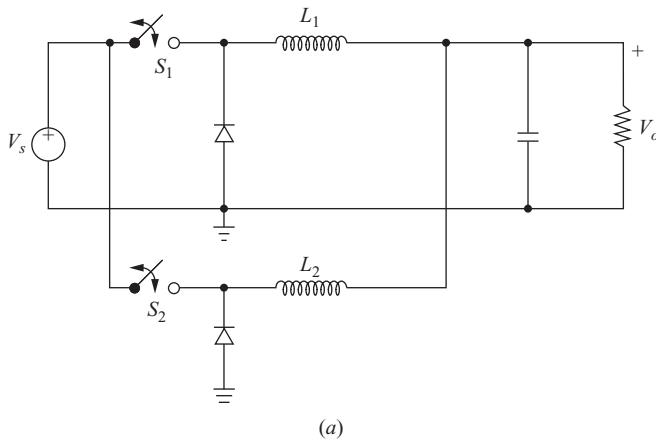


Figure 6-16 A SEPIC circuit using mutually coupled inductors.

6.9 INTERLEAVED CONVERTERS

Interleaving, also called *multiphasing*, is a technique that is useful for reducing the size of filter components. An interleaved buck converter is shown in Fig. 6-17a. This is equivalent to a parallel combination of two sets of switches, diodes, and inductors connected to a common filter capacitor and load. The switches are operated 180° out of phase, producing inductor currents that are also 180° out of phase. The current entering the capacitor and load resistance is the sum of the inductor currents, which has a smaller peak-to-peak variation and a frequency twice as large as individual inductor currents. This results in a smaller peak-to-peak variation in capacitor current than would be achieved with a single buck converter, requiring less capacitance for the same output ripple voltage. The variation in current coming from the source is also reduced. Figure 6-17b shows the current waveforms.

The output voltage is obtained by taking Kirchhoff's voltage law around either path containing the voltage source, a switch, an inductor, and the output voltage. The voltage across the inductor is $V_s - V_o$ with the switch closed and



(a)

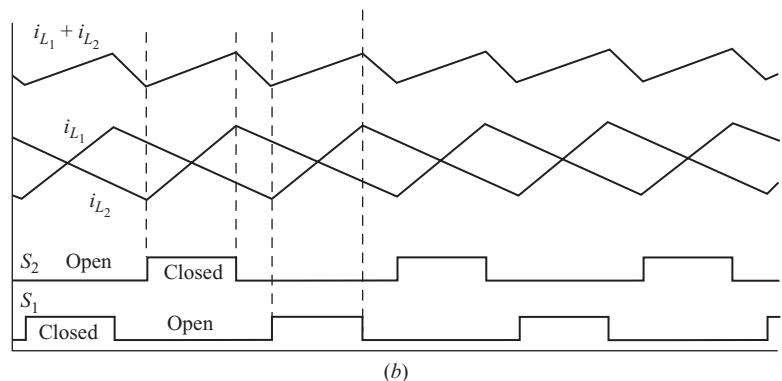


Figure 6-17 (a) An interleaved buck converter; (b) The switching scheme and current waveforms.

is $-V_o$ with the switch open. These are the same as for the buck converter of Fig. 6-3a discussed previously, resulting in

$$V_o = V_s D$$

where D is the duty ratio of each switch.

Each inductor supplies one-half of the load current and output power, so the average inductor current is one-half of what it would be for a single buck converter.

More than two converters can be interleaved. The phase shift between switch closing is $360^\circ/n$, where n is the number of converters in the parallel configuration. Interleaving can be done with the other converters in this chapter and with the converters that are described in Chap. 7. Figure 6-18 shows an interleaved boost converter.

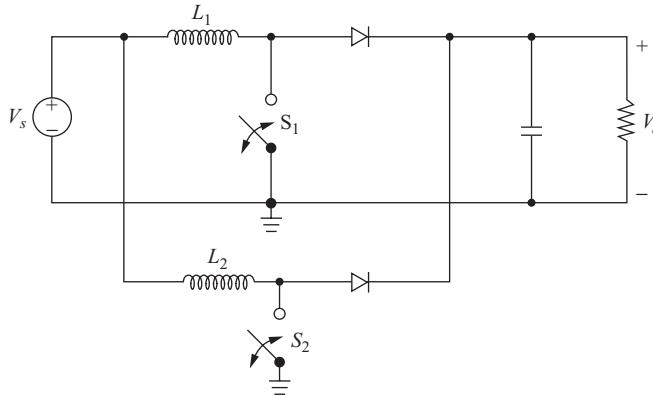


Figure 6-18 An interleaved boost converter.

6.10 NONIDEAL SWITCHES AND CONVERTER PERFORMANCE

Switch Voltage Drops

All the preceding calculations were made with the assumption that the switches were ideal. Voltage drops across conducting transistors and diodes may have a significant effect on converter performance, particularly when the input and output voltages are low. Design of dc-dc converters must account for nonideal components. The buck converter is used to illustrate the effects of switch voltage drops.

Referring again to the analysis of the buck converter of Fig. 6-3a, the input-output voltage relationship was determined using the inductor voltage and current. With nonzero voltage drops across conducting switches, the voltage across the inductor with the switch closed becomes

$$v_L = V_s - V_o - V_Q \quad (6-86)$$

where V_Q is the voltage across the conducting switch. With the switch open, the voltage across the diode is V_D and the voltage across the inductor is

$$v_L = -V_o - V_D \quad (6-87)$$

The average voltage across the inductor is zero for the switching period.

$$V_L = (V_s - V_o - V_Q)D + (-V_o - V_D)(1 - D) = 0$$

Solving for V_o ,

$$V_o = V_s D - V_Q D - V_D(1 - D) \quad (6-88)$$

which is lower than $V_o = V_s D$ for the ideal case.

Switching Losses

In addition to the on-state voltage drops and associated power losses of the switches, other losses occur in the switches as they turn on and off. Figure 6-19a illustrates switch on-off transitions. For this case, it is assumed that the changes in voltage and current are linear and that the timing sequence is as shown. The instantaneous power dissipated in the switch is shown in Fig. 6-19a. Another possible switch on-off transition is shown in Fig. 6-12b. In this case, the voltage and current transitions do not occur simultaneously. This may be closer to actual switching situations, and switching power loss is larger for this case. (See Chap. 10 for additional information.)

The energy loss in one switching transition is the area under the power curve. Since the average power is energy divided by the period, higher switching frequencies result in higher switching losses. One way to reduce switching losses is to modify the circuit to make switching occur at zero voltage and/or zero current. This is the approach of the resonant converter, which is discussed in Chap. 9.

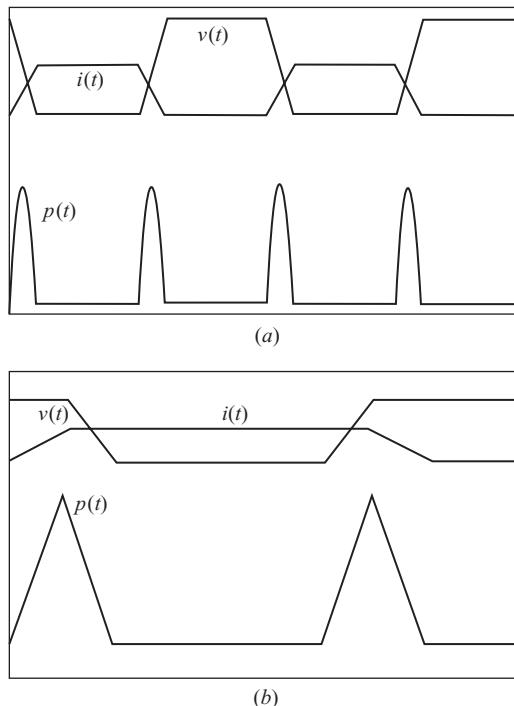


Figure 6-19 Switch voltage, current, and instantaneous power. (a) Simultaneous voltage and current transition; (b) Worst-case transition.

6.11 DISCONTINUOUS-CURRENT OPERATION

Continuous current in the inductor was an important assumption in the previous analyses for dc-dc converters. Recall that continuous current means that the current in the inductor remains positive for the entire switching period. Continuous current is not a necessary condition for a converter to operate, but a different analysis is required for the discontinuous-current case.

Buck Converter with Discontinuous Current

Figure 6-20 shows the inductor and source currents for discontinuous-current operation for the buck converter of Fig 6-3a. The relationship between output and input voltages is determined by first recognizing that the average inductor voltage is zero for periodic operation. From the inductor voltage shown in Fig. 6-20c,

$$(V_s - V_o)DT - V_oD_1T = 0$$

which is rearranged to get

$$(V_s - V_o)D = V_oD_1 \quad (6-89)$$

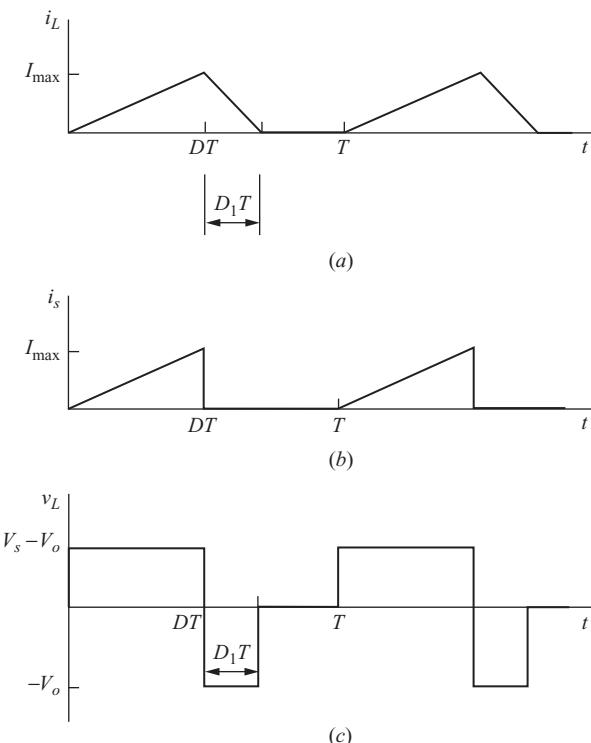


Figure 6-20 Buck converter discontinuous current.

(a) Inductor current; (b) Source current; (c) Inductor voltage.

$$\frac{V_o}{V_s} = \left(\frac{D}{D + D_1} \right) \quad (6-90)$$

Next, the average inductor current equals the average resistor current because the average capacitor current is zero. With the output voltage assumed constant,

$$I_L = I_R = \frac{V_o}{R}$$

Computing the average inductor current from Fig. 6-20a,

$$I_L = \frac{1}{T} \left(\frac{1}{2} I_{\max} DT + \frac{1}{2} I_{\max} D_1 T \right) = \frac{1}{2} I_{\max} (D + D_1)$$

which results in

$$\frac{1}{2} I_{\max} (D + D_1) = \frac{V_o}{R} \quad (6-91)$$

Since the current starts at zero, the maximum current is the same as the change in current over the time that the switch is closed. With the switch closed, the voltage across the inductor is

$$v_L = V_s - V_o$$

which results in

$$\frac{di_L}{dt} = \frac{V_s - V_o}{L} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{I_{\max}}{DT} \quad (6-92)$$

Solving for I_{\max} and using Eq. (6-89) for $(V_s - V_o)D$,

$$I_{\max} = \Delta i_L = \left(\frac{V_s - V_o}{L} \right) DT = \frac{V_o D_1 T}{L} \quad (6-93)$$

Substituting for I_{\max} in Eq. (6-91),

$$\frac{1}{2} I_{\max} (D + D_1) = \frac{1}{2} \left(\frac{V_o D_1 T}{L} \right) (D + D_1) = \frac{V_o}{R} \quad (6-94)$$

which gives

$$D_1^2 + DD_1 - \frac{2L}{RT} = 0$$

Solving for D_1 ,

$$D_1 = \frac{-D + \sqrt{D^2 + 8L/RT}}{2} \quad (6-95)$$

Substituting for D_1 in Eq. (6-90),

$$V_o = V_s \left(\frac{D}{D + D_1} \right) = V_s \left[\frac{2D}{D + \sqrt{D^2 + 8L/RT}} \right] \quad (6-96)$$

The boundary between continuous and discontinuous current occurs when $D_1 = 1 - D$. Recall that another condition that occurs at the boundary between continuous and discontinuous current is $I_{\min} = 0$ in Eq. (6-12).

EXAMPLE 6-9

Buck Converter with Discontinuous Current

For the buck converter of Fig. 6-3a,

$$V_s = 24 \text{ V}$$

$$L = 200 \mu\text{H}$$

$$R = 20 \Omega$$

$$C = 1000 \mu\text{F}$$

$$f = 10 \text{ kHz} \quad \text{switching frequency}$$

$$D = 0.4$$

(a) Show that the inductor current is discontinuous, (b) Determine the output voltage V_o .

■ Solution

(a) For discontinuous current, $D_1 < 1 - D$, and D_1 is calculated from Eq. (6-95).

$$\begin{aligned} D_1 &= \frac{-D + \sqrt{D^2 + 8L/RT}}{2} \\ &= \frac{1}{2} \left(-0.4 + \sqrt{0.4^2 + \frac{8(200)(10)^{-6}(10,000)}{20}} \right) = 0.29 \end{aligned}$$

Comparing D_1 to $1 - D$, $0.29 < (1 - 0.4)$ shows that the inductor current is discontinuous. Alternatively, the minimum inductor current computed from Eq. (6-12) is $I_{\min} = -0.96 \text{ A}$. Since negative inductor current is not possible, inductor current must be discontinuous.

(b) Since D_1 is calculated and discontinuous current is verified, the output voltage can be computed from Eq. (6-96).

$$V_o = V_s \left(\frac{D}{D + D_1} \right) = 20 \left(\frac{0.4}{0.4 + 0.29} \right) = 13.9 \text{ V}$$

Figure 6-21 shows the relationship between output voltage and duty ratio for the buck converter of Example 6-9. All parameters except D are those of Example 6-9. Note the linear relationship between input and output for continuous current and the nonlinear relationship for discontinuous current. For a given duty ratio, the output voltage is greater for discontinuous-current operation than it would be if current were continuous.

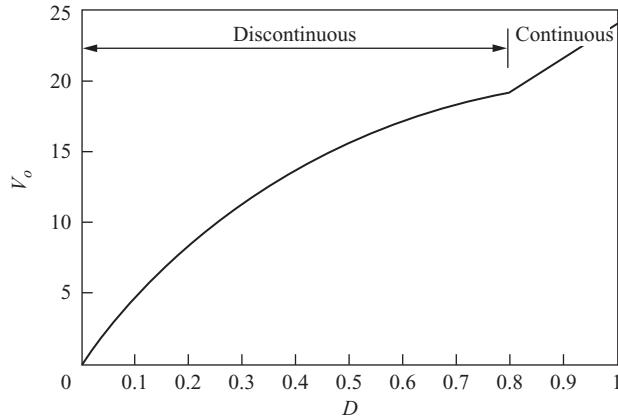


Figure 6-21 V_o versus duty ratio for the buck converter of Example 6-9.

Boost Converter with Discontinuous Current

The boost converter will also operate for discontinuous inductor current. In some cases, the discontinuous-current mode is desirable for control reasons in the case of a regulated output. The relationship between output and input voltages is determined from two relationships:

1. The average inductor voltage is zero.
2. The average current in the diode is the same as the load current.

The inductor and diode currents for discontinuous current have the basic waveforms as shown in Fig. 6-22a and c. When the switch is on, the voltage across the inductor is V_s . When the switch is off and the inductor current is positive, the inductor voltage is $V_s - V_o$. The inductor current decreases until it reaches zero and is prevented from going negative by the diode. With the switch open and the diode off, the inductor current is zero. The average voltage across the inductor is

$$V_s DT + (V_s - V_o)D_1 T = 0$$

which results in

$$V_o = V_s \left(\frac{D + D_1}{D_1} \right) \quad (6-97)$$

The average diode current (Fig. 6-22c) is

$$I_D = \frac{1}{T} \left(\frac{1}{2} I_{\max} D_1 T \right) = \frac{1}{2} I_{\max} D_1 \quad (6-98)$$

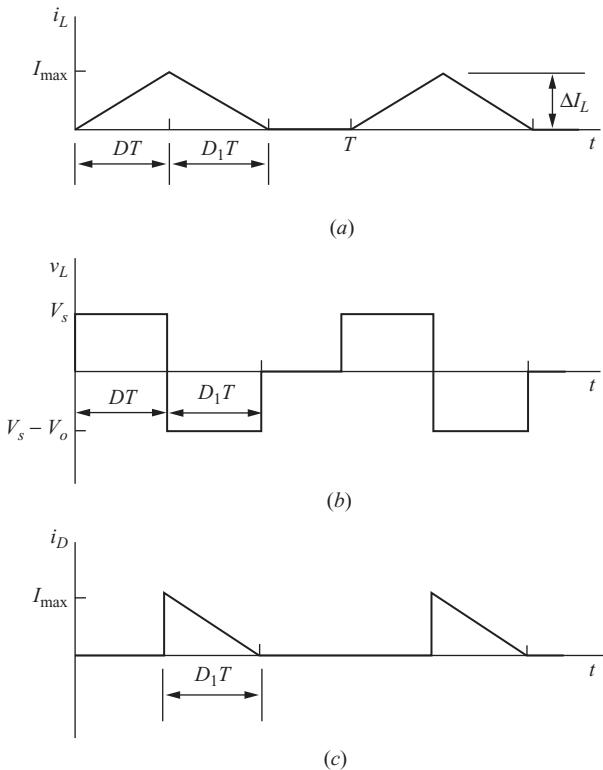


Figure 6-22 Discontinuous current in the boost converter.
(a) Inductor current; (b) Inductor voltage; (c) Diode current.

Current I_{\max} is the same as the change in inductor current when the switch is closed.

$$I_{\max} = \Delta i_L = \frac{V_s DT}{L} \quad (6-99)$$

Substituting for I_{\max} in Eq. (6-98) and setting the result equal to the load current,

$$I_D = \frac{1}{2} \left(\frac{V_s DT}{L} \right) D_1 = \frac{V_o}{R} \quad (6-100)$$

Solving for D_1 ,

$$D_1 = \left(\frac{V_o}{V_s} \right) \left(\frac{2L}{RDT} \right) \quad (6-101)$$

Substituting the preceding expression for D_1 into Eq. (6-97) results in the quadratic equation

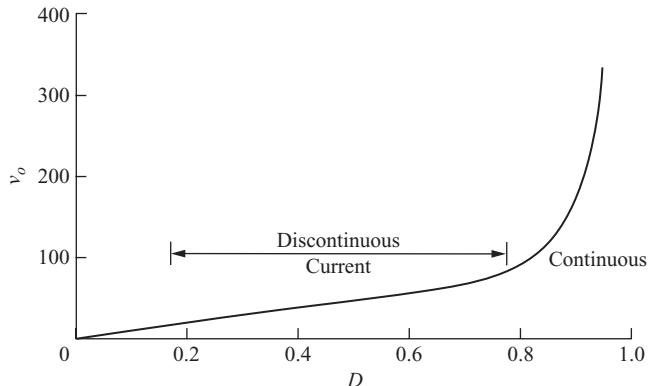


Figure 6-23 Output voltage of boost converter.

$$\left(\frac{V_o}{V_s}\right)^2 - \frac{V_o}{V_s} - \frac{D^2 RT}{2L} = 0$$

Solving for V_o/V_s ,

$$\frac{V_o}{V_s} = \frac{1}{2} \left(1 + \sqrt{1 + \frac{2D^2 RT}{L}} \right) \quad (6-102)$$

The boundary between continuous and discontinuous current occurs when $D_1 = 1 - D$. Another condition at the boundary is when I_{\min} in Eq. (6-30) is zero.

Whether the boost converter is operating in the continuous or discontinuous mode depends on the combination of circuit parameters, including the duty ratio. As the duty ratio for a given boost converter is varied, the converter may go into and out of the discontinuous mode. Figure 6-23 shows the output voltage for a boost converter as the duty ratio is varied.

EXAMPLE 6-10

Boost Converter with Discontinuous Current

The boost converter of Fig. 6-8a has parameters

$$\begin{aligned} V_s &= 20 \text{ V} \\ D &= 0.6 \\ L &= 100 \mu\text{H} \\ R &= 50 \Omega \\ C &= 100 \mu\text{F} \\ f &= 15 \text{ kHz} \end{aligned}$$

- (a) Verify that the inductor current is discontinuous, (b) determine the output voltage, and (c) determine the maximum inductor current.

■ Solution

- (a) First assume that the inductor current is continuous and compute the minimum from Eq. (6-30), resulting in $I_{\min} = -1.5$ A. Negative inductor current is not possible, indicating discontinuous current.
- (b) Equation (6-102) gives the output voltage

$$V_o = \frac{V_s}{2} \left(1 + \sqrt{1 + \frac{2D^2R}{Lf}} \right) = \frac{20}{2} \left[1 + \sqrt{1 + \frac{2(0.6)^2(50)}{100(10)^{-6}(15,000)}} \right] = 60 \text{ V}$$

Note that a boost converter with the same duty ratio operating with continuous current would have an output of 50 V.

- (c) The maximum inductor current is determined from Eq. (6-99).

$$I_{\max} = \frac{V_s D}{Lf} = \frac{(20)(0.6)}{100(10)^{-6}(15,000)} = 8 \text{ A}$$

6.12 SWITCHED-CAPACITOR CONVERTERS

In switched-capacitor converters, capacitors are charged in one circuit configuration and then reconnected in a different configuration, producing an output voltage different from the input. Switched-capacitor converters do not require an inductor and are also known as *inductorless converters* or *charge pumps*. Switched-capacitor converters are useful for applications that require small currents, usually less than 100 mA. Applications include use in RS-232 data signals that require both positive and negative voltages for logic levels; in flash memory circuits, where large voltages are needed to erase stored information; and in drivers for LEDs and LCD displays.

The basic types of switched-capacitor converters are the step-up (boost), the inverting, and the step-down (buck) circuits. The following discussion introduces the concepts of switched-capacitor converters.

The Step-Up Switched-Capacitor Converter

A common application of a switched-capacitor converter is the step-up (boost) converter. The basic principle is shown in Fig. 6-24a. A capacitor is first connected across the source to charge it to V_s . The charged capacitor is then connected in series with the source, producing an output voltage of $2V_s$.

A switching scheme to accomplish this is shown in Fig. 6-24b. The switch pair labeled 1 is closed and opened in a phase sequence opposite to that of switch pair 2. Switch pair 1 closes to charge the capacitor and then opens. Switch pair 2 then closes to produce an output of $2V_s$.

The switches can be implemented with transistors, or they can be implemented with transistors and diodes, as shown in Fig. 6-24c. Transistor M_1 is turned on, and C_1 is charged to V_s through D_1 . Next, M_1 is turned off and M_2 is turned on. Kirchhoff's voltage law around the path of the source, the charged

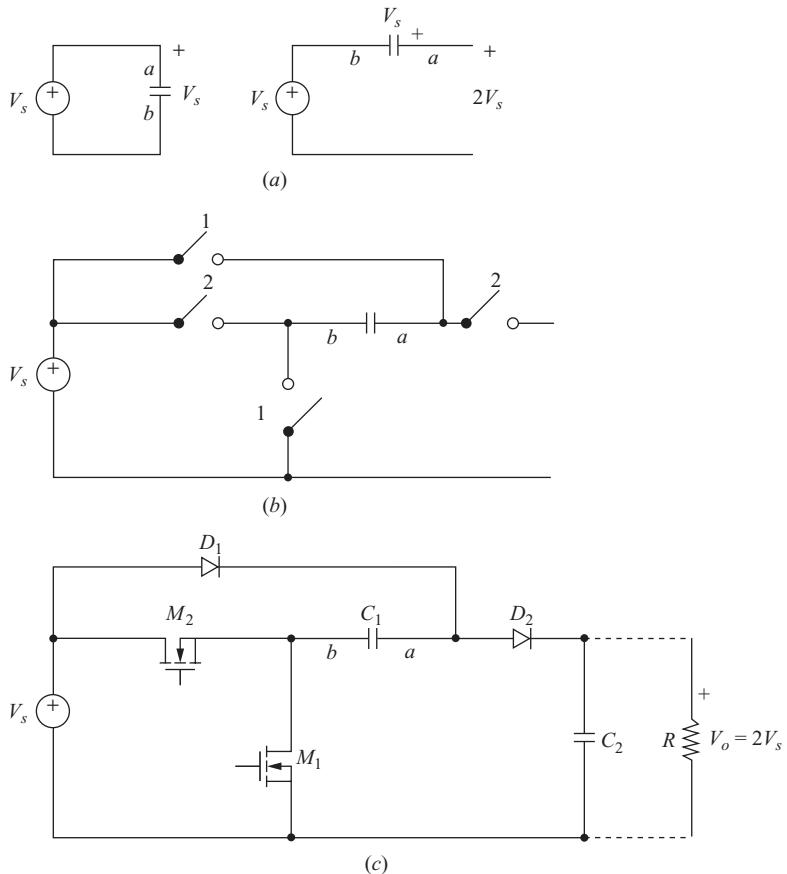


Figure 6-24 A switched-capacitor step-up converter. (a) A capacitor is charged and then reconnected to produce a voltage of twice that of the source; (b) A switch arrangement; (c) An implementation using transistors and diodes and showing a second capacitor C_2 to sustain the output voltage during switching.

capacitor C_1 , and V_o shows that $V_o = 2V_s$. The capacitor C_2 on the output is required to sustain the output voltage and to supply load current when C_1 is disconnected from the load. With C_2 included, it will take several switching cycles to charge it and achieve the final output voltage. With the resistor connected, current will flow from the capacitors, but the output voltage will be largely unaffected if the switching frequency is sufficiently high and capacitor charges are replenished in short time intervals. The output will be less than $2V_s$ for real devices because of voltage drops in the circuit.

Converters can be made to step up the input voltage to values greater than $2V_s$. In Fig. 6-25a, two capacitors are charged and then reconnected to create a

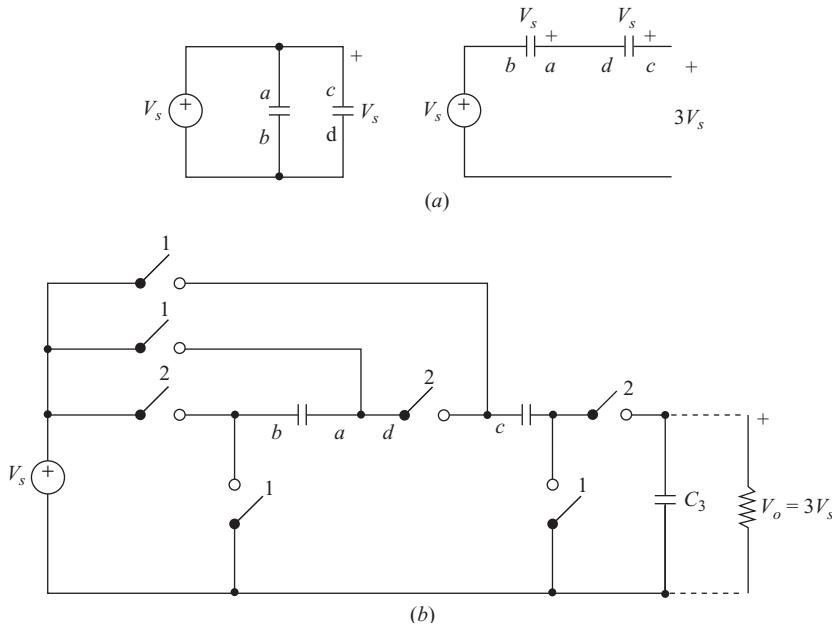


Figure 6-25 A step-up switched-capacitor converter to produce 3 times the source voltage. (a) Each capacitor is charged to V_s and reconnected to produce an output of $3V_s$; (b) A switch arrangement also shows an output capacitor to sustain the output voltage during switching.

voltage of $3V_s$. A switching arrangement to implement this circuit is shown in Fig. 6-25b. Switch sets 1 and 2 open and close alternately. The circuit includes an output capacitor C_3 to sustain the voltage across the load during the switching cycle.

The Inverting Switched-Capacitor Converter

The inverting switched-capacitor converter is useful for producing a negative voltage from a single voltage source. For example, -5 V can be made from a 5 -V source, thereby creating a $+/- 5$ -V supply. The basic concept is shown in Fig. 6-26a. A capacitor is charged to the source voltage and then connected to the output with opposite polarity.

A switching scheme to accomplish this is shown in Fig. 6-26b. Switch pairs 1 and 2 open and close in opposite phase sequence. Switch pair 1 closes to charge the capacitor and then opens. Switch pair 2 then closes to produce an output of $-V_s$.

A switch configuration to implement the inverting circuit is shown in Fig. 6-26c. An output capacitor C_2 is included to sustain the output and supply current to the load during the switching cycle. Transistor M_1 is turned on, charging C_1 to V_s through D_1 . Transistor M_1 is turned off and M_2 is turned on, charging C_2 with a

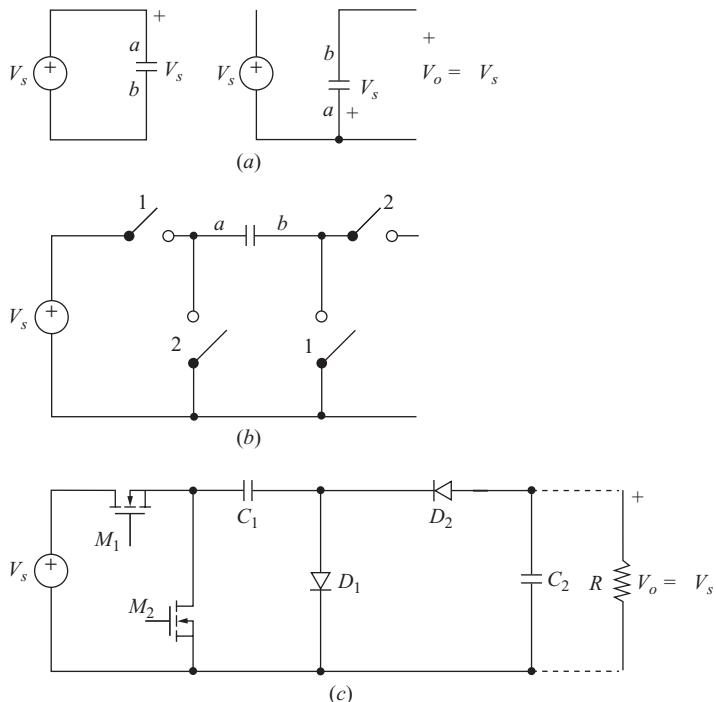


Figure 6-26 The inverting switched-capacitor converter. (a) The capacitor is charged to V_s and then reconnected to produce an output of $-V_s$; (b) A switch arrangement; (c) An implementation using transistors and diodes and showing a second capacitor to sustain the output voltage during switching.

polarity that is positive on the bottom. After several switching cycles, the output voltage is $-V_s$.

The Step-Down Switched-Capacitor Converter

A step-down (buck) switched-capacitor converter is shown in Fig. 6-27. In Fig. 6-27a, two capacitors of equal value are connected in series, resulting in a voltage of $V_s/2$ across each. The capacitors are then reconnected in parallel, making the output voltage $V_s/2$. A switching scheme to accomplish this is shown in Fig. 6-27b. Switch pairs 1 and 2 open and close in opposite phase sequence. With the resistor connected, current will flow from the capacitors, but the output voltage will be unaffected if the switching frequency is sufficiently high and capacitor charges are replenished in short time intervals.

A switch configuration to implement the inverting circuit is shown in Fig. 6-27c. Transistor M_1 is turned on, and both capacitors charge through D_1 .

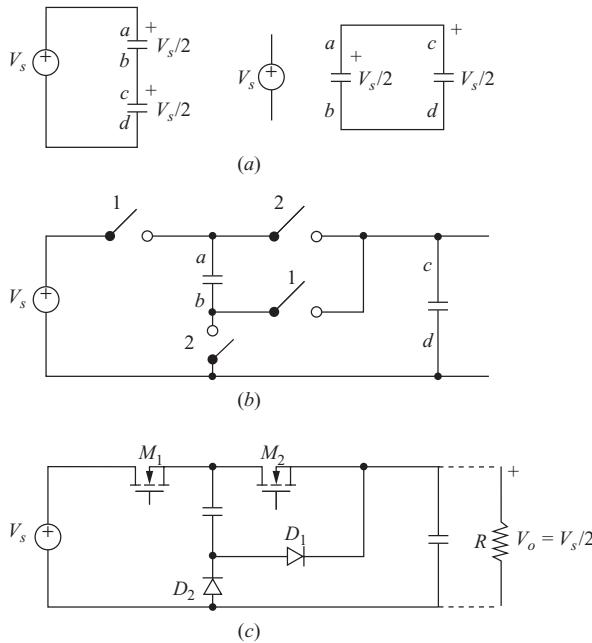


Figure 6-27 The step-down switched-capacitor converter.

(a) The capacitors are in series and each is charged to $V_s/2$, followed by the capacitors in parallel, with the output voltage at $V_s/2$; (b) A switch arrangement; (c) An implementation using transistors and diodes.

Transistor M_1 is turned off, and M_2 is turned on, connecting the capacitors in parallel through D_2 . And D_2 is forward-biased as the capacitors discharge into the load resistor.

6.13 PSPICE SIMULATION OF DC-DC CONVERTERS

The circuit model to be used for PSpice simulation of the dc-dc converters discussed in this chapter depends on the ultimate goal of the simulation. To predict the behavior of a circuit with the goal of producing the periodic voltage and current waveforms requires a circuit model that includes a switch. A voltage-controlled switch is convenient for this application. If the circuit includes an ideal diode and lossless inductors and capacitors, the simulation results will be first-order approximations of circuit behavior, much the same as the analytical work done previously in this chapter. By including parasitic elements and using nonideal switching devices in the circuit model, the simulation will be useful to investigate how a real circuit is expected to depart from the ideal.

Another simulation goal may be to predict the dynamic behavior of a dc-dc converter for changes in the source voltage or load current. A disadvantage of

using the cycle-to-cycle switched model is that the time for overall circuit transients may be orders of magnitude larger than the switching period, thereby making the program execution time quite long. A circuit model that does not include the cycle-by-cycle details but does simulate the large-scale dynamic behavior by using averaging techniques may be preferred. PSpice simulations for both cycle-to-cycle and large-scale dynamic behavior are discussed in this section.

A Switched PSpice Model

A voltage-controlled switch is a simple way to model a transistor switch that would actually be used in a physical converter. The voltage-controlled switch has an on resistance that could be selected to match the transistor's, or the on resistance could be chosen negligibly small to simulate an ideal switch. A pulse voltage source acts as the control for the switch.

When periodic closing and opening of the switch in a dc-dc converter begins, a transient response precedes the steady-state voltages and currents described earlier in this chapter. The following example illustrates a PSpice simulation for a buck converter using idealized models for circuit components.

EXAMPLE 6-11

Buck Converter Simulation Using Idealized Components

Use PSpice to verify the buck converter design in Example 6-3.

The buck converter has the following parameters:

$$V_s = 3.3 \text{ V}$$

$$L = 1 \mu\text{H}$$

$$C = 667 \mu\text{F} \quad \text{with an ESR of } 15 \text{ m}\Omega$$

$$R = 0.3 \Omega \quad \text{for a load current of } 4 \text{ A}$$

$$D = 0.364 \quad \text{for an output of } 1.2 \text{ V}$$

$$\text{Switching frequency} = 500 \text{ kHz}$$

■ Solution

A PSpice model for the buck converter is shown in Fig. 6-28. A voltage-controlled switch (Sbreak) is used for the switching transistor, with the on resistance R_{on} set to $1 \text{ m}\Omega$ to approximate an ideal device. An ideal diode is simulated by letting the diode parameter n (the emission coefficient in the diode equation) be 0.001. The switch is controlled by a pulse voltage source. The parameter statements file facilitates modification of the circuit file for other buck converters. Initial conditions for the inductor current and capacitor voltage are assumed to be zero to demonstrate the transient behavior of the circuit.

Figure 6-29a shows the Probe output for inductor current and capacitor voltage. Note that there is a transient response of the circuit before the steady-state periodic condition is reached. From the steady-state portion of the Probe output shown in Fig. 6-29b, the maximum and minimum values of the output voltage are 1.213 and 1.1911 V, respectively, for a peak-to-peak variation of about 22 mV, agreeing well with the 24-mV design objective. The maximum and minimum inductor currents are about 4.77 and 3.24 A, agreeing well with the 4.8- and 3.2-A design objectives.

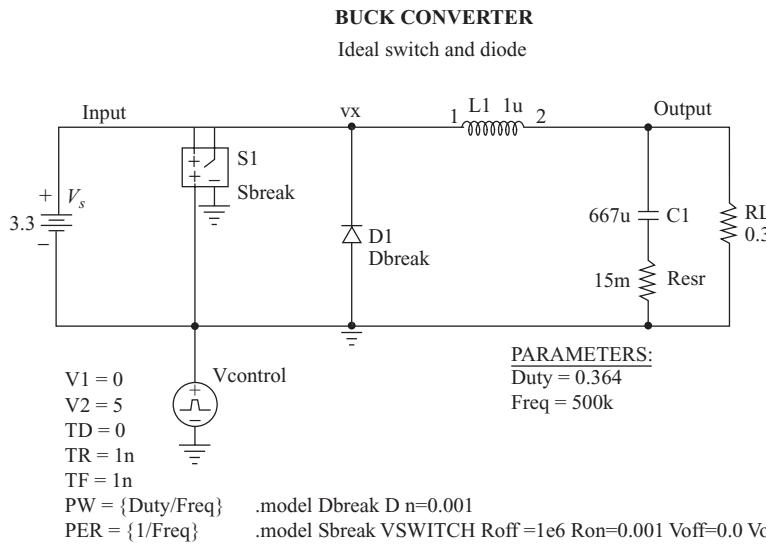


Figure 6-28 PSpice circuit for the buck converter.

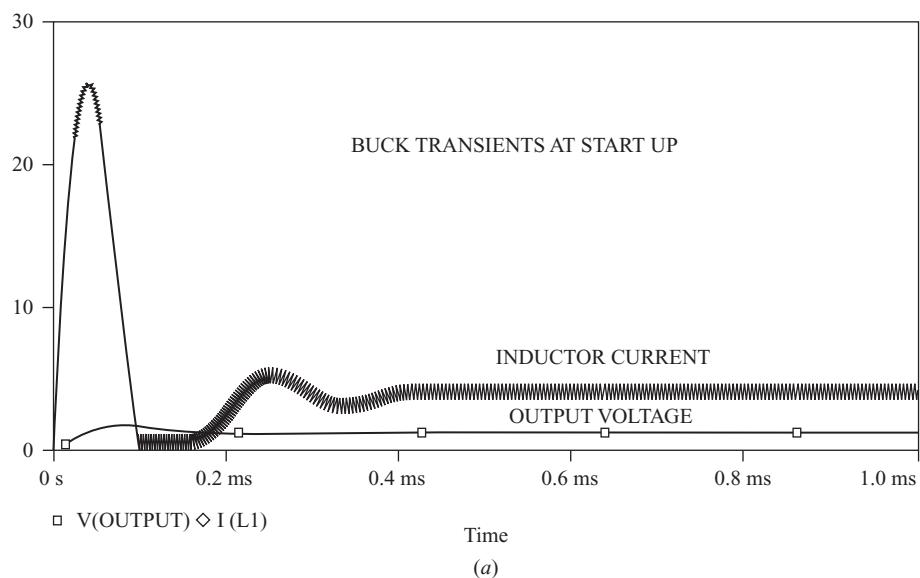


Figure 6-29 Probe output for Example 6-11 (a) showing the transient at start-up and (b) in steady state.

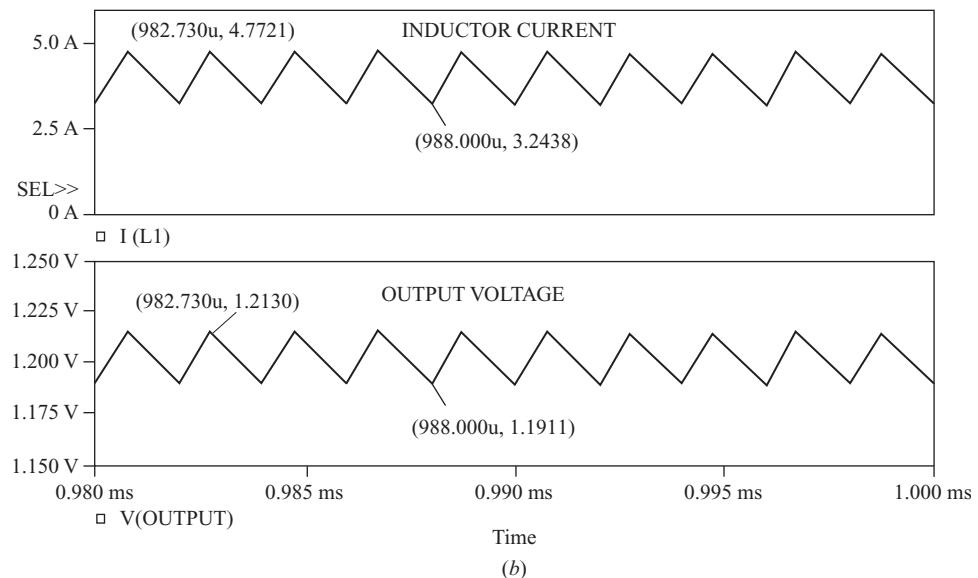


Figure 6-29 (continued)

An Averaged Circuit Model

PSpice simulation of the dc-dc buck converter in Example 6-11 includes both the large scale transient behavior and the cycle-to-cycle waveforms of voltage and current. If the goal of a simulation is to determine the large-scale transient behavior, the cycle-to-cycle response merely adds to the execution time of the program. A more time-efficient way to simulate the transient behavior of dc-dc converters is to use a circuit model that produces the *average* values of voltages and currents only, rather than including the detailed variations around the averages. In general, transient behavior for dc-dc converters can be predicted by analyzing linear networks, with the response equal to the average value of the switching waveforms. The discussion that follows is focused on the buck converter operating in the continuous-current mode.

The transient behavior of the average output voltage can be described using linear circuit analysis. The input v_x to the RLC circuit of the buck converter of Fig. 6-3a has an average value of $\bar{V}_x = V_s D$. The response of the RLC circuit to a step input voltage of $v_x(t) = (V_s D)u(t)$ represents the average of the output voltage and current waveforms when the converter is turned on. This represents the same large-scale transient that was present in the PSpice simulation shown in Fig. 6-29a.

For complete simulation of the large-scale behavior of a dc-dc converter, it is desirable to include the proper voltage and current relationships between the source and the load. Taking the buck converter as an example, the relationship between average voltage and current at the input and output for continuous inductor current is given by

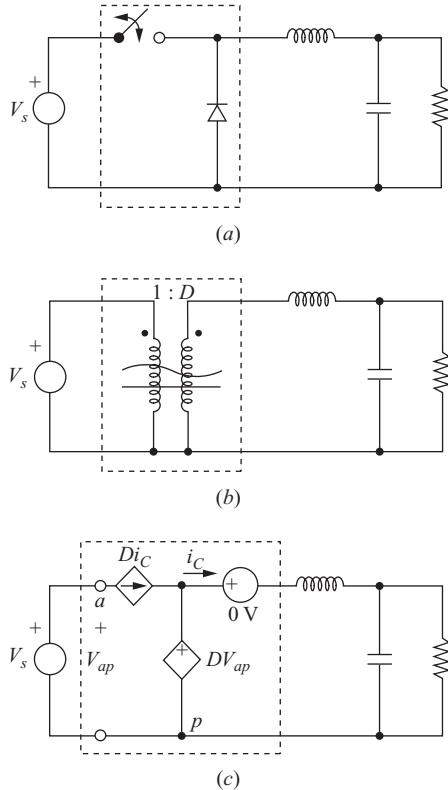


Figure 6-30 (a) Buck converter with switch;
 (b) Circuit model for averaged buck converter;
 (c) PSpice circuit.

$$\frac{V_o}{V_s} = \frac{I_s}{I_o} = D \quad (6-103)$$

Since $V_o = V_s D$ and $I_o = I_s/D$, the switch in a model for computing average voltage and current is the same as a “transformer” which has a turns ratio of $1:D$. Circuit models for a buck converter using a $1:D$ transformer and a PSpice circuit for implementing the averaged model are shown in Fig. 6-30. The circuit symbol for the transformer indicates that the model is valid for both ac and dc signals.

The following example illustrates the use of the PSpice model to simulate the response of average voltage and current for a buck converter.

EXAMPLE 6-12

Averaged Buck Converter

Use the averaged circuit of Fig. 6-30c to simulate the buck converter having parameters

$$V_s = 10 \text{ V}$$

$$D = 0.2$$

$$L = 400 \mu\text{H}$$

$$C = 400 \mu\text{F}$$

$$R = 2 \Omega$$

$$f = 5 \text{ kHz}$$

Use initial conditions of zero for inductor current and capacitor voltage.

■ Solution

The PSpice implementation of the averaged model is shown in Fig. 6-31a. The simulation results from both a switched model and for the averaged model are shown in Fig. 6-31b. Note that the switched model shows the cycle-to-cycle variation, while the average model shows only the averaged values.

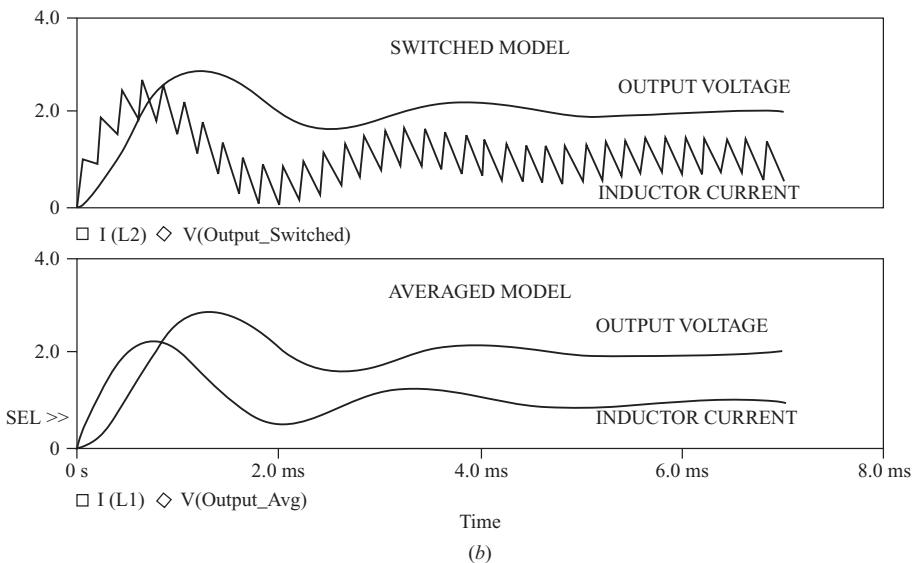
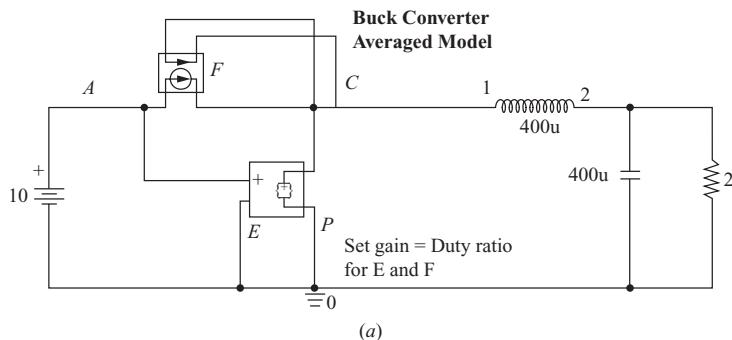


Figure 6-31 (a) PSpice implementation of the averaged buck converter model; (b) Probe output for both the switched model and the averaged model.

The averaged model can be quite useful in investigating the dynamic behavior of the converter when it is subjected to changes in operating parameters. Such an analysis is essential when the output is regulated through a feedback loop which is designed to keep the output at a set level by adjusting the duty ratio of the switch to accommodate variations in the source or the load. Closed-loop response is discussed in Chap. 7 on dc power supplies.

The following example illustrates the use of the averaged circuit model to simulate a step change in load resistance.

EXAMPLE 6-13
Step Change in Load

Use the averaged buck converter model to determine the dynamic response when the load resistance is changed. The circuit parameters are

$$\begin{aligned}V_s &= 50 \text{ V} \\L &= 1 \text{ mH} \quad \text{with a series resistance of } 0.4 \Omega \\C &= 100 \mu\text{F} \quad \text{with an equivalent series resistance of } 0.5 \Omega \\R &= 4 \Omega, \quad \text{stepped to } 2 \Omega \text{ and back to } 4 \Omega \\D &= 0.4 \\ \text{Switching frequency} &= 5 \text{ kHz}\end{aligned}$$

Solution

Step changes in load are achieved by switching a second 4- Ω resistor across the output at 6 ms and disconnecting it at 16 ms. The averaged model shows the transients associated with output voltage and inductor current (Fig. 6-32b). Also shown for comparison are the results of a different simulation using a switch, showing the cycle-to-cycle variations in voltage and current.

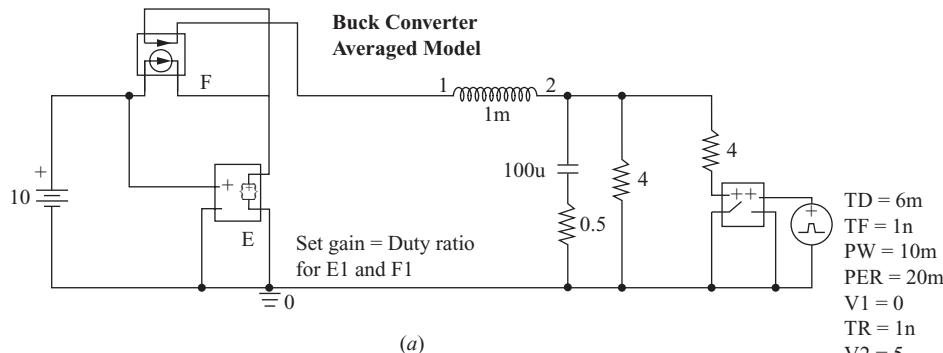


Figure 6-32 (a) PSpice implementation of the averaged model with a switched load;
(b) Probe results for both the switched model and the averaged model.

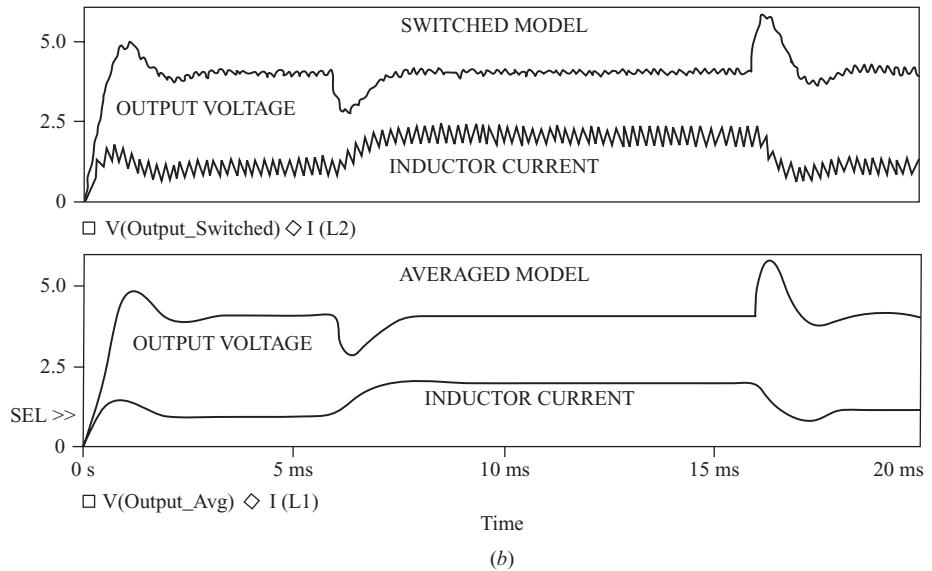
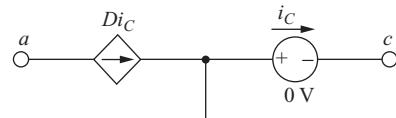
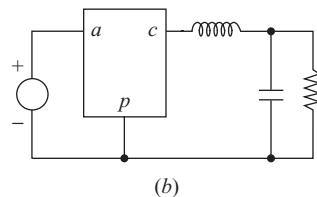


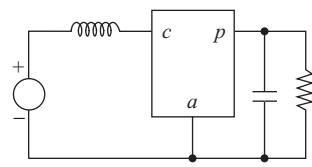
Figure 6-32 (continued)



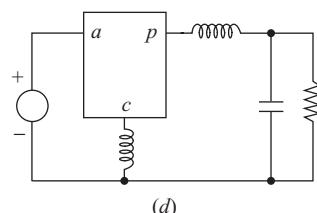
(a)



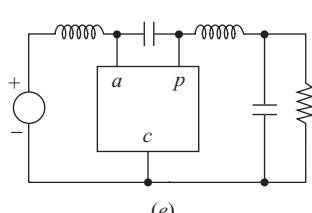
(b)



(c)



(d)



(e)

Figure 6-33
Averaged switch
model in dc-dc
converters. (a) PSpice
averaged model for
switch and diode;
(b) Buck equivalent;
(c) Boost equivalent;
(d) Buck-boost
equivalent; (e) Cuk
equivalent.

The averaged switch model can be used to simulate the other dc-dc converters discussed in this chapter. Figure 6-33 shows how the average switch model is used in the boost, buck-boost, and Ćuk converters for continuous-current operation. The designation of the switch terminals *a*, *p*, and *c* represents active, passive, and common terminals.

6.14 Summary

- A switched-mode dc-dc converter is much more efficient than a linear converter because of reduced losses in the electronic switch.
- A buck converter has an output voltage less than the input.
- A boost converter has an output voltage greater than the input.
- Buck-boost and Ćuk converters can have output voltages greater than or less than the input, but there is a polarity reversal.
- A SEPIC (single-ended primary-inductor converter) can have an output voltage greater than or less than the input with no polarity reversal.
- Output voltage is generally reduced from the theoretical value when switch drops and inductor resistances are included in the analysis.
- Capacitor equivalent series resistance (ESR) may produce an output voltage ripple much greater than that of the capacitance alone.
- Interleaved converters have parallel switch/inductor paths to reduce the current variation in the output capacitor.
- Discontinuous-current modes for dc-dc converters are possible and sometimes desirable, but input-output relationships are different from those for the continuous-current modes.
- Switched-capacitor converters charge capacitors in one configuration and then use switches to reconnect the capacitors to produce an output voltage different from the input.
- PSpice can be used to simulate dc-dc converters by using a voltage-controlled switch or by using an averaged circuit model.

6.15 Bibliography

- S. Ang and A. Oliva, *Power-Switching Converters*, 2d ed., Taylor & Francis, Boca Raton, Fla., 2005.
- C. Basso, *Switch-Mode Power Supplies*, McGraw-Hill, New York, 2008.
- B. K. Bose, *Power Electronics and Motor Drives: Advances and Trends*, Elsevier/Academic Press, Boston, 2006.
- R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2d ed., Kluwer Academic, Boston, 2001.
- W. Gu, “Designing a SEPIC Converter,” National Semiconductor Application Note 1484, 2007, <http://www.national.com/an/AN/AN-1484.pdf>.
- P. T. Krein, *Elements of Power Electronics*, Oxford University Press, New York, 1998.
- D. Maksimović, and S. Dhar, “Switched-Capacitor DC-DC Converters for Low-Power On-Chip Applications,” *IEEE Annual Power Electronics Specialists Conference*, vol. 1, pp. 54–59, 1999.
- R. D. Middlebrook and, S. Ćuk, *Advances in Switched-Mode Power Conversion*, vols. I and II, TESLAco, Pasadena, Calif., 1981.
- N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3d ed., Wiley, New York, 2003.

- A. I. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design*, McGraw-Hill, New York, 2009.
- M. H. Rashid, *Power Electronics: Circuits, Devices, and Systems*, 3d ed., Prentice-Hall, Upper Saddle River, N.J., 2004.
- “SEPIC Equations and Component Ratings,” MAXIM Application Note 1051, 2002, <http://www.maxim-ic.com/an1051>.
- V. Vorperian, “Simplified Analysis of PWM Converters Using Model of PWM Switch”, *IEEE Transactions on Aerospace and Electronic Systems*, May 1990.

Problems

Linear Converters

- 6-1.** What is the relationship between V_o/V_s and efficiency for the linear converter described in Sec. 6.1?
- 6-2.** A dc power supply must step down a 100-V. source to 30 V. The output power is 100 W. (a) Determine the efficiency of the linear converter of Fig. 6-1 when it is used for this application. (b) How much energy is lost in the transistor in 1 yr? (c) Using the electric rate in your area, what is the cost of the energy loss for 1 yr?

Basic Switched Converter

- 6-3.** The basic dc-dc converter of Fig. 6-2a has a source of 100 V and a load resistance of $10\ \Omega$. The duty ratio of the switch is $D = 0.6$, and the switching frequency is 1 kHz. Determine (a) the average voltage across the load, (b) the rms voltage across the load, and (c) the average power absorbed by the load. (d) What would happen if the switching frequency were increased to 2 kHz?

Buck Converter

- 6-4.** The buck converter of Fig. 6-3a has the following parameters: $V_s = 24\text{ V}$, $D = 0.65$, $L = 25\ \mu\text{H}$, $C = 15\ \mu\text{F}$, and $R = 10\ \Omega$. The switching frequency is 100 kHz. Determine (a) the output voltage, (b) the maximum and minimum inductor currents, and (c) the output voltage ripple.
- 6-5.** The buck converter of Fig. 6-3a has the following parameters: $V_s = 15\text{ V}$, $D = 0.6$, $L = 10\ \mu\text{H}$, $C = 50\ \mu\text{F}$, and $R = 5\ \Omega$. The switching frequency is 150 kHz. Determine (a) the output voltage, (b) the maximum and minimum inductor currents, and (c) the output voltage ripple.
- 6-6.** The buck converter of Fig. 6-3a has an input of 50 V and an output of 25 V. The switching frequency is 100 kHz, and the output power to a load resistor is 125 W. (a) Determine the duty ratio. (b) Determine the value of inductance to limit the peak inductor current to 6.25 A. (c) Determine the value of capacitance to limit the output voltage ripple to 0.5 percent.
- 6-7.** A buck converter has an input of 6 V and an output of 1.5 V. The load resistor is $3\ \Omega$, the switching frequency is 400 kHz, $L = 5\ \mu\text{H}$, and $C = 10\ \mu\text{F}$. (a) Determine the duty ratio. (b) Determine the average, peak, and rms inductor currents. (c) Determine the average source current. (d) Determine the peak and average diode current.
- 6-8.** The buck converter of Fig. 6-3a has $V_s = 30\text{ V}$, $V_o = 20\text{ V}$, and a switching frequency of 40 kHz. The output power is 25 W. Determine the size of the inductor such that the minimum inductor current is 25 percent of the average inductor current.

- 6-9.** A buck converter has an input voltage that varies between 50 and 60 V and a load that varies between 75 and 125 W. The output voltage is 20 V. For a switching frequency of 100 kHz, determine the minimum inductance to provide for continuous current for every operating possibility.
- 6-10.** A buck converter has an input voltage that varies between 10 and 15 V and a load current that varies between 0.5 A and 1.0 A. The output voltage is 5 V. For a switching frequency of 200 kHz, determine the minimum inductance to provide for continuous current for every operating possibility.
- 6-11.** Design a buck converter such that the output voltage is 15 V when the input is 48 V. The load is $8\ \Omega$. Design for continuous inductor current. The output voltage ripple must be no greater than 0.5 percent. Specify the switching frequency and the value of each of the components. Assume ideal components.
- 6-12.** Specify the voltage and current ratings for each of the components in the design of Prob. 6-11.
- 6-13.** Design a buck converter to produce an output of 15 V from a 24-V source. The load is 2 A. Design for continuous inductor current. Specify the switching frequency and the values of each of the components. Assume ideal components.
- 6-14.** Design a buck converter that has an output of 12 V from an input of 18 V. The output power is 10 W. The output voltage ripple must be no more than 100 mV p-p. Specify the duty ratio, switching frequency, and inductor and capacitor values. Design for continuous inductor current. Assume ideal components.
- 6-15.** The voltage V_x in Fig. 6-3a for the buck converter with continuous inductor current is the pulsed waveform of Fig. 6-2c. The Fourier series for this waveform has a dc term of $V_s D$. The ac terms have a fundamental frequency equal to the switching frequency and amplitudes given by

$$V_n = \frac{\sqrt{2}V_s}{n\pi} \sqrt{1 - \cos(2\pi nD)} \quad n = 1, 2, 3, \dots$$

Using ac circuit analysis, determine the amplitude of the first ac term of the Fourier series for voltage across the load for the buck converter in Example 6-1. Compare your result with the peak-to-peak voltage ripple determined in the example. Comment on your results.

- 6-16.** (a) If the equivalent series resistance of the capacitor in the buck converter in Example 6-2 is $0.5\ \Omega$, recompute the output voltage ripple. (b) Recompute the required capacitance to limit the output voltage ripple to 0.5 percent if the ESR of the capacitor is given by $r_C = 50(10)^{-6}/C$, where C is in farads.

Boost Converter

- 6-17.** The boost converter of Fig. 6-8 has parameter $V_s = 20\text{ V}$, $D = 0.6$, $R = 12.5\ \Omega$, $L = 10\ \mu\text{H}$, $C = 40\ \mu\text{F}$, and the switching frequency is 200 kHz. (a) Determine the output voltage. (b) Determine the average, maximum, and minimum inductor currents. (c) Determine the output voltage ripple. (d) Determine the average current in the diode. Assume ideal components.
- 6-18.** For the boost converter in Prob. 6-17, sketch the inductor and capacitor currents. Determine the rms values of these currents.
- 6-19.** A boost converter has an input of 5 V and an output of 25 W at 15 V. The minimum inductor current must be no less than 50 percent of the average. The

output voltage ripple must be less than 1 percent. The switching frequency is 300 kHz. Determine the duty ratio, minimum inductor value, and minimum capacitor value.

- 6-20. Design a boost converter to provide an output of 18 V from a 12-V source. The load is 20 W. The output voltage ripple must be less than 0.5 percent. Specify the duty ratio, the switching frequency, the inductor size and rms current rating, and the capacitor size and rms current rating. Design for continuous current. Assume ideal components.
- 6-21. The ripple of the output voltage of the boost converter was determined assuming that the capacitor current was constant when the diode was off. In reality, the current is a decaying exponential with a time constant RC . Using the capacitance and resistance values in Example 6-4, determine the change in output voltage while the switch is closed by evaluating the voltage decay in the RC circuit. Compare it to that determined from Eq. (6-34).
- 6-22. For the boost converter with a nonideal inductor, produce a family of curves of V_o/V_s similar to Fig. 6-10a for $r_L/R = 0.1, 0.3, 0.5$, and 0.7 .

Buck-boost Converter

- 6-23. The buck-boost converter of Fig. 6-11 has parameters $V_s = 12$ V, $D = 0.6$, $R = 10$ Ω , $L = 10$ μH , $C = 20$ μF , and a switching frequency of 200 kHz. Determine (a) the output voltage, (b) the average, maximum, and minimum inductor currents, and (c) the output voltage ripple.
- 6-24. Sketch the inductor and capacitor currents for the buck-boost converter in Prob. 6-23. Determine the rms values of these currents.
- 6-25. The buck-boost converter of Fig. 6-11 has $V_s = 24$ V, $V_o = -36$ V, and a load resistance of 10Ω . If the switching frequency is 100 kHz, (a) determine the inductance such that the minimum current is 40 percent of the average and (b) determine the capacitance required to limit the output voltage ripple to 0.5 percent.
- 6-26. Design a buck-boost converter to supply a load of 75 W at 50 V from a 40-V source. The output ripple must be no more than 1 percent. Specify the duty ratio, switching frequency, inductor size, and capacitor size.
- 6-27. Design a dc-dc converter to produce a -15 -V output from a source that varies from 12 to 18 V. The load is a $15\text{-}\Omega$ resistor.
- 6-28. Design a buck-boost converter that has a source that varies from 10 to 14 V. The output is regulated at -12 V. The load varies from 10 to 15 W. The output voltage ripple must be less than 1 percent for any operating condition. Determine the range of the duty ratio of the switch. Specify values of the inductor and capacitor, and explain how you made your design decisions.

Ćuk Converter

- 6-29. The Ćuk converter of Fig. 6-13a has parameters $V_s = 12$ V, $D = 0.6$, $L_1 = 200$ μH , $L_2 = 100$ μH , $C_1 = C_2 = 2$ μF , and $R = 12 \Omega$, and the switching frequency is 250 kHz. Determine (a) the output voltage, (b) the average and the peak-to-peak variation of the currents in L_1 and L_2 , and (c) the peak-to-peak variation in the capacitor voltages.
- 6-30. The Ćuk converter of Fig. 6-13a has an input of 20 V and supplies an output of 1.0 A at 10 V. The switching frequency is 100 kHz. Determine the values of L_1

and L_2 such that the peak-to-peak variation in inductor currents is less than 10 percent of the average.

- 6-31.** Design a Ćuk converter that has an input of 25 V and an output of -30 V. The load is 60 W. Specify the duty ratio, switching frequency, inductor values, and capacitor values. The maximum change in inductor currents must be 20 percent of the average currents. The ripple voltage across C_1 must be less than 5 percent, and the output ripple voltage must be less than 1 percent.

SEPIC Circuit

- 6-32.** The SEPIC circuit of Fig. 6-14a has $V_s = 5$ V, $V_o = 12$ V, $C_1 = C_2 = 50 \mu\text{F}$, $L_1 = 10 \mu\text{H}$, and $L_2 = 20 \mu\text{H}$. The load resistor is 4Ω . Sketch the currents in L_1 and L_2 , indicating average, maximum, and minimum values. The switching frequency is 100 kHz.
- 6-33.** The SEPIC circuit of Fig. 6-14a has $V_s = 3.3$ V, $D = 0.7$, $L_1 = 4 \mu\text{H}$, and $L_2 = 10 \mu\text{H}$. The load resistor is 5Ω . The switching frequency is 300 kHz. (a) Determine the maximum and minimum values of the currents in L_1 and L_2 . (b) Determine the variation in voltage across each capacitor.
- 6-34.** The relationship between input and output voltages for the SEPIC circuit of Fig. 6-14a expressed in Eq. (6-74) was developed using the average voltage across L_1 . Derive the relationship using the average voltage across L_2 .
- 6-35.** A SEPIC circuit has an input voltage of 15 V and is to have an output of 6 V. The load resistance is 2Ω , and the switching frequency is 250 kHz. Determine values of L_1 and L_2 such that the variation in inductor current is 40 percent of the average value. Determine values of C_1 and C_2 such that the variation in capacitor voltage is 2 percent.
- 6-36.** A SEPIC circuit has an input voltage of 9 V and is to have an output of 2.7 V. The output current is 1 A, and the switching frequency is 300 kHz. Determine values of L_1 and L_2 such that the variation in inductor current is 40 percent of the average value. Determine values of C_1 and C_2 such that the variation in capacitor voltage is 2 percent.

Nonideal Effects

- 6-37.** The boost converter of Example 6-4 has a capacitor with an equivalent series resistance of 0.6Ω . All other parameters are unchanged. Determine the output voltage ripple.
- 6-38.** Equation (6-88) expresses the output voltage of a buck converter in terms of input, duty ratio, and voltage drops across the nonideal switch and diode. Derive an expression for the output voltage of a buck-boost converter for a nonideal switch and diode.

Discontinuous Current

- 6-39.** The buck converter of Example 6-2 was designed for a $10-\Omega$ load. (a) What is the limitation on the load resistance for continuous-current operation? (b) What would be the range of output voltage for a load resistance range of 5 to 20Ω ? (c) Redesign the converter so inductor current remains continuous for a load resistance range of 5 to 20Ω .

- 6-40.** The boost converter of Example 6-4 was designed for a $50\text{-}\Omega$ load. (a) What is the limitation on the load resistance for continuous-current operation? (b) What would be the range of output voltage for a load resistance range of 25 to $100\ \Omega$? (c) Redesign the converter so inductor current remains continuous for a load resistance range of 25 to $100\ \Omega$.
- 6-41.** Section 6.11 describes the buck and boost converters for discontinuous-current operation. Derive an expression for the output voltage of a buck-boost converter when operating in the discontinuous-current mode.

Switched-capacitor Converters

- 6-42.** Capacitors C_1 and C_2 in Fig. P6-42 are equal in value. In the first part of the switching cycle, the switches labeled 1 are closed while the switches labeled 2 are open. In the second part of the cycle, switches 1 are opened and then switches 2 are closed. Determine the output voltage V_o at the end of the switching cycle. *Note:* A third capacitor would be placed from V_o to ground to sustain the output voltage during subsequent switching cycles.

PSpice

- 6-43.** Simulate the buck converter of Example 6-11, but use the IRF150 MOSFET from the PSpice device library for the switch. Use an idealized gate drive circuit of a pulsed voltage source and small resistance. Use the default model for the diode. Use Probe to graph $p(t)$ versus t for the switch for steady-state conditions. Determine the average power loss in the switch.
- 6-44.** Simulate the buck converter of Example 6-1 using PSpice. (a) Use an ideal switch and ideal diode. Determine the output ripple voltage. Compare your PSpice results with the analytic results in Example 6-1. (b) Determine the steady-state output voltage and voltage ripple using a switch with an on resistance of $2\ \Omega$ and the default diode model.
- 6-45.** Show that the equivalent circuits for the PSpice averaged models in Fig. 6-33 satisfy the average voltage and current input-output relationships for each of the converters.

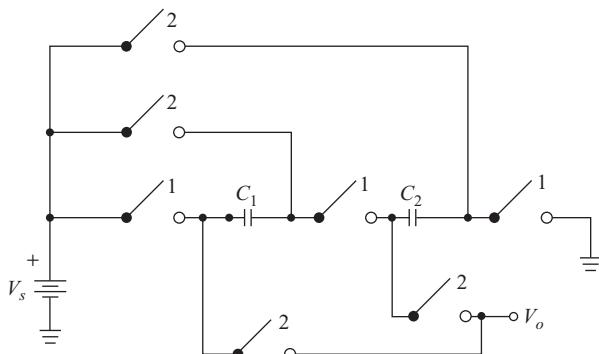


Figure P6-42

DC Power Supplies

7.1 INTRODUCTION

A basic disadvantage of the dc-dc converters discussed in Chap. 6 is the electrical connection between the input and the output. If the input supply is grounded, that same ground will be present on the output. A way to isolate the output from the input electrically is with a transformer. If the dc-dc converter has a first stage that rectifies an ac power source to dc, a transformer could be used on the ac side. However, not all applications require ac to dc conversion as a first stage. Moreover, a transformer operating at a low frequency (50 or 60 Hz) requires a large magnetic core and is therefore relatively large, heavy, and expensive.

A more efficient method of providing electrical isolation between input and output of a dc-dc converter is to use a transformer in the switching scheme. The switching frequency is much greater than the ac power-source frequency, enabling the transformer to be small. Additionally, the transformer turns ratio provides increased design flexibility in the overall relationship between the input and the output of the converter. With the use of multiple transformer windings, switching converters can be designed to provide multiple output voltages.

7.2 TRANSFORMER MODELS

Transformers have two basic functions: to provide electrical isolation and to step up or step down time-varying voltages and currents. A two-winding transformer

is depicted in Fig. 7-1a. An idealized model for the transformer, as shown in Fig. 7-1b, has input-output relationships

$$\begin{aligned}\frac{v_1}{v_2} &= \frac{N_1}{N_2} \\ \frac{i_1}{i_2} &= \frac{N_2}{N_1}\end{aligned}\quad (7-1)$$

The dot convention is used to indicate relative polarity between the two windings. When the voltage at the dotted terminal on one winding is positive, the voltage at the dotted terminal on the other winding is also positive. When current enters the dotted terminal on one winding, current leaves the dotted terminal on the other winding.

A more complete transformer model is shown in Fig. 7-1c. Resistors r_1 and r_2 represent resistances of the conductors, L_1 and L_2 represent leakage inductances of the windings, L_m represents magnetizing inductance, and r_m represents core loss. The ideal transformer is incorporated into this model to represent the voltage and current transformation between primary and secondary.

In some applications in this chapter, the ideal transformer representation is sufficient for preliminary investigation of a circuit. The ideal model assumes that the series resistances and inductances are zero and that the shunt elements are infinite. A somewhat better approximation for power supply applications includes the magnetizing inductance L_m , as shown in Fig. 7-1d. The value of L_m is an important design parameter for the flyback converter.

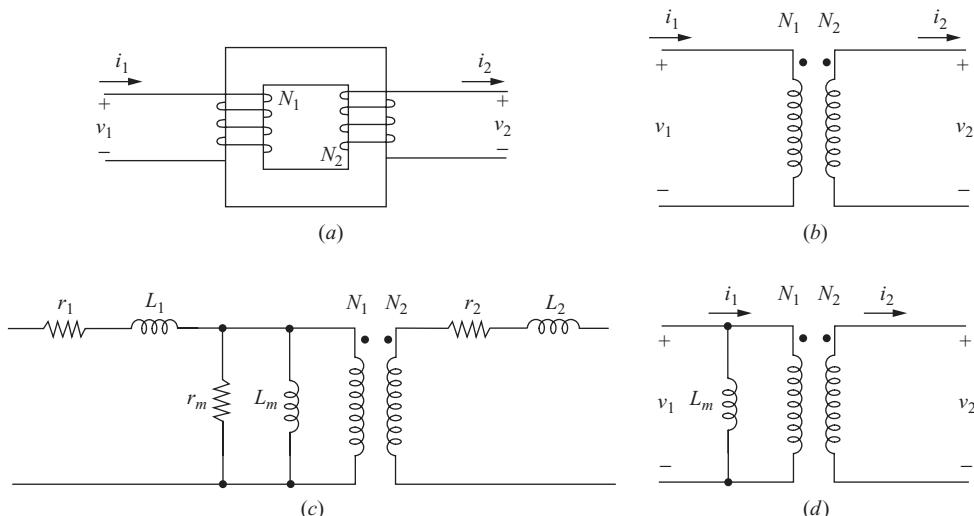


Figure 7-1 (a) Transformer; (b) Ideal model; (c) Complete model; (d) Model used for most power electronics circuits.

The leakage inductances L_1 and L_2 are usually not crucial to the general operation of the power electronics circuits described in this chapter, but they are important when considering switching transients. Note that in ac power system applications, the leakage inductance is normally the important analysis and design parameter.

For periodic voltage and current operation for a transformer circuit, the magnetic flux in the core must return to its starting value at the end of each switching period. Otherwise, flux will increase in the core and eventually cause saturation. A saturated core cannot support a voltage across a transformer winding, and this will lead to device currents that are beyond the design limits of the circuit.

7.3 THE FLYBACK CONVERTER

Continuous-Current Mode

A dc-dc converter that provides isolation between input and output is the flyback circuit of Fig. 7-2a. In a first analysis, Fig. 7-2b uses the transformer model which includes the magnetizing inductance L_m , as in Fig. 7-1d. The effects of

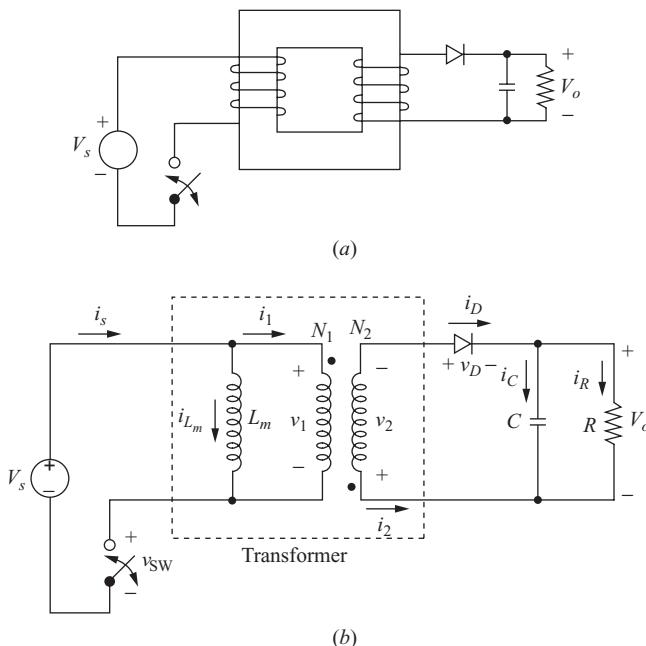


Figure 7-2 (a) Flyback converter; (b) Equivalent circuit using a transformer model that includes the magnetizing inductance; (c) Circuit for the switch on; (d) Circuit for the switch off.

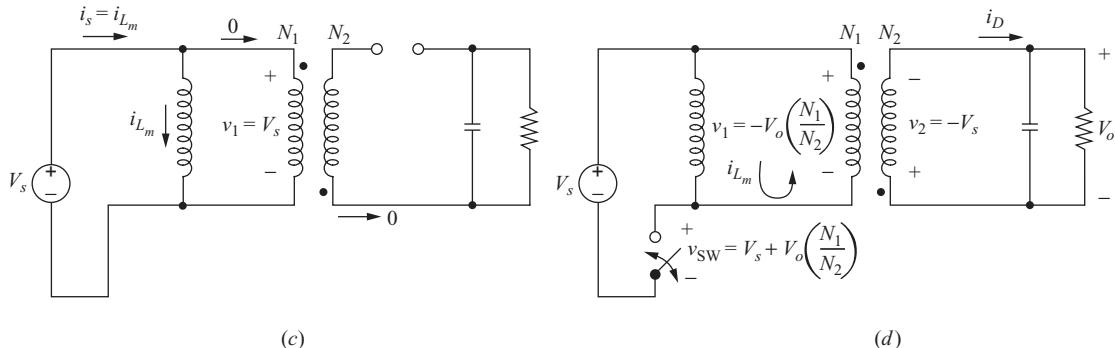


Figure 7-2 (continued)

losses and leakage inductances are important when considering switch performance and protection, but the overall operation of the circuit is best understood with this simplified transformer model. Note the polarity of the transformer windings in Fig. 7-2.

Additional assumptions for the analysis are made:

1. The output capacitor is very large, resulting in a constant output voltage V_o .
2. The circuit is operating in the steady state, implying that all voltages and currents are periodic, beginning and ending at the same points over one switching period.
3. The duty ratio of the switch is D , being closed for time DT and open for $(1 - D)T$.
4. The switch and diode are ideal.

The basic operation of the flyback converter is similar to that of the buck-boost converter described in Chap. 6. Energy is stored in L_m when the switch is closed and is then transferred to the load when the switch is open. The circuit is analyzed for both switch positions to determine the relationship between input and output.

Analysis for the Switch Closed On the source side of the transformer (Fig. 7-2c),

$$v_1 = V_s = L_m \frac{di_{L_m}}{dt}$$

$$\frac{di_{L_m}}{dt} = \frac{\Delta i_{L_m}}{\Delta t} = \frac{\Delta i_{L_m}}{DT} = \frac{V_s}{L_m}$$

Solving for the change in current in the transformer magnetizing inductance,

$$(\Delta i_{L_m})_{\text{closed}} = \frac{V_s DT}{L_m} \quad (7-2)$$

On the load side of the transformer,

$$v_2 = v_1 \left(\frac{N_2}{N_1} \right) = V_s \left(\frac{N_2}{N_1} \right)$$

$$v_D = -V_o - V_s \left(\frac{N_2}{N_1} \right) < 0$$

$$i_2 = 0$$

$$i_1 = 0$$

Since the diode is off, $i_2 = 0$, which means that $i_1 = 0$. So while the switch is closed, current is increasing linearly in the magnetizing inductance L_m , and there is no current in the windings of the ideal transformer in the model. Remember that in the actual transformer, this means that the current is increasing linearly in the physical primary winding, and no current exists in the secondary winding.

Analysis for the Switch Open When the switch opens (Fig. 7-2d), the current cannot change instantaneously in the inductance L_m , so the conduction path must be through the primary turns of the ideal transformer. The current i_{L_m} enters the undotted terminal of the primary and must exit the undotted terminal of the secondary. This is allowable since the diode current is positive. Assuming that the output voltage remains constant at V_o , the transformer secondary voltage v_2 becomes $-V_o$. The secondary voltage transforms back to the primary, establishing the voltage across L_m at

$$v_1 = -V_o \left(\frac{N_1}{N_2} \right)$$

Voltages and currents for an open switch are

$$v_2 = -V_o$$

$$v_1 = v_2 \left(\frac{N_1}{N_2} \right) = -V_o \left(\frac{N_1}{N_2} \right)$$

$$L_m \frac{di_{L_m}}{dt} = v_1 = -V_o \left(\frac{N_1}{N_2} \right)$$

$$\frac{di_{L_m}}{dt} = \frac{\Delta i_{L_m}}{\Delta t} = \frac{\Delta i_{L_m}}{(1-D)T} = \frac{-V_o}{L_m} \left(\frac{N_1}{N_2} \right)$$

Solving for the change in transformer magnetizing inductance with the switch open,

$$(\Delta i_{L_m})_{\text{open}} = \frac{-V_o(1-D)T}{L_m} \left(\frac{N_1}{N_2} \right) \quad (7-3)$$

Since the net change in inductor current must be zero over one period for steady-state operation, Eqs. (7-2) and (7-3) show

$$(\Delta i_{L_m})_{\text{closed}} + (\Delta i_{L_m})_{\text{open}} = 0$$

$$\frac{V_s DT}{L_m} - \frac{V_o(1-D)T}{L_m} \left(\frac{N_1}{N_2} \right) = 0$$

Solving for V_o ,

$$V_o = V_s \left(\frac{D}{1-D} \right) \left(\frac{N_2}{N_1} \right)$$

(7-4)

Note that the relation between input and output for the flyback converter is similar to that of the buck-boost converter but includes the additional term for the transformer ratio.

Other currents and voltages of interest while the switch is open are

$$\begin{aligned} i_D &= -i_1 \left(\frac{N_1}{N_2} \right) = i_{L_m} \left(\frac{N_1}{N_2} \right) \\ v_{sw} &= V_s - v_1 = V_s + V_o \left(\frac{N_1}{N_2} \right) \\ i_R &= \frac{V_o}{R} \\ i_C &= i_D - i_R = i_{L_m} \left(\frac{N_1}{N_2} \right) - \frac{V_o}{R} \end{aligned} \quad (7-5)$$

Note that v_{sw} , the voltage across the open switch, is greater than the source voltage. If the output voltage is the same as the input and the turns ratio is 1, for example, the voltage across the switch will be twice the source voltage. Circuit currents are shown in Fig. 7-3.

The power absorbed by the load resistor must be the same as that supplied by the source for the ideal case, resulting in

$$P_s = P_o$$

or
$$V_s I_s = \frac{V_o^2}{R} \quad (7-6)$$

The average source current I_s is related to the average of the magnetizing inductance current I_{L_m} by

$$I_s = \frac{(I_{L_m})DT}{T} = I_{L_m} D \quad (7-7)$$

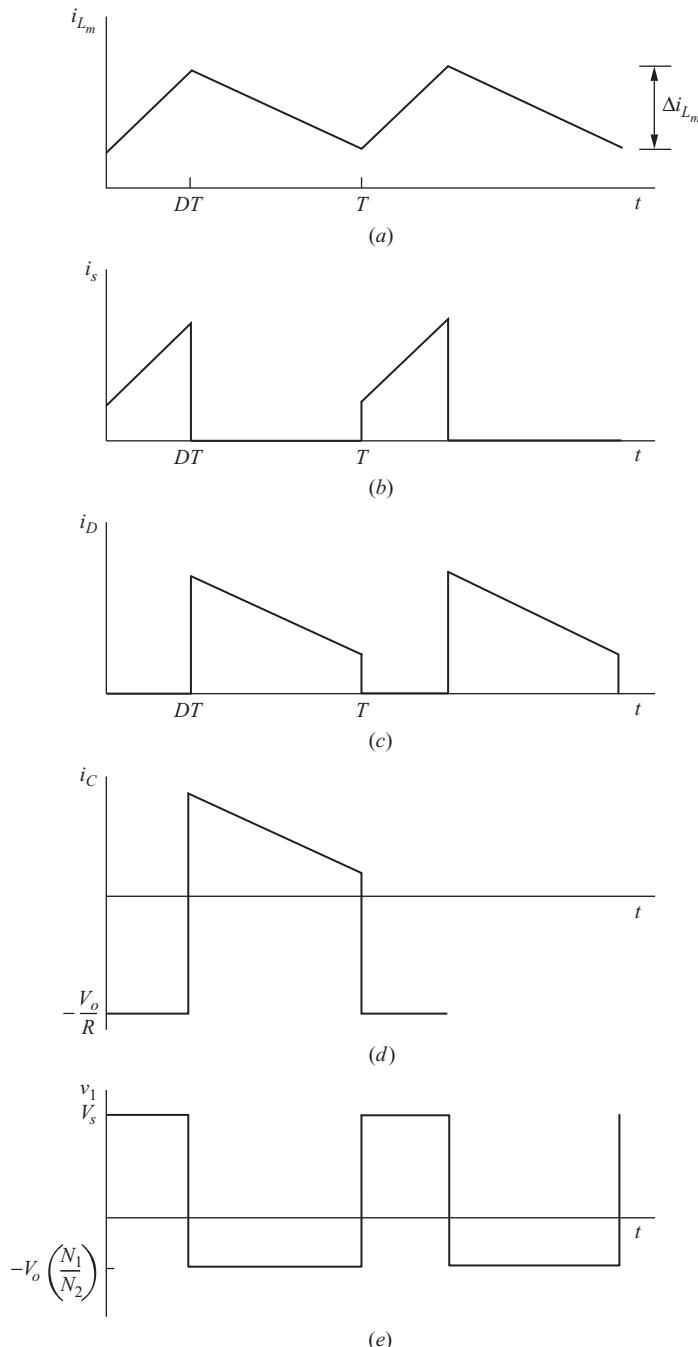


Figure 7-3 Flyback converter current and voltage waveforms.
 (a) Magnetizing inductance current; (b) Source current; (c) Diode current; (d) Capacitor current; (e) Transformer primary voltage.

Substituting for I_s in Eq. (7-6) and solving for I_{L_m} ,

$$\begin{aligned} V_s I_{L_m} D &= \frac{V_o^2}{R} \\ I_{L_m} &= \frac{V_o^2}{V_s D R} \end{aligned} \quad (7-8)$$

Using Eq. (7-4) for V_s , the average inductor current is also expressed as

$$I_{L_m} = \frac{V_s D}{(1 - D)^2 R} \left(\frac{N_2}{N_1} \right)^2 = \frac{V_o}{(1 - D) R} \left(\frac{N_2}{N_1} \right) \quad (7-9)$$

The maximum and minimum values of inductor current are obtained from Eqs. (7-9) and (7-2).

$$\begin{aligned} I_{L_{m,\max}} &= I_{L_m} + \frac{\Delta i_{L_m}}{2} \\ &= \frac{V_s D}{(1 - D)^2 R} \left(\frac{N_2}{N_1} \right)^2 + \frac{V_s D T}{2 L_m} \end{aligned} \quad (7-10)$$

$$\begin{aligned} I_{L_{m,\min}} &= I_{L_m} - \frac{\Delta i_{L_m}}{2} \\ &= \frac{V_s D}{(1 - D)^2 R} \left(\frac{N_2}{N_1} \right)^2 - \frac{V_s D T}{2 L_m} \end{aligned} \quad (7-11)$$

Continuous-current operation requires that $I_{L_{m,\min}} > 0$ in Eq. (7-11). At the boundary between continuous and discontinuous current,

$$\begin{aligned} I_{L_{m,\min}} &= 0 \\ \frac{V_s D}{(1 - D)^2 R} \left(\frac{N_2}{N_1} \right)^2 &= \frac{V_s D T}{2 L_m} = \frac{V_s D}{2 L_m f} \end{aligned}$$

where f is the switching frequency. Solving for the minimum value of L_m that will allow continuous current,

$$(L_m)_{\min} = \frac{(1 - D)^2 R}{2 f} \left(\frac{N_1}{N_2} \right)^2$$

(7-12)

In a flyback converter design, L_m is selected to be larger than $L_{m,\min}$ to ensure continuous current operation. A convenient expression relating inductance and current variation is found from Eq. (7-2).

$$L_m = \frac{V_s D T}{\Delta i_{L_m}} = \frac{V_s D}{\Delta i_{L_m} f} \quad (7-13)$$

The output configuration for the flyback converter is the same as for the buck-boost converter, so the output ripple voltages for the two converters are also the same.

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} \quad (7-14)$$

As with the converters described in Chap. 6, the equivalent series resistance of the capacitor can contribute significantly to the output voltage ripple. The peak-to-peak variation in capacitor current is the same as the maximum current in the diode and the transformer secondary. Using Eq. (7-5), the voltage ripple due to the ESR is

$$\Delta V_{o, \text{ESR}} = \Delta i_C r_C = I_{L_{m,\max}} \left(\frac{N_1}{N_2} \right) r_C \quad (7-15)$$

EXAMPLE 7-1

Flyback Converter

A flyback converter of Fig. 7-2 has the following circuit parameters:

$$\begin{aligned} V_s &= 24 \text{ V} \\ N_1/N_2 &= 3.0 \\ L_m &= 500 \mu\text{H} \\ R &= 5 \Omega \\ C &= 200 \mu\text{F} \\ f &= 40 \text{ kHz} \\ V_o &= 5 \text{ V} \end{aligned}$$

Determine (a) the required duty ratio D ; (b) the average, maximum, and minimum values for the current in L_m ; and (c) the output voltage ripple. Assume that all components are ideal.

■ Solution

(a) Rearranging Eq. (7-4) yields

$$\begin{aligned} V_o &= V_s \left(\frac{D}{1 - D} \right) \left(\frac{N_2}{N_1} \right) \\ D &= \frac{1}{(V_s/V_o)(N_2/N_1) + 1} = \frac{1}{(24/5)(1/3) + 1} = 0.385 \end{aligned}$$

(b) Average current in L_m is determined from Eq. (7-8).

$$I_{L_m} = \frac{V_o^2}{V_s DR} = \frac{5^2}{(24)(0.385)(5)} = 540 \text{ mA}$$

The change in i_{L_m} can be calculated from Eq. (7-2).

$$\Delta i_{L_m} = \frac{V_s D}{L_m f} = \frac{(24)(0.385)}{500(10)^{-6}(40,000)} = 460 \text{ mA}$$

Maximum and minimum inductor currents can be computed from

$$I_{L_{m,\max}} = I_{L_m} + \frac{\Delta i_{L_m}}{2} = 540 + \frac{460}{2} = 770 \text{ mA}$$

$$I_{L_{m,\min}} = I_{L_m} - \frac{\Delta i_{L_m}}{2} = 540 - \frac{460}{2} = 310 \text{ mA}$$

Equations (7-10) and (7-11), which are derived from the above computation, could also be used directly to obtain the maximum and minimum currents. Note that a positive $I_{L_{m,\min}}$ verifies continuous current in L_m .

- (c) Output voltage ripple is computed from Eq. (7-14).

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} = \frac{0.385}{(5)[200(10)^{-6}](40,000)} = 0.0096 = 0.96\%$$

EXAMPLE 7-2

Flyback Converter Design, Continuous-Current Mode

Design a converter to produce an output voltage of 36 V from a 3.3-V source. The output current is 0.1 A. Design for an output ripple voltage of 2 percent. Include ESR when choosing a capacitor. Assume for this problem that the ESR is related to the capacitor value by $r_C = 10^{-5}/C$.

■ Solution

Considering a boost converter for this application and calculating the required duty ratio from Eq. (6-27),

$$D = 1 - \frac{V_s}{V_o} = 1 - \frac{3.3}{36} = 0.908$$

The result of a high duty ratio will likely be that the converter will not function as desired because of losses in the circuit (Fig. 6-10). Therefore, a boost converter would not be a good choice. A flyback converter is much better suited for this application.

As a somewhat arbitrary design decision, start by letting the duty ratio be 0.4. From Eq. (7-4), the transformer turns ratio is calculated to be

$$\left(\frac{N_2}{N_1}\right) = \frac{V_o}{V_s} \left(\frac{1-D}{D}\right) = \frac{36}{3.3} \left(\frac{1-0.4}{0.4}\right) = 16.36$$

Rounding, let $N_2/N_1 = 16$. Recalculating the duty ratio using a turns ratio of 16 gives $D = 0.405$.

To determine L_m , first compute the average current in L_m from Eq. (7-9), using $I_o = V_o/R$.

$$I_{L_m} = \frac{V_o}{(1-D)R} \left(\frac{N_2}{N_1}\right) = \frac{I_o}{1-D} \left(\frac{N_2}{N_1}\right) = \left(\frac{0.1}{1-0.405}\right) 16 = 2.69 \text{ A}$$

Let the current variation in L_m be 40 percent of the average current: $\Delta i_{L_m} = 0.4(2.69) = 1.08 \text{ A}$. As another somewhat arbitrary choice, let the switching frequency be 100 kHz. Using Eq. (7-13),

$$L_m = \frac{V_s D}{\Delta i_{L_m} f} = \frac{3.3(0.405)}{1.08(100,000)} = 12.4 \mu\text{H}$$

Maximum and minimum currents in L_m are found from Eqs. (7-10) and (7-11) as 3.23 and 2.15 A, respectively.

The output voltage ripple is to be limited to 2 percent, which is $0.02(36) = 0.72 \text{ V}$. Assume that the primary cause of the voltage ripple will be the voltage drop across the equivalent series resistance $\Delta i_C r_C$. The peak-to-peak variation in capacitor current is the same as in the diode and the transformer secondary and is related to current in L_m by

$$\Delta i_C = I_{L_m, \max} \left(\frac{N_1}{N_2} \right) = (3.23 \text{ A}) \left(\frac{1}{16} \right) = 0.202 \text{ A}$$

Using Eq. (7-15),

$$r_C = \frac{\Delta V_o, \text{ESR}}{\Delta i_C} = \frac{0.72 \text{ V}}{0.202 \text{ A}} = 3.56 \Omega$$

Using the relationship between ESR and capacitance given in this problem,

$$C = \frac{10^{-5}}{r_C} = \frac{10^{-5}}{3.56} = 2.8 \mu\text{F}$$

The ripple voltage due to the capacitance only is obtained from Eq. (7-14) as

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} = \frac{0.405}{(36 \text{ V}/0.1 \text{ A})[2.8(10)^{-6}](100,000)} = 0.004 = 0.04\%$$

showing that the assumption that the voltage ripple is primarily due to the ESR was correct. A standard value of 3.3 μF would be a good choice. Note that the designer should consult manufacturers' specifications for ESR when selecting a capacitor.

The turns ratio of the transformer, current variation, and switching frequency were selected somewhat arbitrarily, and many other combinations are suitable.

Discontinuous-Current Mode in the Flyback Converter

For the discontinuous-current mode for the flyback converter, the current in the transformer increases linearly when the switch is closed, just as it did for the continuous-current mode. However, when the switch is open, the current in the transformer magnetizing inductance decreases to zero before the start of the next switching cycle, as shown in Fig. 7-4. While the switch is closed, the increase in inductor current is described by Eq. (7-2). Since the current starts at zero, the maximum value is also determined from Eq. (7-2).

$$I_{L_m, \max} = \frac{V_s D T}{L_m} \quad (7-16)$$

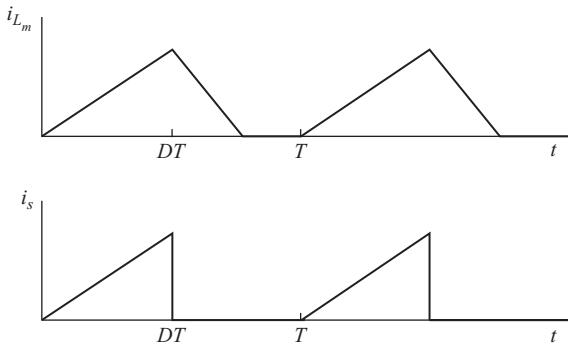


Figure 7-4 Discontinuous current for the flyback converter.

The output voltage for discontinuous-current operation can be determined by analyzing the power relationships in the circuit. If the components are ideal, the power supplied by the dc source is the same as the power absorbed by the load resistor. Power supplied by the source is the dc voltage times average source current, and load power is V_o^2/R :

$$\begin{aligned} P_s &= P_o \\ V_s I_s &= \frac{V_o^2}{R} \end{aligned} \quad (7-17)$$

Average source current is the area under the triangular waveform of Fig. 7-4b divided by the period, resulting in

$$I_s = \left(\frac{1}{2} \right) \left(\frac{V_s D T}{L_m} \right) (D T) \left(\frac{1}{T} \right) = \frac{V_s D^2 T}{2 L_m} \quad (7-18)$$

Equating source power and load power [Eq. (7-17)],

$$\frac{V_s^2 D^2 T}{2 L_m} = \frac{V_o^2}{R} \quad (7-19)$$

Solving for V_o for discontinuous-current operation in the flyback converter,

$$V_o = V_s D \sqrt{\frac{TR}{2L_m}} = V_s D \sqrt{\frac{R}{2L_m f}} \quad (7-20)$$

EXAMPLE 7-3

Flyback Converter, Discontinuous Current

For the flyback converter in Example 7-1, the load resistance is increased from 5 to $20\ \Omega$ with all other parameters remaining unchanged. Show that the magnetizing inductance current is discontinuous, and determine the output voltage.

■ Solution

Using $L_m = 500 \mu\text{H}$, $f = 40 \text{ kHz}$, $N_1/N_2 = 3$, $D = 0.385$, and $R = 20 \Omega$, the minimum inductor current from Eq. (7-11) is calculated as

$$\begin{aligned} I_{L_m,\min} &= \frac{V_s D}{(1 - D)^2 R} \left(\frac{N_2}{N_1} \right)^2 - \frac{V_s D T}{2 L_m} \\ &= \frac{(24)(0.385)}{(1 - 0.385)^2 (20)} \left(\frac{1}{3} \right)^2 - \frac{(24)(0.385)}{2(500)(10)^{-6}(40,000)} = -95 \text{ mA} \end{aligned}$$

Since negative current in L_m is not possible, i_{L_m} must be discontinuous. Equivalently, the minimum inductance for continuous current can be calculated from Eq. (7-12).

$$(L_m)_{\min} = \frac{(1 - D)^2 R}{2f} \left(\frac{N_1}{N_2} \right)^2 = \frac{(1 - 0.385)^2 20}{2(40,000)} (3)^2 = 850 \mu\text{H}$$

which is more than the $500 \mu\text{H}$ specified, also indicating discontinuous current.

Using Eq. (7-20),

$$V_o = V_s D \sqrt{\frac{R}{2L_m f}} = (24)(0.385) \sqrt{\frac{20}{2(500)(10)^{-6}(40,000)}} = 6.53 \text{ V}$$

For the current in L_m in the discontinuous-current mode, the output voltage is no longer 5 V but increases to 6.53 V. Note that for any load that causes the current to be continuous, the output would remain at 5 V.

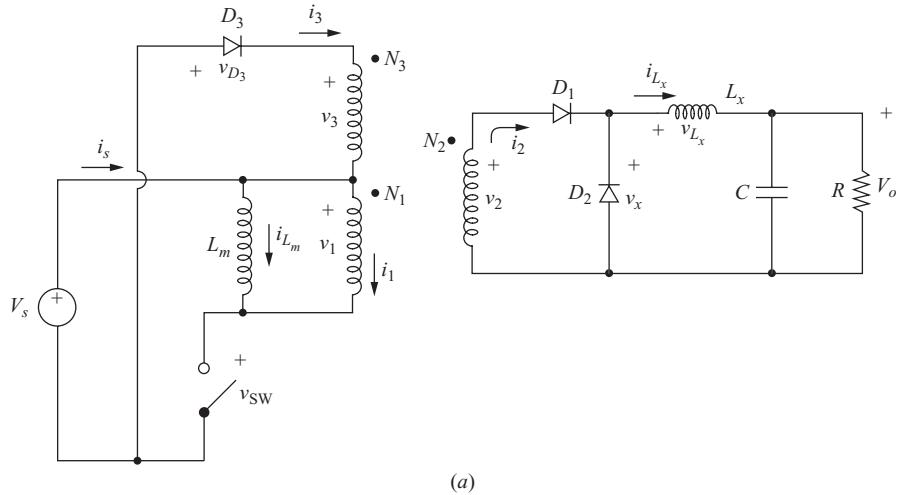
Summary of Flyback Converter Operation

When the switch is closed in the flyback converter of Fig. 7-2a, the source voltage is across the transformer magnetizing inductance L_m and causes i_{L_m} to increase linearly. Also while the switch is closed, the diode on the output is reverse-biased, and load current is supplied by the output capacitor. When the switch is open, energy stored in the magnetizing inductance is transferred through the transformer to the output, forward-biasing the diode and supplying current to the load and to the output capacitor. The input-output voltage relationship in the continuous-current mode of operation is like that of the buck-boost dc-dc converter but includes a factor for the turns ratio.

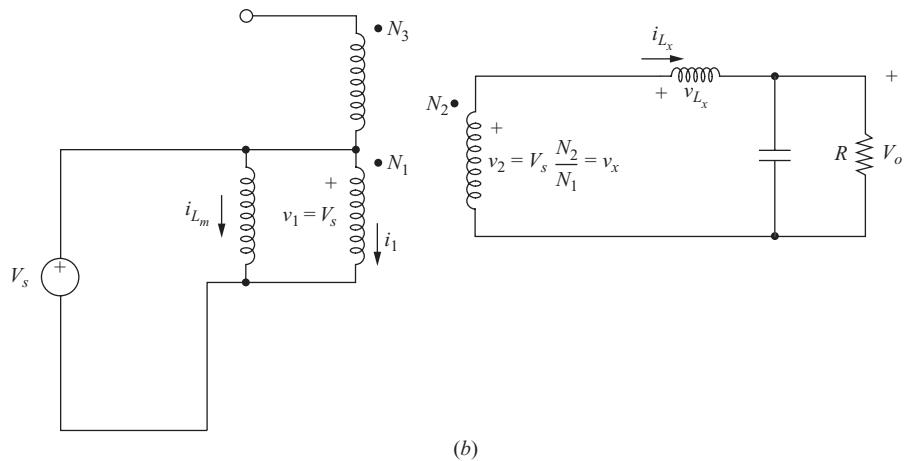
7.4 THE FORWARD CONVERTER

The forward converter, shown in Fig. 7-5a, is another magnetically coupled dc-dc converter. The switching period is T , the switch is closed for time DT and open for $(1 - D)T$. Steady-state operation is assumed for the analysis of the circuit, and the current in inductance L_x is assumed to be continuous.

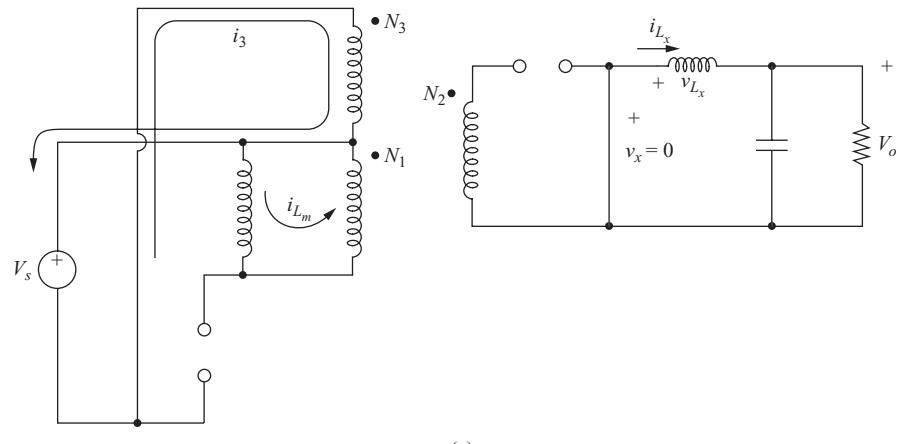
The transformer has three windings: windings 1 and 2 transfer energy from the source to the load when the switch is closed; winding 3 is used to provide a path for the magnetizing current when the switch is open and to reduce the magnetizing current to zero before the start of each switching period. The transformer



(a)



(b)



(c)

Figure 7-5 (a) Forward dc-dc converter; (b) Circuit for switch closed; (c) Circuit for switch open.

is modeled as three ideal windings with a magnetizing inductance L_m , which is placed across winding 1. Leakage inductance and losses are not included in this simplified transformer model.

For the forward converter, energy is transferred from the source to the load while the switch is closed. Recall that for the flyback converter, energy was stored in L_m when the switch was closed and transferred to the load when the switch was open. In the forward converter, L_m is not a parameter that is included in the input-output relationship and is generally made large.

Analysis for the Switch Closed The equivalent circuit for the forward converter with the switch closed is shown in Fig. 7-5b. Closing the switch establishes the voltage across transformer winding 1, resulting in

$$\begin{aligned} v_1 &= V_s \\ v_2 &= v_1 \left(\frac{N_2}{N_1} \right) = V_s \left(\frac{N_2}{N_1} \right) \\ v_3 &= v_1 \left(\frac{N_3}{N_1} \right) = V_s \left(\frac{N_3}{N_1} \right) \end{aligned} \quad (7-21)$$

The voltage across D_3 is

$$V_{D_3} = -V_s - v_3 < 0$$

showing that D_3 is off. A positive v_2 forward-biases D_1 and reverse-biases D_2 .

The relationship between input and output voltages can be determined by examining the current in inductor L_x . Assuming the output is held at a constant V_o ,

$$\begin{aligned} v_{L_x} &= v_2 - V_o = V_s \left(\frac{N_2}{N_1} \right) - V_o = L_x \frac{di_{L_x}}{dt} \\ \frac{di_{L_x}}{dt} &= \frac{V_s(N_2/N_1) - V_o}{L_x} = \frac{\Delta i_{L_x}}{\Delta t} = \frac{\Delta i_{L_x}}{DT} \\ (\Delta i_{L_x})_{\text{closed}} &= \left[V_s \left(\frac{N_2}{N_1} \right) - V_o \right] \frac{DT}{L_x} \end{aligned} \quad (7-22)$$

The voltage across the magnetizing inductance L_m is also V_s , resulting in

$$\Delta i_{L_m} = \frac{V_s DT}{L_m} \quad (7-23)$$

Equations (7-22) and (7-23) show that the current is increasing linearly in both L_x and L_m while the switch is closed. The current in the switch and in the physical transformer primary is

$$i_{\text{sw}} = i_1 + i_{L_m} \quad (7-24)$$

Analysis for the Switch Open Figure 7-5c shows the circuit with the switch open. The currents in L_x and L_m do not change instantaneously when the switch

is opened. Continuity of i_{L_m} establishes $i_1 = -i_{L_m}$. Looking at the transformation from winding 1 to 2, current out of the dotted terminal on 1 would establish current into the dotted terminal on 2, but diode D_1 prevents current in that direction.

For the transformation from winding 1 to 3, current out of the dotted terminal of winding 1 forces current into the dotted terminal of winding 3. Diode D_3 is then forward-biased to provide a path for winding 3 current, which must go back to the source.

When D_3 is on, the voltage across winding 3 is established at

$$v_3 = -V_s$$

With v_3 established, v_1 and v_2 become

$$\begin{aligned} v_1 &= v_3 \left(\frac{N_1}{N_3} \right) = -V_s \left(\frac{N_1}{N_3} \right) \\ v_2 &= v_3 \left(\frac{N_2}{N_3} \right) = -V_s \left(\frac{N_2}{N_3} \right) \end{aligned} \quad (7-25)$$

With D_1 off and positive current in L_x , D_2 must be on. With D_2 on, the voltage across L_x is

$$v_{L_x} = -V_o = L_x \frac{di_{L_x}}{dt}$$

resulting in

$$\begin{aligned} \frac{di_{L_x}}{dt} &= \frac{-V_o}{L} = \frac{\Delta i_{L_x}}{\Delta t} = \frac{\Delta i_{L_x}}{(1-D)T} \\ (\Delta i_{L_x})_{\text{open}} &= \frac{-V_o(1-D)T}{L_x} \end{aligned} \quad (7-26)$$

Therefore, the inductor current decreases linearly when the switch is open.

For steady-state operation, the net change in inductor current over one period must be zero. From Eq. (7-22) and (7-26),

$$(\Delta i_{L_x})_{\text{closed}} + (\Delta i_{L_x})_{\text{open}} = 0$$

$$\left[V_s \left(\frac{N_2}{N_1} \right) - V_o \right] \frac{DT}{L_x} - \frac{V_o(1-D)T}{L_x} = 0$$

Solving for V_o ,

$$V_o = V_s D \left(\frac{N_2}{N_1} \right)$$

(7-27)

Note that the relationship between input and output voltage is similar to that for the buck dc-dc converter except for the added term for the turns ratio. Current in L_x must be continuous for Eq. (7-27) to be valid.

Meanwhile, the voltage across L_m is v_1 , which is negative, resulting in

$$\begin{aligned} v_{L_m} = v_1 &= -V_s \left(\frac{N_1}{N_3} \right) = L_m \frac{di_{L_m}}{dt} \\ \frac{di_{L_m}}{dt} &= -\frac{V_s}{L_m} \left(\frac{N_1}{N_3} \right) \end{aligned} \quad (7-28)$$

The current in L_m should return to zero before the start of the next period to reset the transformer core (return the magnetic flux to zero). When the switch opens, Eq. (7-28) shows that i_{L_m} decreases linearly. Since D_3 will prevent i_{L_m} from going negative, Eq. (7-28) is valid as long as i_{L_m} is positive. From Eq. (7-28),

$$\frac{\Delta i_{L_m}}{\Delta t} = -\frac{V_s}{L_m} \left(\frac{N_1}{N_3} \right) \quad (7-29)$$

For i_{L_m} to return to zero after the switch is opened, the decrease in current must equal the increase in current given by Eq. (7-22). Letting ΔT_x be the time for i_{L_m} to decrease from the peak back to zero,

$$\frac{\Delta i_{L_m}}{\Delta T_x} = -\frac{V_s DT}{L_m} = -\frac{V_s}{L_m} \left(\frac{N_1}{N_3} \right) \quad (7-30)$$

Solving for ΔT_x ,

$$\Delta T_x = DT \left(\frac{N_3}{N_1} \right) \quad (7-31)$$

The time at which the current i_{L_m} reaches zero t_0 , is

$$t_0 = DT + \Delta T_x = DT + DT \left(\frac{N_3}{N_1} \right) = DT \left(1 + \frac{N_3}{N_1} \right) \quad (7-32)$$

Because the current must reach zero before the start of the next period,

$$\begin{aligned} t_0 &< T \\ sDT \left(1 + \frac{N_3}{N_1} \right) &< T \\ D \left(1 + \frac{N_3}{N_1} \right) &< 1 \end{aligned} \quad (7-33)$$

For example, if the ratio $N_3/N_1 = 1$ (a common practice), then the duty ratio D must be less than 0.5. The voltage across the open switch is $V_s - v_1$, resulting in

$$v_{sw} = \begin{cases} V_s - v_1 = V_s - \left(-V_s \frac{N_1}{N_3} \right) = V_s \left(1 + \frac{N_1}{N_3} \right) & \text{for } DT < t < t_0 \\ V_s & \text{for } t_0 < t < T \end{cases} \quad (7-34)$$

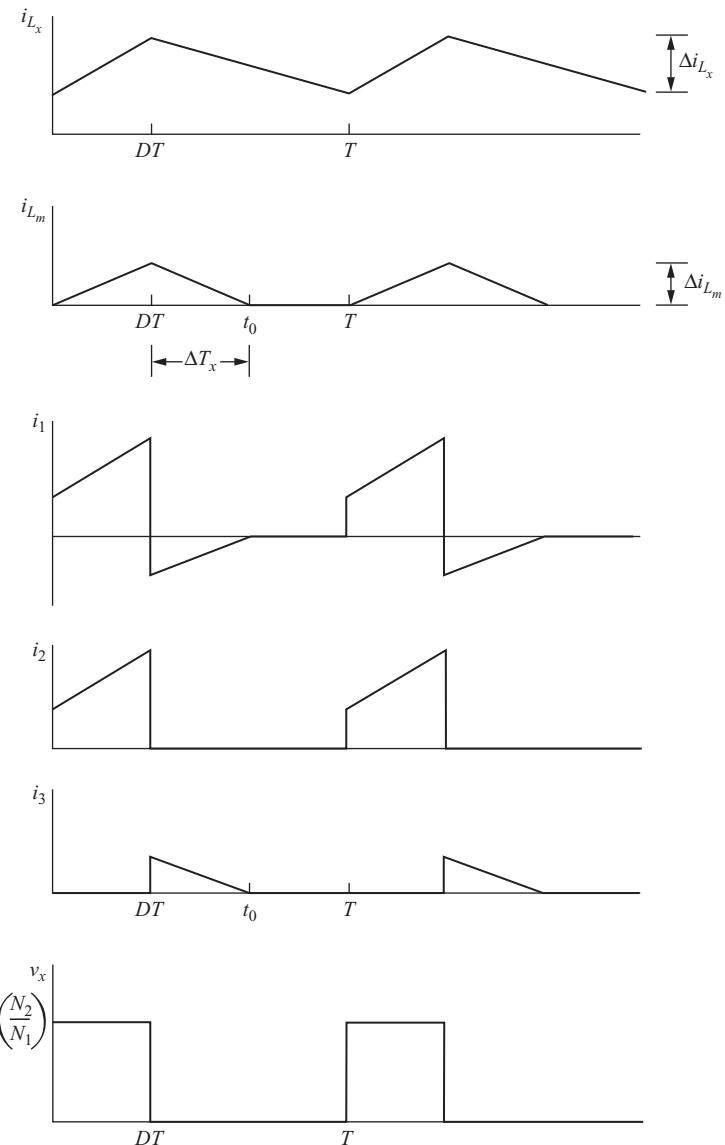


Figure 7-6 Current and voltage waveforms for the forward converter.

Forward converter current and voltage waveforms are shown in Fig. (7-6).

The circuit configuration on the output of the forward converter is the same as that for the buck converter, so the output voltage ripple based on an ideal capacitance is also the same.

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8L_x C f^2} \quad (7-35)$$

The equivalent series resistance of the capacitor often dominates the output voltage ripple. The peak-to-peak voltage variation due to the ESR is

$$\Delta V_{o, \text{ESR}} = \Delta i_C r_C = \Delta i_{L_x} r_C = \left[\frac{V_o(1-D)}{L_x f} \right] r_C \quad (7-36)$$

where Eq. (7-26) is used for Δi_{L_x} .

Summary of Forward Converter Operation

When the switch is closed, energy is transferred from the source to the load through the transformer. The voltage on the transformer secondary is a pulsed waveform, and the output is analyzed like that of the buck dc-dc converter. Energy stored in the magnetizing inductance while the switch is closed can be returned to the input source via a third transformer winding while the switch is open.

EXAMPLE 7-4

Forward Converter

The forward converter of Fig. 7-5a has the following parameters:

$$V_s = 48 \text{ V}$$

$$R = 10 \Omega$$

$$L_x = 0.4 \text{ mH}, \quad L_m = 5 \text{ mH}$$

$$C = 100 \mu\text{F}$$

$$f = 35 \text{ kHz}$$

$$N_1/N_2 = 1.5, \quad N_1/N_3 = 1$$

$$D = 0.4$$

(a) Determine the output voltage, the maximum and minimum currents in L_x , and the output voltage ripple. (b) Determine the peak current in the transformer primary winding. Verify that the magnetizing current is reset to zero during each switching period. Assume all components are ideal.

■ Solution

(a) The output voltage is determined from Eq. (7-27).

$$V_o = V_s D \left(\frac{N_2}{N_1} \right) = 48(0.4) \left(\frac{1}{1.5} \right) = 12.8 \text{ V}$$

Average current in L_x is the same as the current in the load.

$$I_{L_x} = \frac{V_o}{R} = \frac{12.8}{10} = 1.28 \text{ A}$$

The change in i_{L_x} is determined from Eq. (7-22) or (7-26). Using Eq. (7-26),

$$\Delta i_{L_x} = \frac{V_o(1 - D)}{L_x f} = \frac{12.8(1 - 0.4)}{0.4(10)^{-3}(35,000)} = 0.55 \text{ A}$$

Maximum and minimum currents in L_x are then

$$I_{L_{x,\max}} = I_{L_x} + \frac{\Delta i_{L_x}}{2} = 1.28 + \frac{0.55}{2} = 1.56 \text{ A}$$

$$I_{L_{x,\min}} = I_{L_x} - \frac{\Delta i_{L_x}}{2} = 1.28 - \frac{0.55}{2} = 1.01 \text{ A}$$

- (b) Current in the primary winding of the transformer is the sum of the reflected current from the secondary and the magnetizing currents. The peak secondary current is the same as $I_{L_{x,\max}}$. The peak magnetizing current is obtained from Eq. (7-23).

$$I_{L_{m,\max}} = \Delta i_{L_m} = \frac{V_s DT}{L_m} = \frac{48(0.4)}{5(10)^{-3}(35,000)} = 0.11 \text{ A}$$

The peak current in the transformer primary is therefore

$$I_{\max} = I_{L_{x,\max}} \left(\frac{N_2}{N_1} \right) + I_{L_{m,\max}} = 1.56 \left(\frac{1}{1.5} \right) + 0.11 = 1.15 \text{ A}$$

The time for the magnetizing current to return to zero after the switch is opened is determined from Eq. (7-31).

$$\Delta T_x = DT \left(\frac{N_3}{N_1} \right) = \frac{0.4(1)}{35,000} = 11.4 \mu\text{s}$$

Since the switch is closed for $DT = 11.4 \mu\text{s}$, the time at which the magnetizing current reaches zero is $22.8 \mu\text{s}$ [Eq. (7-32)], which is less than the switching period of $28.6 \mu\text{s}$.

EXAMPLE 7-5

Forward Converter Design

Design a forward converter such that the output is 5 V when the input is 170 V. The output current is 5 A. The output voltage ripple must not exceed 1 percent. Choose the transformer turns ratio, duty ratio, and switching frequency. Choose L_x such that the current in it is continuous. Include the ESR when choosing a capacitor. For this problem, use $r_C = 10^{-5}/C$.

■ Solution

Let the turns ratio $N_1/N_3 = 1$. This results in a maximum duty ratio of 0.5 for the switch. For margin, let $D = 0.35$. From Eq. (7-27),

$$\frac{N_1}{N_2} = \frac{V_s D}{V_o} = \frac{170(0.35)}{5} = 11.9$$

Rounding, let $N_1/N_2 = 12$. Recalculating D for $N_1/N_2 = 12$ yields

$$D = \frac{V_o}{V_s} \left(\frac{N_1}{N_2} \right) = \left(\frac{5}{170} \right)(12) = 0.353$$

The inductor L_x and the capacitor are selected using the same design criteria as discussed for the buck converter in Chap. 6. For this design, let $f = 300$ kHz. The average current in L_x is 5 A, the same as average current in the load since the average current in the capacitor is zero. Let the variation in inductor current be 2 A, which is 40 percent of the average value. From Eq. (7-26),

$$L_x = \frac{V_o(1 - D)T}{\Delta i_{L_x}} = \frac{V_o(1 - D)}{0.4I_{L_x}f} = \frac{5(1 - 0.353)}{0.4(5)(300,000)} = 5.39 \mu\text{H}$$

A standard value of 5.6 μH is suitable for this design and would result in a slightly smaller Δi_{L_x} .

For a 1 percent output voltage ripple,

$$\Delta v_o \leq (0.01)(5) = 0.05 \text{ V}$$

The capacitor size is determined by assuming that the voltage ripple is produced primarily by the equivalent series resistance, or

$$\Delta V_o \approx \Delta V_{o,\text{ESR}} = \Delta i_C r_C = (2 \text{ A})(r_C) = 0.05 \text{ V}$$

$$r_C = \frac{0.05 \text{ V}}{2 \text{ A}} = 0.025 \Omega = 25 \text{ m}\Omega$$

The designer would now search for a capacitor having a 25-m Ω or lower ESR. Using $r_C = 10^{-5}/C$ given in this problem,

$$C = \frac{10^{-5}}{0.025} = 400 \mu\text{F}$$

A standard value of 470 μF is suitable.

7.5 THE DOUBLE-ENDED (TWO-SWITCH) FORWARD CONVERTER

The forward converter discussed in Sec. 7.4 has a single transistor switch and is referred to as a single-ended converter. The double-ended (two-switch) forward converter shown in Fig. 7-7 is a variation of the forward converter. In this circuit, the switching transistors are turned on and off simultaneously. When the switches are on, the voltage across the primary transformer winding is V_s . The voltage across the secondary winding is positive, and energy is transferred to the load, as it was for the forward converter discussed in Sec. 7.4. Also when the switches are on, the current in the magnetizing inductance is increasing. When the switches turn off, diode D_1 prevents i_{L_m} from flowing in the secondary (and hence primary) winding of the transformer and forces the magnetizing current to flow in diodes D_3 and D_4 and back to the source. This establishes the primary voltage at $-V_s$, causing a linear decrease in magnetizing current. If the duty ratio of the switches is less than 0.5, the transformer core resets (the magnetic flux returns to zero) during every cycle.

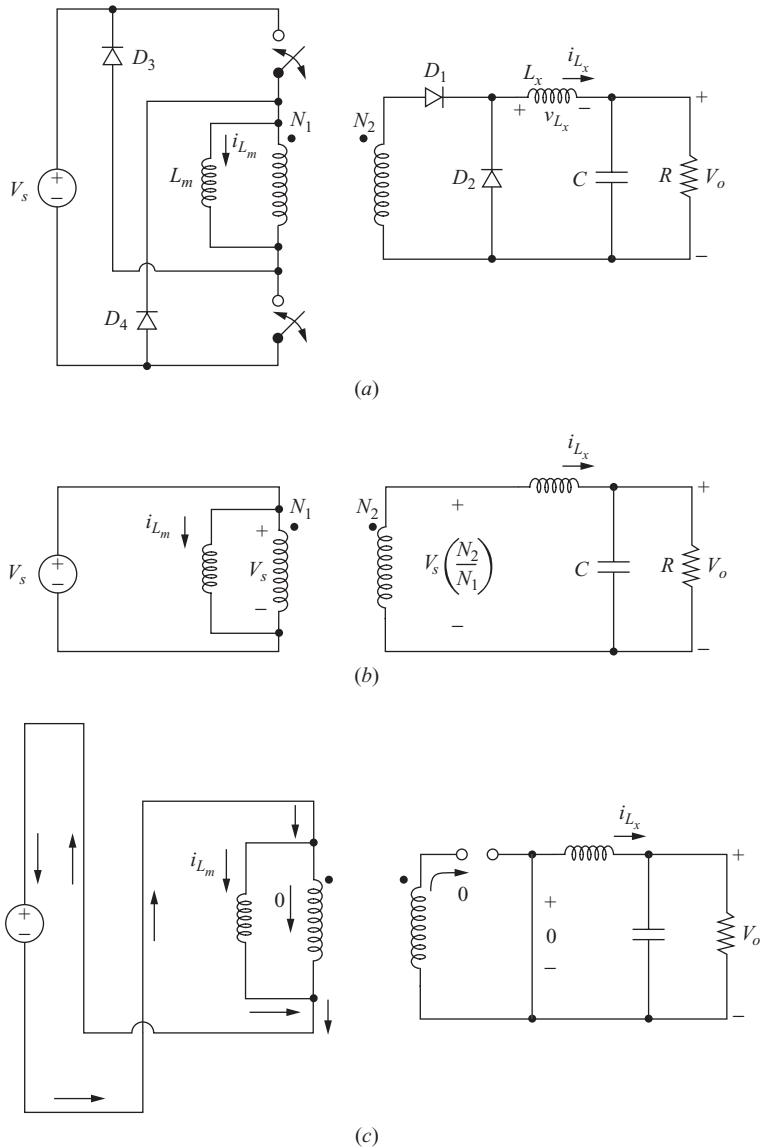


Figure 7-7 (a) Double-ended forward converter; (b) Circuit for the switches closed; (c) Circuit for the switches open.

The output voltage is the same as for the single-ended forward converter [Eq. (7-27)]. An advantage of the double-ended forward converter is that the voltage across an off transistor is V_s rather than $V_s(1 + N_1/N_3)$ as it was for the single-ended forward converter. This is an important feature for high-voltage applications.

7.6 THE PUSH-PULL CONVERTER

Another dc-dc converter that has transformer isolation is the push-pull converter shown in Fig. 7-8a. As with the forward converter, the transformer magnetizing inductance is not a design parameter. The transformer is assumed to be ideal for

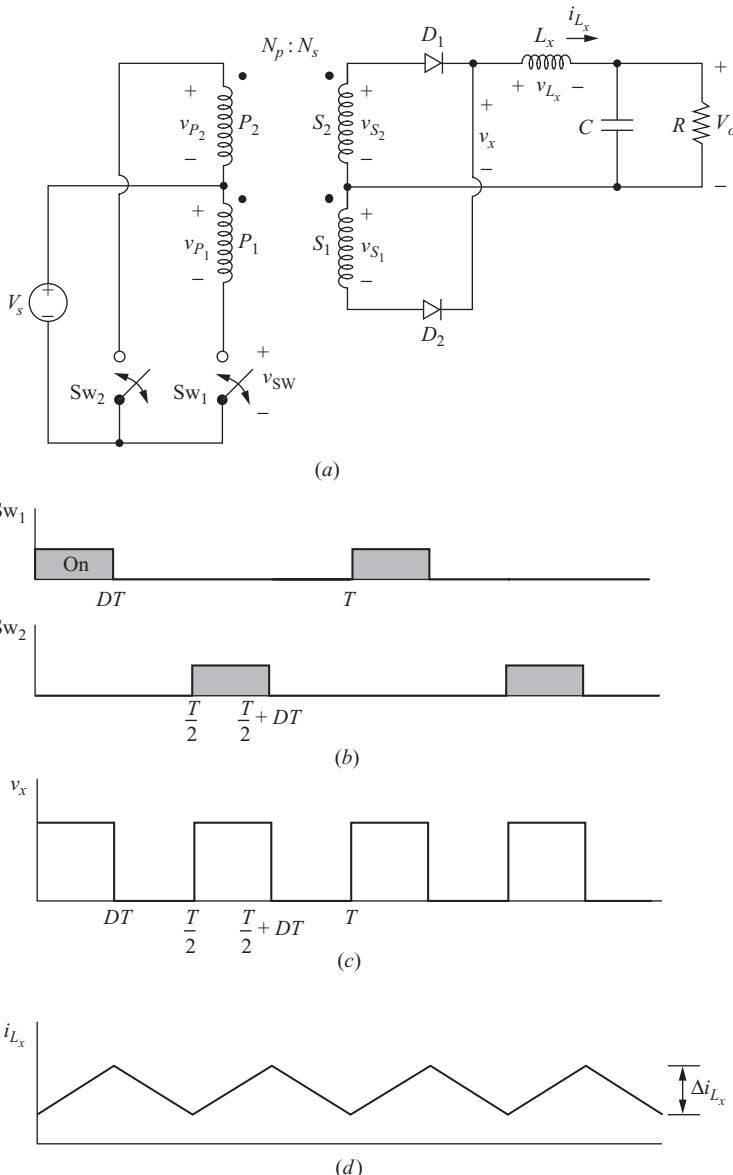


Figure 7-8 (a) Push-pull converter; (b) Switching sequence; (c) Voltage v_x ; (d) Current in L_x .

this analysis. Switches S_{w_1} and S_{w_2} turn on and off with the switching sequence shown in Fig. 7-8b. Analysis proceeds by analyzing the circuit with either switch closed and then with both switches open.

Switch S_{w_1} Closed Closing S_{w_1} establishes the voltage across primary winding P_1 at

$$v_{P_1} = V_s \quad (7-37)$$

The voltage across P_1 is transformed to the three other windings, resulting in

$$\begin{aligned} v_{S_1} &= V_s \left(\frac{N_S}{N_P} \right) \\ v_{S_2} &= V_s \left(\frac{N_S}{N_P} \right) \end{aligned} \quad (7-38)$$

$$v_{P_2} = V_s$$

$$v_{S_{w_2}} = 2V_s$$

Diode D_1 is forward-biased, D_2 is reverse-biased, and

$$v_x = v_{S_2} = V_s \left(\frac{N_S}{N_P} \right) \quad (7-39)$$

$$v_{L_x} = v_x - V_o = V_s \left(\frac{N_S}{N_P} \right) - V_o$$

Assuming a constant output voltage V_o , the voltage across L_x is a constant, resulting in a linearly increasing current in L_x . In the interval when S_{w_1} is closed, the change in current in L_x is

$$\begin{aligned} \frac{\Delta i_{L_x}}{\Delta t} &= \frac{\Delta i_{L_x}}{DT} = \frac{V_s(N_S/N_P) - V_o}{L_x} \\ (\Delta i_{L_x})_{\text{closed}} &= \left[\frac{V_s(N_S/N_P) - V_o}{L_x} \right] DT \end{aligned} \quad (7-40)$$

Switch S_{w_2} Closed Closing S_{w_2} establishes the voltage across primary winding P_2 at

$$v_{P_2} = -V_s \quad (7-41)$$

The voltage across P_2 is transformed to the three other windings, resulting in

$$\begin{aligned} v_{P_1} &= -V_s \\ v_{S_1} &= -V_s \left(\frac{N_S}{N_P} \right) \\ v_{S_2} &= -V_s \left(\frac{N_S}{N_P} \right) \\ v_{S_{w_1}} &= 2V_s \end{aligned} \quad (7-42)$$

Diode D_2 is forward-biased, D_1 is reverse-biased, and

$$\begin{aligned} v_x &= -v_{S_2} = V_s \left(\frac{N_S}{N_P} \right) \\ v_{L_x} &= v_x - V_o = V_s \left(\frac{N_S}{N_P} \right) - V_o \end{aligned} \quad (7-43)$$

which is a positive pulse. The current in L_x increases linearly while Sw_2 is closed, and Eq. (7-40) applies.

Both Switches Open With both switches open, the current in each of the primary windings is zero. The current in the filter inductor L_x must maintain continuity, resulting in both D_1 and D_2 becoming forward-biased. Inductor current divides evenly between the transformer secondary windings. The voltage across each secondary winding is zero, and

$$\begin{aligned} v_x &= 0 \\ v_{L_x} &= v_x - V_o = -V_o \end{aligned} \quad (7-44)$$

The voltage across L_x is $-V_o$, resulting in a linearly decreasing current in L_x . The change in current while both switches are open is

$$\frac{\Delta i_{L_x}}{\Delta t} = \frac{\Delta i_{L_x}}{T/2 - DT} = -\frac{V_o}{L_x}$$

Solving for Δi_{L_x} ,

$$(\Delta i_{L_x})_{\text{open}} = -\left(\frac{V_o}{L_x}\right)\left(\frac{1}{2} - D\right)T \quad (7-45)$$

Since the net change in inductor current over one period must be zero for steady-state operation,

$$\begin{aligned} (\Delta i_{L_x})_{\text{closed}} + (\Delta i_{L_x})_{\text{open}} &= 0 \\ \left[\frac{V_s(N_S/N_P) - V_o}{L_x} \right] DT + \left(\frac{V_o}{L_x} \right) \left(\frac{1}{2} - D \right) T &= 0 \end{aligned} \quad (7-46)$$

Solving for V_o ,

$$V_o = 2V_s \left(\frac{N_S}{N_P} \right) D \quad (7-47)$$

where D is the duty ratio of *each* switch. The above analysis assumes continuous current in the inductor. Note that the result is similar to that for the buck converter, discussed in Chap. 6. Ripple voltage on the output is derived in a manner similar to the buck converter. The output ripple for the push-pull converter is

$$\frac{\Delta V_o}{V_o} = \frac{1 - 2D}{32L_xCf^2} \quad (7-48)$$

As with the other converters analyzed previously, the equivalent series resistance of the capacitor is usually responsible for most of the voltage output ripple. Recognizing that $\Delta i_C = \Delta i_{L_x}$ and using Eq. (7-45),

$$\Delta V_{o,ESR} = \Delta i_C r_C = \Delta i_{L_x} r_C = \left[\frac{V_o \left(\frac{1}{2} - D \right)}{L_x f} \right] r_C \quad (7-49)$$

The preceding analysis neglected the magnetizing inductance of the transformer. If L_m were included in the equivalent circuit, i_{L_m} would increase linearly when Sw_1 was closed, circulate while both Sw_1 and Sw_2 were open, and decrease linearly when Sw_2 was closed. Because Sw_1 and Sw_2 are closed for equal intervals, the net change in i_{L_m} is zero, and the transformer core is reset during each period in the ideal case. In actual applications of the push-pull converter, control techniques are used to ensure that the core is reset.

Summary of Push-Pull Operation

Pulses of opposite polarity are produced on the primary and secondary windings of the transformer by switching Sw_1 and Sw_2 (Fig. 7-8). The diodes on the secondary rectify the pulse waveform and produce a waveform v_x at the input of the low-pass filter, as shown in Fig. 7-8c. The output is analyzed like that of the buck converter discussed in Chap. 6.

EXAMPLE 7-6

Push-Pull Converter

A push-pull converter has the following parameters:

$$\begin{aligned} V_s &= 30 \text{ V} \\ N_P/N_S &= 2 \\ D &= 0.3 \\ L_x &= 0.5 \text{ mH} \\ R &= 6 \Omega \\ C &= 50 \mu\text{F} \\ f &= 10 \text{ kHz} \end{aligned}$$

Determine V_o , the maximum and minimum values of i_{L_x} , and the output ripple voltage. Assume all components are ideal.

■ Solution

Using Eq. (7-47), the output voltage is

$$V_o = 2V_s \left(\frac{N_S}{N_P} \right) D = (2)(30) \left(\frac{1}{2} \right) (0.3) = 9.0 \text{ V}$$

Average inductor current is the same as average load current,

$$I_{L_x} = \frac{V_o}{R} = \frac{9}{6} = 1.5 \text{ A}$$

The change in i_{L_x} is determined from Eq. (7-45).

$$\Delta i_{L_x} = \frac{V_o(1 - D)T}{L_x} = \frac{9(0.5 - 0.3)}{0.5(10)^{-3}(10,000)} = 0.36 \text{ A}$$

resulting in maximum and minimum currents of

$$I_{L_{x,\max}} = I_{L_x} + \frac{\Delta i_{L_x}}{2} = 1.68 \text{ A}$$

$$I_{L_{x,\min}} = I_{L_x} - \frac{\Delta i_{L_x}}{2} = 1.32 \text{ A}$$

Output voltage ripple is determined from Eq. (7-48).

$$\begin{aligned} \frac{\Delta V_o}{V_o} &= \frac{1 - 2D}{32f^2 L_x C} = \frac{1 - 2(0.3)}{32(10,000)^2(0.5)(10)^{-3}(50)(10)^{-6}} \\ &= 0.005 = 0.5\% \end{aligned}$$

7.7 FULL-BRIDGE AND HALF-BRIDGE DC-DC CONVERTERS

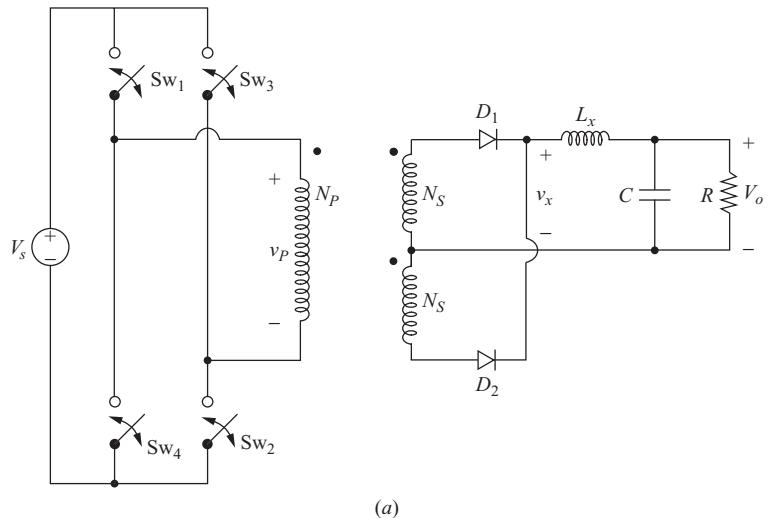
The full-bridge and half-bridge converters shown in Figs. 7-9 and 7-10 are similar in operation to the push-pull converter. Assuming that the transformer is ideal, the full-bridge converter of Fig. 7-9a has switch pairs (Sw_1, Sw_2) and (Sw_3, Sw_4) alternate closing. When Sw_1 and Sw_2 are closed, the voltage across the transformer primary is V_s . When Sw_3 and Sw_4 are closed, the transformer primary voltage is $-V_s$. For an ideal transformer, having all switches open will make $v_p = 0$. With a proper switching sequence, the voltage v_p across the transformer primary is the alternating pulse waveform shown in Fig. 7-9c. Diodes D_1 and D_2 on the transformer secondary rectify this waveform to produce the voltage v_x as shown in Fig. 7-9d. This v_x is identical to the v_x shown in Fig. 7-8c for the push-pull converter. Hence the output of the full-bridge converter is analyzed as for the push-pull converter, resulting in

$$V_o = 2V_s \left(\frac{N_S}{N_P} \right) D \quad (7-50)$$

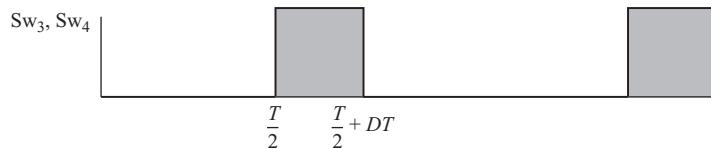
where D is the duty ratio of *each* switch pair.

Note that the maximum voltage across an open switch for the full-bridge converter is V_s , rather than $2V_s$ as for the push-pull and single-ended forward converters. Reduced voltage stress across an open switch is important when the input voltage is high, giving the full-bridge converter an advantage.

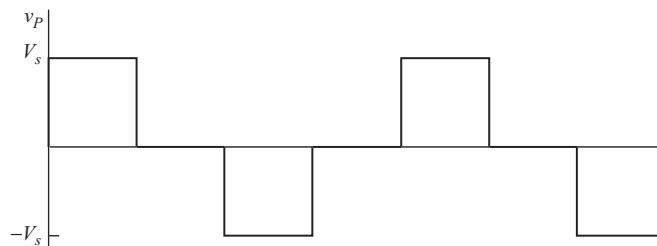
The half-bridge converter of Fig. 7-10a has capacitors C_1 and C_2 which are large and equal in value. The input voltage is equally divided between the



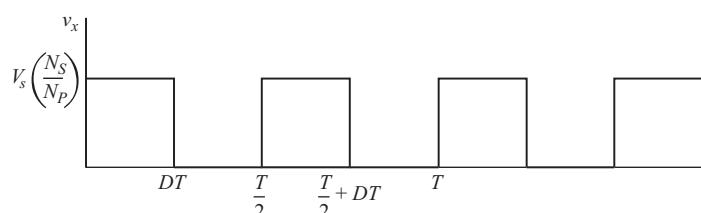
(a)



(b)

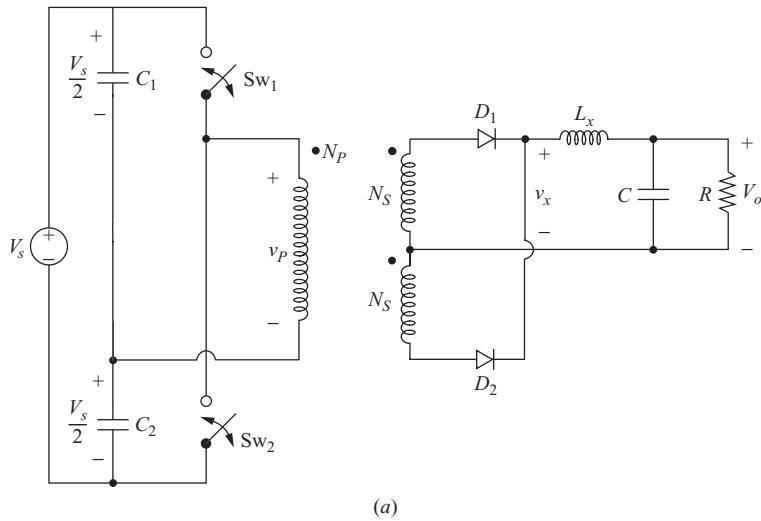


(c)

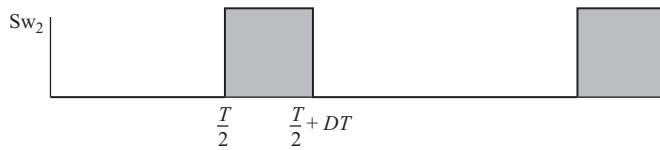
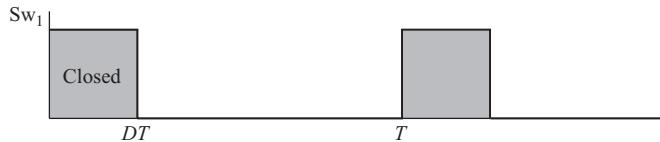


(d)

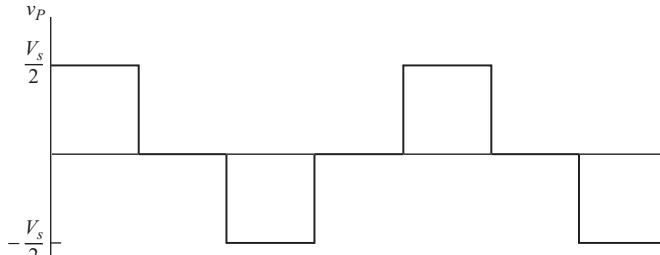
Figure 7-9 (a) Full-bridge converter; (b) Switching sequence; (c) Voltage on the transformer primary; (d) Voltage v_x .



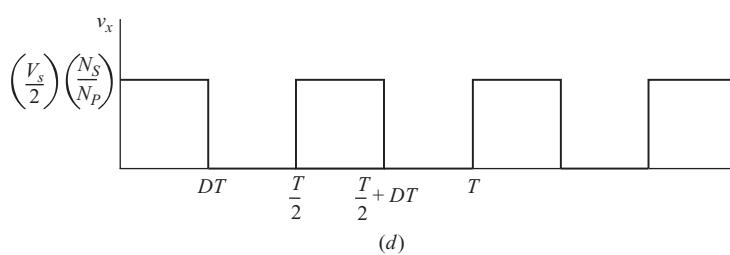
(a)



(b)



(c)



(d)

Figure 7-10 (a) Half-bridge converter; (b) Switching sequence; (c) Voltage on the transformer primary; (d) Voltage v_x .

capacitors. Switches Sw_1 and Sw_2 close with the sequence shown, producing an alternating voltage pulse v_p on the transformer primary. The rectified secondary voltage v_x has the waveform shown in Fig. 7-10d. Voltage v_x is the same form as for the push-pull and the full-bridge converters, but the amplitude is one-half the value. The relationship between the input and output voltages for the half-bridge converter is

$$V_o = V_s \left(\frac{N_S}{N_P} \right) D \quad (7-51)$$

where D is the duty ratio of each switch. The voltage across an open switch for the half-bridge converter is V_s .

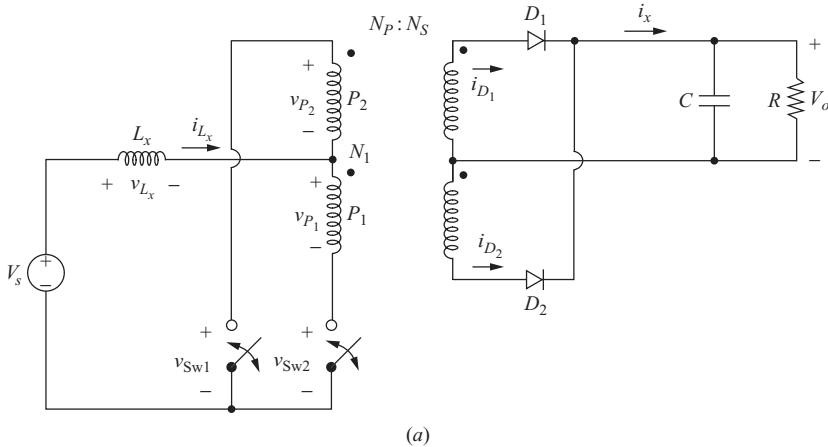
7.8 CURRENT-FED CONVERTERS

The converters described thus far in this chapter are called *voltage-fed converters*. Another method of controlling output is to establish a constant source current and use the switches to direct the current. Current control has advantages over voltage control for some converters. A circuit that operates by switching current rather than voltage is called a *current-fed converter*. Figure 7-11 shows a circuit that is a modification of the push-pull converter. The inductor L_x has been moved from the output side of the transformer to the input side. A large inductor in this position establishes a nearly constant source current. Switch Sw_1 directs the current through winding P_1 , and switch Sw_2 directs the current through winding P_2 . With both switches closed, the current divides evenly between the windings. At least one switch must be closed to provide a current path.

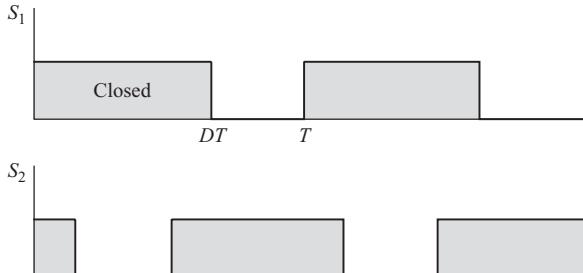
The switching sequence and waveforms are shown in Fig. 7-11. The following analysis assumes that L_x is large and the current in it is a constant I_{L_x} . The transformer is assumed to be ideal.

Sw₁ Closed and Sw₂ Open The inductor current I_{L_x} flows through primary winding P_1 and through D_1 on the secondary when switch 1 is closed and switch 2 is open. D_1 is on, D_2 is off, and the following equations apply:

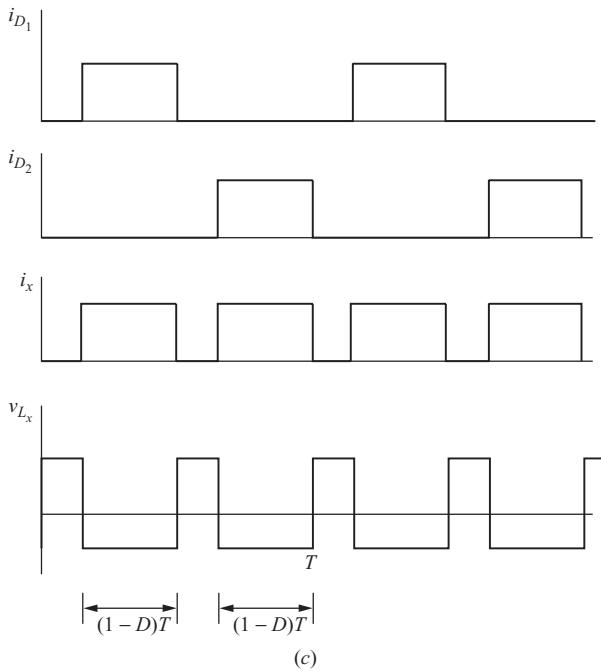
$$\begin{aligned} i_{D_1} &= I_{L_x} \left(\frac{N_P}{N_S} \right) \\ v_{P_1} &= V_o \left(\frac{N_P}{N_S} \right) \\ v_{L_x} &= V_s - v_{P_1} = V_s - V_o \left(\frac{N_P}{N_S} \right) \\ v_{\text{Sw}_2} &= v_{P_1} + v_{P_2} = 2V_o \left(\frac{N_P}{N_S} \right) \end{aligned} \quad (7-52)$$



(a)



(b)



(c)

Figure 7-11 (a) A current-fed converter; (b) Switching sequence; (c) Current and voltage waveforms.

Sw₁ Open and Sw₂ Closed With switch 1 open and switch 2 closed, I_{L_x} flows through primary winding P_2 and through D_2 on the secondary. D_1 is off and D_2 is on, and the following equations apply:

$$\begin{aligned} i_{D_2} &= I_{L_x} \left(\frac{N_P}{N_S} \right) \\ v_{P_2} &= V_o \left(\frac{N_P}{N_S} \right) \\ v_{L_x} &= V_s - V_o \left(\frac{N_P}{N_S} \right) \\ v_{\text{Sw}_1} &= v_{P_1} + v_{P_2} = 2V_o \left(\frac{N_P}{N_S} \right) \end{aligned} \quad (7-53)$$

Both Sw₁ and Sw₂ Closed With both switches closed, I_{L_x} divides evenly between the two primary windings, and both D_1 and D_2 are off. The voltage on each primary winding is zero:

$$v_{P_1} = v_{P_2} = 0$$

Inductor L_x then has the source voltage across it:

$$v_{L_x} = V_s \quad (7-54)$$

The average voltage across L_x must be zero for steady-state operation. During one switching period, $v_{L_x} = V_s - V_o(N_P/N_S)$ for two intervals of $(1 - D)T$ when only one switch is closed, and $v_{L_x} = V_s$ for the remaining time, which is $T - 2(1 - D)T = (2D - 1)T$. The average inductor voltage is thus expressed as

$$V_{L_x} = V_s(2D - 1)T + \left[V_s - V_o \left(\frac{N_P}{N_S} \right) \right] 2(1 - D)T = 0 \quad (7-55)$$

Solving for V_o ,

$$V_o = \frac{V_s}{2(1 - D)} \left(\frac{N_S}{N_P} \right)$$

(7-56)

where D is the duty ratio of *each* switch. This result is similar to that of the boost converter. Note that the duty ratio of each switch must be greater than 0.5 to prevent an open circuit in the path of the inductor current.

EXAMPLE 7-7

Current-Fed Converter

The current-fed converter of Fig. 7-11 has an input inductor L_x that is large enough to assume that the source current is essentially constant. The source voltage is 30 V, and the

load resistor is 6Ω . The duty ratio of each switch is 0.7, and the transformer has a turns ratio of $N_P/N_S = 2$. Determine (a) the output voltage, (b) the current in L_x , and (c) the maximum voltage across each switch.

■ Solution

(a) The output voltage is determined by using Eq. (7-56).

$$V_o = \frac{V_s}{2(1-D)} \left(\frac{N_S}{N_P} \right) = \frac{30}{2(1-0.7)} \left(\frac{1}{2} \right) = 25 \text{ V}$$

(b) To determine I_{L_x} , recognize that the power delivered to the load must be the same as that supplied by the source in the ideal case:

$$P_s = P_o$$

which can be expressed as

$$I_{L_x} V_s = \frac{V_o^2}{R}$$

Solving for I_{L_x} ,

$$I_{L_x} = \frac{V_o^2}{V_s R} = \frac{25^2}{30(6)} = 3.47 \text{ A}$$

(c) The maximum voltage across each switch is determined from Eqs. (7-52) and (7-53).

$$V_{sw,\max} = 2V_o \left(\frac{N_P}{N_S} \right) = 2(25)(2) = 100 \text{ V}$$

7.9 MULTIPLE OUTPUTS

The dc power supply circuits discussed thus far in this chapter have only one output voltage. With additional transformer windings, multiple outputs are possible. Flyback and forward converters with two outputs are shown in Fig. 7-12.

Multiple outputs are useful when different output voltages are necessary. The duty ratio of the switch and the turns ratio of the primary to the specific secondary winding determine the output/input voltage ratio. An example is a single converter with three windings on the output producing voltages of 12, 5, and -5 V with respect to a common ground on the output side. Multiple outputs are possible with all the dc power supply topologies discussed in this chapter. Note, however, that only one of the outputs can be regulated with a feedback control loop. Other outputs will follow according to the duty ratio and the load.

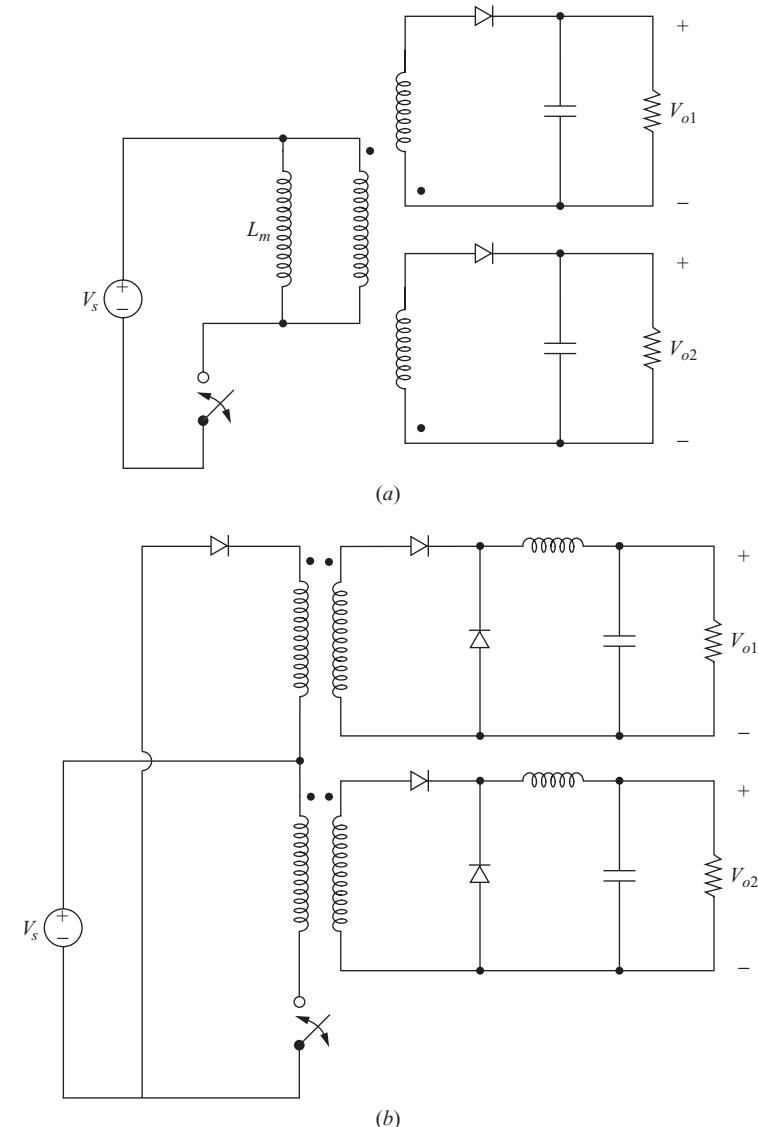


Figure 7-12 (a) Flyback and (b) forward converters with two outputs.

7.10 CONVERTER SELECTION

In theory, any power supply circuit can be designed for any application, depending on how much the designer is willing to spend for components and control circuitry. In practice, some circuits are much more suited to particular applications than others.

The flyback converter, having a low parts count, is a simple circuit to implement and is very popular for low-power applications. The main disadvantages are that the

transformer core must be made large as power requirements increase, and the voltage stress across the switch is high ($2V_s$). Typical applications can go up to about 150 W, but the flyback converter is used most often for an output power of 10 W or less.

The forward converter is a popular circuit for low and medium power levels, up to about 500 W. It has one transistor as does the flyback, but it requires a smaller transformer core. Disadvantages are high voltage stress for the transistor and the extra cost of the filter inductor. The double-ended forward converter can be used to reduce the switch voltage stress, but the drive circuit for one of the transistors must be floating with respect to ground.

The push-pull converter is used for medium to high power requirements, typically up to 1000 W. Advantages include transistor drive circuits that have a common point and a relatively small transformer core because it is excited in both directions. Disadvantages include a high voltage stress for the transistors and potential core saturation problems caused by a dc imbalance in nonideal circuits.

The half-bridge converter is also used for medium power requirements, up to about 500 W, and has some of the same advantages as the push-pull. The voltage stress on the switches is limited to V_s .

The full-bridge converter is often the circuit of choice for high-power applications, up to about 2000 W. The voltage stress on the transistors is limited to V_s . Extra transistors and floating drive circuits are disadvantages.

A method of reducing switching losses is to use a resonant converter topology. Resonant converters switch at voltage or current zeros, thus reducing the switch power loss, enabling high switching frequencies and reduced component sizes. Resonant converters are discussed in Chap. 9.

7.11 POWER FACTOR CORRECTION

Power supplies often have an ac source as the input, and the first stage is a full-wave rectifier that converts the ac input to a dc voltage. Figure 7-13, as discussed in Chap. 4, is one such arrangement. The diodes conduct for only a small amount of time during each cycle, resulting in currents that are highly nonsinusoidal. The result is a large total harmonic distortion (THD) of current coming from the ac

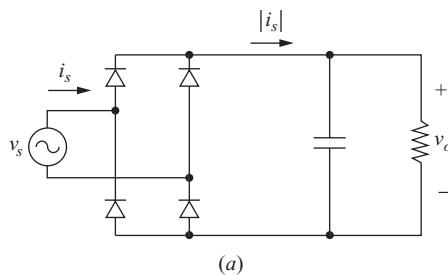


Figure 7-13 (a) Fullwave rectifier and (b) voltage and current waveforms. The source current is highly nonsinusoidal because the diodes conduct for a short time interval.

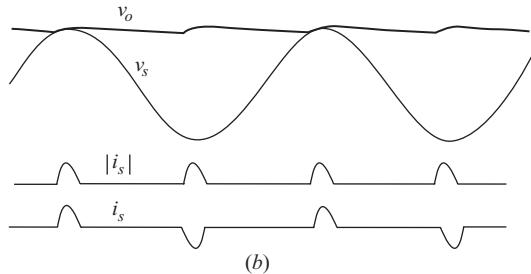


Figure 7-13 (continued)

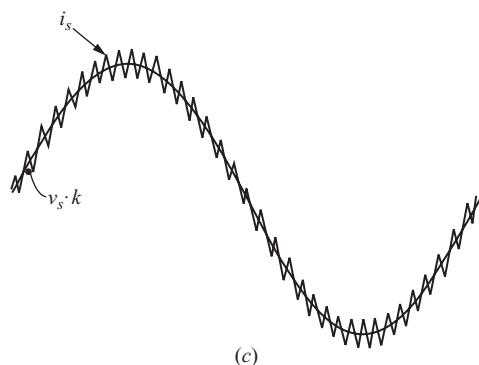
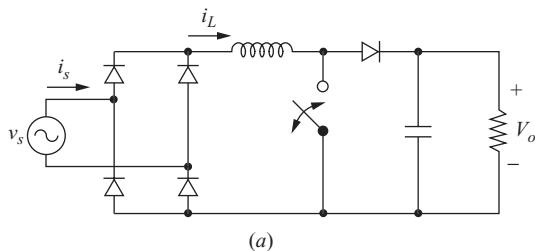


Figure 7-14 (a) A rectifier circuit used to produce a high power factor and low THD; (b) Current in the inductor for continuous-current mode (CCM) operation; (c) Current from the ac source.

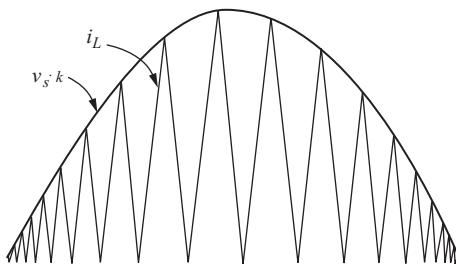


Figure 7-15 Discontinuous-current mode (DCM) power factor correction.

source. A large THD corresponds to a low power factor (see Chap. 2). The resistor represents any load on the output, which may be a dc-dc converter.

A way to improve the power factor (and reduce the THD) is with a power factor correction circuit, as shown in Fig. 7-14a. A boost converter is used to make the current in the inductor approximate a sinusoid. When the switch is closed, the inductor current increases. When the switch is open, the inductor current decreases. By using appropriate switching intervals, the inductor current can be made to follow the sinusoidal shape of the full-wave rectified input voltage.

The voltage on the output of the diode bridge is a full-wave rectified sinusoid. The current in the inductor is of the general form as shown in Fig. 7-14b, and the resulting current from the ac source is shown in Fig. 7-14c. This current is predominantly at the same frequency and phase angle as the voltage, making the power factor quite high and the THD quite low. This type of switching scheme is called continuous-current mode (CCM) power factor correction (PFC). In an actual implementation, the switching frequency would be much greater than is shown in the figure.

Another type of switching scheme produces a current like that shown in Fig. 7-15. In this scheme, the inductor current varies between zero and a peak that follows a sinusoidal shape. This type of switching scheme is called discontinuous-current mode (DCM) power factor correction. DCM is used with low-power circuits, while CCM is more suitable for high-power applications.

In both the CCM and DCM schemes, the output of the power factor correction (PFC) stage is a large dc voltage, usually on the order of 400 V. The output of the PFC stage will go to a dc-dc converter. For example, a forward converter can be used to step down the 400-V output of the PFC stage to 5 V.

Other converter topologies in addition to the boost converter can be used for power factor correction. The SEPIC and Ćuk converters are well suited for this purpose.

7.12 PSPICE SIMULATION OF DC POWER SUPPLIES

PSpice simulations of the magnetically coupled dc-dc converters discussed in this chapter are similar to those of the dc-dc converters of Chap. 6. For initial investigation, the switches can be implemented with voltage-controlled switches

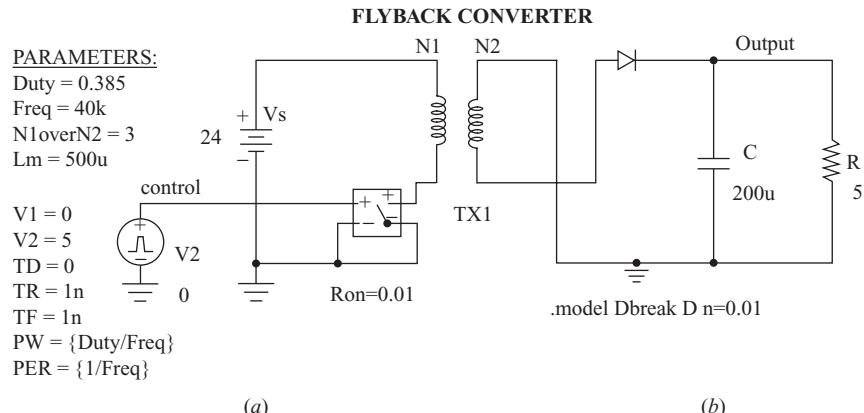


Figure 7-16 (a) The flyback converter circuit for simulation; (b) Probe output showing the transient and steady-state output voltage.

rather than with transistors, simplifying the switching and allowing examination of the overall circuit behavior.

Transformers can be modeled in PSpice as two or more inductances with ideal coupling. Since inductance is proportional to the square of the turns in a winding, the transformer turns ratio is

$$\frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}} \quad (7-57)$$

For the flyback converter, let $L_1 = L_m$ and determine L_2 from Eq. (7-57). For other converters where L_m is not a design parameter, let L_1 be any large value and determine L_2 accordingly. For two-winding transformers, the part XFRM_LINEAR can serve as a template.

Figures 7-16 and 7-17 show circuits for the flyback and forward converter topologies. The flyback simulation uses the XFRM_LINEAR part, and the forward simulation uses mutually coupled inductors. The switches and diodes are idealized by setting $R_{on} = 0.01 \Omega$ for the switches and $n = 0.01$ for the diodes. Just as with the dc-dc converters in Chap. 6, transient voltages and currents precede the steady-state waveforms that were presented in the earlier discussion of the converters in this chapter.

7.13 POWER SUPPLY CONTROL

In ideal switching dc-dc converters, the output voltage is a function of the input voltage and duty ratio. In real circuits with nonideal components, the output is also a function of the load current because of resistances in the components. A power supply output is regulated by modulating the duty ratio to compensate for variations in the input or load. A feedback control system for power supply control compares output voltage to a reference and converts the error to a duty ratio.

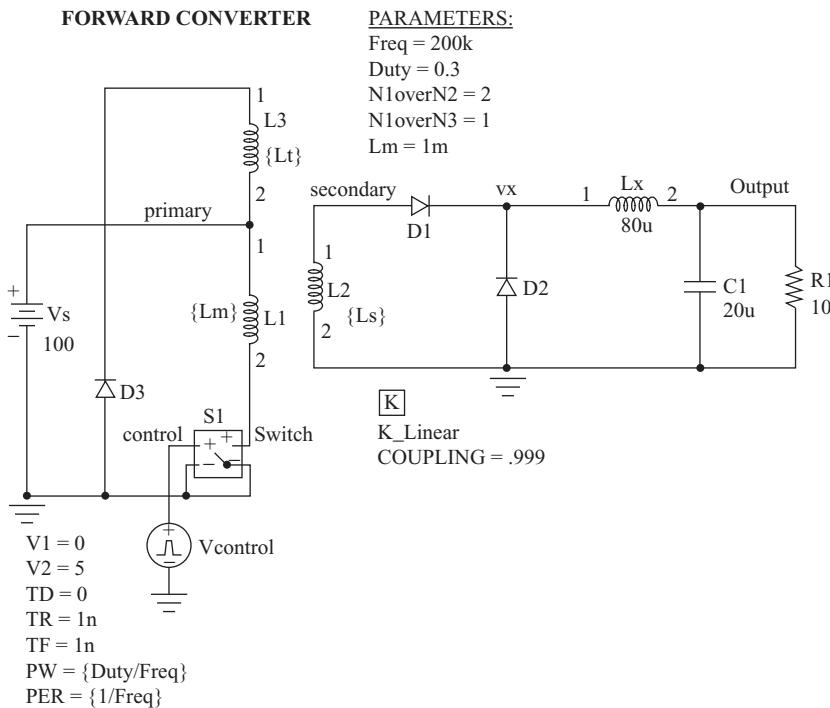


Figure 7-17 The forward converter circuit for simulation.

The buck converter operating in the continuous-current mode is used to illustrate the basics of power supply control. Figure 7-18a shows the converter and feedback loop consisting of

1. The switch, including the diode and drive circuit
2. The output filter
3. A compensated error amplifier
4. A pulse-width modulating circuit that converts the output of the compensated error amplifier to a duty ratio to drive the switch

The regulated converter is represented by the closed-loop system of Fig. 7-18b.

Control Loop Stability

Performance and stability of the control loop for regulating the output voltage for a converter can be determined from the open-loop characteristics:

1. The gain at low frequencies should be large so the steady-state error between the output and the reference signal is small.
2. The gain at the converter's switching frequency should be small.

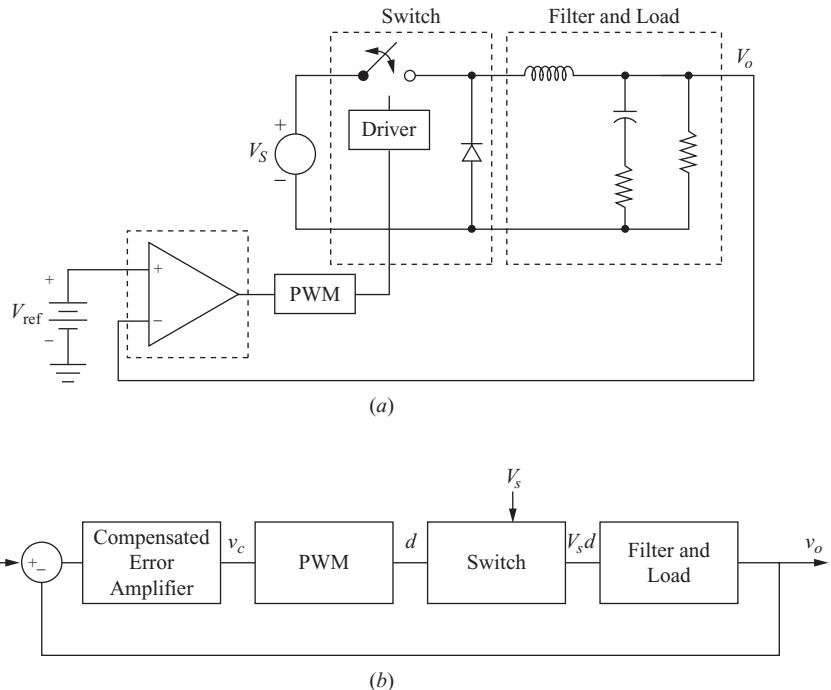


Figure 7-18 (a) Buck converter with feedback; (b) Control representation.

3. The open-loop phase shift at the crossover frequency (the frequency where the open-loop gain is unity) must lag by less than 180° . If the phase lag were 180° (or -180°), negative feedback provides a shift of another 180° , resulting in a total of 360° (or zero). A gain of magnitude 1 and phase of 360° around the loop make the loop unstable. The open-loop phase shift less than -180° at crossover is called the *phase margin*. A phase margin of at least 45° is a commonly used criterion for stability. Figure 7-19 illustrates the concept of phase margin. Note that phase margin is the angle between the phase shift and zero when the 180° phase angle of the inverting operational amplifier is included, which is convenient for use with PSpice analysis.

The transfer function of each block of the system in Fig. 7-18b must be developed to describe the control properties.

Small-Signal Analysis

Control loop analysis is based on the dynamic behavior of voltages, currents, and switching, unlike the steady-state analysis where the averaged circuit quantities are constants. Dynamic behavior can be described in terms of small-signal

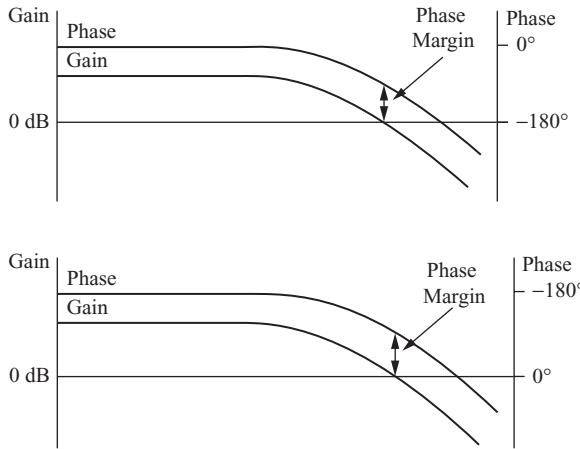


Figure 7-19 Phase margin. (a) In classical control theory, the phase margin is the angle difference between -180° and the open-loop phase angle at the crossover frequency, where the open-loop gain magnitude is 0 dB; (b) The phase margin is between zero and the phase angle when the 180° phase angle of the inverting operational amplifier is included, which is convenient for PSpice simulation.

variations around a steady-state operating point. Output voltage, duty ratio, inductor current, source voltage, and other quantities are represented as

$$\begin{aligned} v_o &= V_o + \tilde{v}_o \\ d &= D + \tilde{d} \\ i_L &= I_L + \tilde{i}_L \\ v_s &= V_s + \tilde{v}_s \end{aligned} \tag{7-58}$$

In these equations, the steady-state or dc term is represented by the uppercase letters, the \sim (tilde) quantity represents the ac term or small-signal perturbation, and the sum is the total quantity, represented by the lowercase letters.

Switch Transfer Function

For control purposes, the average values of voltages and currents are of greater interest than the instantaneous values that occur during the switching period. Equivalent representations of the switch in a buck converter are shown in Fig. 7-20. The relationship between input and output for the switch for a time-varying duty ratio is represented by the ideal transformation of $1 : d$ shown in Fig. 7-20b. Here, d represents a time-varying duty ratio consisting of a dc (constant) component D plus a small-signal component \tilde{d} .

$$d = D + \tilde{d} \tag{7-59}$$

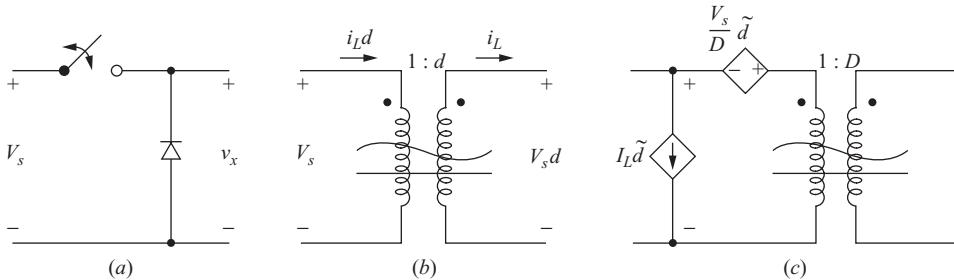


Figure 7-20 Switch models. (a) Switch and diode; (b) Model representing the transformation of average voltage and average current; (c) Model that separates steady-state and small-signal components.

An alternative representation of the switch shown in Fig. 7-20c separates the steady-state and small-signal components. The transformer secondary voltage v_x is related to the source voltage by

$$v_x = v_s d = (V_s + \tilde{v}_s)(D + \tilde{d}) = V_s D + \tilde{v}_s D + V_s \tilde{d} + \tilde{v}_s \tilde{d} \quad (7-60)$$

Neglecting the product of the small-signal terms,

$$v_x \doteq V_s D + \tilde{v}_s D + V_s \tilde{d} = v_s D + V_s \tilde{d} \quad (7-61)$$

Similarly, the current on the source side of the transformer is related to the secondary current by

$$i_s = i_L d = (I_L + \tilde{i}_L)(D + \tilde{d}) \doteq i_L D + I_L \tilde{d} \quad (7-62)$$

The circuit of Fig. 7-20c, with the transformer ratio fixed at D and the small-signal terms included with the dependent sources, satisfies the voltage and current requirements of the switch expressed in Eqs. (7-61) and (7-62).

Filter Transfer Function

The input to the buck converter filter is the switch output, which is $v_x = v_s d$ on an averaged circuit basis in the continuous current mode. The RLC filter of the buck converter has a transfer function developed from a straightforward application of circuit analysis in the s domain. From Fig. 7-21a, the transfer function of the filter with the load resistor is

$$\frac{v_o(s)}{v_x(s)} = \frac{v_o(s)}{V_s d(s)} = \frac{1}{LC[s^2 + s(1/RC) + 1/LC]} \quad (7-63)$$

$$\text{or } \frac{v_o(s)}{d(s)} = \frac{V_s}{LC[s^2 + s(1/RC) + 1/LC]} \quad (7-64)$$

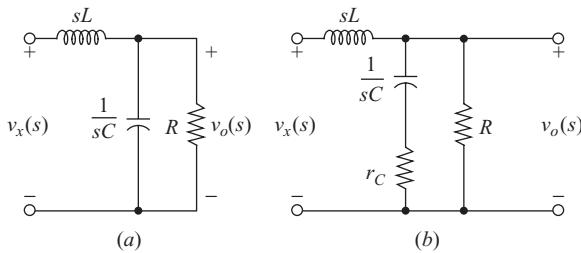


Figure 7-21 Circuits for deriving the filter transfer function (a) with an ideal capacitor and (b) with the ESR of the capacitor.

The above transfer function is based on ideal filter components. An equivalent series resistance (ESR) of r_C for a nonideal capacitor in Fig. 7-21b results in a filter transfer function of

$$\frac{v_o(s)}{d(s)} = \frac{V_s}{LC} \left[\frac{1 + sr_C R}{s^2(1 + r_C/R) + s(1/RC + r_C/L) + 1/LC} \right] \quad (7-65)$$

Since $r_C \ll R$ in practical circuits, the transfer function becomes approximately

$$\frac{v_o(s)}{d(s)} \approx \frac{V_s}{LC} \left[\frac{1 + sr_C R}{s^2 + s(1/RC + r_C/L) + 1/LC} \right] \quad (7-66)$$

The numerator of Eq. (7-66) shows that the ESR of the capacitor produces a zero in the transfer function, which may be important in determining system stability.

A general technique for establishing the switch and filter transfer function is state-space averaging. A development of this method is shown in App. B.

Pulse-Width Modulation Transfer Function

The pulse-width modulation (PWM) circuit converts the output from the compensated error amplifier to a duty ratio. The error amplifier output voltage v_c is compared to a sawtooth waveform with amplitude V_p , as shown in Fig. 7-22. The output of the PWM circuit is high while v_c is larger than the sawtooth and is zero when v_c is less than the sawtooth. If the output voltage falls below the reference, the error between the converter output and the reference signal increases, causing v_c to increase and the duty ratio to increase. Conversely, a rise in output voltage reduces the duty ratio. A transfer function for the PWM process is derived from the linear relation

$$d = \frac{v_c}{V_p} \quad (7-67)$$

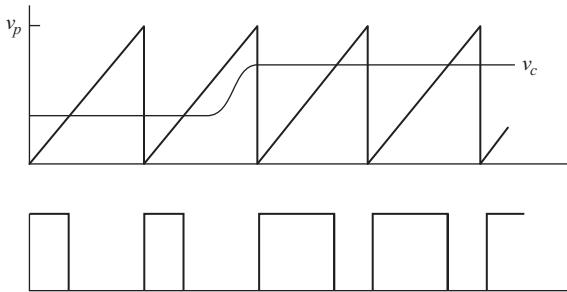


Figure 7-22 The PWM process. The output is high when v_c from the compensated error amplifier is higher than the sawtooth waveform.

The transfer function of the PWM circuit is therefore

$$\frac{d(s)}{v_c(s)} = \frac{1}{V_p} \quad (7-68)$$

Type 2 Error Amplifier with Compensation

The error amplifier compares the converter output voltage with a reference voltage to produce an error signal that is used to adjust the duty ratio of the switch. Compensation associated with the amplifier determines control loop performance and provides for a stable control system.

The transfer function of the compensated error amplifier should give a total loop characteristic consistent with the stability criteria described previously. Namely, the amplifier should have a high gain at low frequencies, a low gain at high frequencies, and an appropriate phase shift at the crossover frequency.

An amplifier that suits this purpose for many applications is shown in Fig. 7-23a. This is commonly referred to as a type 2 compensated error amplifier. (A type 1 amplifier is a simple integrator with one resistor on the input and one capacitor as feedback.). The amplifier is analyzed for the small-signal transfer function, so the dc reference voltage V_{ref} has no effect on the small-signal portion of the analysis. Furthermore, a resistor can be placed between the inverting input terminal and ground to act as a voltage divider to adjust the converter output voltage, and that resistor will have no effect on the small-signal analysis because the small-signal voltage at the noninverting terminal, and therefore at the inverting terminal, is zero.

The small-signal transfer function (with dc terms set to zero) of the amplifier is expressed in terms of input and feedback impedances Z_i and Z_f , where

$$Z_f = \left(R_2 + \frac{1}{sC_1} \right) \parallel \frac{1}{sC_2} = \frac{(R_2 + 1/sC_1)(1/sC_2)}{R_2 + 1/sC_1 + 1/sC_2} \quad (7-69)$$

$$Z_i = R_1$$

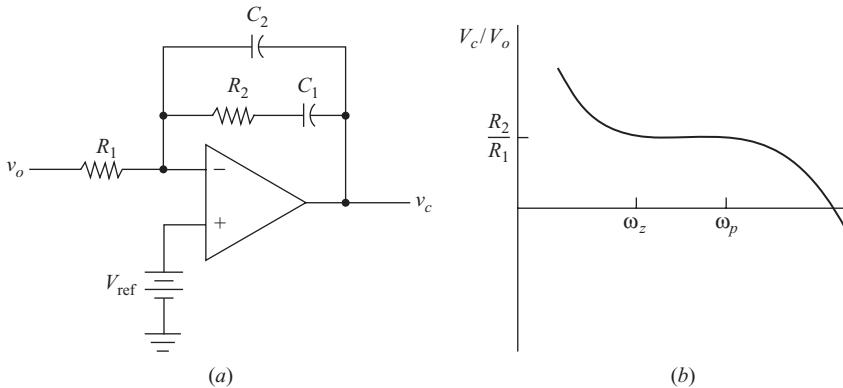


Figure 7-23 (a) Type 2 compensated error amplifier; (b) Frequency response.

The gain function $G(s)$ is expressed as the ratio of the compensated error amplifier small-signal output \tilde{v}_c to the input, which is the converter output \tilde{v}_o .

$$G(s) = \frac{\tilde{v}_c(s)}{\tilde{v}_o(s)} = -\frac{Z_f}{Z_i} = -\frac{(R_2 + 1/sC_1)(1/sC_2)}{R_1(R_2 + 1/sC_1 + 1/sC_2)} \quad (7-70)$$

Rearranging terms and assuming $C_2 \ll C_1$,

$$G(s) = \frac{\tilde{v}_c(s)}{\tilde{v}_o(s)} = -\frac{s + 1/R_2C_2}{R_1C_2s[s + (C_1 + C_2)/R_2C_1C_2]} \approx -\frac{s + 1/R_2C_1}{R_1C_2s(s + 1/R_2C_2)} \quad (7-71)$$

The above transfer function has a pole at the origin and a zero and pole at

$$\omega_z = \frac{1}{R_2C_1} \quad (7-72)$$

$$\omega_p = \frac{C_1 + C_2}{R_2C_1C_2} \approx \frac{1}{R_2C_2} \quad (7-73)$$

The frequency response of this amplifier has the form shown in Fig. 7-23b. The values of R_1 , R_2 , C_1 , and C_2 are chosen to make the overall control system have the desired attributes.

The combined frequency response of the transfer functions of the PWM circuit, the switch, and the output filter of a converter is shown in Fig. 7-24. The ESR of the filter capacitor puts a zero at $\omega = 1/r_c C$. A simulation program such as PSpice is useful to determine the frequency response. Otherwise, the transfer function may be evaluated with $s = j\omega$.

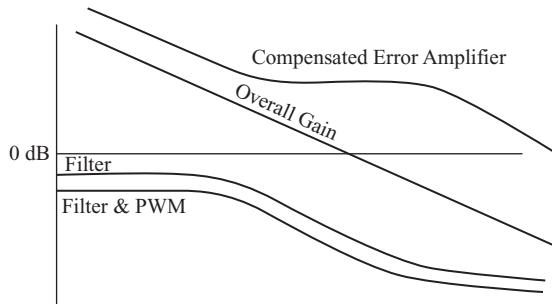


Figure 7-24 The control loop transfer function frequency response.

EXAMPLE 7-8

A Type 2 Amplifier Control Loop for a Buck Converter

The source voltage for a buck converter is $V_s = 6$ V, and the output voltage is to be regulated at 3.3 V. The load resistance is 2Ω , $L = 100 \mu\text{H}$ with negligible internal resistance, and $C = 75 \mu\text{F}$ with an ESR of 0.4Ω . The PWM circuit has a sawtooth voltage with peak value $V_p = 1.5$ V. A type 2 compensated error amplifier has $R_1 = 1 \text{ k}\Omega$, $R_2 = 2.54 \text{ k}\Omega$, $C_1 = 48.2 \text{ nF}$, and $C_2 = 1.66 \text{ nF}$. The switching frequency is 50 kHz. Use PSpice to determine the crossover frequency and the phase margin.

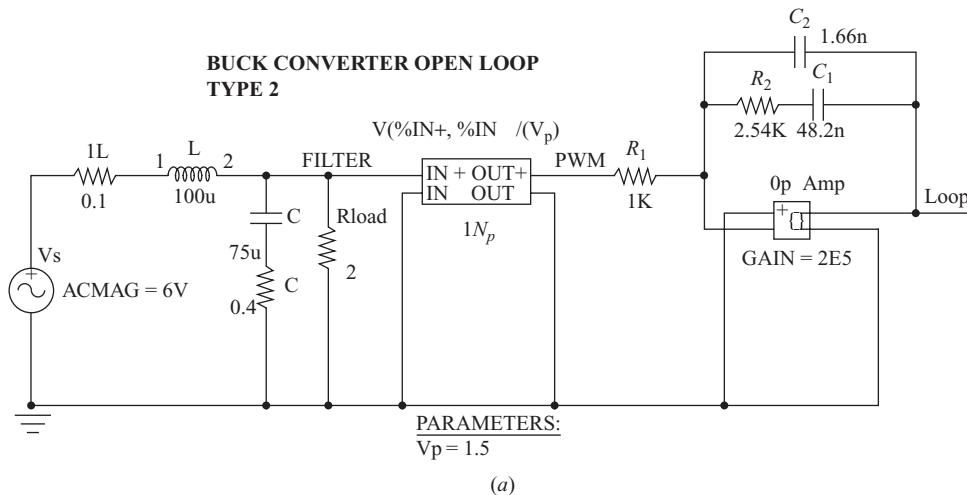


Figure 7-25 (a) PSpice circuit for simulating the open-loop response of a buck converter;
 (b) Probe output for Example 7-8 showing a crossover frequency of 6.83 kHz and a phase margin of approximately 45° .

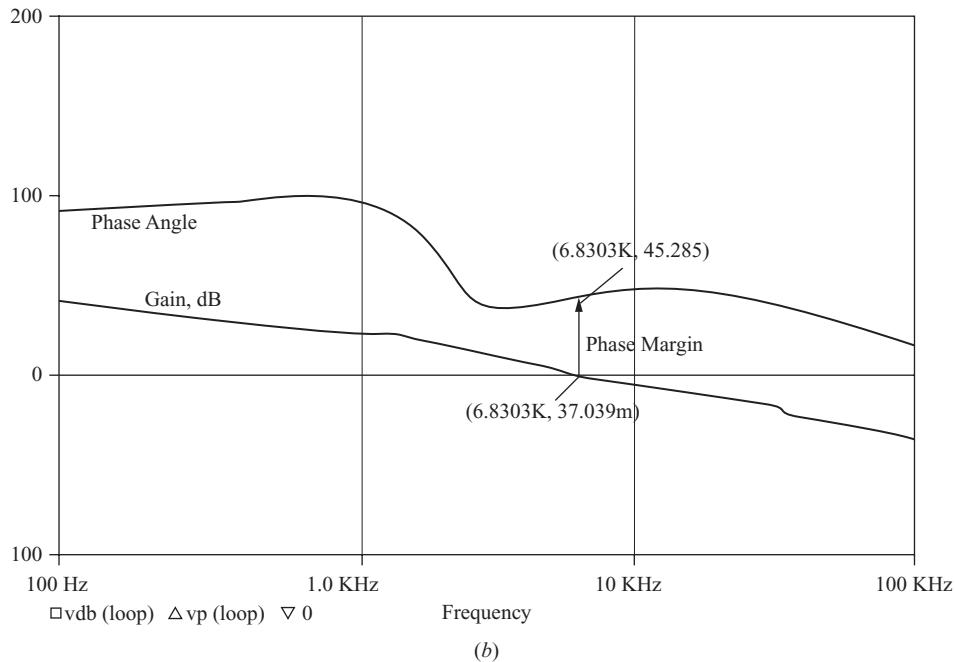


Figure 7-25 (continued).

Solution

A PSpice circuit for the filter, compensated error amplifier, and PWM converter is shown in Fig. 7-25a. The input voltage source is the ac source V_{ac} , the PWM function of $1/V_p$ is implemented with the dependent source EVALUE, and the ideal op-amp is implemented with a high-gain voltage-controlled voltage source.

The Probe output shown in Fig. 7-25b reveals the crossover frequency to be 6.83 kHz. The phase margin is the angle greater than zero (or 360°) because the operational amplifier contains the inversion (180°) for negative feedback (Fig. 7-19a). The Probe output shows the phase margin to be slightly larger than 45° . The gain is low, -23.8 dB, at the 50-kHz switching frequency. Therefore, this circuit meets the criteria for a stable control system.

Design of a Type 2 Compensated Error Amplifier

The midfrequency gain and the location of the pole and zero of the transfer function of the compensated error amplifier must be selected to provide the desired total open-loop crossover frequency and phase margin required for stability.

The transfer function of the compensated error amplifier in Eq. (7-71) can be expressed for $s = j\omega$ as

$$G(j\omega) = \frac{\tilde{v}_c(j\omega)}{\tilde{v}_o(j\omega)} = -\frac{j\omega + \omega_z}{R_1 C_2 j\omega(j\omega + \omega_p)} \quad (7-74)$$

For the middle frequencies, $\omega_z \ll \omega \ll \omega_p$, resulting in

$$G(j\omega) = \frac{\tilde{v}_c(j\omega)}{\tilde{v}_o(j\omega)} \approx -\frac{j\omega}{R_1 C_2 j\omega \omega_p} = -\frac{1}{R_1 C_2 (1/R_2 C_2)} = -\frac{R_2}{R_1} \quad (7-75)$$

The phase angle θ_{comp} of the compensated error amplifier transfer function of Eq. (7-74) is

$$\begin{aligned} \theta_{\text{comp}} &= -180^\circ + \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - 90^\circ - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) \\ &= -270^\circ + \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) \end{aligned} \quad (7-76)$$

The -180° is from the negative sign, and the -90° is from the pole at the origin. Note that in this development the inverting amplifier phase shift of -180° is included in Eq. (7-76). In some developments of this method, the inverting amplifier phase shift is omitted at this point and then included later.

The following is a design procedure for the type 2 compensated error amplifier.

1. Choose the desired crossover frequency of the total open-loop transfer function. This is usually around an order of magnitude less than the converter switching frequency. Some designers go as high as 25 percent of the switching frequency.
2. Determine the transfer function and frequency response of all elements in the control circuit except for the compensated error amplifier.
3. Determine the midfrequency gain of the compensated error amplifier required to achieve the overall desired crossover frequency. This establishes the R_2/R_1 ratio as in Eq. (7-75).
4. Choose the desired phase margin needed to ensure stability, typically greater than 45° . Having established R_1 and R_2 for the midfrequency gain, the pole and zero, ω_p and ω_z , are determined by C_1 and C_2 . The phase angle θ_{comp} of the compensated error amplifier at the crossover frequency ω_{co} is

$$\theta_{\text{comp}} = -270^\circ + \tan^{-1}\left(\frac{\omega_{\text{co}}}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_{\text{co}}}{\omega_p}\right) \quad (7-77)$$

A procedure for selecting the pole and zero frequencies is the K factor method [see Venable (1983) and Basso (2008) in the Bibliography]. Using the K factor method, the value of K is determined as follows:

Let the zero and pole of the transfer function be at

$$\omega_z = \frac{\omega_{\text{co}}}{K} \quad (7-78)$$

and

$$\omega_p = K\omega_{\text{co}} \quad (7-79)$$

Then

$$K = \frac{\omega_{co}}{\omega_z} = \frac{\omega_p}{\omega_{co}} \quad (7-80)$$

The phase angle of the compensated error amplifier at crossover in Eq. (7-77) is then

$$\theta_{comp} = -270^\circ + \tan^{-1} K - \tan^{-1} \left(\frac{1}{K} \right) \quad (7-81)$$

Using the trigonometric identity

$$\tan^{-1}(x) + \tan^{-1} \left(\frac{1}{x} \right) = 90^\circ \quad (7-82)$$

gives

$$\tan^{-1} \left(\frac{1}{K} \right) = 90^\circ - \tan^{-1}(K) \quad (7-83)$$

Equation (7-81) becomes

$$\theta_{comp} = -270^\circ + \tan^{-1}(K) - (90^\circ - \tan^{-1}(K)) = 2\tan^{-1}(K) - 360^\circ = 2\tan^{-1}(K) \quad (7-84)$$

Solving for K ,

$$K = \tan \left(\frac{\theta_{comp}}{2} \right) \quad (7-85)$$

The angle θ_{comp} is the desired phase angle of the compensated error amplifier at the crossover frequency. From Eq. (7-84), the phase angle of the compensated error amplifier can range from 0 to 180° for $0 < K < \infty$.

The required phase angle of the compensated error amplifier to obtain the desired phase margin is determined, establishing the value of K . If the desired crossover frequency ω_{co} is known, then ω_z and ω_p are obtained from Eqs. (7-78) and (7-79). Then C_1 and C_2 are determined from Eqs. (7-71) and (7-72).

$$\begin{aligned} \omega_z &= \frac{1}{R_2 C_1} = \frac{\omega_{co}}{K} \\ C_1 &= \frac{K}{\omega_{co} R_2} = \frac{K}{2\pi f_{co} R_2} \end{aligned} \quad (7-86)$$

$$\begin{aligned} \omega_p &= \frac{1}{R_2 C_2} = K \omega_{co} \\ C_2 &= \frac{1}{K \omega_{co} R_2} = \frac{1}{K 2\pi f_{co} R_2} \end{aligned} \quad (7-87)$$

EXAMPLE 7-9

Design of a Type 2 Compensated Error Amplifier

For a buck converter shown in Fig. 7-26a,

- $V_s = 10 \text{ V}$ with an output of 5 V
 $f = 100 \text{ kHz}$
 $L = 100 \mu\text{H}$ with a series resistance of 0.1Ω
 $C = 100 \mu\text{F}$ with an equivalent series resistance of 0.5Ω
 $R = 5 \Omega$
 $V_p = 3 \text{ V}$ in PWM circuit

Design a type 2 compensated error amplifier that results in a stable control system.

■ Solution

1. The crossover frequency of the total open-loop transfer function (the frequency where the gain is 1, or 0 dB) should be well below the switching frequency. Let $f_{co} = 10 \text{ kHz}$.
2. A PSpice simulation of the frequency response of the filter with load resistor (Fig. 7-26b) shows that the converter (V_s and the filter) gain at 10 kHz is -2.24 dB and the phase angle is -101° . The PWM converter has a gain of $1/V_p = 1/3 = -9.5 \text{ dB}$. The combined gain of the filter and PWM converter is then $-2.24 \text{ dB} - 9.54 \text{ dB} = -11.78 \text{ dB}$.

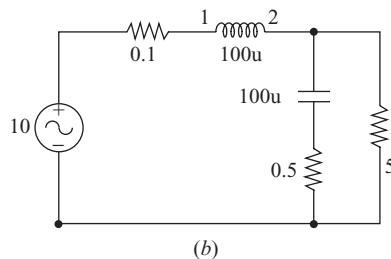
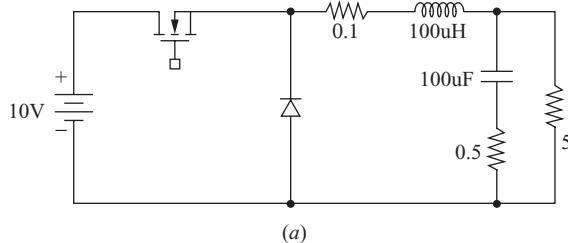


Figure 7-26 (a) Buck converter circuit; (b) The ac circuit for determining the frequency response of the converter.

3. The compensated error amplifier should therefore have a gain of +11.78 dB at 10 kHz to make the loop gain 0 dB. Converting the gain in decibels to a ratio of v_o/v_i ,

$$11.78 \text{ dB} = 20 \log\left(\frac{\tilde{v}_c}{\tilde{v}_o}\right)$$

$$\frac{\tilde{v}_c}{\tilde{v}_o} = 10^{11.78/20} = 3.88$$

Using Eq. (7-75), the magnitude of the midfrequency gain is

$$\frac{R_2}{R_1} = 3.88$$

Letting $R_1 = 1 \text{ k}\Omega$, R_2 is then $3.88 \text{ k}\Omega$.

4. The phase angle of the compensated error amplifier at crossover must be adequate to give a phase margin of at least 45° . The required phase angle of the amplifier is

$$\theta_{\text{comp}} = \theta_{\text{phase margin}} - \theta_{\text{converter}} = 45^\circ - (-101^\circ) = 146^\circ$$

A K factor of 3.27 is obtained from Eq. (7-85).

$$K = \tan\left(\frac{\theta_{\text{comp}}}{2}\right) = \tan\left(\frac{146^\circ}{2}\right) = \tan(73^\circ) = 3.27$$

Using Eq. (7-86) to get C_1 ,

$$C_1 = \frac{K}{2\pi f_{\text{co}} R_2} = \frac{3.27}{2\pi(10,000)(3880)} = 13.4 \text{ nF}$$

Using Eq. (7-87) to get C_2 ,

$$C_2 = \frac{1}{K2\pi f_{\text{co}} R_2} = \frac{1}{3.27(2\pi)(10,000)(3880)} = 1.25 \text{ nF}$$

A PSpice simulation of the control loop gives a crossover frequency of 9.41 kHz and a phase margin of 46° , verifying the design.

PSpice Simulation of Feedback Control

Simulation is a valuable tool in the design and verification of a closed-loop control system for dc power supplies. Figure 7.27a shows a PSpice implementation using idealized switches and ETABLE sources for the op-amp and for the comparator in the PWM function. The input is 6 V, and the output is to be regulated at 3.3 V. The phase margin of this circuit is 45° when the load is 2Ω , and slightly greater than 45° when the load changes to $2\parallel 4 \Omega$. The switching frequency is 100 kHz. A step change in load occurs at $t = 1.5 \text{ ms}$. If the circuit were unregulated, the output voltage would change as the load current changed because of the inductor resistance. The control circuit adjusts the duty ratio to compensate for changes in operating conditions.

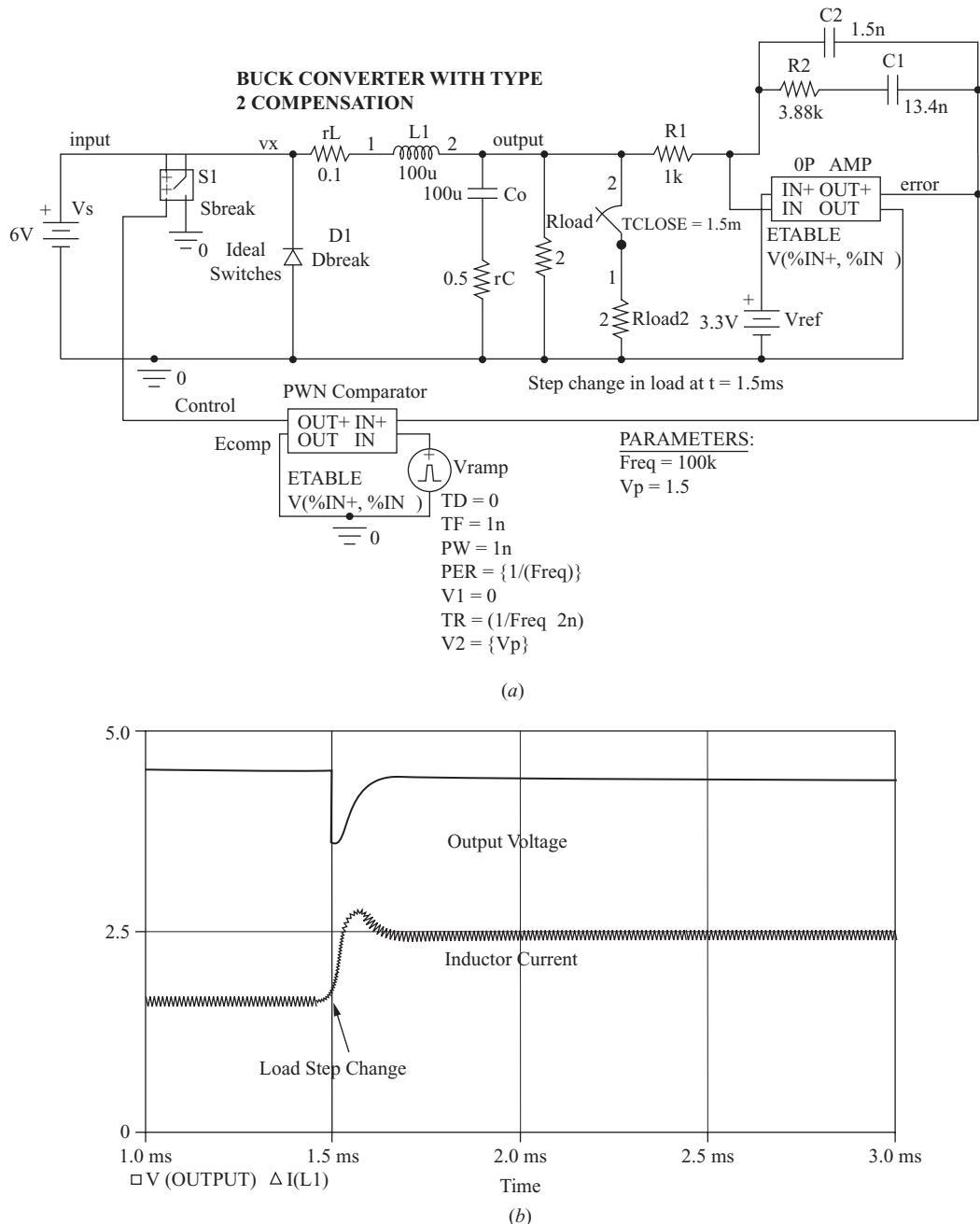


Figure 7-27 (a) PSpice circuit for a regulated buck converter; (b) Output voltage and inductor current for a step change in load.

Figure 7-27b shows the output voltage and inductor current, verifying that the control circuit is stable.

Type 3 Error Amplifier with Compensation

The type 2 compensation circuit described previously is sometimes not capable of providing sufficient phase angle difference to meet the stability criterion of a 45° phase margin. Another compensation circuit, known as the type 3 amplifier, is shown in Fig. 7-28a. The type 3 amplifier provides an additional phase angle boost compared to the type 2 circuit and is used when an adequate phase margin is not achievable using the type 2 amplifier.

The small-signal transfer function is expressed in terms of input and feedback impedances Z_i and Z_f ,

$$G(s) = \frac{\tilde{v}_c(s)}{\tilde{v}_o(s)} = -\frac{Z_f}{Z_i} = -\frac{(R_2 + 1/sC_1)\parallel 1/sC_2}{R_1\parallel(R_3 + 1/sC_3)} \quad (7-88)$$

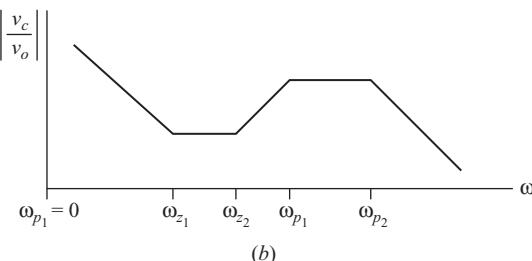
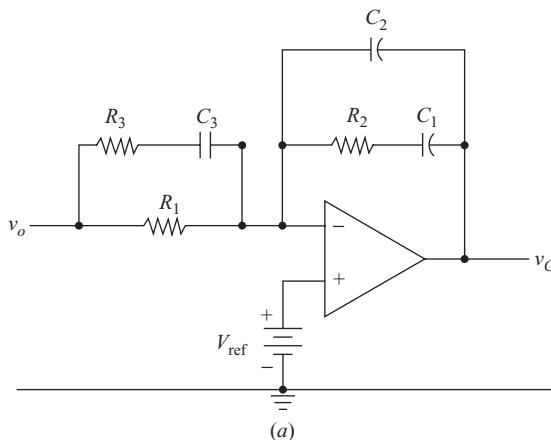


Figure 7-28 (a) Type 3 compensated error amplifier;
(b) Bode magnitude plot.

resulting in

$$G(s) = -\frac{R_1 + R_3}{R_1 R_3 C_3} \frac{\left(s + \frac{1}{R_2 C_1}\right)\left(s + \frac{1}{(R_1 + R_3)C_3}\right)}{s\left(s + \frac{C_1 + C_2}{R_2 C_1 C_2}\right)\left(s + \frac{1}{R_3 C_3}\right)} \quad (7-89)$$

The reference voltage V_{ref} is purely dc and has no effect on the small-signal transfer function. Assuming $C_2 \ll C_1$ and $R_3 \ll R_1$,

$$G(s) \approx -\frac{1}{R_3 C_2} \frac{(s + 1/R_2 C_1)(s + 1/R_1 C_3)}{s(s + 1/R_2 C_2)(s + 1/R_3 C_3)} \quad (7-90)$$

An inspection of the transfer function of Eq. (7-90) shows that there are two zeros and three poles, including the pole at the origin. A particular placement of the poles and zeros produces the Bode plot of the transfer function shown in Fig. 7-28b.

$$G(j\omega) = -\frac{1}{R_3 C_2} \frac{(j\omega + \omega_{z_1})(j\omega + \omega_{z_2})}{j\omega(j\omega + \omega_{p_2})(j\omega + \omega_{p_3})} \quad (7-91)$$

The zeros and poles of the transfer function are

$$\begin{aligned} \omega_{z_1} &= \frac{1}{R_2 C_2} \\ \omega_{z_2} &= \frac{1}{(R_1 + R_3)C_3} \approx \frac{1}{R_1 C_3} \\ \omega_{p_1} &= 0 \\ \omega_{p_2} &= \frac{C_1 + C_2}{R_2 C_1 C_2} \approx \frac{1}{R_2 C_2} \\ \omega_{p_3} &= \frac{1}{R_3 C_3} \end{aligned} \quad (7-92)$$

The phase angle of the compensated error amplifier is

$$\begin{aligned} \theta_{\text{comp}} &= -180^\circ + \tan^{-1}\left(\frac{\omega}{\omega_{z_1}}\right) + \tan^{-1}\left(\frac{\omega}{\omega_{z_2}}\right) - 90^\circ - \tan^{-1}\left(\frac{\omega}{\omega_{p_2}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p_3}}\right) \\ &= -270^\circ + \tan^{-1}\left(\frac{\omega}{\omega_{z_1}}\right) + \tan^{-1}\left(\frac{\omega}{\omega_{z_2}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p_2}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p_3}}\right) \end{aligned} \quad (7-93)$$

The -180° is from the negative sign, and the -90° is from the pole at the origin.

Design of a Type 3 Compensated Error Amplifier

The K factor method can be used for the type 3 amplifier in a similar way as it was used in the type 2 circuit. Using the K factor method, the zeros are placed at the same frequency to form a double zero, and the second and third poles are placed at the same frequency to form a double pole:

$$\begin{aligned} \omega_z &= \omega_{z_1} = \omega_{z_2} \\ \omega_p &= \omega_{p_2} = \omega_{p_3} \end{aligned} \quad (7-94)$$

The first pole remains at the origin.

The double zeros and poles are placed at frequencies

$$\begin{aligned}\omega_z &= \frac{\omega_{co}}{\sqrt{K}} \\ \omega_p &= \omega_{co}\sqrt{K}\end{aligned}\quad (7-95)$$

The amplifier transfer function from Eq. (7-91) can then be written as

$$G(j\omega) = -\frac{1}{R_3C_2} \frac{(j\omega + \omega_z)^2}{j\omega(j\omega + \omega_p)^2} \quad (7-96)$$

At the crossover frequency ω_{co} , the gain is

$$G(j\omega_{co}) = -\frac{1}{R_3C_2} \frac{(j\omega_{co} + \omega_z)^2}{j\omega_{co}(j\omega_{co} + \omega_p)^2} \quad (7-97)$$

The phase angle of the amplifier at the crossover frequency is then

$$\theta_{comp} = -270^\circ + 2\tan^{-1}\left(\frac{\omega_{co}}{\omega_z}\right) - 2\tan^{-1}\left(\frac{\omega_{co}}{\omega_p}\right) \quad (7-98)$$

Using Eq. (7-95) for ω_z and ω_p ,

$$\theta_{comp} = -270^\circ + 2\tan^{-1}\left(\frac{\omega_{co}}{\omega_{co}/\sqrt{K}}\right) - 2\tan^{-1}\left(\frac{\omega_{co}}{\omega_{co}\sqrt{K}}\right) \quad (7-99)$$

resulting in

$$\begin{aligned}\theta_{comp} &= -270^\circ + 2\tan^{-1}\sqrt{K} - 2\tan^{-1}\left(\frac{1}{\sqrt{K}}\right) \\ &= -270^\circ + 2\left[\tan^{-1}\sqrt{K} - \tan^{-1}\left(\frac{1}{\sqrt{K}}\right)\right]\end{aligned}\quad (7-100)$$

By using the identity

$$\tan^{-1}(x) + \tan^{-1}\left(\frac{1}{x}\right) = 90^\circ \quad (7-101)$$

making

$$\tan^{-1}\left(\frac{1}{\sqrt{K}}\right) = 90^\circ - \tan^{-1}(\sqrt{K}) \quad (7-102)$$

Eq. (7-100) becomes

$$\begin{aligned}\theta_{comp} &= -270^\circ + 2[\tan^{-1}\sqrt{K} + (-90^\circ - \tan^{-1}\sqrt{K})] \\ \theta_{comp} &= -450^\circ + 4\tan^{-1}\sqrt{K} = -90^\circ + 4\tan^{-1}\sqrt{K}\end{aligned}\quad (7-103)$$

Solving for K ,

$$K = \tan\left(\frac{\theta_{\text{comp}} + 90^\circ}{4}\right)^2 \quad (7-104)$$

From Eq. (7-103), the maximum angle of the compensated error amplifier is 270° . Recall that the maximum phase angle of the type 2 amplifier is 180° .

The phase angle of the compensated error amplifier is

$$\theta_{\text{comp}} = \theta_{\text{phase margin}} - \theta_{\text{converter}} \quad (7-105)$$

The minimum phase margin is usually 45° , and the phase angle of the converter at the desired crossover frequency can be determined from a PSpice simulation.

At the crossover frequency ω_{co} ,

$$\begin{aligned} G(j\omega_{\text{co}}) &= -\frac{1}{R_3C_2} \frac{(j\omega_{\text{co}} + \omega_z)^2}{j\omega_{\text{co}}(j\omega_{\text{co}} + \omega_p)^2} \\ &\approx -\frac{1}{R_3C_2} \frac{(j\omega_{\text{co}})^2}{j\omega_{\text{co}}(\omega_p)^2} = -\frac{1}{R_3C_2} \frac{j\omega_{\text{co}}}{(\omega_p)^2} \end{aligned} \quad (7-106)$$

Using Eqs. (7-95) and (7-92),

$$\omega_{\text{co}} = \sqrt{K}\omega_z = \frac{\sqrt{K}}{R_1C_3} \quad (7-107)$$

$$\omega_p = \frac{1}{R_2C_2} = \frac{1}{R_3C_3} \Rightarrow \omega_p^2 = \frac{1}{R_2C_2R_3C_3} \quad (7-108)$$

Equation (7-106) becomes

$$G(j\omega_{\text{co}}) = -\frac{1}{R_3C_2} \frac{j\omega_{\text{co}}}{(\omega_p)^2} = -\frac{1}{R_3C_2} \frac{j\sqrt{K}/R_1C_3}{1/R_2C_2R_3C_3} = -\frac{j\sqrt{K}R_2}{R_1} \quad (7-109)$$

In the design of a type 3 compensated error amplifier, first choose R_1 and then compute R_2 from Eq. (7-109). Other component values can then be determined from

$$\omega_z = \frac{\omega_{\text{co}}}{\sqrt{K}} = \frac{1}{R_2C_1} = \frac{1}{R_1C_3} \quad (7-110)$$

$$\text{and } \omega_p = \omega_{\text{co}}\sqrt{K} = \frac{1}{R_2C_2} = \frac{1}{R_3C_3} \quad (7-111)$$

The resulting equations are

$$\begin{aligned}
 R_2 &= \frac{|G(j\omega_{co})|R_1}{\sqrt{K}} \\
 C_1 &= \frac{\sqrt{K}}{\omega_{co}R_2} = \frac{\sqrt{K}}{2\pi f_{co}R_2} \\
 C_2 &= \frac{1}{\omega_{co}R_2\sqrt{K}} = \frac{1}{2\pi f_{co}R_2\sqrt{K}} \\
 C_3 &= \frac{\sqrt{K}}{\omega_{co}R_1} = \frac{\sqrt{K}}{2\pi f_{co}R_1} \\
 R_3 &= \frac{1}{\omega_{co}\sqrt{K}C_3} = \frac{1}{2\pi f_{co}\sqrt{K}C_3}
 \end{aligned} \tag{7-112}$$

EXAMPLE 7-10

Design of a Type 3 Compensated Error Amplifier

For the buck converter shown in Fig. 7-29a,

$$V_s = 10 \text{ V} \quad \text{with an output of } 5 \text{ V}$$

$$f = 100 \text{ kHz}$$

$$L = 100 \mu\text{H} \quad \text{with a series resistance of } 0.1 \Omega$$

$$C = 100 \mu\text{F} \quad \text{with an equivalent series resistance of } 0.1 \Omega$$

$$R = 5 \Omega$$

$$V_p = 3 \text{ V} \quad \text{in PWM circuit}$$

Design a type 3 compensated error amplifier that results in a stable control system. Design for a crossover frequency of 10 kHz and a phase margin of 45°. Note that all parameters are the same as in Example 7-8 except that the ESR of the capacitor is much smaller.

Solution

A PSpice ac frequency sweep shows that the output voltage is -10.5 dB at 10 kHz and the phase angle is -144°. The PWM circuit produces an additional gain of -9.5 dB. Therefore, the compensating error amplifier must have a gain of $10.5 + 9.5 = 20$ dB at 10 kHz. A gain of 20 dB corresponds to a gain of 10.

The required phase angle of the amplifier is determined from Eq. (7-105),

$$\theta_{\text{comp}} = \theta_{\text{phase margin}} - \theta_{\text{converter}} = 45^\circ - (-144^\circ) = 189^\circ$$

Solving for K in Eq. (7-104) yields.

$$K = \left[\tan\left(\frac{189^\circ + 90^\circ}{4}\right) \right]^2 = [\tan(69.75^\circ)]^2 = 7.35$$

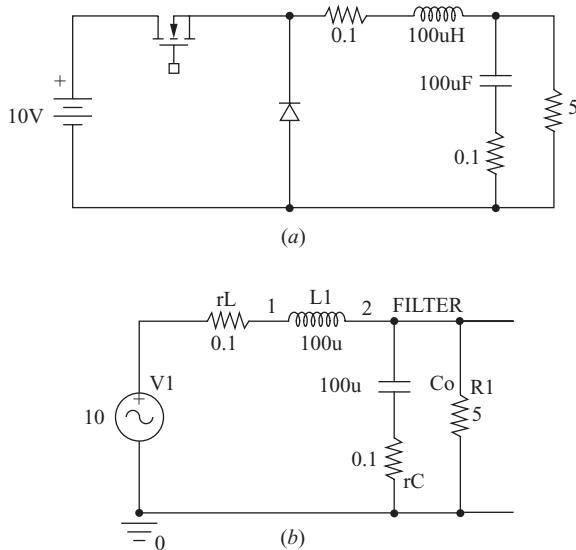


Figure 7-29 (a) Buck converter circuit; (b) The ac circuit used to determine the frequency response.

Letting $R_1 = 1 \text{ k}\Omega$, the other component values are computed from Eq. (7-112).

$$R_2 = \frac{|G(j\omega_{co})|R_1}{\sqrt{K}} = \frac{10(1000)}{\sqrt{7.35}} = 3.7 \text{ k}\Omega$$

$$C_1 = \frac{\sqrt{K}}{2\pi f_{co} R_2} = \frac{\sqrt{7.35}}{2\pi(10,000)(3700)} = 11.6 \text{ nF}$$

$$C_2 = \frac{1}{2\pi f_{co} R_2 \sqrt{K}} = \frac{1}{2\pi(10,000)(3700)\sqrt{7.35}} = 1.58 \text{ nF}$$

$$C_3 = \frac{\sqrt{K}}{2\pi f_{co} R_1} = \frac{\sqrt{7.35}}{2\pi(10,000)(1000)} = 43.1 \text{ nF}$$

$$R_3 = \frac{1}{2\pi f_{co} \sqrt{K} C_3} = \frac{1}{2\pi(10,000)\sqrt{7.35}(43.1)(10)^{-9}} = 136 \Omega$$

A PSpice simulation of the converter, compensated error amplifier, and PWM circuit gives a crossover frequency of 10 kHz with a phase margin of 49°.

Note that attempting to use a type 2 compensated error amplifier for this circuit is unsuccessful because the required phase angle at the crossover frequency is greater than 180°. Comparing this converter with that of Example 7-8, the ESR of the capacitor here is smaller. Low capacitor ESR values often necessitate use of the type 3 rather than the type 2 circuit.

Table 7-1 Type 3 Compensating error amplifier zeros and poles and frequency placement

Zero or Pole	Expression	Placement
First zero	$\omega_{z_1} = \frac{1}{R_2 C_2}$	50% to 100% of ω_{LC}
Second zero	$\omega_{z_2} = \frac{1}{(R_1 + R_3)C_3} \approx \frac{1}{R_1 C_3}$	At ω_{LC}
First pole	$\omega_{p_1} = 0$	—
Second pole	$\omega_{p_2} = \frac{C_1 + C_2}{R_2 C_1 C_2} \approx \frac{1}{R_2 C_2}$	At the ESR zero = $1/r_C C$
Third pole	$\omega_{p_3} = \frac{1}{R_3 C_3}$	At one-half the switching frequency, $2\pi f_{sw}/2$

Manual Placement of Poles and Zeros in the Type 3 Amplifier

As an alternative to the K factor method described previously, some designers place the poles and zeros of the type 3 amplifier at specified frequencies. In placing the poles and zeros, a frequency of particular interest is the resonant frequency of the LC filter in the converter. Neglecting any resistance in the inductor and capacitor,

$$\omega_{LC} = \frac{1}{\sqrt{LC}} \quad f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad (7-113)$$

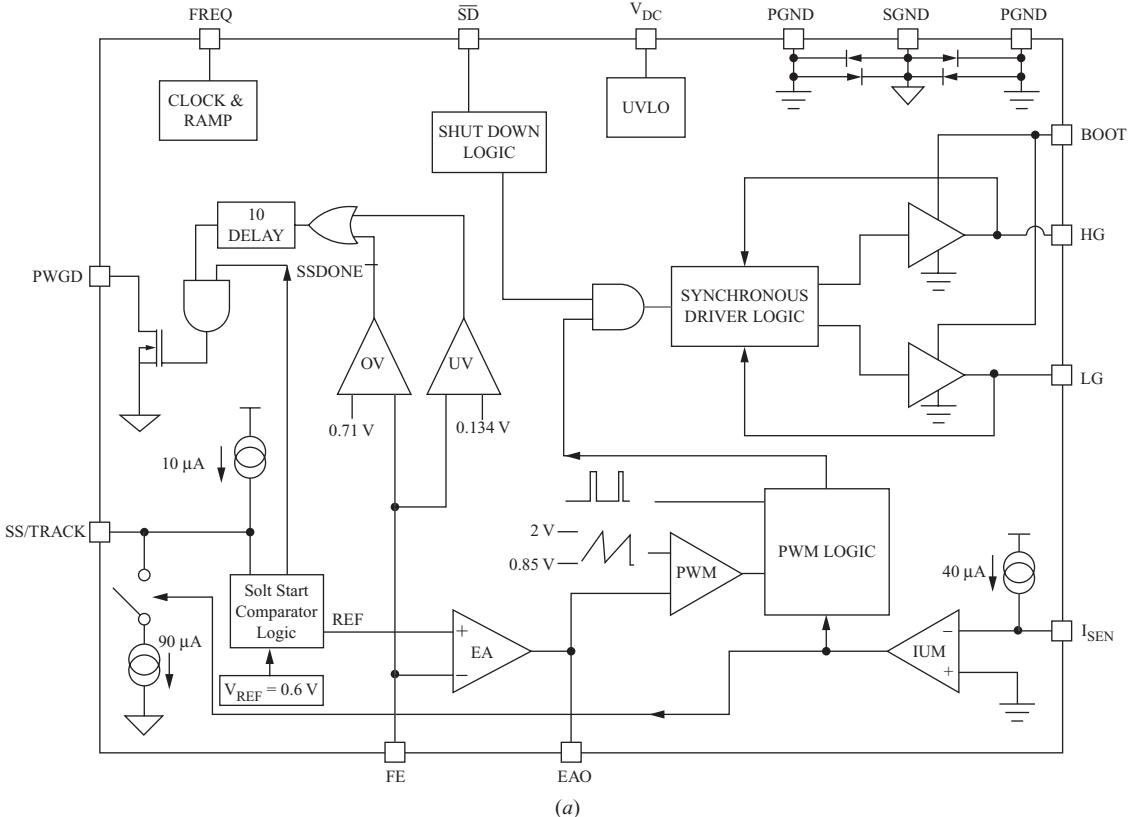
The first zero is commonly placed at 50 to 100 percent of f_{LC} , the second zero is placed at f_{LC} , the second pole is placed at the ESR zero in the filter transfer function ($1/r_C C$), and the third pole is placed at one-half the switching frequency. Table 7-1 indicates placement of the type 3 error amplifier poles and zeros.

7.14 PWM CONTROL CIRCUITS

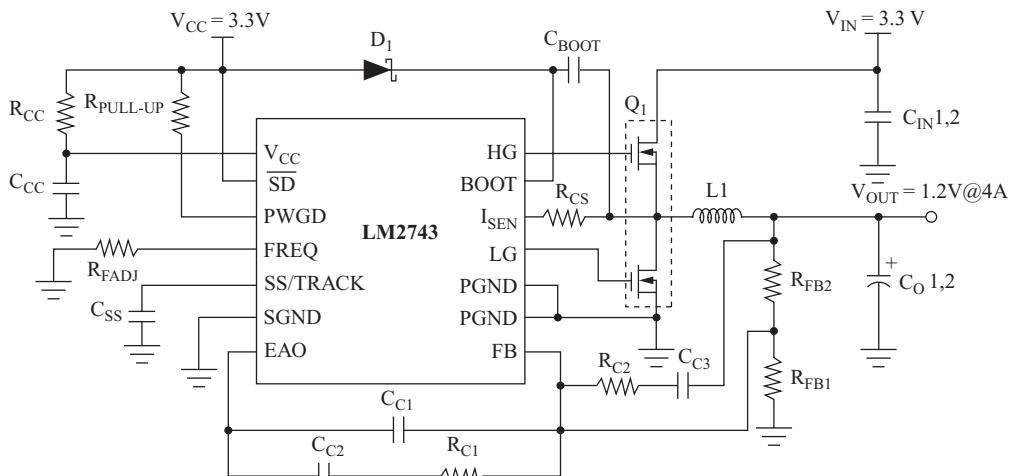
The major elements of the feedback control of dc power supplies are available in a single integrated circuit (IC). The National Semiconductor LM2743 is one example of an integrated circuit for dc power supply control. The IC contains the error amplifier op-amp, PWM circuit, and driver circuits for the MOSFETs in a dc-dc converter using synchronous rectification. The block diagram of the IC is shown in Fig. 7-30a, and a typical application is shown in Fig. 7-30b.

7.15 THE AC LINE FILTER

In many dc power supply applications, the power source is the ac power system. The voltage and current from the ac system are often contaminated by high-frequency electrical noise. An ac line filter suppresses conductive radio-frequency interference (RFI) noise from entering or leaving the power supply.



(a)



(b)

Figure 7-30 (a) The National Semiconductor LM2743 block diagram; (b) An application in a buck converter circuit (with permission from National Semiconductor Corporation¹).

¹Copyright © 2003 National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, CA 95051. All rights reserved, <http://www.national.com>.

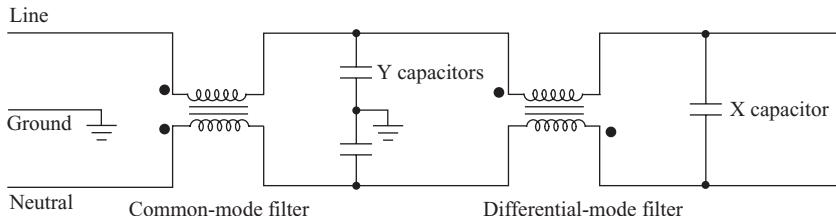


Figure 7-31 A typical ac line filter.

A single-phase ac input to a power supply has a line (or phase) wire, a neutral wire, and a ground wire. Common-mode noise consists of currents in the line and neutral conductors that are in phase and return through the ground path. Differential-mode noise consists of high-frequency currents that are 180° out of phase in the line and neutral conductors, which means that current enters from the line and returns in the neutral.

A typical ac line filter circuit is shown in Fig. 7-31. The first stage is a common-mode filter, consisting of a transformer with adjacent polarity markings and a capacitor connected from each line to ground. The capacitors in this stage are referred to as the *Y capacitors*. The second stage of the filter, consisting of a transformer with opposite polarity markings and a single capacitor connected across the ac lines, removes differential-mode noise from the ac signal. The capacitor in this stage is referred to as the *X capacitor*.

7.16 THE COMPLETE DC POWER SUPPLY

A complete dc power supply consists of an input ac line filter, a power factor correction stage, and a dc-dc converter, as illustrated in the block diagram of Fig. 7-32. The power factor correction stage is discussed in Sec. 7.11, and the dc-dc converter could be any of the converters discussed in this chapter or in Chap. 6.

Low-power applications such as cell phone chargers can be implemented with a topology like that shown in Fig. 7-33. A full-wave rectifier with a capacitor filter (Chap. 4) produces a dc voltage from the ac line voltage source, and a flyback dc-dc converter reduces the dc voltage to the appropriate level for the application. An optically coupled feedback loop preserves electrical isolation between the source and the load, and a control circuit adjusts the duty ratio of the switch for a regulated output. Integrated-circuit packages include the control

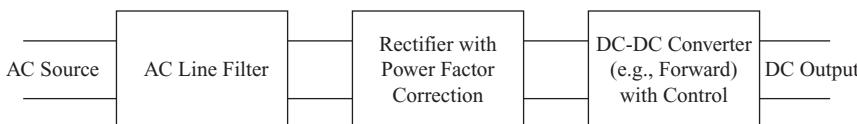


Figure 7-32 A complete power supply when the source is the ac power system.

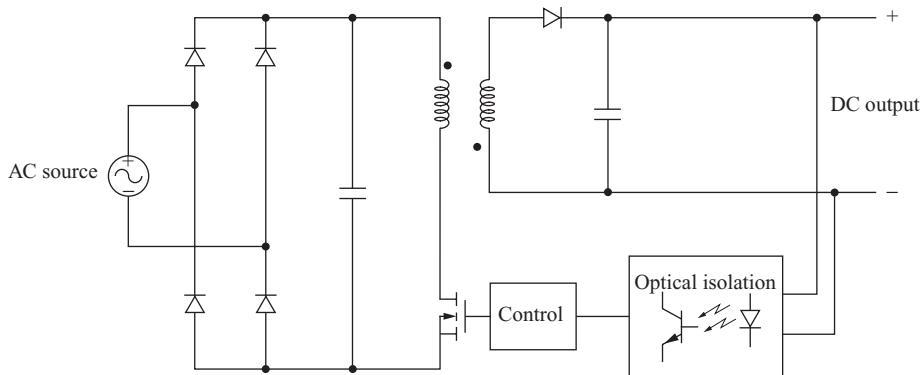


Figure 7-33 An off-line power supply for low-power applications.

function and the switching transistor. Some such integrated circuits can be powered directly from the high-voltage output of the rectifier, and others require another winding on the flyback converter to produce the IC supply voltage. This type of power supply is often called an off-line converter.

7.17 Bibliography

- S. Ang and A. Oliva, *Power-Switching Converters*, 2d ed., Taylor & Francis, Boca Raton, Fla., 2005.
- C. Basso, *Switch-Mode Power Supplies*, McGraw-Hill, New York, 2008.
- B. K. Bose, *Power Electronics and Motor Drives: Advances and Trends*, Elsevier/Academic Press, Boston, 2006.
- M. Day, “Optimizing Low-Power DC/DC Designs—External versus Internal Compensation,” Texas Instruments, Incorporated, 2004.
- R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2d ed., Kluwer Academic, 2001.
- A. J. Forsyth and S. V. Mollov, “Modeling and Control of DC-DC converters,” *Power Engineering Journal*, vol. 12, no. 5, 1998, pp. 229–236.
- Y. M. Lai, *Power Electronics Handbook*, edited by M. H. Rashid, Academic Press, Calif., San Diego, 2001, Chapter 20.
- LM2743 Low Voltage N-Channel MOSFET Synchronous Buck Regulator Controller, National Semiconductor, 2005.
- D. Mattingly, “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators,” Intersil Technical Brief TB417.1, Milpitas, Calif., 2003.
- N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3d ed., Wiley, New York, 2003.
- G. Moschopoulos and P. Jain, “Single-Phase Single-Stage Power-Factor-Corrected Converter Topologies,” *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, February 2005, pp. 23–35.
- M. Nave, *Power Line Filter Design for Switched-Mode Power Supplies*, Van Nostrand Reinhold, Princeton, N.J., 1991.
- A. I. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design*, McGraw-Hill, New York, 2009.

- M. H. Rashid, *Power Electronics: Circuits, Devices, and Systems*, 3d ed., Prentice-Hall, Upper Saddle River, N.J., 2004.
- M. Qiao, P. Parto, and R. Amirani, "Stabilize the Buck Converter with Transconductance Amplifier," International Rectifier Application Note AN-1043, 2002.
- D. Venable, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," *Proceedings Powercon 10*, 1983.
- V. Vorperian, "Simplified Analysis of PWM Converters Using Model of PWM Switch," *IEEE Transactions on Aerospace and Electronic Systems*, May 1990.
- "8-Pin Synchronous PWM Controller," International Rectifier Data Sheet No. PD94173 revD, 2005.

Problems

Flyback Converter

- 7.1** The flyback converter of Fig. 7-2 has parameters $V_s = 36$ V, $D = 0.4$, $N_1/N_2 = 2$, $R = 20 \Omega$, $L_m = 100 \mu\text{H}$, and $C = 50 \mu\text{F}$, and the switching frequency is 100 kHz. Determine (a) the output voltage; (b) the average, maximum, and minimum inductor currents; and (c) the output voltage ripple.
- 7.2** The flyback converter of Fig. 7-2 has parameters $V_s = 4.5$ V, $D = 0.6$, $N_1/N_2 = 0.4$, $R = 15 \Omega$, $L_m = 10 \mu\text{H}$, and $C = 10 \mu\text{F}$, and the switching frequency is 250 kHz. Determine (a) the output voltage; (b) the average, maximum, and minimum inductor currents; and (c) the output voltage ripple.
- 7.3** The flyback converter of Fig. 7-2 has an input of 44 V, an output of 3 V, a duty ratio of 0.32, and a switching frequency of 300 kHz. The load resistor is 1 Ω .
 (a) Determine the transformer turns ratio. (b) Determine the transformer magnetizing inductance L_m such that the minimum inductor current is 40 percent of the average.
- 7.4** Design a flyback converter for an input of 24 V and an output of 40 W at 40 V. Specify the transformer turns ratio and magnetizing inductance, switching frequency, and capacitor to limit the ripple to less than 0.5 percent.
- 7.5** (a) What is the value of load resistance that separates continuous and discontinuous magnetizing inductance current in the flyback converter of Example 7-1? (b) Graph V_o/V_s as the load changes from 5 to 20 Ω .
- 7.6** For the flyback converter operating in the discontinuous-current mode, derive an expression for the time at which the magnetizing current i_{L_m} returns to zero.

Forward Converter

- 7.7** The forward converter of Fig. 7-5a has parameters $V_s = 100$ V, $N_1/N_2 = N_1/N_3 = 1$, $L_m = 1 \text{ mH}$, $L_x = 70 \mu\text{H}$, $R = 20 \Omega$, $C = 33 \mu\text{F}$, and $D = 0.35$, and the switching frequency is 150 kHz. Determine (a) the output voltage and output voltage ripple; (b) the average, maximum, and minimum values of the current in L_x ; (c) the peak current in L_m in the transformer model; and (d) the peak current in the switch and the physical transformer primary.
- 7.8** The forward converter of Fig. 7-5a has parameters $V_s = 170$ V, $N_1/N_2 = 10$, $N_1/N_3 = 1$, $L_m = 340 \mu\text{H}$, $L_x = 20 \mu\text{H}$, $R = 10 \Omega$, $C = 10 \mu\text{F}$, $D = 0.3$, and the switching frequency is 500 kHz. (a) Determine the output voltage and output voltage ripple. (b) Sketch the currents in L_x , L_m , each transformer winding, and V_s .

- (c) Determine the power returned to the source by the tertiary (third) transformer winding from the recovered stored energy in L_m .
- 7.9** A forward converter has a source of 80 V and a load of 250 W at 50 V. The output filter has $L_x = 100 \mu\text{H}$ and $C = 150 \mu\text{F}$. The switching frequency is 100 kHz.
- (a) Select a duty ratio and transformer turns ratios N_1/N_2 and N_1/N_3 to provide the required output voltage. Verify continuous current in L_x . (b) Determine the output voltage ripple.
- 7.10** The forward converter of Fig. 7-5a has parameters $V_s = 100 \text{ V}$, $N_1/N_2 = 5$, $N_1/N_3 = 1$, $L_m = 333 \mu\text{H}$, $R = 2.5 \Omega$, $C = 10 \mu\text{F}$, and $D = 0.25$, and the switching frequency is 375 kHz. (a) Determine the output voltage and output voltage ripple. (b) Sketch the currents i_{L_x} , I_1 , i_2 , i_3 , i_{L_m} , and i_s . Determine the power returned to the source by the tertiary (third) transformer winding from the recovery storage energy in L_m .
- 7.11** A forward converter has parameters $V_s = 125 \text{ V}$, $V_o = 50 \text{ V}$, and $R = 25 \Omega$, and the switching frequency is 250 kHz. Determine (a) the transformer turns ratio N_1/N_2 such that the duty ratio is 0.3, (b) the inductance L_x such that the minimum current in L_x is 40 percent of the average current, and (c) the capacitance required to limit the output ripple voltage to 0.5 percent.
- 7.12** Design a forward converter to meet these specifications: $V_s = 170 \text{ V}$, $V_o = 48 \text{ V}$, output power-150 W, and the output voltage ripple must be less than 1 percent. Specify the transformer turns ratios, the duty ratio of the switch, the switching frequency, the value of L_x to provide continuous current, and the output capacitance.
- 7.13** Design a forward converter to produce an output voltage of 30 V when the input dc voltage is unregulated and varies from 150 to 175 V. The output power varies from 20 to 50 W. The duty ratio of the switch is varied to compensate for the fluctuations in the source to regulate the output at 30 V. Specify the switching frequency and range of required duty ratio of the switch, the turns ratios of the transformer, the value of L_x , and the capacitance required to limit the output ripple to less than 0.2 percent. Your design must work for all operating conditions.
- 7.14** The current waveforms in Fig. 7-6 for the forward converter show the transformer currents based on the transformer model of Fig. 7-1d. Sketch the currents that exist in the three windings of the physical three-winding transformer. Assume that $N_1/N_2 = N_1/N_3 = 1$.

Push-Pull Converter

- 7.15** The push-pull converter of Fig. 7-8a has the following parameters: $V_s = 50 \text{ V}$, $N_p/N_s = 2$, $L_x = 60 \mu\text{H}$, $C = 39 \mu\text{F}$, $R = 8 \Omega$, $f = 150 \text{ kHz}$, and $D = 0.35$. Determine (a) the output voltage, (b) the maximum and minimum inductor currents, and (c) the output voltage ripple.
- 7.16** For the push-pull converter in Prob. 7-12, sketch the current in L_x , D_1 , D_2 , Sw_1 , Sw_2 , and the source.
- 7.17** The push-pull converter of Fig. 7-8a has a transformer with a magnetizing inductance $L_m = 2 \text{ mH}$ which is placed across winding P_1 in the model. Sketch the current in L_m for the circuit parameters given in Prob. 7-11.
- 7.18** For the push-pull converter of Fig. 7-8a, (a) sketch the voltage waveform v_{L_x} and (b) derive the expression for output voltage [Eq. (7-44)] on the basis that the average inductor voltage is zero.

Current-Fed Converter

- 7.19** The current-fed converter of Fig. 7-11a has an input voltage of 24 V and a turns ratio $N_p/N_s = 2$. The load resistance is 10Ω , and the duty ratio of each switch is 0.65. Determine the output voltage and the input current. Assume that the input inductor is very large. Determine the maximum voltage across each switch.
- 7.20** The current-fed converter of Fig. 7-11a has an input voltage of 30 V and supplies a load of 40 W at 50 V. Specify a transformer turns ratio and a switch duty ratio. Determine the average current in the inductor.
- 7.21** The output voltage for the current-fed converter of Fig. 7-11a was derived on the basis of the average inductor voltage being zero. Derive the output voltage [Eq. (7-56)] on the basis that the power supplied by the source must equal the power absorbed by the load for an ideal converter.

PSpice

- 7.22** Run a PSpice simulation for the flyback converter in Example 7-2. Use the voltage-controlled switch Sbreak with $R_{on} = 0.2 \Omega$, and use the default diode model Dbreak. Display the output for voltage for steady-state conditions. Compare output voltage and output voltage ripple to the results from Example 7-2. Display the transformer primary and secondary current, and determine the average value of each. Comment on the results.
- 7.23** Run a PSpice simulation for the forward converter of Example 7-4. Use the voltage-controlled switch Sbreak with $R_{on} = 0.2 \Omega$ and use the default diode model Dbreak. Let the capacitance be $20 \mu\text{F}$. Display the steady-state currents in L_x and each of the transformer windings. Comment on the results.

Control

- 7.24** Design a type 2 compensated error amplifier (Fig. 7-23a) that will give a phase angle at crossover $\theta_{co} = -210^\circ$ and a gain of 20 dB for a crossover frequency of 12 kHz.
- 7.25** A buck converter has a filter transfer function that has a magnitude of -15 dB and phase angle of -105° at 5 kHz. The gain of the PWM circuit is -9.5 dB . Design a type 2 compensated error amplifier (Fig. 7-23a) that will give a phase margin of at least 45° for a crossover frequency of 5 kHz.
- 7.26** A buck converter has $L = 50 \mu\text{H}$, $C = 20 \mu\text{F}$, $r_c = 0.5 \Omega$, and a load resistance $R = 4 \Omega$. The PWM converter has $V_p = 3 \text{ V}$. A type 2 error amplifier has $R_1 = 1 \text{ k}\Omega$, $R_2 = 5.3 \text{ k}\Omega$, $C_1 = 11.4 \text{ nF}$, and $C_2 = 1.26 \text{ nF}$. Use PSpice to determine the phase margin of the control loop (as in Example 7-8) and comment on the stability. Run a PSpice control loop simulation as in Example 7-10.
- 7.27** A buck converter has $L = 200 \mu\text{H}$ with a series resistance $r_L = 0.2 \Omega$, $C = 100 \mu\text{F}$ with $r_c = 0.5 \Omega$, and a load $R = 4 \Omega$. The PWM converter has $V_p = 3 \text{ V}$. (a) Use PSpice to determine the magnitude and phase angle of the filter and load at 10 kHz. (b) Design a type 2 compensated error amplifier (Fig. 7-23a) that will give a phase margin of at least 45° at a crossover frequency of 10 kHz. Verify your results with a PSpice simulation of a step change in load resistance from 4 to 2Ω as in Example 7-10. Let $V_s = 20 \text{ V}$ and $V_{ref} = 8 \text{ V}$.

- 7.28** A buck converter has $L = 200 \mu\text{H}$ with a series resistance $r_L = 0.1 \Omega$, $C = 200 \mu\text{F}$ with $r_c = 0.4 \Omega$, and a load $R = 5 \Omega$. The PWM converter has $V_p = 3 \text{ V}$. (a) Use PSpice to determine the magnitude and phase angle of the filter and load at 8 kHz. (b) Design a type 2 compensated error amplifier (Fig. 7-23a) that will give a phase margin of at least 45° at a crossover frequency of 10 kHz. Verify your results with a PSpice simulation of a step change in load resistance as in Fig. 7-27. Let $V_s = 20 \text{ V}$ and $V_{\text{ref}} = 8 \text{ V}$.
- 7.29** For the type 3 compensated error amplifier of Fig. 7-28a, determine the K factor for an error amplifier phase angle of 195° . For a gain of 15 dB at a crossover frequency of 15 kHz, determine the resistance and capacitance values for the amplifier.
- 7.30** The frequency response of a buck converter shows that the output voltage is -8 dB , and the phase angle is -140° at 15 kHz. The ramp function in the PWM control circuit has a peak value of 3 V. Use the K factor method to determine values of the resistors and capacitors for the type 3 error amplifier of Fig. 7-28a for a crossover frequency of 15 kHz.
- 7.31** The buck converter circuit of Fig. 7-29 has $L = 40 \mu\text{H}$, $r_L = 0.1 \Omega$, $C_o = 500 \mu\text{F}$, $r_C = 30 \text{ m}\Omega$, and $R_L = 3 \Omega$. The ramp function in the PWM control circuit has a peak value of 3 V. Use the K factor method to design a type 3 compensated error amplifier for a stable control system with a crossover frequency of 10 kHz. Specify the resistor and capacitor values in the error amplifier.

8

CHAPTER

Inverters

Converting dc to ac

8.1 INTRODUCTION

Inverters are circuits that convert dc to ac. More precisely, inverters transfer power from a dc source to an ac load. The controlled full-wave bridge converters in Chap. 4 can function as inverters in some instances, but an ac source must pre-exist in those cases. In other applications, the objective is to create an ac voltage when only a dc voltage source is available. The focus of this chapter is on inverters that produce an ac output from a dc input. Inverters are used in applications such as adjustable-speed ac motor drives, uninterruptible power supplies (UPS), and running ac appliances from an automobile battery.

8.2 THE FULL-BRIDGE CONVERTER

The full-bridge converter of Fig 8-1a is the basic circuit used to convert dc to ac. The full-bridge converter was introduced as part of a dc power supply circuit in Chap. 7. In this application, an ac output is synthesized from a dc input by closing and opening the switches in an appropriate sequence. The output voltage v_o can be $+V_{dc}$, $-V_{dc}$, or zero, depending on which switches are closed. Figure 8-1b to e shows the equivalent circuits for switch combinations.

Switches Closed	Output Voltage v_o
S_1 and S_2	$+V_{dc}$
S_3 and S_4	$-V_{dc}$
S_1 and S_3	0
S_2 and S_4	0

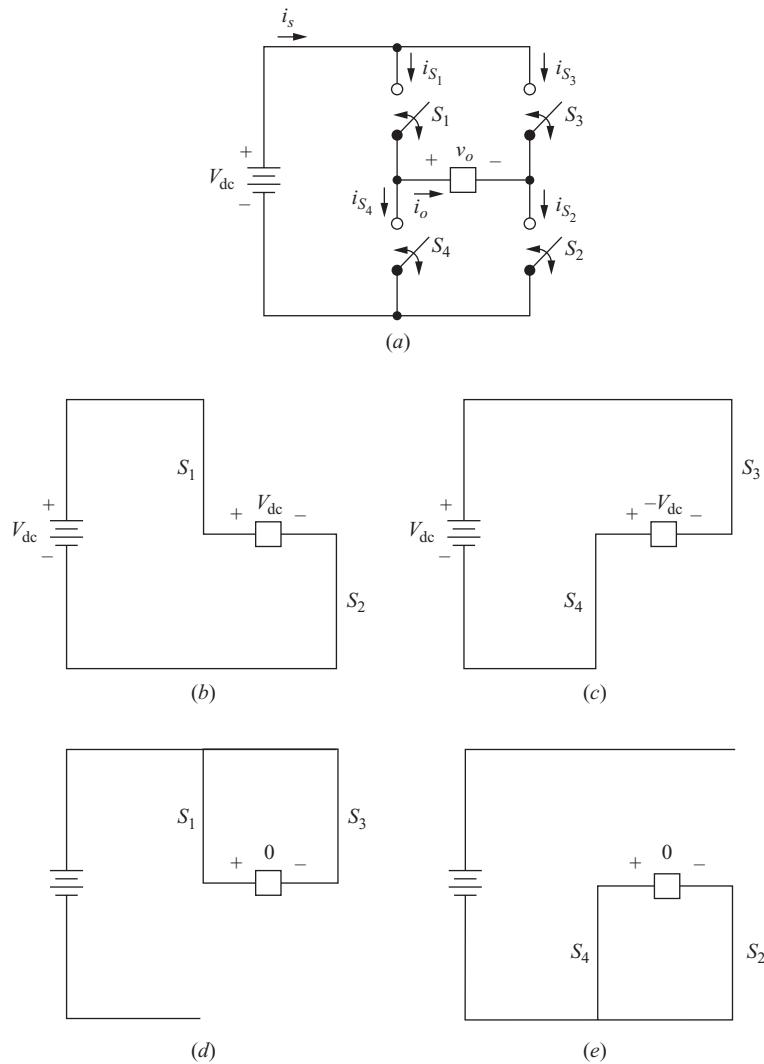


Figure 8-1 (a) Full-bridge converter; (b) S_1 and S_2 closed; (c) S_3 and S_4 closed; (d) S_1 and S_3 closed; (e) S_2 and S_4 closed.

Note that S_1 and S_4 should not be closed at the same time, nor should S_2 and S_3 . Otherwise, a short circuit would exist across the dc source. Real switches do not turn on or off instantaneously, as was discussed in Chap. 6. Therefore, switching transition times must be accommodated in the control of the switches. Overlap of switch “on” times will result in a short circuit, sometimes called a *shoot-through* fault, across the dc voltage source. The time allowed for switching is called *blanking* time.

8.3 THE SQUARE-WAVE INVERTER

The simplest switching scheme for the full-bridge converter produces a square wave output voltage. The switches connect the load to $+V_{dc}$ when S_1 and S_2 are closed or to $-V_{dc}$ when S_3 and S_4 are closed. The periodic switching of the load voltage between $+V_{dc}$ and $-V_{dc}$ produces a square wave voltage across the load. Although this alternating output is nonsinusoidal, it may be an adequate ac waveform for some applications.

The current waveform in the load depends on the load components. For the resistive load, the current waveform matches the shape of the output voltage. An inductive load will have a current that has more of a sinusoidal quality than the voltage because of the filtering property of the inductance. An inductive load presents some considerations in designing the switches in the full-bridge circuit because the switch currents must be bidirectional.

For a series RL load and a square wave output voltage, assume switches S_1 and S_2 in Fig. 8-1a close at $t = 0$. The voltage across the load is $+V_{dc}$, and current begins to increase in the load and in S_1 and S_2 . The current is expressed as the sum of the forced and natural responses

$$\begin{aligned} i_o(t) &= i_f(t) + i_n(t) \\ &= \frac{V_{dc}}{R} + Ae^{-t/\tau} \quad \text{for } 0 \leq t \leq T/2 \end{aligned} \tag{8-1}$$

where A is a constant evaluated from the initial condition and $\tau = L/R$.

At $t = T/2$, S_1 and S_2 open, and S_3 and S_4 close. The voltage across the RL load becomes $-V_{dc}$, and the current has the form

$$i_o(t) = \frac{-V_{dc}}{R} + Be^{-(t-T/2)/\tau} \quad \text{for } T/2 \leq t \leq T \tag{8-2}$$

where the constant B is evaluated from the initial condition.

When the circuit is first energized and the initial inductor current is zero, a transient occurs before the load current reaches a steady-state condition. At steady state, i_o is periodic and symmetric about zero, as illustrated in Fig. 8-2. Let the initial condition for the current described in Eq. (8-1) be I_{min} , and let the initial condition for the current described in Eq. (8-2) be I_{max} .

Evaluating Eq. (8-1) at $t = 0$,

$$i_o(0) = \frac{V_{dc}}{R} + Ae^0 = I_{min}$$

or

$$A = I_{min} - \frac{V_{dc}}{R} \tag{8-3}$$

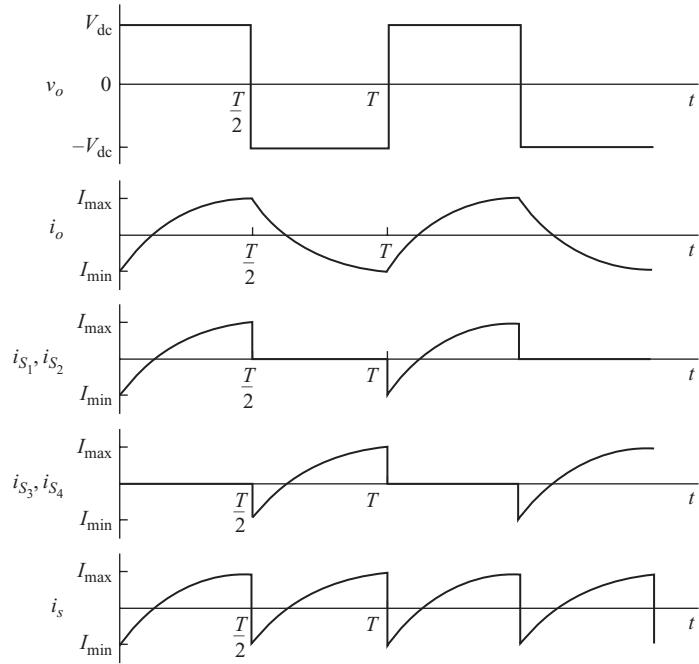


Figure 8-2 Square wave output voltage and steady-state current waveform for an RL load.

Likewise, Eq. (8-2) is evaluated at $t = T/2$.

$$i_o(T/2) = \frac{-V_{dc}}{R} + Be^0 = I_{max}$$

or

$$B = I_{max} + \frac{V_{dc}}{R} \quad (8-4)$$

In steady state, the current waveforms described by Eqs. (8-1) and (8-2) then become

$$i_o(t) = \begin{cases} \frac{V_{dc}}{R} + \left(I_{min} - \frac{V_{dc}}{R} \right) e^{-t/\tau} & \text{for } 0 < t < \frac{T}{2} \\ \frac{-V_{dc}}{R} + \left(I_{max} + \frac{V_{dc}}{R} \right) - e^{(t-T/2)/\tau} & \text{for } \frac{T}{2} < t < T \end{cases} \quad (8-5)$$

An expression is obtained for I_{\max} by evaluating the first part of Eq. (8-5) at $t = T/2$

$$i(T/2) = I_{\max} = \frac{V_{dc}}{R} + \left(I_{\min} - \frac{V_{dc}}{R} \right) e^{-(T/2\tau)} \quad (8-6)$$

and by symmetry,

$$I_{\min} = -I_{\max} \quad (8-7)$$

Substituting $-I_{\max}$ for I_{\min} in Eq. (8-6) and solving for I_{\max} ,

$$I_{\max} = -I_{\min} = \frac{V_{dc}}{R} \left(\frac{1 - e^{-T/2\tau}}{1 + e^{-T/2\tau}} \right) \quad (8-8)$$

Thus, Eqs. (8-5) and (8-8) describe the current in an RL load in the steady state when a square wave voltage is applied. Figure 8-2 shows the resulting currents in the load, source, and switches.

Power absorbed by the load can be determined from $I_{\text{rms}}^2 R$, where rms load current is determined from the defining equation from Chap. 2. The integration may be simplified by taking advantage of the symmetry of the waveform. Since the square each of the current half-periods is identical, only the first half-period needs to be evaluated:

$$I_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^T i^2(t) dt} = \sqrt{\frac{2}{T} \int_0^{T/2} \left[\frac{V_{dc}}{R} + \left(I_{\min} - \frac{V_{dc}}{R} \right) e^{-t/\tau} \right]^2 dt} \quad (8-9)$$

If the switches are ideal, the power supplied by the source must be the same as absorbed by the load. Power from a dc source is determined from

$$P_{dc} = V_{dc} I_s \quad (8-10)$$

as was derived in Chap. 2.

EXAMPLE 8-1

Square-Wave Inverter with RL Load

The full-bridge inverter of Fig. 8-1 has a switching sequence that produces a square wave voltage across a series RL load. The switching frequency is 60 Hz, $V_{dc} = 100$ V, $R = 10 \Omega$, and $L = 25$ mH. Determine (a) an expression for load current, (b) the power absorbed by the load, and (c) the average current in the dc source.

■ Solution

(a) From the parameters given,

$$T = 1/f = 1/60 = 0.0167 \text{ s}$$

$$\tau = L/R = 0.025/10 = 0.0025 \text{ s}$$

$$T/2\tau = 3.33$$

Equation (8-8) is used to determine the maximum and minimum current.

$$I_{\max} = -I_{\min} = \frac{100}{10} \left(\frac{1 - e^{-3.33}}{1 + e^{-3.33}} \right) = 9.31 \text{ A}$$

Equation (8-5) is then evaluated to give load current.

$$\begin{aligned} i_o(t) &= \frac{100}{10} + \left(-9.31 - \frac{100}{10} \right) e^{-t/0.0025} \\ &= 10 - 19.31 e^{-t/0.0025} \quad 0 \leq t \leq \frac{1}{120} \\ i_o(t) &= -\frac{100}{10} + \left(9.31 + \frac{100}{10} \right) e^{-(t-0.0167/2)/0.0025} \\ &= -10 + 19.31 e^{-(t-0.00835)/0.0025} \quad \frac{1}{120} \leq t \leq \frac{1}{60} \end{aligned}$$

(b) Power is computed from $I_{\text{rms}}^2 R$, where I_{rms} is computed from Eq. (8-9).

$$I_{\text{rms}} = \sqrt{\frac{1}{120} \int_0^{1/120} [(10 - 19.31)e^{-t/0.0025}]^2 dt} = 6.64 \text{ A}$$

Power absorbed by the load is

$$P = I_{\text{rms}}^2 R = (6.64)^2 (10) = 441 \text{ W}$$

(c) Average source current can also be computed by equating source and load power, assuming a lossless converter. Using Eq. (8-10),

$$I_s = \frac{P_{\text{dc}}}{V_{\text{dc}}} = \frac{441}{100} = 4.41 \text{ A}$$

Average power could also be computed from the average of the current expression in part (a).

The switch currents in Fig. 8-2 show that the switches in the full-bridge circuit must be capable of carrying both positive and negative currents for RL loads. However, real electronic devices may conduct current in one direction only. This problem is solved by placing feedback diodes in parallel (anitparallel) with each switch. During the time interval when the current in the switch must be negative, the feedback diode carries the current. The diodes are reverse-biased when current is positive in the switch. Figure 8-3a shows the full-bridge inverter with switches implemented as insulated gate bipolar transistors (IGBTs) with feedback diodes. Transistor and diode currents for a square wave voltage and an RL load are indicated in Fig 8-3b. Power semiconductor modules often include feedback diodes with the switches.

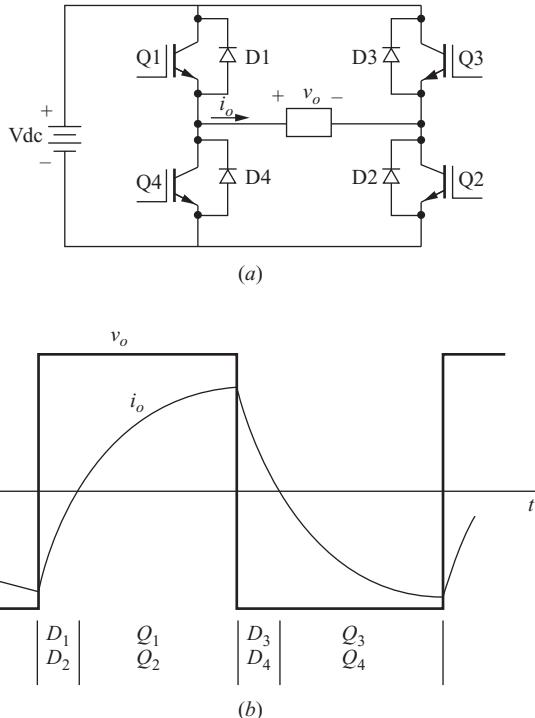


Figure 8-3 (a) Full-bridge inverter using IGBTs;
(b) Steady-state current for an *RL* load.

When IGBTs Q_1 and Q_2 are turned off in Fig. 8-3a, the load current must be continuous and will transfer to diodes D_3 and D_4 , making the output voltage $-V_{dc}$, effectively turning on the switch paths 3 and 4 before Q_3 and Q_4 are turned on. IGBTs Q_3 and Q_4 must be turned on before the load current decays to zero.

8.4 FOURIER SERIES ANALYSIS

The Fourier series method is often the most practical way to analyze load current and to compute power absorbed in a load, especially when the load is more complex than a simple resistive or *RL* load. A useful approach for inverter analysis is to express the output voltage and load current in terms of a Fourier series. With no dc component in the output,

$$v_o(t) = \sum_{n=1}^{\infty} V_n \sin(n\omega_0 t + \theta_n) \quad (8-11)$$

and

$$i_o(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega_0 t + \phi_n) \quad (8-12)$$

Power absorbed by a load with a series resistance is determined from $I_{\text{rms}}^2 R$, where the rms current can be determined from the rms currents at each of the components in the Fourier series by

$$I_{\text{rms}} = \sqrt{\sum_{n=1}^{\infty} I_{n,\text{rms}}^2} = \sqrt{\sum_{n=1}^{\infty} \left(\frac{I_n}{\sqrt{2}} \right)^2} \quad (8-13)$$

where

$$I_n = \frac{V_n}{Z_n} \quad (8-14)$$

and Z_n is the load impedance at harmonic n .

Equivalently, the power absorbed in the load resistor can be determined for each frequency in the Fourier series. Total power can be determined from

$$P = \sum_{n=1}^{\infty} P_n = \sum_{n=1}^{\infty} I_{n,\text{rms}}^2 R \quad (8-15)$$

where $I_{n,\text{rms}}$ is $I_n / \sqrt{2}$.

In the case of the square wave, the Fourier series contains the odd harmonics and can be represented as

$$v_o(t) = \sum_{n \text{ odd}} \frac{4V_{\text{dc}}}{n\pi} \sin n\omega_0 t \quad (8-16)$$

EXAMPLE 8-2

Fourier Series Solution for the Square-Wave Inverter

For the inverter in Example 8-1 ($V_{\text{dc}} = 100 \text{ V}$, $R = 10 \Omega$, $L = 25 \text{ mH}$, $f = 60 \text{ Hz}$), determine the amplitudes of the Fourier series terms for the square wave load voltage, the amplitudes of the Fourier series terms for load current, and the power absorbed by the load.

■ Solution

The load voltage is represented as the Fourier series in Eq. (8-16). The amplitude of each voltage term is

$$V_n = \frac{4V_{\text{dc}}}{n\pi} = \frac{4(400)}{n\pi}$$

The amplitude of each current term is determined from Eq. (8-14),

$$I_n = \frac{V_n}{Z_n} = \frac{V_n}{\sqrt{R^2 + (n\omega_0 L)^2}} = \frac{4(400)/n\pi}{\sqrt{10^2 + [n(2\pi 60)(0.025)]^2}}$$

Power at each frequency is determined from Eq. (8-15).

$$P_n = I_{n,\text{rms}}^2 R = \left(\frac{I_n}{\sqrt{2}} \right)^2 R$$

Table 8-1 Fourier Series Quantities for Example 8-2

<i>n</i>	<i>f_n</i> (Hz)	<i>V_n</i> (V)	<i>Z_n</i> (Ω)	<i>I_n</i> (A)	<i>P_n</i> (W)
1	60	127.3	13.7	9.27	429.3
3	180	42.4	30.0	1.42	10.0
5	300	25.5	48.2	0.53	1.40
7	420	18.2	66.7	0.27	0.37
9	540	14.1	85.4	0.17	0.14

Table 8-1 summarizes the Fourier series quantities for the circuit of Example 8-1. As the harmonic number *n* increases, the amplitude of the Fourier voltage component decreases and the magnitude of the corresponding impedance increases, both resulting in small currents for higher-order harmonics. Therefore, only the first few terms of the series are of practical interest. Note how the current and power terms become vanishingly small for all but the first few frequencies.

Power absorbed by the load is computed from Eq. (8-15).

$$P = \sum P_n = 429.3 + 10.0 + 1.40 + 0.37 + 0.14 + \dots \approx 441 \text{ W}$$

which agrees with the result in Example 8-1.

8.5 TOTAL HARMONIC DISTORTION

Since the objective of the inverter is to use a dc voltage source to supply a load requiring ac, it is useful to describe the quality of the ac output voltage or current. The quality of a nonsinusoidal wave can be expressed in terms of total harmonic distortion (THD), defined in Chap. 2. Assuming no dc component in the output,

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} (V_{n,\text{rms}})^2}}{V_{1,\text{rms}}} = \frac{\sqrt{V_{\text{rms}}^2 - V_{1,\text{rms}}^2}}{V_{1,\text{rms}}} \quad (8-17)$$

The THD of current is determined by substituting current for voltage in the above equation. The THD of load current is often of greater interest than that of output voltage. This definition for THD is based on the Fourier series, so there is some benefit in using the Fourier series method for analysis when the THD must be determined. Other measures of distortion such as distortion factor, as presented in Chap. 2, can also be applied to describe the output waveform for inverters.

EXAMPLE 8-3

THD for a Square-Wave Inverter

Determine the total harmonic distortion of the load voltage and the load current for the square-wave inverter in Examples 8-1 and 8-2.

■ Solution

Use the Fourier series for the square wave in Eq. (8-16) and the definition of THD in Eq. (8-17). The rms value of the square wave voltage is the same as the peak value, and the fundamental frequency component is the first term in Eq. (8-16),

$$V_{\text{rms}} = V_{\text{dc}}$$

$$V_{1,\text{rms}} = \frac{V_1}{\sqrt{2}} = \frac{4V_{\text{dc}}}{\sqrt{2}\pi}$$

Using Eq. (8-17) to compute the total harmonic distortion for voltage,

$$\text{THD}_V = \frac{\sqrt{V_{\text{rms}}^2 - V_{1,\text{rms}}^2}}{V_{1,\text{rms}}} = \frac{\sqrt{V_{\text{dc}}^2 - (4V_{\text{dc}}/\sqrt{2}\pi)^2}}{4V_{\text{dc}}/\sqrt{2}\pi} = 0.483 = 48.3\%$$

The THD of the current is computed using the truncated Fourier series which was determined in Example 8-2.

$$\begin{aligned} \text{THD}_I &= \frac{\sqrt{\sum_{n=2}^{\infty} (I_{n,\text{rms}})^2}}{I_{1,\text{rms}}} \\ &\approx \frac{\sqrt{(1.42/\sqrt{2})^2 + (0.53/\sqrt{2})^2 + (0.27/\sqrt{2})^2 + (0.17/\sqrt{2})^2}}{9.27/\sqrt{2}} = 0.167 = 16.7\% \end{aligned}$$

8.6 PSPICE SIMULATION OF SQUARE-WAVE INVERTERS

Computer simulation of inverter circuits can include various levels of circuit detail. If only the current waveform in the load is desired, it is sufficient to provide a source that will produce the appropriate voltage that would be expected on the inverter output. For example, a full-bridge inverter producing a square wave output might be replaced with a square wave voltage source using the VPULSE source. This simplified simulation will predict the behavior of the current in the load but will give no direct information about the switches. Also, this approach assumes that the switching operation correctly produces the desired output.

EXAMPLE 8-4

PSpice Simulation for Example 8-1

For a series (RL) load in a full-bridge inverter circuit with a square wave output, the dc supply is 100 V, $R = 10 \Omega$, $L = 25 \text{ mH}$, and the switching frequency is 60 Hz (Example 8-1). (a) Assuming ideal switches, use PSpice to determine the maximum and minimum

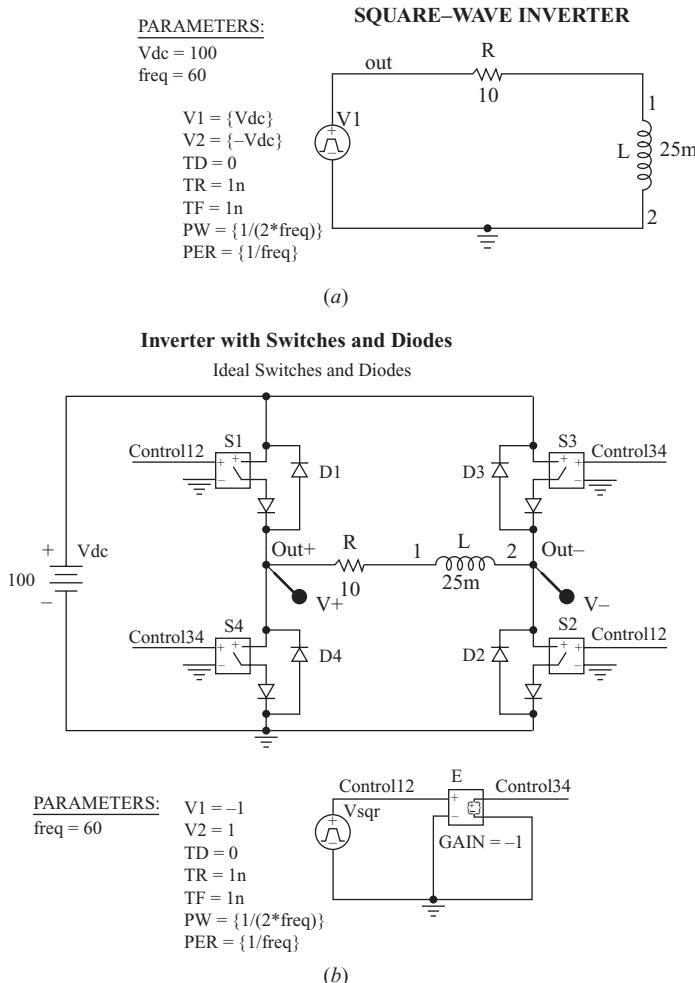


Figure 8-4 (a) Square-wave inverter simulation using an ideal source; (b) Square-wave inverter using switches and diodes.

current in the load in the steady state. (b) Determine the power absorbed by the load.
(c) Determine the total harmonic distortion of the load current.

■ Solution 1

Since individual switch currents are not of concern in this problem, a square wave voltage source (VPULSE), as shown in Fig. 8-4a, across the load can simulate the converter output.

Set up a simulation profile for a transient analysis having a run time of 50 ms (three periods), and start saving data after 16.67 ms (one period) so the output represents steady-state current.

Fourier analysis is performed under *Simulation Settings, Output File Options, Perform Fourier Analysis, Center Frequency: 60 Hz, Number of Harmonics: 15, Output Variables: V(OUT) I(R)*.

- (a) When in Probe, enter the expression $I(R)$ to obtain a display of the current in the load resistor. The first period contains the start-up transient, but steady-state current like that in Fig. 8-2 is displayed thereafter. The maximum and minimum steady-state current values are approximately 9.31 and -9.31 A , which can be obtained precisely by using the cursor option.
- (b) Average power can be obtained from Probe by displaying load current, making sure that the data represent the steady-state condition and entering the expression $\text{AVG}(W(R))$ or $\text{AVG}(V(\text{OUT})*I(R))$. This shows that the resistor absorbs approximately 441 W. The rms current is determined by entering $\text{RMS}(I(R))$, resulting in 6.64 A, as read from the end of the trace. These results agree with the analysis in Example 8-1.
- (c) The THD is obtained from the Fourier series for $I(R)$ in the output file as 16.7 percent, agreeing with the Fourier analysis in Examples 8-2 and 8-3. Note that the THD for the square wave in the output file is 45 percent, which is lower than the 48.3 percent computed in Example 8-3. The THD in PSpice is based on the truncated Fourier series through $n = 15$. The magnitudes of higher-order harmonics are not insignificant for the square wave, and omitting them underestimates the THD. The higher-order current harmonics are small, so there is little error in omitting them from the analysis. The number of harmonics in the output file can be increased if desired.

■ Solution 2

The inverter is simulated using the full-bridge circuit of Fig. 8-4b. (This requires the full version of PSpice.) The result of this simulation gives information about the currents and voltages for the switching devices. Voltage-controlled switches (Sbreak) and the default diode (Dbreak) are used. Diodes are included in the switch model to make the switches unidirectional. The model for Sbreak is changed so $R_{\text{on}} = 0.01\ \Omega$, and the model for Dbreak is changed so $n = 0.01$, approximating an ideal diode. The output voltage is between nodes out+ and out-. Models for the switches and diodes can be changed to determine the behavior of the circuit using realistic switching devices.

8.7 AMPLITUDE AND HARMONIC CONTROL

The amplitude of the fundamental frequency for a square wave output from of the full-bridge inverter is determined by the dc input voltage [Eq. (8-16)]. A controlled output can be produced by modifying the switching scheme. An output voltage of the form shown in Fig. 8-5a has intervals when the output is zero as well as $+V_{\text{dc}}$ and $-V_{\text{dc}}$. This output voltage can be controlled by adjusting the interval α on each side of the pulse where the output is zero. The rms value of the voltage waveform in Fig 8-5a is

$$V_{\text{rms}} = \sqrt{\frac{1}{\pi} \int_{-\alpha}^{\alpha} V_{\text{dc}}^2 d(\omega t)} = V_{\text{dc}} \sqrt{1 - \frac{2\alpha}{\pi}} \quad (8-18)$$

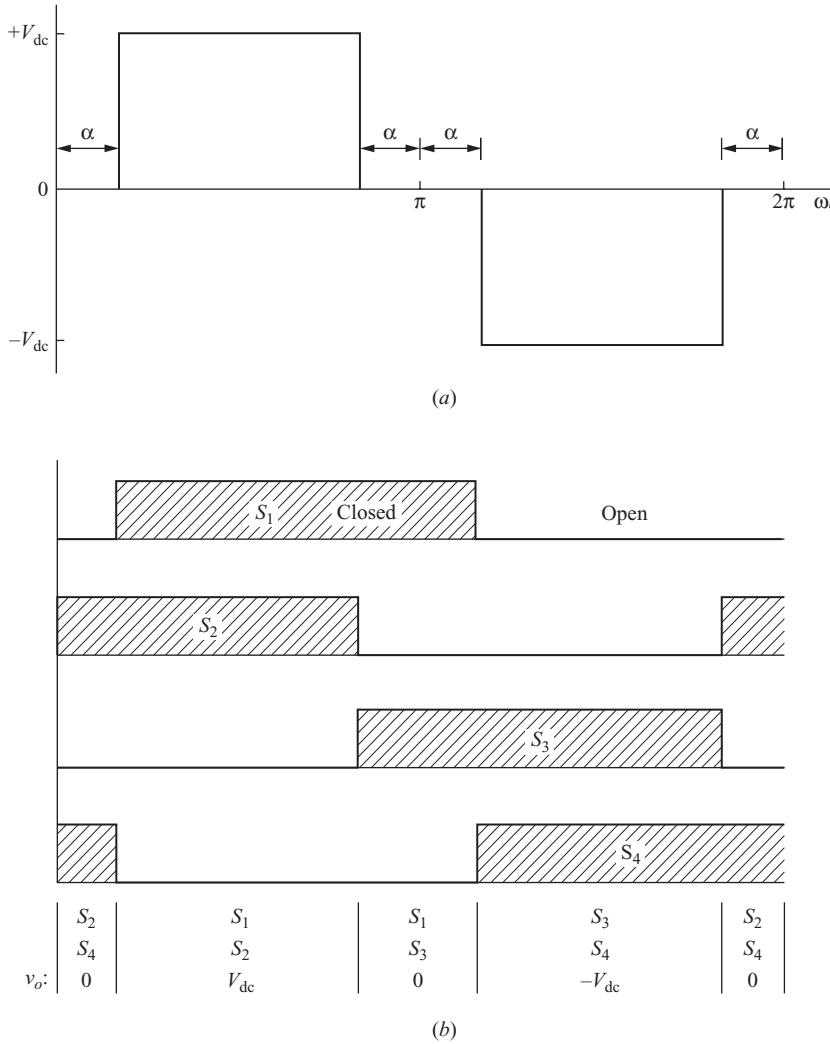


Figure 8-5 (a) Inverter output for amplitude and harmonic control; (b) Switching sequence for the full-bridge inverter of Fig. 8-1a.

The Fourier series of the waveform is expressed as

$$v_o(t) = \sum_{n \text{ odd}} V_n \sin(n\omega_0 t) \quad (8-19)$$

Taking advantage of half-wave symmetry, the amplitudes are

$$V_n = \frac{2}{\pi} \int_{\alpha}^{\pi-\alpha} V_{dc} \sin(n\omega_0 t) d(\omega_0 t) = \frac{4V_{dc}}{n\pi} \cos(n\alpha) \quad (8-20)$$

where α is the angle of zero voltage on each end of the pulse. The amplitude of each frequency of the output is a function of α . In particular, the amplitude of the fundamental frequency ($n = 1$) is controllable by adjusting α :

$$V_1 = \left(\frac{4V_{dc}}{\pi} \right) \cos \alpha \quad (8-21)$$

Harmonic content can also be controlled by adjusting α . If $\alpha = 30^\circ$, for example, $V_3 = 0$. This is significant because the third harmonic can be eliminated from the output voltage and current. Other harmonics can be eliminated by choosing a value of α which makes the cosine term in Eq. (8-20) to go to zero. Harmonic n is eliminated if

$$\alpha = \frac{90^\circ}{n} \quad (8-22)$$

The switching scheme required to produce an output like Fig. 8-5a must provide intervals when the output voltage is zero, as well as $\pm V_{dc}$. The switching sequence of Fig. 8-5b is a way to implement the required output waveform.

Amplitude control and harmonic reduction may not be compatible. For example, establishing α at 30° to eliminate the third harmonic fixes the amplitude of the output fundamental frequency at $V_1 = (4V_{dc}/\pi) \cos 30^\circ = 1.1V_{dc}$ and removes further controllability. To control both amplitude and harmonics using this switching scheme, it is necessary to be able to control the dc input voltage to the inverter. A dc-dc converter (Chap. 6 and 7) placed between the dc source and the inverter can provide a controlled dc input to the inverter.

A graphical representation of the integration in the Fourier series coefficient of Eq. (8-20) gives some insight into harmonic elimination. Recall from Chap. 2 that the Fourier coefficients are determined from the integral of the product of the waveform and a sinusoid. Figure 8-6a shows the output waveform for $\alpha = 30^\circ$ and the sinusoid of $\omega = 3\omega_o$. The product of these two waveforms has an area of zero, showing that the third harmonic is zero. Figure 8-6b shows the waveform for $\alpha = 18^\circ$ and the sinusoid of $\omega = 5\omega_o$, showing that the fifth harmonic is eliminated for this value of α .

Other switching schemes can eliminate multiple harmonics. For example, the output waveform shown in Fig. 8-6c eliminates both the third and fifth harmonics, as indicated by the areas of both being zero.

EXAMPLE 8-5

Harmonic Control of the Full-Bridge Inverter Output

Design an inverter that will supply the series RL load of the previous examples ($R = 10 \Omega$ and $L = 25 \text{ mH}$) with a fundamental-frequency current amplitude of 9.27 A, but with a THD of less than 10 percent. A variable dc source is available.

■ Solution

A square-wave inverter produces a THD for current of 16.7 percent (Example 8-3), which does not meet the specification. The dominant harmonic current is for $n = 3$, so a switching

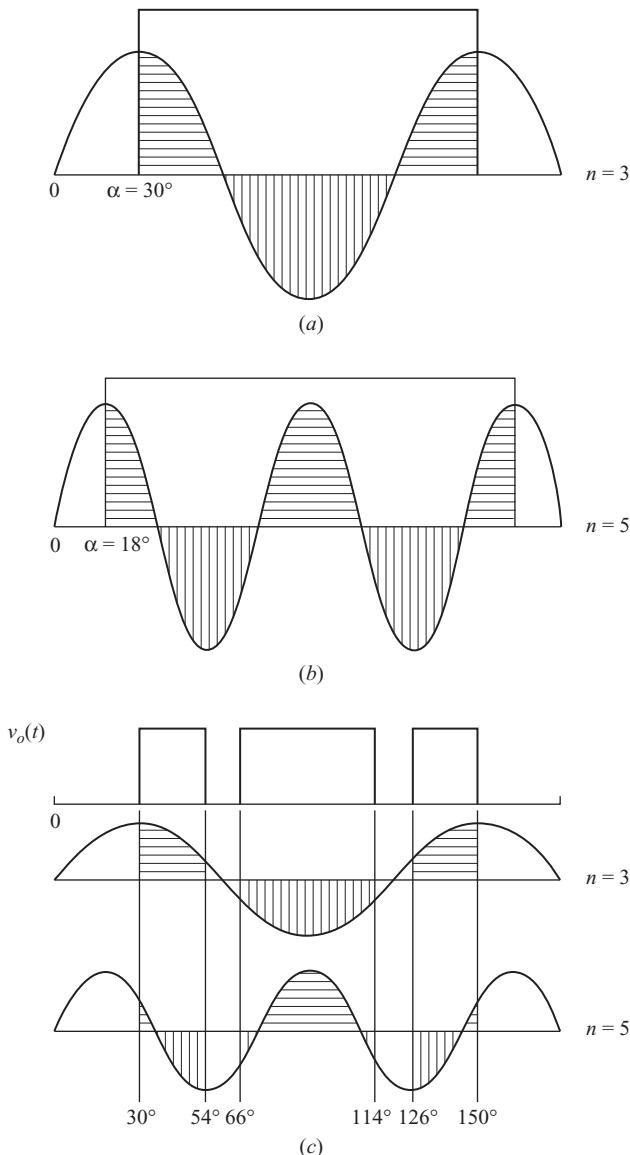


Figure 8-6 Harmonic elimination; (a) Third harmonic; (b) Fifth harmonic; (c) Third and fifth harmonics.

scheme to eliminate the third harmonic will reduce the THD. The required voltage amplitude at the fundamental frequency is

$$V_1 = I_1 Z_1 = I_1 \sqrt{R^2 + (\omega_0 L)^2} = 9.27 \sqrt{10^2 + [2\pi 60(0.025)]^2} = 127 \text{ V}$$

Using the switching scheme of Fig. 8-5b, Eq. (8-21) describes the amplitude of the fundamental-frequency voltage,

$$V_1 = \left(\frac{4V_{dc}}{\pi} \right) \cos \alpha$$

Solving for the required dc input with $\alpha = 30^\circ$,

$$V_{dc} = \frac{V_1\pi}{4 \cos \alpha} = \frac{127\pi}{4 \cos 30^\circ} = 116 \text{ V}$$

Other harmonic voltages are described by Eq. (8-20), and currents for these harmonics are determined from voltage amplitude and load impedance using the same technique as for the square-wave inverter of Example 8-2. The results are summarized in Table 8-2.

Table 8-2 Fourier Series Quantities for Example 8-5

<i>n</i>	<i>f_n</i> (Hz)	<i>V_n</i> (V)	<i>Z_n</i> (Ω)	<i>I_n</i> (A)
1	60	127	13.7	9.27
3	180	0	30.0	0
5	300	25.5	48.2	0.53
7	420	18.2	66.7	0.27
9	540	0	85.4	0
11	660	11.6	104	0.11

The THD of the load current is then

$$\text{THD}_1 = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,\text{rms}}^2}}{I_{1,\text{rms}}} \approx \frac{\sqrt{(0.53/\sqrt{2})^2 + (0.27/\sqrt{2})^2 + (0.11/\sqrt{2})^2}}{9.27/\sqrt{2}} = 0.066 = 6.6\%$$

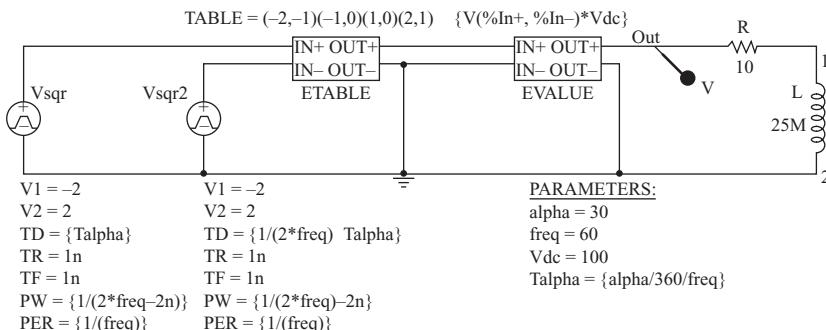
which more than satisfies the design specifications.

A PSpice circuit for the full-bridge inverter with harmonic and amplitude control is shown in Fig. 8-7a. The user must enter the parameters alpha, output fundamental frequency, dc input voltage to the bridge, and load. The Probe output for voltage and current is shown in Fig. 8-7b. The current is scaled by a factor of 10 to show its relationship to the voltage waveform. The THD of the load current is obtained from the Fourier analysis in the output file as 6.6 percent.

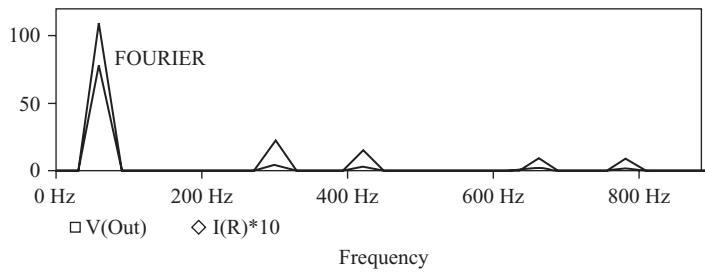
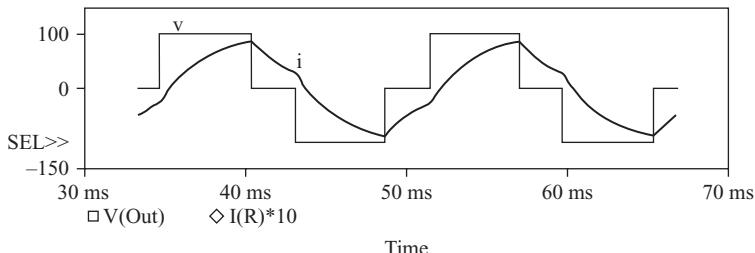
8.8 THE HALF-BRIDGE INVERTER

The half-bridge converter of Fig. 8-8 can be used as an inverter. This circuit was introduced in Chap. 7 as applied to dc power supply circuits. In this circuit, the number of switches is reduced to 2 by dividing the dc source voltage into two parts with the capacitors. Each capacitor will be the same value and will have

INVERTER WITH AMPLITUDE AND HARMONIC CONTROL



(a)

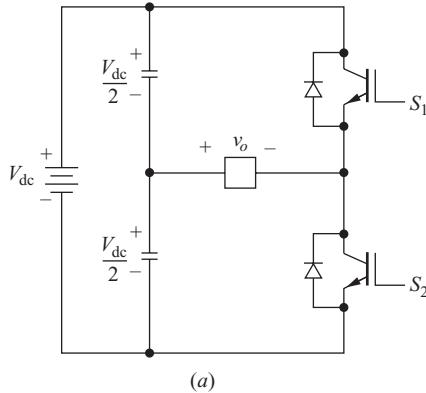


(b)

Figure 8-7 (a) A PSpice circuit for Example 8-5 to produce the voltage waveform in Fig. 8-5a; (b) Probe output for showing harmonic elimination.

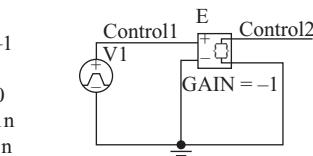
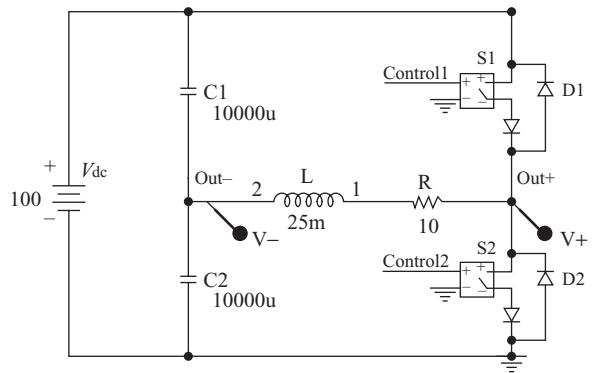
voltage $V_{dc}/2$ across it. When S_1 is closed, the load voltage is $-V_{dc}/2$. When S_2 is closed, the load voltage is $+V_{dc}/2$. Thus, a square wave output or a bipolar pulse-width-modulated output, as described in Sec. 8.10, can be produced.

The voltage across an open switch is twice the load voltage, or V_{dc} . As with the full-bridge inverter, blanking time for the switches is required to prevent a short circuit across the source, and feedback diodes are required to provide continuity of current for inductive loads.



HALF-BRIDGE INVERTER

Ideal Switches and Diodes



(b)

Figure 8-8 (a) A half-bridge inverter using IGBTs. The output is $\pm V_{dc}$; (b) A PSpice implementation using voltage-controlled switches and diodes.

8.9 MULTILEVEL INVERTERS

The H bridge inverter previously illustrated in Figs. 8-1 and 8-3 produces output voltages of V_{dc} , 0, and $-V_{dc}$. The basic H bridge switching concept can be expanded to other circuits that can produce additional output voltage levels.

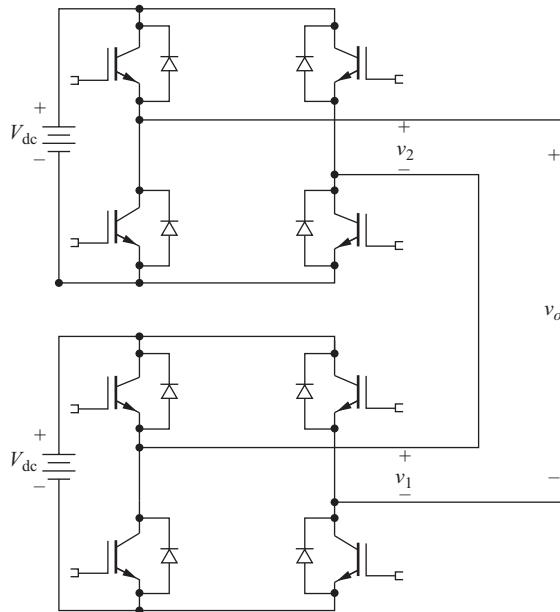


Figure 8-9 An inverter with two dc sources, each with an H bridge implemented with IGBTs.

These multilevel-output voltages are more sinelike in quality and thus reduce harmonic content. The multilevel inverter is suitable for applications including adjustable-speed motor drives and interfacing renewable energy sources such as photovoltaics to the electric power grid.

Multilevel Converters with Independent DC Sources

One multilevel inverter method uses independent dc sources, each with an H bridge. A circuit with two dc voltage sources is shown in Fig. 8-9. The output of each of the H bridges is $+V_{dc}$, $-V_{dc}$, or 0, as was illustrated in Fig. 8-1. The total instantaneous voltage v_o on the output of the multilevel converter is any combination of individual bridge voltages. Thus, for a two-source inverter, v_o can be any of the five levels $+2V_{dc}$, V_{dc} , 0, $-V_{dc}$, or $-2V_{dc}$.

Each H bridge operates with a switching scheme like that of Fig. 8.5 in Sec. 8.7, which was used for amplitude or harmonic control. Each bridge operates at a different delay angle α , resulting in bridge and total output voltages like those shown in Fig. 8-10.

The Fourier series for the total output voltage v_o for the two-source circuit contains only the odd-numbered harmonics and is

$$v_o(t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,7,\dots}^{\infty} [\cos(n\alpha_1) + \cos(n\alpha_2)] \frac{\sin(n\omega_0 t)}{n} \quad (8-23)$$

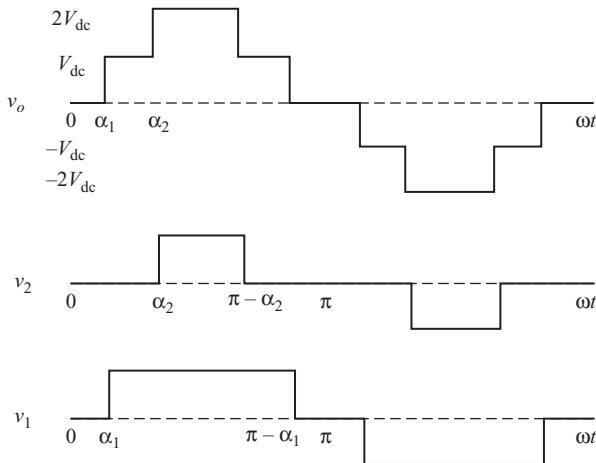


Figure 8-10 Voltage output of each of the H bridges and the total voltage for the two-source multilevel inverter of Fig. 8-9.

The Fourier coefficients for this series are

$$V_n = \frac{4V_{dc}}{n\pi} [\cos(n\alpha_1) + \cos(n\alpha_2)] \quad (8-24)$$

The modulation index M_i is the ratio of the amplitude of the fundamental frequency component of v_o to the amplitude of the fundamental frequency component of a square wave of amplitude $2V_{dc}$, which is $2(4V_{dc}/\pi)$.

$$M_i = \frac{V_1}{2(4V_{dc}/\pi)} = \frac{\cos \alpha_1 + \cos \alpha_2}{2} \quad (8-25)$$

Some harmonics can be eliminated from the output voltage waveform with the proper selection of α_1 and α_2 in Eq. (8-24). For the two-source converter, harmonic m can be eliminated by using delay angles such that

$$\cos(m\alpha_1) + \cos(m\alpha_2) = 0 \quad (8-26)$$

To eliminate the m th harmonic and also meet a specified modulation index for the two-source inverter requires the simultaneous solution to Eq. (8-26) and the additional equation derived from Eq. (8-25),

$$\cos(\alpha_1) + \cos(\alpha_2) = 2M_i \quad (8-27)$$

To solve Eqs. (8-26) and (8-27) simultaneously requires an iterative numerical method such as the Newton-Raphson method.

EXAMPLE 8-6

A Two-Source Multilevel Inverter

For the two-source multilevel inverter of Fig. 8-9 with $V_{dc} = 100$ V: (a) Determine the Fourier coefficients through $n = 9$ and the modulation index for $\alpha_1 = 20^\circ$ and $\alpha_2 = 40^\circ$. (b) Determine α_1 and α_2 such that the third harmonic ($n = 3$) is eliminated and $M_i = 0.8$.

Solution

Using Eq. 8-24 to evaluate the Fourier coefficients,

$$V_n = \frac{4V_{dc}}{n\pi} [\cos(n\alpha_1) + \cos(n\alpha_2)] = \frac{4(100)}{n\pi} [\cos(n20^\circ) + \cos(n40^\circ)]$$

resulting in $V_1 = 217$, $V_3 = 0$, $V_5 = -28.4$, $V_7 = -10.8$, and $V_9 = 0$. Note that the third and ninth harmonics are eliminated. The even harmonics are not present.

The modulation index M_i is evaluated from Eq. (8-25).

$$M_i = \frac{\cos\alpha_1 + \cos\alpha_2}{2} = \frac{\cos 20^\circ + \cos 40^\circ}{2} = 0.853$$

The amplitude of the fundamental frequency voltage is therefore 85.3 percent of that of a square wave of ± 200 V.

- (b) To achieve simultaneous elimination of the third harmonic and a modulation index of $M_i = 0.8$ requires the solution to the equations

$$\cos(3\alpha_1) + \cos(3\alpha_2) = 0$$

and

$$\cos(\alpha_1) + \cos(\alpha_2) = 2M_i = 1.6$$

Using an iterative method, $\alpha_1 = 7.6^\circ$ and $\alpha_2 = 52.4^\circ$.

The preceding concept can be extended to a multilevel converter having several dc sources. For k separate sources connected in cascade, there are $2k+1$ possible voltage levels. As more dc sources and H bridges are added, the total output voltage has more steps, producing a staircase waveform that more closely approaches a sinusoid. For a five-source system as shown in Fig. 8-11, there are 11 possible output voltage levels, as illustrated in Fig. 8-12.

The Fourier series for a staircase waveform such as that in Fig. 8-12 for k separate dc sources each equal to V_{dc} is

$$v_o(t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,7,\dots}^{\infty} [\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_k)] \frac{\sin(n\omega_0 t)}{n} \quad (8-28)$$

The magnitudes of the Fourier coefficients are thus

$$V_n = \frac{4V_{dc}}{n\pi} [\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_k)] \quad (8-29)$$

for $n = 1, 3, 5, 7, \dots$

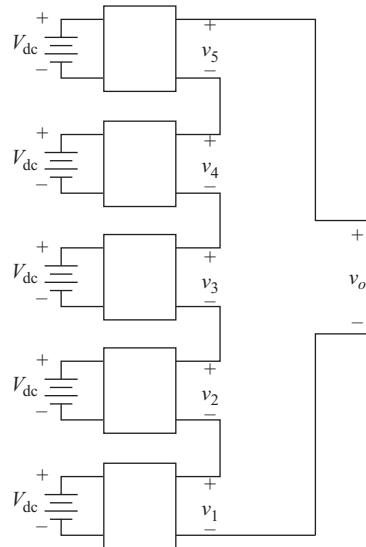


Figure 8-11 A five-source cascade multilevel converter.

The modulation index M_i for k dc sources each equal to V_{dc} is

$$M_i = \frac{V_i}{4kV_{dc}/\pi} = \frac{\cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_k)}{k} \quad (8-30)$$

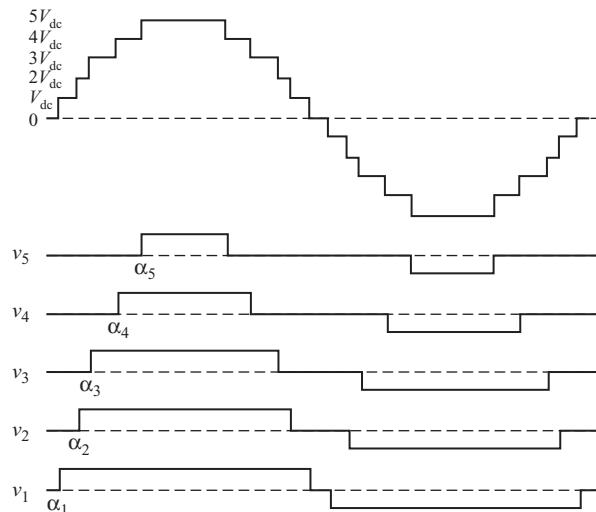


Figure 8-12 Voltages at each H bridge in Fig. 8-11 and the total output voltage.

Specific harmonics can be eliminated from the output voltage. To eliminate the m th harmonic, the delay angles must satisfy the equation

$$\cos(m\alpha_1) + \cos(m\alpha_2) + \cdots + \cos(m\alpha_k) = 0 \quad (8-31)$$

For k dc sources, $k - 1$ harmonics can be eliminated while establishing a particular M_i .

EXAMPLE 8-7

A Five-Source Multilevel Inverter

Determine the delay angles required for a five-source cascade multilevel converter that will eliminate harmonics 5, 7, 11, and 13 and will have a modulation index $M_i = 0.8$.

■ Solution

The delay angles must satisfy these simultaneous equations:

$$\begin{aligned} \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) &= 0 \\ \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) &= 0 \\ \cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) &= 0 \\ \cos(13\alpha_1) + \cos(13\alpha_2) + \cos(13\alpha_3) + \cos(13\alpha_4) + \cos(13\alpha_5) &= 0 \\ \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) &= 5M_i = 5(0.8) = 4 \end{aligned}$$

An iteration method such as the Newton-Raphson method must be used to solve these equations. The result is $\alpha_1 = 6.57^\circ$, $\alpha_2 = 18.94^\circ$, $\alpha_3 = 27.18^\circ$, $\alpha_4 = 45.14^\circ$, and $\alpha_5 = 62.24^\circ$. See the references in the Bibliography for information on the technique.

Equalizing Average Source Power with Pattern Swapping

In the two-source inverter of Fig. 8-9 using the switching scheme of Fig. 8-10, the source and H bridge producing the voltage v_1 supplies more average power (and energy) than the source and H bridge producing v_2 due to longer pulse widths in both the positive and negative half cycles. If the dc sources are batteries, one battery will discharge faster than the other. A technique known as pattern swapping or duty swapping equalizes the average power supplied by each dc source.

The principle of pattern swapping is to have each dc source conduct for an equal amount of time on average. An alternate switching scheme for the two-source circuit is shown in Fig. 8-13. In this scheme, the first source conducts for a longer time in the first half-cycle while the second source conducts for more time in the second half-cycle. Thus, over one complete period, the sources conduct equally, and average power from each source is the same.

For the five-source converter in Fig. 8-11, a switching scheme to equalize average power is shown in Fig. 8-14. Note that five half cycles are required to equalize power.

A variation of the H bridge multilevel inverter is to have the dc sources be of different values. The output voltage would be a staircase waveform, but not in equal

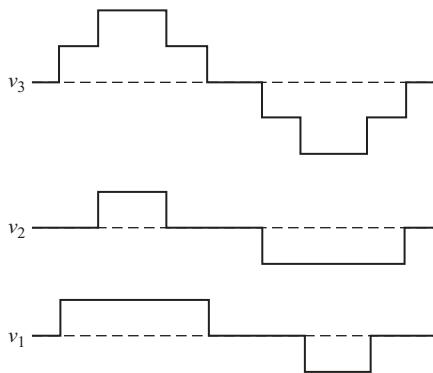


Figure 8-13 Pattern swapping to equalize average power in each source for the two-source inverter of Fig. 8-9.

voltage increments. The Fourier series of the output voltage would have different-valued harmonic amplitudes which may be an advantage in some applications.

Because independent voltage sources are needed, the multiple-source implementation of multilevel converters is best suited in applications where batteries, fuel cells, or photovoltaics are the sources.

Diode-Clamped Multilevel Inverters

A multilevel converter circuit that has the advantage of using a single dc source rather than multiple sources is the diode-clamped multilevel converter shown in Fig. 8-15a. In this circuit, the dc voltage source is connected to a pair of series capacitors, each charged to $V_{dc}/2$. The following analysis shows how the output voltage can have the levels of V_{dc} , $V_{dc}/2$, 0, $-V_{dc}/2$, or $-V_{dc}$.

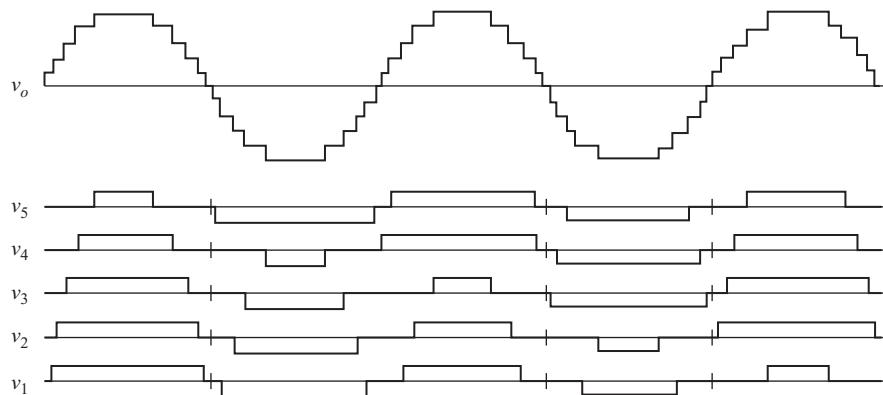


Figure 8-14 Pattern swapping to equalize average source power for the five-source multilevel inverter of Fig. 8-11.

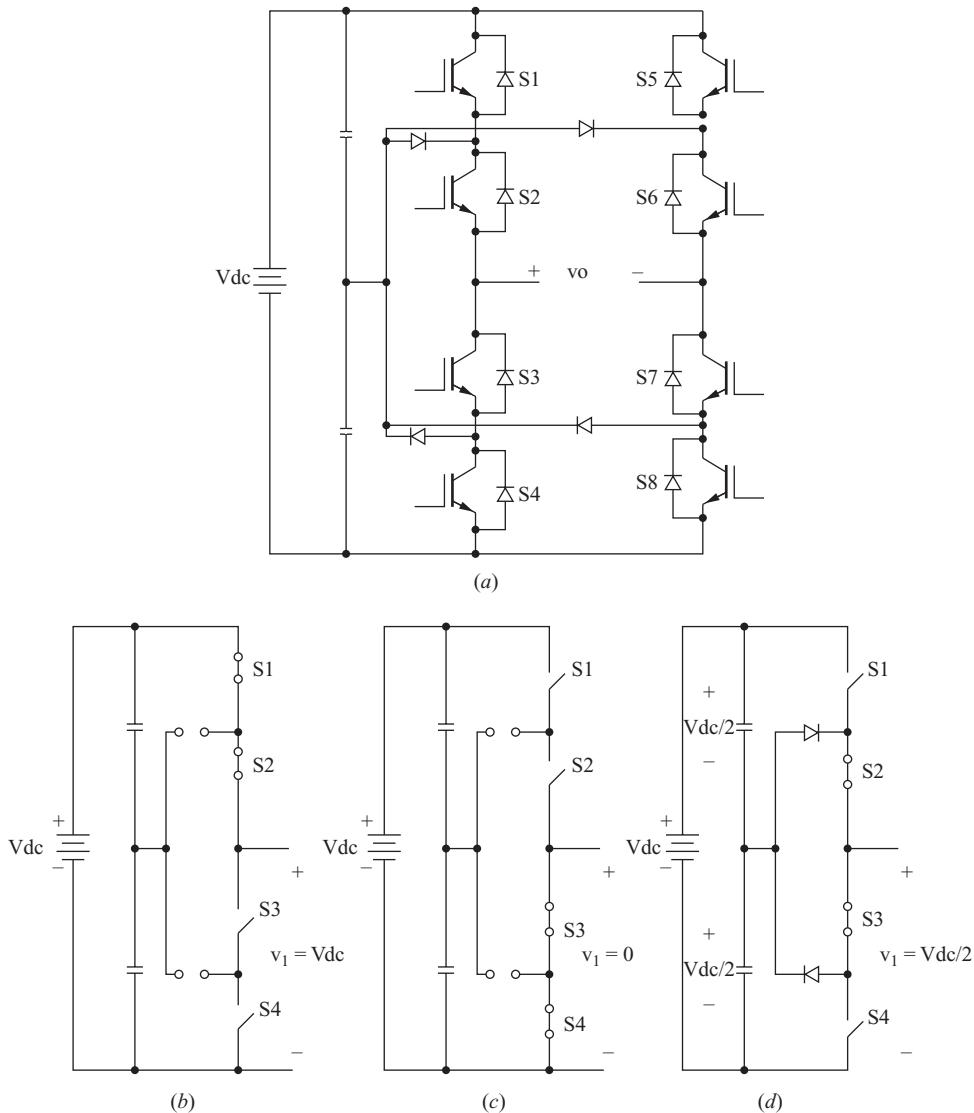


Figure 8-15 (a) A diode-clamped multilevel inverter implemented with IGBTs. (b) Analysis for one-half of the circuit for $v_1 = V_{dc}$, (c) for $v_1 = 0$, and (d) for $v_1 = \frac{1}{2}V_{dc}$.

For the analysis, consider only the left half of the bridge, as shown in Fig. 8-15b, c, and d. With S_1 and S_2 closed and S_3 and S_4 open, $V_1 = V_{dc}$ (Fig. 8-15b). The diodes are off for this condition. With S_1 and S_2 open and S_3 and S_4 closed, $V_1 = 0$ (Fig. 8-15c). The diodes are off for this condition also. To produce a voltage of $V_{dc}/2$, S_2 and S_3 are closed, and S_1 and S_4 are open (Fig. 8-15d). The voltage v_1 is that of the lower capacitor, at voltage $V_{dc}/2$, connected through the antiparallel diode path that can carry load current in either direction. Note that for each of

in these circuits, two switches are open, and the voltage of the source divides between the two, thus reducing the voltage stress across each switch compared to the H bridge circuit of Fig. 8-1.

Using a similar analysis, the right half of the bridge can also produce the voltages V_{dc} , 0, and $-V_{dc}/2$. The output voltage is the difference of the voltages between each half bridge, resulting in the five levels

$$v_o \in \left\{ V_{dc}, \frac{1}{2}V_{dc}, 0, -\frac{1}{2}V_{dc}, -V_{dc} \right\} \quad (8-32)$$

with multiple ways to achieve some of them. The switch control can establish delay angles α_1 and α_2 , to produce an output voltage like that in Fig. 8-10 for the cascaded H bridge, except that the maximum value is V_{dc} instead of $2V_{dc}$.

More output voltage levels are achieved with additional capacitors and switches. Figure 8-16 shows the dc source divided across three series capacitors.

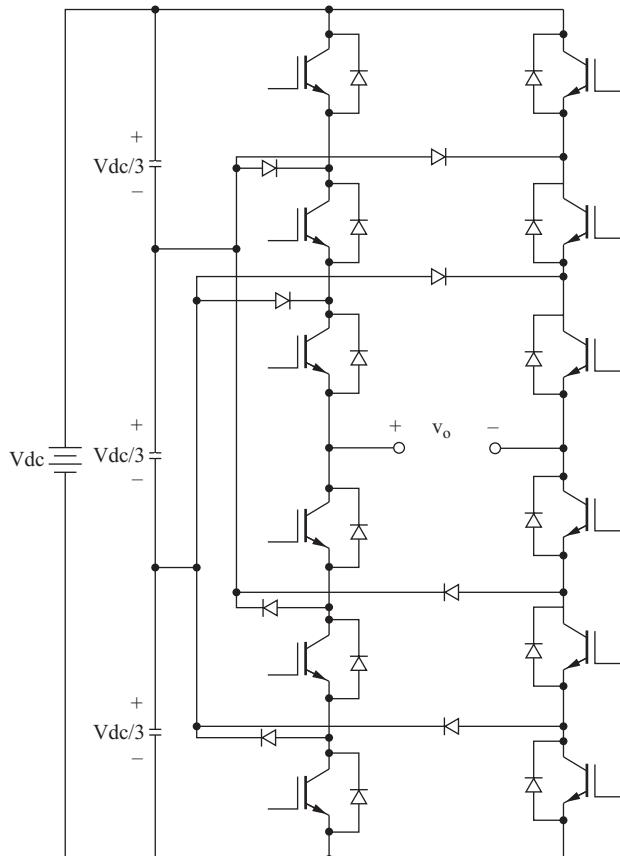


Figure 8-16 A diode-clamped multilevel inverter that produces four voltage levels on each side of the bridge and seven output voltage levels.

The voltage across each capacitor is $\frac{1}{3}$ V, producing the four voltage levels on each side of the bridge of V_{dc} , $\frac{2}{3}V_{dc}$, $\frac{1}{3}V_{dc}$, and 0. The output voltage can then have the seven levels

$$v_o \in \left\{ V_{dc}, \frac{2}{3}V_{dc}, \frac{1}{3}V_{dc}, 0, -\frac{1}{3}V_{dc}, -\frac{2}{3}V_{dc}, -V_{dc} \right\} \quad (8-33)$$

8.10 PULSE-WIDTH-MODULATED OUTPUT

Pulse-width modulation (PWM) provides a way to decrease the total harmonic distortion of load current. A PWM inverter output, with some filtering, can generally meet THD requirements more easily than the square wave switching scheme. The unfiltered PWM output will have a relatively high THD, but the harmonics will be at much higher frequencies than for a square wave, making filtering easier.

In PWM, the amplitude of the output voltage can be controlled with the modulating waveforms. *Reduced filter requirements to decrease harmonics and the control of the output voltage amplitude are two distinct advantages of PWM.* Disadvantages include more complex control circuits for the switches and increased losses due to more frequent switching.

Control of the switches for sinusoidal PWM output requires (1) a reference signal, sometimes called a modulating or control signal, which is a sinusoid in this case and (2) a carrier signal, which is a triangular wave that controls the switching frequency. Bipolar and unipolar switching schemes are discussed next.

Bipolar Switching

Figure 8-17 illustrates the principle of sinusoidal bipolar pulse-width modulation. Figure 8-17a shows a sinusoidal reference signal and a triangular carrier signal. When the instantaneous value of the sine reference is larger than the triangular carrier, the output is at $+V_{dc}$, and when the reference is less than the carrier, the output is at $-V_{dc}$:

$$\begin{aligned} v_o &= +V_{dc} && \text{for } v_{\text{sine}} > v_{\text{tri}} \\ v_o &= -V_{dc} && \text{for } v_{\text{sine}} < v_{\text{tri}} \end{aligned} \quad (8-34)$$

This version of PWM is *bipolar* because the output alternates between plus and minus the dc supply voltage.

The switching scheme that will implement bipolar switching using the full-bridge inverter of Fig. 8-1 is determined by comparing the instantaneous reference and carrier signals:

S_1 and S_2 are on when $v_{\text{sine}} > v_{\text{tri}}$ ($v_o = +V_{dc}$)

S_3 and S_4 are on when $v_{\text{sine}} < v_{\text{tri}}$ ($v_o = -V_{dc}$)

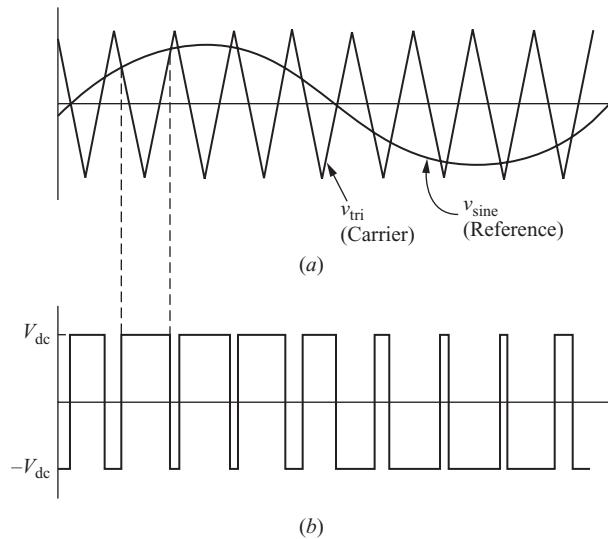


Figure 8-17 Bipolar pulse-width modulation. (a) Sinusoidal reference and triangular carrier; (b) Output is $+V_{\text{dc}}$ when $v_{\text{sine}} > v_{\text{tri}}$ and is $-V_{\text{dc}}$ when $v_{\text{sine}} < v_{\text{tri}}$.

Unipolar Switching

In a unipolar switching scheme for pulse-width modulation, the output is switched either from high to zero or from low to zero, rather than between high and low as in bipolar switching. One unipolar switching scheme has switch controls in Fig. 8-1 as follows:

- S_1 is on when $v_{\text{sine}} > v_{\text{tri}}$
- S_2 is on when $-v_{\text{sine}} < v_{\text{tri}}$
- S_3 is on when $-v_{\text{sine}} > v_{\text{tri}}$
- S_4 is on when $v_{\text{sine}} < v_{\text{tri}}$

Note that switch pairs (S_1, S_4) and (S_2, S_3) are complementary—when one switch in a pair is closed, the other is open. The voltages v_a and v_b in Fig. 8-18a alternate between $+V_{\text{dc}}$ and zero. The output voltage $v_o = v_{ab} = v_a - v_b$ is as shown in Fig. 8-18d.

Another unipolar switching scheme has only one pair of switches operating at the carrier frequency while the other pair operates at the reference frequency, thus having two high-frequency switches and two low-frequency switches. In this switching scheme,

- S_1 is on when $v_{\text{sine}} > v_{\text{tri}}$ (high frequency)
- S_4 is on when $v_{\text{sine}} < v_{\text{tri}}$ (high frequency)

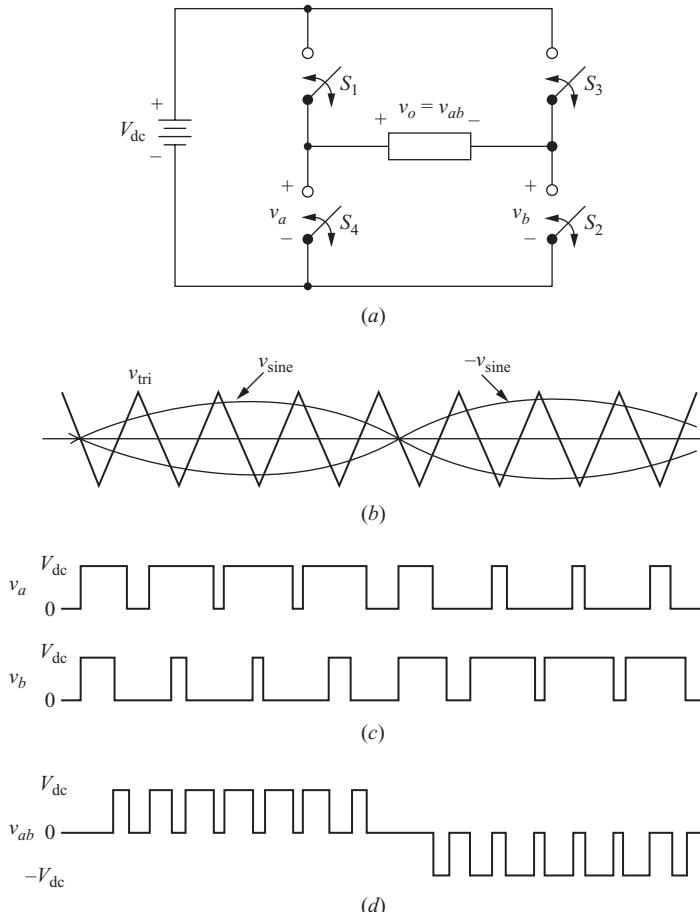


Figure 8-18 (a) Full-bridge converter for unipolar PWM; (b) Reference and carrier signals; (c) Bridge voltages v_a and v_b ; (d) Output voltage.

S_2 is on when $v_{sine} > 0$ (low frequency)
 S_3 is on when $v_{sine} < 0$ (low frequency)

where the sine and triangular waves are as shown in Fig. 8-19a. Alternatively, S_2 and S_3 could be the high-frequency switches, and S_1 and S_4 could be the low-frequency switches.

8.11 PWM DEFINITIONS AND CONSIDERATIONS

At this point, some definitions and considerations relevant when using PWM should be stated.

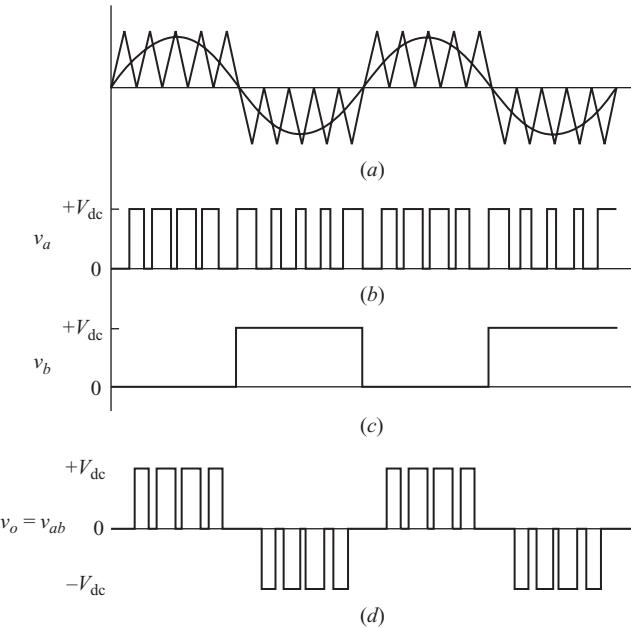


Figure 8-19 Unipolar PWM with high- and low-frequency switches. (a) Reference and control signals; (b) v_a (Fig. 8-18a); (c) v_b ; (d) output $v_a - v_b$.

1. *Frequency modulation ratio m_f* The Fourier series of the PWM output voltage has a fundamental frequency which is the same as the reference signal. Harmonic frequencies exist at and around multiples of the switching frequency. The magnitudes of some harmonics are quite large, sometimes larger than the fundamental. However, because these harmonics are located at high frequencies, a simple low-pass filter can be quite effective in removing them. Details of the harmonics in PWM are given in the next section. The *frequency modulation ratio m_f* is defined as the ratio of the frequencies of the carrier and reference signals,

$$m_f = \frac{f_{\text{carrier}}}{f_{\text{reference}}} = \frac{f_{\text{tri}}}{f_{\text{sine}}} \quad (8-35)$$

Increasing the carrier frequency (increasing m_f) increases the frequencies at which the harmonics occur. A disadvantage of high switching frequencies is higher losses in the switches used to implement the inverter.

2. *Amplitude modulation ratio m_a* . The *amplitude modulation ratio m_a* is defined as the ratio of the amplitudes of the reference and carrier signals:

$$m_a = \frac{V_{m, \text{reference}}}{V_{m, \text{carrier}}} = \frac{V_{m, \text{sine}}}{V_{m, \text{tri}}} \quad (8-36)$$

If $m_a \leq 1$, the amplitude of the fundamental frequency of the output voltage V_1 is linearly proportional to m_a . That is,

$$V_1 = m_a V_{dc} \quad (8-37)$$

The amplitude of the fundamental frequency of the PWM output is thus controlled by m_a . This is significant in the case of an unregulated dc supply voltage because the value of m_a can be adjusted to compensate for variations in the dc supply voltage, producing a constant-amplitude output. Alternatively, m_a can be varied to change the amplitude of the output. If m_a is greater than 1, the amplitude of the output increases with m_a , but not linearly.

3. *Switches.* The switches in the full-bridge circuit must be capable of carrying current in either direction for pulse-width modulation just as they did for square wave operation. Feedback diodes across the switching devices are necessary, as was done in the inverter in Fig. 8-3a. Another consequence of real switches is that they do not turn on or off instantly. Therefore, it is necessary to allow for switching times in the control of the switches just as it was for the square-wave inverter.
4. *Reference voltage.* The sinusoidal reference voltage must be generated within the control circuit of the inverter or taken from an outside reference. It may seem as though the function of the inverter bridge is unnecessary because a sinusoidal voltage must be present before the bridge can operate to produce a sinusoidal output. However, there is very little power required from the reference signal. The power supplied to the load is provided by the dc power source, and this is the intended purpose of the inverter. The reference signal is not restricted to a sinusoid, and other waveshapes can function as the reference signal.

8.12 PWM HARMONICS

Bipolar Switching

The Fourier series of the bipolar PWM output illustrated in Fig. 8-17 is determined by examining each pulse. The triangular waveform is synchronized to the reference as shown in Fig 8-17a, and m_f is chosen to be an odd integer. The PWM output then exhibits odd symmetry, and the Fourier series can then be expressed

$$v_o(t) = \sum_{n=1}^{\infty} V_n \sin(n\omega_0 t) \quad (8-38)$$

For the k th pulse of the PWM output in Fig. 8-20, the Fourier coefficient is

$$\begin{aligned} V_{nk} &= \frac{2}{\pi} \int_0^T v(t) \sin(n\omega_0 t) d(\omega_0 t) \\ &= \frac{2}{\pi} \left[\int_{\alpha_k}^{\alpha_k + \delta_k} V_{dc} \sin(n\omega_0 t) d(\omega_0 t) + \int_{\alpha_k + \delta_k}^{\alpha_{k+1}} -(V_{dc}) \sin(n\omega_0 t) d(\omega_0 t) \right] \end{aligned}$$

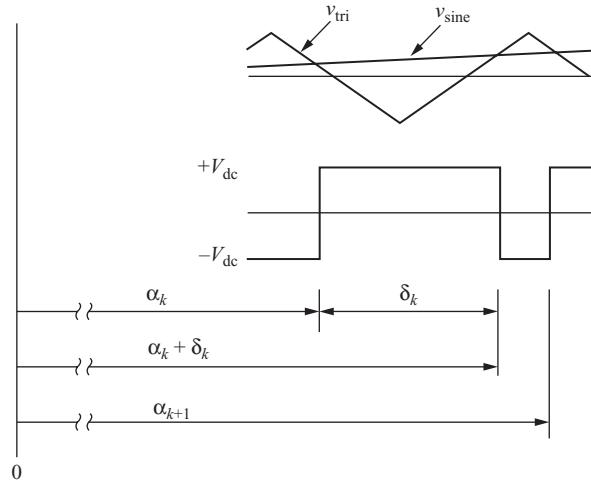


Figure 8-20 Single PWM pulse for determining Fourier series for bipolar PWM.

Performing the integration,

$$V_{nk} = \frac{2V_{dc}}{n\pi} [\cos n\alpha_k + \cos n\alpha_{k+1} - 2 \cos n(\alpha_k + \delta_k)] \quad (8-39)$$

Each Fourier coefficient V_n for the PWM waveform is the sum of V_{nk} for the p pulses over one period,

$$V_n = \sum_{k=1}^p V_{nk} \quad (8-40)$$

The normalized frequency spectrum for bipolar switching for $m_a=1$ is shown in Fig. 8-21. The harmonic amplitudes are a function of m_a because the

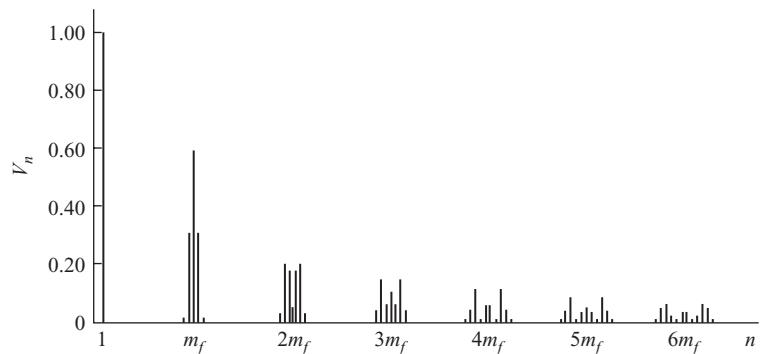


Figure 8-21 Frequency spectrum for bipolar PWM with $m_a = 1$.

Table 8-3 Normalized Fourier Coefficients V_n/V_{dc} for Bipolar PWM

$m_a = 1$	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
$n=1$	1.00	0.90	0.80	0.70	0.60	0.50	0.40	0.30	0.20
$n=m_f$	0.60	0.71	0.82	0.92	1.01	1.08	1.15	1.20	1.24
$n=m_f \pm 2$	0.32	0.27	0.22	0.17	0.13	0.09	0.06	0.03	0.02

width of each pulse depends on the relative amplitudes of the sine and triangular waves. The first harmonic frequencies in the output spectrum are at and around m_f . Table 8-3 indicates the first harmonics in the output for bipolar PWM. The Fourier coefficients are not a function of m_f if m_f is large (≥ 9).

EXAMPLE 8-8

A PWM Inverter

The full-bridge inverter is used to produce a 60-Hz voltage across a series RL load using bipolar PWM. The dc input to the bridge is 100 V, the amplitude modulation ratio m_a is 0.8, and the frequency modulation ratio m_f is 21 [$f_{tri} = (21)(60) = 1260$ Hz]. The load has a resistance of $R = 10 \Omega$ and series inductance $L = 20$ mH. Determine (a) the amplitude of the 60-Hz component of the output voltage and load current, (b) the power absorbed by the load resistor, and (c) the THD of the load current.

Solution

(a) Using Eq. (8-38) and Table 8-3, the amplitude of the 60-Hz fundamental frequency is

$$V_1 = m_a V_{dc} = (0.8)(100) = 80 \text{ V}$$

The current amplitudes are determined using phasor analysis:

$$I_n = \frac{V_n}{Z_n} = \frac{V_n}{\sqrt{R^2 + (n\omega_0 L)^2}} \quad (8-41)$$

For the fundamental frequency,

$$I_1 = \frac{80}{\sqrt{10^2 + [(1)(2\pi 60)(0.02)]^2}} = 6.39 \text{ A}$$

(b) With $m_f = 21$, the first harmonics are at $n = 21, 19$, and 23 . Using Table 8-3,

$$V_{21} = (0.82)(100) = 82 \text{ V}$$

$$V_{19} = V_{23} = (0.22)(100) = 22 \text{ V}$$

Current at each of the harmonics is determined from Eq. (8-41).

Power at each frequency is determined from

$$P_n = (I_{n,\text{rms}})^2 R = \left(\frac{I_n}{\sqrt{2}} \right)^2 R$$

Table 8-4 Fourier Series Quantities for the PWM Inverter of Example 8-8

<i>n</i>	<i>f_n</i> (Hz)	<i>V_n</i> (V)	<i>Z_n</i> (Ω)	<i>I_n</i> (A)	<i>I_{n,rms}</i> (A)	<i>P_n</i> (W)
1	60	80.0	12.5	6.39	4.52	204.0
19	1140	22.0	143.6	0.15	0.11	0.1
21	1260	81.8	158.7	0.52	0.36	1.3
23	1380	22.0	173.7	0.13	0.09	0.1

The resulting voltage amplitudes, currents, and powers at these frequencies are summarized in Table 8-4.

Power absorbed by the load resistor is

$$P = \sum P_n \approx 204.0 + 0.1 + 1.3 + 0.1 = 205.5 \text{ W}$$

Higher-order harmonics contribute little power and can be neglected.

- (c) The THD of the load current is determined using Eq. (8-17) with the rms current of the harmonics approximated by the first few terms indicated in Table 8-4.

$$\text{THD}_1 = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,\text{rms}}^2}}{I_{1,\text{rms}}} \approx \frac{\sqrt{(0.11)^2 + (0.36)^2 + (0.09)^2}}{4.52} = 0.087 = 8.7\%$$

By using the truncated Fourier series in Table 8-4, the THD will be underestimated. However, since the impedance of the load increases and the amplitudes of the harmonics generally decrease as *n* increases, the above approximation should be acceptable. (Including currents through *n* = 100 gives a THD of 9.1 percent.)

EXAMPLE 8-9

PWM Inverter Design

Design a bipolar PWM inverter that will produce a 75-V rms 60-Hz output from a 150-V dc source. The load is a series *RL* combination with *R* = 12 Ω and *L* = 60 mH. Select the switching frequency such that the current THD is less than 10 percent.

■ Solution

The required amplitude modulation ratio is determined from Eq. (8-38),

$$m_a = \frac{V_1}{V_{dc}} = \frac{75\sqrt{2}}{150} = 0.707$$

The current amplitude at 60 Hz is

$$I_1 = \frac{V_1}{Z_1} = \frac{75\sqrt{2}}{\sqrt{12^2 + [(2\pi 60)(0.06)]^2}} = 4.14 \text{ A}$$

The rms value of the harmonic current has a limit imposed by the required THD,

$$\sqrt{\sum_{n=2}^{\infty}(I_{n,\text{rms}})^2} < 0.1 I_{1,\text{rms}} = 0.1 \left(\frac{4.14}{\sqrt{2}} \right) = 0.293 \text{ A}$$

The term that will produce the dominant harmonic current is at the switching frequency. As an approximation, assume that the harmonic content of the load current is the same as the dominant harmonic at the carrier frequency:

$$\sqrt{\sum_{n=2}^{\infty}(I_{n,\text{rms}})^2} \approx I_{mf,\text{rms}} = \frac{I_{mf}}{\sqrt{2}}$$

The amplitude of the current harmonic at the carrier frequency is then approximated as

$$I_{mf} < (0.1)(4.14) = 0.414 \text{ A}$$

Table 8-3 indicates that the normalized voltage harmonic for $n = m_f$ and for $m_a = 0.7$ is 0.92. The voltage amplitude for $n = m_f$ is then

$$V_{mf} = 0.92 V_{dc} = (0.92)(150) = 138 \text{ V}$$

The minimum load impedance at the carrier frequency is then

$$Z_{mf} = \frac{V_{mf}}{I_{mf}} = \frac{138}{0.414} = 333 \Omega$$

Because the impedance at the carrier frequency must be much larger than the 12Ω load resistance, assume the impedance at the carrier frequency is entirely inductive reactance,

$$Z_{mf} \approx \omega L = m_f \omega_0 L$$

For the load impedance to be greater than 333Ω ,

$$m_f \omega_0 L > 333$$

$$m_f > \frac{333}{(377)(0.06)} = 14.7$$

Selecting m_f to be at least 15 would marginally meet the design specifications. However, the estimate of the harmonic content used in the calculations will be low, so a higher carrier frequency is a more prudent selection. Let $m_f = 17$, which is the next odd integer. The carrier frequency is then

$$f_{\text{tri}} = m_f f_{\text{ref}} = (17)(60) = 1020 \text{ Hz}$$

Further increasing m_f would reduce the current THD, but at the expense of larger switching losses. A PSpice simulation, as discussed later in this chapter, can be used to verify that the design meets the specifications.

Unipolar Switching

With the unipolar switching scheme in Fig. 8-18, some harmonics that were in the spectrum for the bipolar scheme are absent. The harmonics in the output begin at around $2m_f$, and m_f is chosen to be an even integer. Figure 8-22 shows the frequency spectrum for unipolar switching with $m_a = 1$.

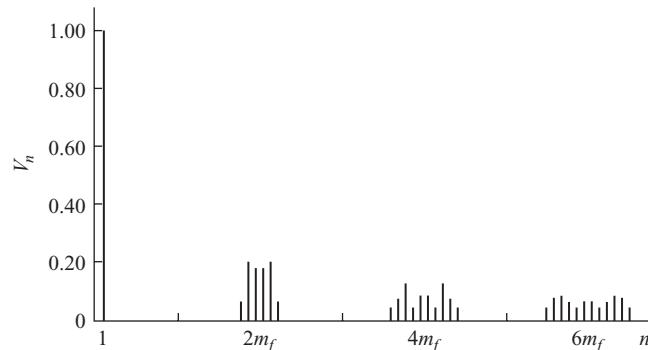


Figure 8-22 Frequency spectrum for unipolar PWM with $m_a = 1$.

Table 8-5 indicates the first harmonics in the output for unipolar PWM.

The unipolar PWM scheme using high- and low-frequency switches shown in Fig. 8-19 will have similar results as indicated above, but the harmonics will begin at around m_f rather than $2m_f$.

Table 8-5 Normalized Fourier Coefficients V_n/V_{dc} for Unipolar PWM in Fig. 8-18

	$m_a = 1$	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
$n=1$	1.00	0.90	0.80	0.70	0.60	0.50	0.40	0.30	0.20	0.10
$n=2m_f \pm 1$	0.18	0.25	0.31	0.35	0.37	0.36	0.33	0.27	0.19	0.10
$n=2m_f \pm 3$	0.21	0.18	0.14	0.10	0.07	0.04	0.02	0.01	0.00	0.00

8.13 CLASS D AUDIO AMPLIFIERS

The reference signal for the PWM control circuit can be an audio signal, and the full-bridge circuit could be used as a PWM audio amplifier. A PWM audio amplifier is referred to as a *class D amplifier*. The triangular wave carrier signal for this application is typically 250 kHz to provide adequate sampling, and the PWM waveform is low-pass filtered to recover the audio signal and deliver power to a speaker. The spectrum of the PWM output signal is dynamic in this case.

Class D amplifiers are much more efficient than other types of audio power amplifiers. The class AB amplifier, the traditional circuit for audio applications, has a maximum theoretical efficiency of 78.5 percent for a sine wave of maximum undistorted output. In practice, with real audio signals, class AB efficiency is much lower, on the order of 20 percent. The theoretical efficiency of the class D amplifier is 100 percent because the transistors are used as switches. Because transistor switching and filtering are imperfect, practical class D amplifiers are about 75 percent efficient.

Class D audio amplifiers are becoming more prevalent in consumer electronics applications where greater efficiency results in reduced size and increased

battery life. In high-power applications such as at rock concerts, class D amplifiers are used to reduce the size of the amplifier and for reduced heat requirements in the equipment.

8.14 SIMULATION OF PULSE-WIDTH-MODULATED INVERTERS

Bipolar PWM

PSpice can be used to simulate the PWM inverter switching schemes presented previously in this chapter. As with other power electronics circuits, the level of circuit detail depends on the objective of the simulation. If only the voltages and currents in the load are desired, a PWM source may be created without modeling the individual switches in the bridge circuit. Figure 8-23 shows two ways to produce a bipolar PWM voltage. The first uses an ABM2 block, and the second uses

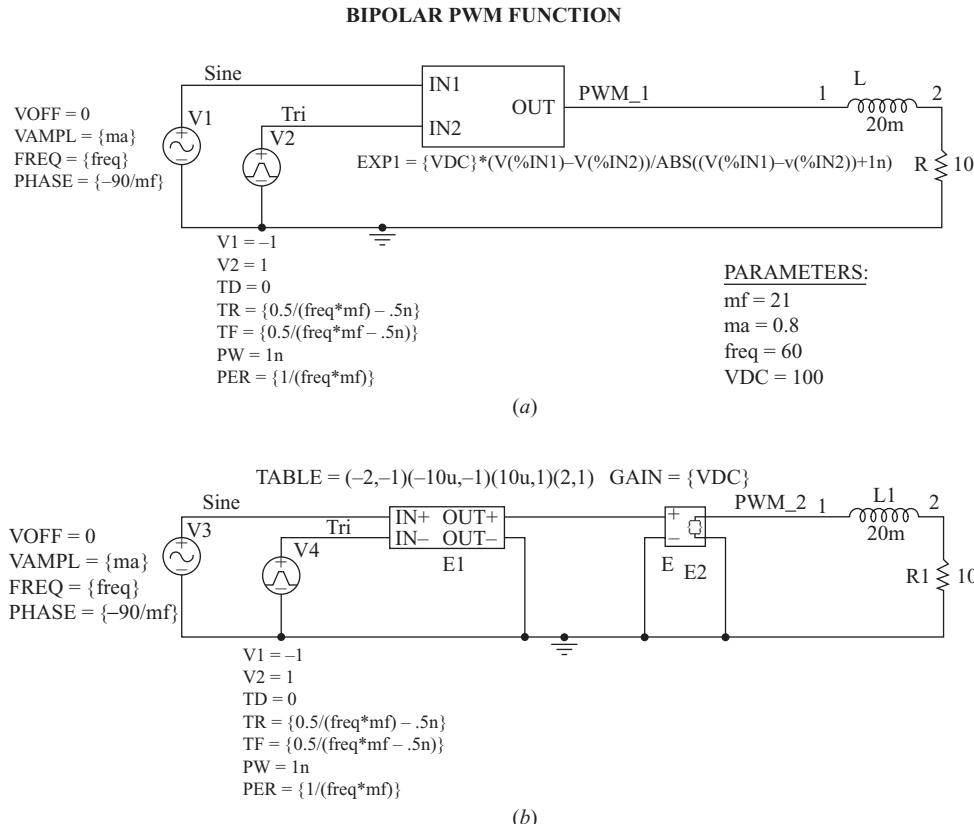


Figure 8-23 PSpice functional circuits for producing a bipolar PWM voltage using (a) an ABM block and (b) an ETABLE voltage source.

a voltage-controlled voltage source ETABLE. Both methods compare a sine wave to a triangular wave. Either method allows the behavior of a specific load to a PWM input to be investigated.

If the load contains an inductance and/or capacitance, there will be an initial transient in the load current. Since the steady-state load current is usually of interest, one or more periods of the load current must be allowed to run before meaningful output is obtained. One way to achieve this in PSpice is to delay output in the transient command, and another way is to restrict the data to steady-state results in Probe. The reference signal is synchronized with the carrier signal as in Fig. 8-17a. When the triangular carrier voltage has negative slope going through zero, the sinusoidal reference voltage must have positive slope going through zero. The triangular waveform starts at the positive peak with negative slope. The phase angle of the reference sinusoid is adjusted to make the zero crossing correspond to that of the triangular wave by using a phase angle of $-90^\circ/m_f$. The following example illustrates a PSpice simulation of a bipolar PWM application.

EXAMPLE 8-10

PSpice Simulation of PWM

Use PSpice to analyze the PWM inverter circuit of Example 8-8.

■ Solution

Using either PWM circuit in Fig. 8-23, the Probe output will be the waveforms shown in Fig. 8-24a. The current is scaled by a factor of 10 to show more clearly its relationship

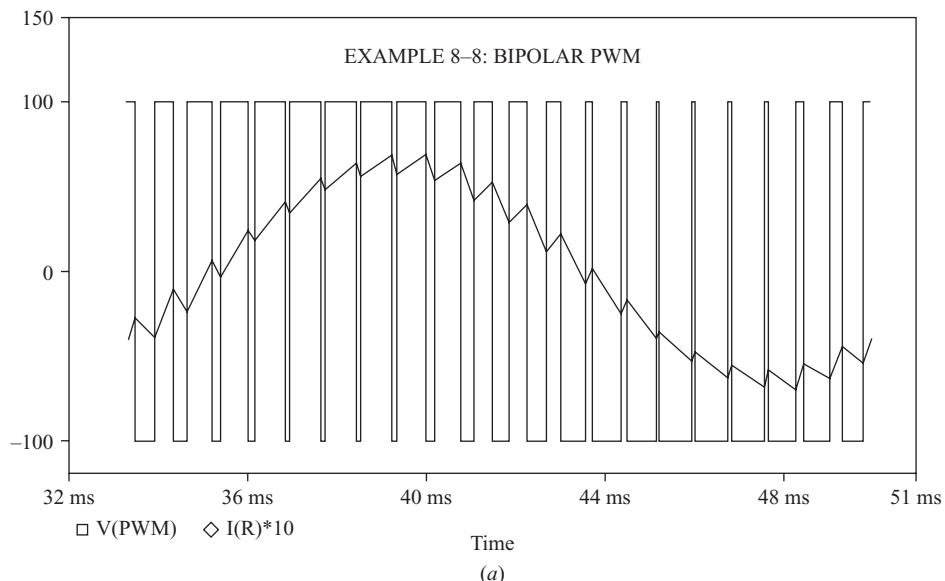
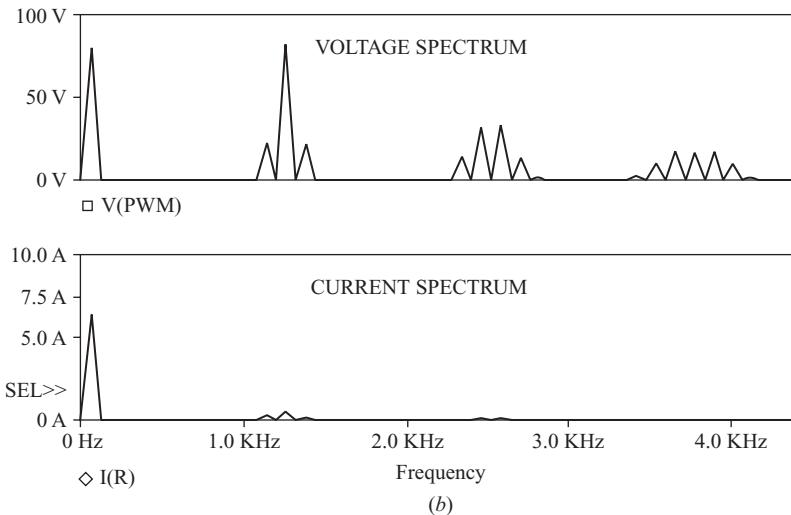


Figure 8-24 (a) Probe output for Example 8-10 showing PWM voltage and load current (current is scaled for illustration); (b) Frequency spectra for voltage and current.

**Figure 8-24 (continued)**

with output voltage. Note the sinelike quality of the current. The Fourier coefficients of voltage and current are determined by using the Fourier option under the x axis menu or by pressing the FFT icon. Figure 8-24b shows the frequency spectra of voltage and current with the range on the x axis selected to show the lower frequencies. The cursor option is used to determine the Fourier coefficients.

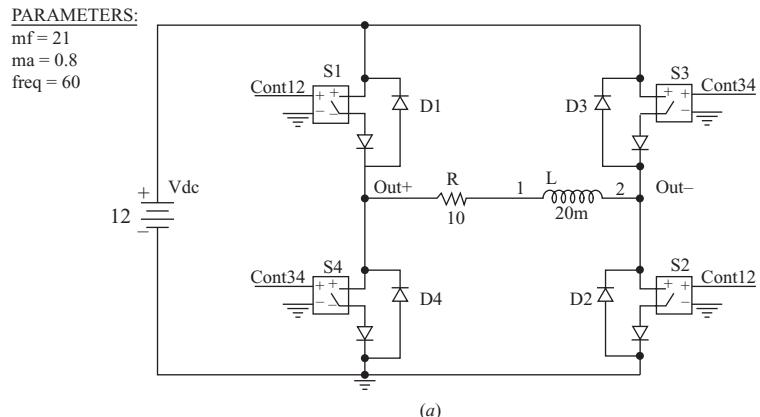
Table 8-6 summarizes the results. Note the close correspondence with the results of Example 8-8.

Table 8-6 PSpice Results of Example 8-10

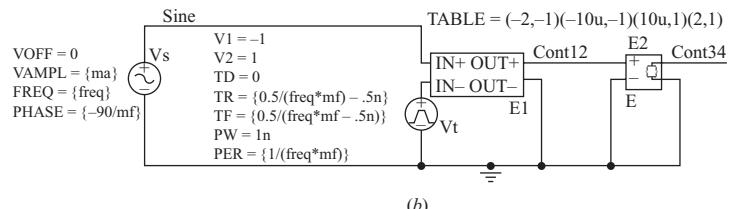
n	f_n (Hz)	V_n (V)	I_n (A)
1	60	79.8	6.37
19	1140	21.8	0.15
21	1260	82.0	0.52
23	1380	21.8	0.13

If the voltages and currents in the source and switches are desired, the PSpice input file must include the switches. A somewhat idealized circuit using voltage-controlled switches with feedback diodes is shown in Fig. 8-25. To simulate pulse-width modulation, the control for the switches in the inverter is the voltage difference between a triangular carrier voltage and a sine reference voltage. While this does not represent a model for real switches, this circuit is useful to simulate either bipolar or unipolar PWM. A more realistic bridge model would include devices such as BJTs, MOSFETs, or IGBTs for the switches. The model that is appropriate will depend on how completely switch performance must be investigated.

BIPOLAR PWM



(a)



(b)

Figure 8-25 PSpice circuits for a PWM inverter (a) using voltage-controlled switches and diodes but requires the full PSpice version and (b) generating a PWM function.

Unipolar PWM

Again, unipolar PWM can be simulated using various levels of switch models. The input file shown in Fig. 8-26 utilizes dependent sources to produce a unipolar PWM output.

UNIPOLAR PWM

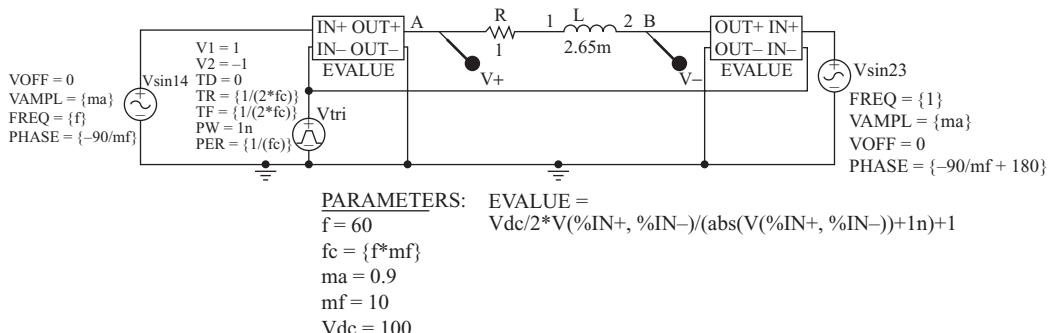


Figure 8-26 A PSpice circuit for generating a unipolar PWM voltage. The output voltage is between nodes A and B.

EXAMPLE 8-11

Pulse-Width Modulation PSpice Simulation

Pulse-width modulation is used to provide a 60-Hz voltage across a series RL load with $R = 1 \Omega$ and $L = 2.65 \text{ mH}$. The dc supply voltage is 100 V. The amplitude of the 60-Hz voltage is to be 90 V, requiring $m_a = 0.9$. Use PSpice to obtain the current waveform in the load and the THD of the current waveform in the load. Use (a) bipolar PWM with $m_f = 21$, (b) bipolar PWM with $m_f = 41$, and (c) unipolar PWM with $m_f = 10$.

Solution

- (a) The PSpice circuit for bipolar PWM (Fig. 8-25b) is run with $m_a = 0.9$ and $m_f = 21$. The voltage across the load and the current in the load resistor are shown in Fig. 8-27a. The currents for the 60-Hz fundamental and the lowest-order harmonics are obtained from the Fourier option under x axis in Probe. The harmonic amplitudes correspond to the peaks, and the cursor option determines precise values. The rms current can be obtained from Probe by entering the expression $\text{RMS}(I(R))$. The total harmonic distortion based on the truncated Fourier series is computed from Eq. (8-17). Results are in the table in this example.
- (b) The PSpice circuit is modified for $m_f = 41$. The voltage and current waveforms are shown in Fig. 8-27b. The resulting harmonic currents are obtained from the Fourier option in Probe.

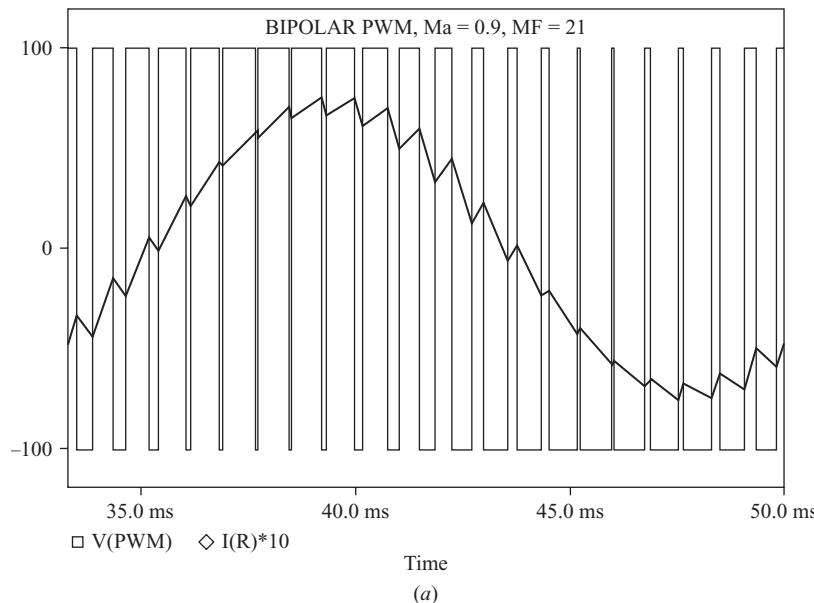


Figure 8-27 Voltage and current for Example 8-11 for (a) bipolar PWM with $m_f = 21$, (b) bipolar PWM with $m_f = 41$, (c) Unipolar PWM with $m_f = 10$.

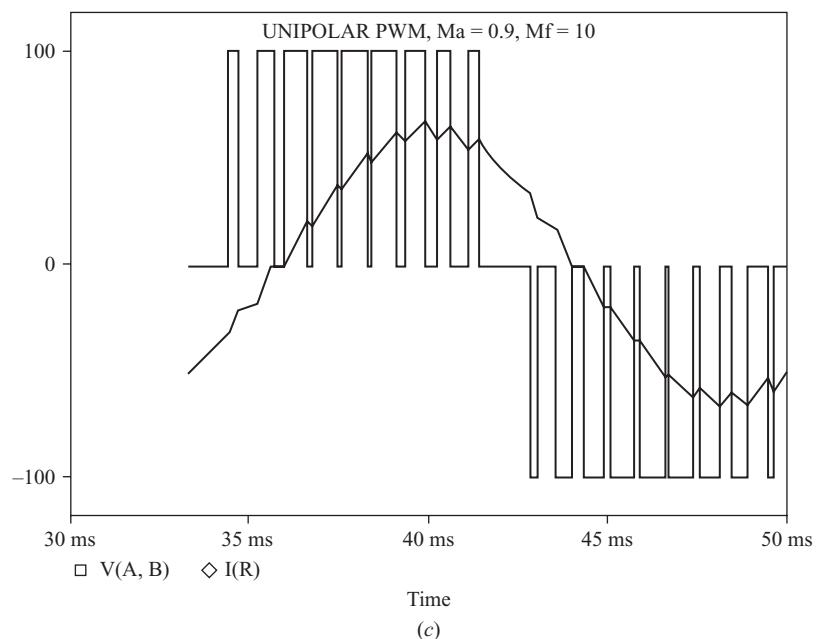
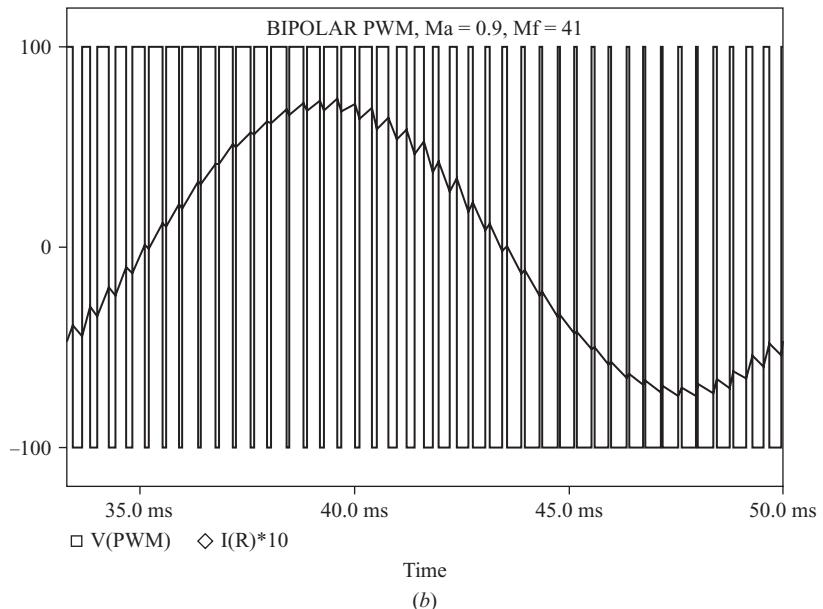


Figure 8-27 (continued)

- (c) The PSpice input file for unipolar switching in Fig. 8-26 is run with the parameter $m_f = 10$. The output voltage and current are shown in Fig. 8-27c. The results of the three simulations for this example are shown in the following table.

Bipolar $m_f = 21$		Bipolar $m_f = 41$		Unipolar $m_f = 10$	
f_n	I_n	f_n	I_n	f_n	I_n
60	63.6	60	64.0	60	62.9
1140	1.41	2340	0.69	1020	1.0
1260	3.39	2460	1.7	1140	1.4
1380	1.15	2580	0.62	1260	1.24
				1380	0.76
I_{rms}	45.1		45.0		44.5
THD	6.1%		3.2%		3.6%

Note that the THD is relatively low in each of these PWM switching schemes, and increasing the switching frequency (increasing m_f) decreases the harmonic currents in this type of a load.

8.15 THREE-PHASE INVERTERS

The Six-Step Inverter

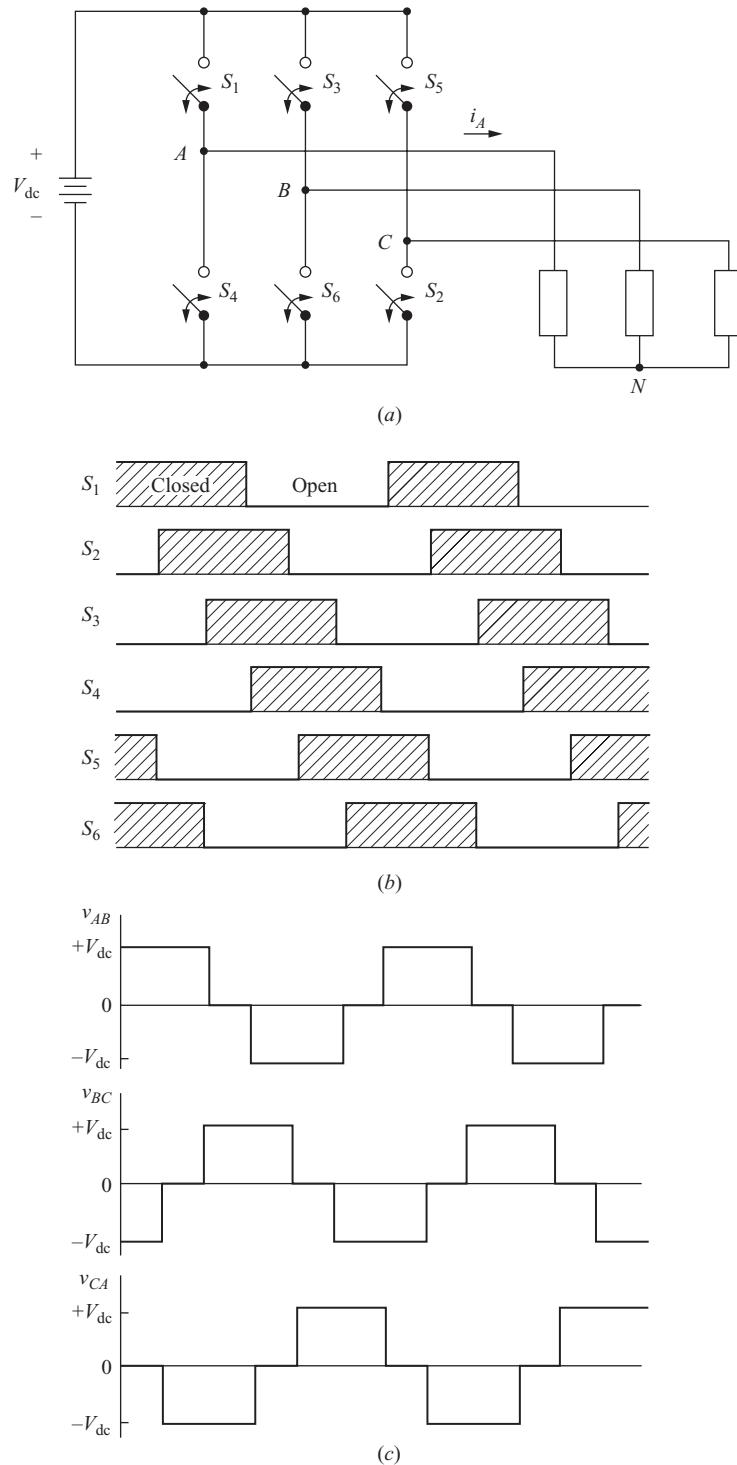
Figure 8-28a shows a circuit that produces a three-phase ac output from a dc input. A major application of this circuit is speed control of induction motors, where the output frequency is varied. The switches are closed and opened in the sequence shown in Fig. 8-28b.

Each switch has a duty ratio of 50 percent (not allowing for blanking time), and a switching action takes place every $T/6$ time interval, or 60° angle interval. Note that switches S_1 and S_4 close and open opposite of each other, as do switch pairs (S_2, S_5) and (S_3, S_6). As with the single-phase inverter, these switch pairs must coordinate so they are not closed at the same time, which would result in a short circuit across the source. With this scheme, the instantaneous voltages v_{A0} , v_{B0} , and v_{C0} are $+V_{dc}$ or zero, and line-to-line output voltages v_{AB} , v_{BC} , and v_{CA} are $+V_{dc}$, 0, or $-V_{dc}$. The switching sequence in Fig. 8-28b produces the output voltages shown in Fig. 8-28c.

The three-phase load connected to this output voltage may be connected in delta or ungrounded neutral wye. For a wye-connected load, which is the more common load connection, the voltage across each phase of the load is a line-to-neutral voltage, shown in Fig. 8-28d. Because of the six steps in the output waveforms for the line-to-neutral voltage resulting from the six switching transitions per period, this circuit with this switching scheme is called a *six-step inverter*.

The Fourier series for the output voltage has a fundamental frequency equal to the switching frequency. Harmonic frequencies are of order $6k \pm 1$ for $k = 1, 2, \dots$ ($n = 5, 7, 11, 13, \dots$). The third harmonic and multiples of the third do not

Figure 8-28 (a) Three-phase inverter; (b) Switching sequence for six-step output; (c) Line-to-line output voltages; (d) Line-to-neutral voltages for an ungrounded Y-connected load; (e) Current in phase A for an RL load.



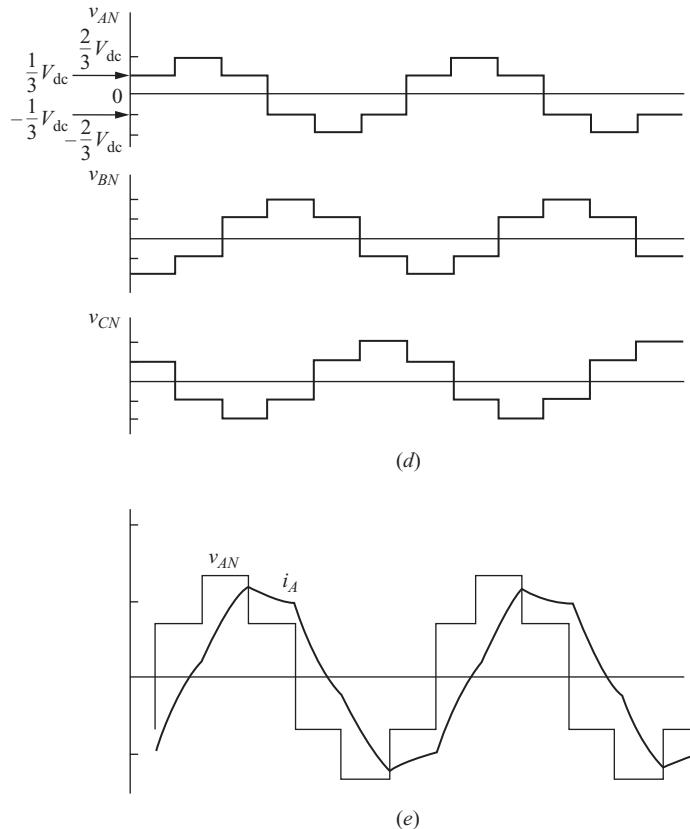


Figure 8-28 (continued)

exist, and even harmonics do not exist. For an input voltage of V_{dc} , the output for an ungrounded wye-connected load has the following Fourier coefficients:

$$V_{n, L-L} = \left| \frac{4V_{dc}}{n\pi} \cos\left(n\frac{\pi}{6}\right) \right|$$

$$V_{n, L-N} = \left| \frac{2V_{dc}}{3n\pi} \left[2 + \cos\left(n\frac{\pi}{3}\right) - \cos\left(n\frac{2\pi}{3}\right) \right] \right| \quad n = 1, 5, 7, 11, 13, \dots \quad (8-42)$$

The THD of both the line-to-line and line-to-neutral voltages can be shown to be 31 percent from Eq. (8-17). The THD of the currents in load-dependent 15 are smaller for an RL load. An example of the line-to-neutral voltage and line current for an RL wye-connected load is shown in Fig. 8-28e.

The output frequency can be controlled by changing the switching frequency. The magnitude of the output voltage depends on the value of the dc supply voltage. To control the output voltage of the six-step inverter, the dc input voltage must be adjusted.

EXAMPLE 8-12**Six-Step Three-Phase Inverter**

For the six-step three-phase inverter of Fig. 8-28a, the dc input is 100 V and the fundamental output frequency is 60 Hz. The load is wye-connected with each phase of the load a series RL connection with $R = 10 \Omega$ and $L = 20 \text{ mH}$. Determine the total harmonic distortion of the load current.

■ Solution

The amplitude of load current at each frequency is

$$I_n = \frac{V_{n,L-N}}{Z_n} = \frac{V_{n,L-N}}{\sqrt{R^2 + (n\omega_0 L)^2}} = \frac{V_{n,L-N}}{\sqrt{10^2 + [n(2\pi 60)(0.02)]^2}}$$

where $V_{n,L-N}$ is determined from Eq. (8-42). Table 8-7 summarizes the results of the Fourier series computation.

Table 8.7 Fourier Components for the Six-Step Inverter of Example 8-12

<i>n</i>	<i>V_{n,L-N}</i> (V)	<i>Z_n</i> (Ω)	<i>I_n</i> (A)	<i>I_{n,rms}</i> (A)
1	63.6	12.5	5.08	3.59
5	12.73	39.0	0.33	0.23
7	9.09	53.7	0.17	0.12
11	5.79	83.5	0.07	0.05
13	4.90	98.5	0.05	0.04

The THD of the load current is computed from Eq. (8-17) as

$$\text{THD}_1 = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,\text{rms}}^2}}{I_{1,\text{rms}}} \approx \frac{\sqrt{(0.23)^2 + (0.12)^2 + (0.05)^2 + (0.04)^2}}{3.59} = 0.07 = 7\%$$

PWM Three-Phase Inverters

Pulse-width modulation can be used for three-phase inverters as well as for single-phase inverters. The advantages of PWM switching are the same as for the single-phase case: reduced filter requirements for harmonic reduction and the controllability of the amplitude of the fundamental frequency.

PWM switching for the three-phase inverter is similar to that of the single-phase inverter. Basically, each switch is controlled by comparing a sinusoidal reference wave with a triangular carrier wave. The fundamental frequency of the output is the same as that of the reference wave, and the amplitude of the output is determined by the relative amplitudes of the reference and carrier waves.

As in the case of the six-step three-phase inverter, switches in Fig. 8-28a are controlled in pairs (S_1, S_4) , (S_2, S_5) , and (S_3, S_6) . When one switch in a pair is closed, the other is open. Each pair of switches requires a separate sinusoidal reference

wave. The three reference sinusoids are 120° apart to produce a balanced three-phase output. Figure 8-29a shows a triangular carrier and the three reference waves. Switch controls are such that

S_1 is on when $v_a > v_{\text{tri}}$

S_2 is on when $v_c > v_{\text{tri}}$

S_3 is on when $v_b > v_{\text{tri}}$

S_4 is on when $v_a < v_{\text{tri}}$

S_5 is on when $v_c < v_{\text{tri}}$

S_6 is on when $v_b < v_{\text{tri}}$

Harmonics will be minimized if the carrier frequency is chosen to be an odd triple multiple of the reference frequency, that is, 3, 9, 15, . . . times the reference. Figure 8-29b shows the line-to-line output voltages for a PWM three-phase inverter.

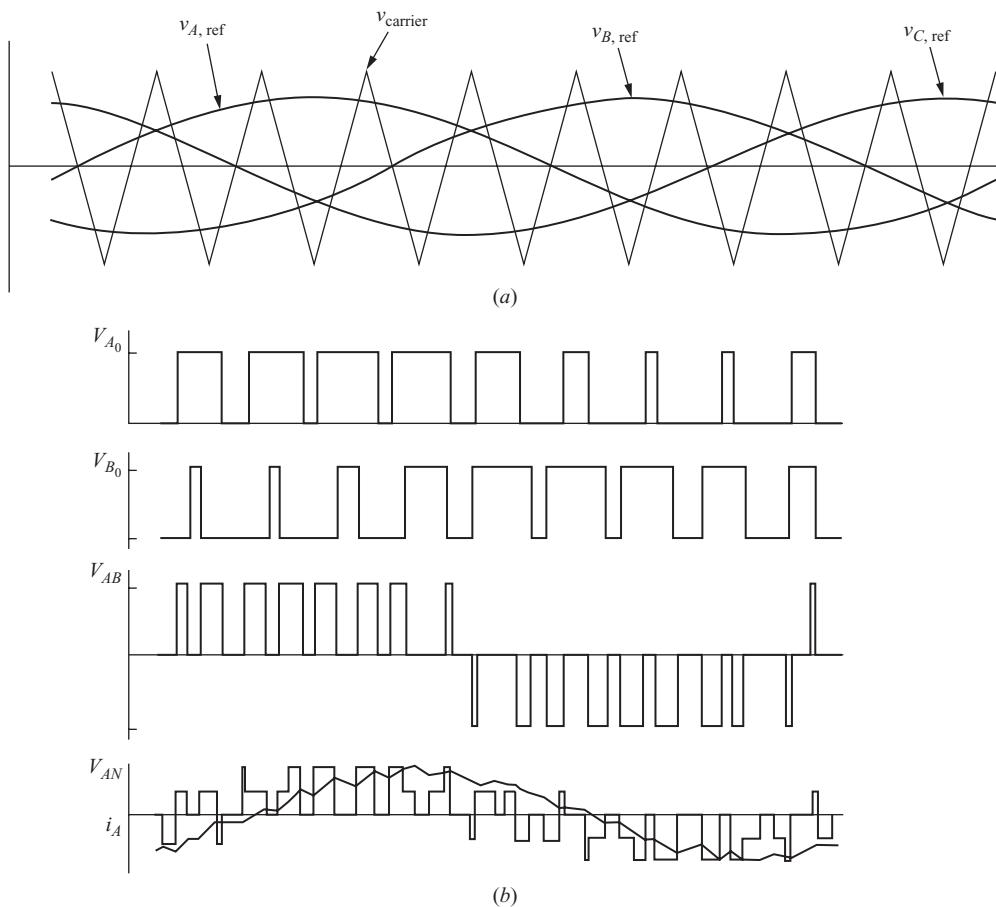


Figure 8-29 (a) Carrier and reference waves for PWM operation with $m_f = 9$ and $m_a = 0.7$ for the three-phase inverter of Fig. 8-28a; (b) Output waveforms—current is for an RL load.

The Fourier coefficients for the line-to-line voltages for the three-phase PWM switching scheme are related to those of single-phase bipolar PWM (V_n in Table 8-3) by

$$V_{n3} = \sqrt{A_{n3}^2 + B_{n3}^2} \quad (8-43)$$

where

$$\begin{aligned} A_{n3} &= V_n \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \\ B_{n3} &= V_n \cos\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \end{aligned} \quad (8-44)$$

Significant Fourier coefficients are listed in Table 8-8.

Table 8-8 Normalized Amplitudes V_{n3}/V_{dc} for Line-to-Line Three-Phase PWM Voltages

	$m_a = 1$	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
$n = 1$	0.866	0.779	0.693	0.606	0.520	0.433	0.346	0.260	0.173	0.087
$m_f = 2$	0.275	0.232	0.190	0.150	0.114	0.081	0.053	0.030	0.013	0.003
$2m_f = 1$	0.157	0.221	0.272	0.307	0.321	0.313	0.282	0.232	0.165	0.086

Multilevel Three-Phase Inverters

Each of the multilevel inverters described in Sec. 8.9 can be expanded to three-phase applications. Figure 8-30 shows a three-phase diode-clamped multilevel inverter circuit. This circuit can be operated to have a stepped-level output similar to the six-step converter, or, as is most often the case, it can be operated to have a pulse-width-modulated output.

8.16 PSPICE SIMULATION OF THREE-PHASE INVERTERS

Six-Step Three-Phase Inverters

PSpice circuits that will simulate a six-step three-phase inverter are shown in Fig. 8-31. The first circuit is for a complete switching scheme described in Fig. 8-28. Voltage-controlled switches with feedback diodes are used for switching. (The full version of PSpice is required for this circuit.) The second circuit is for generating the appropriate output voltages for the converter so load currents can be analyzed. The output nodes of the inverter are nodes *A*, *B*, and *C*. The parameters shown are those in Example 8-12.

PWM Three-Phase Inverters

The circuit in Fig. 8-32 produces the voltages of the PWM three-phase inverter without showing the switching details. Dependent sources compare sine waves to a triangular carrier wave, as in Example 8-8 for the single-phase case.

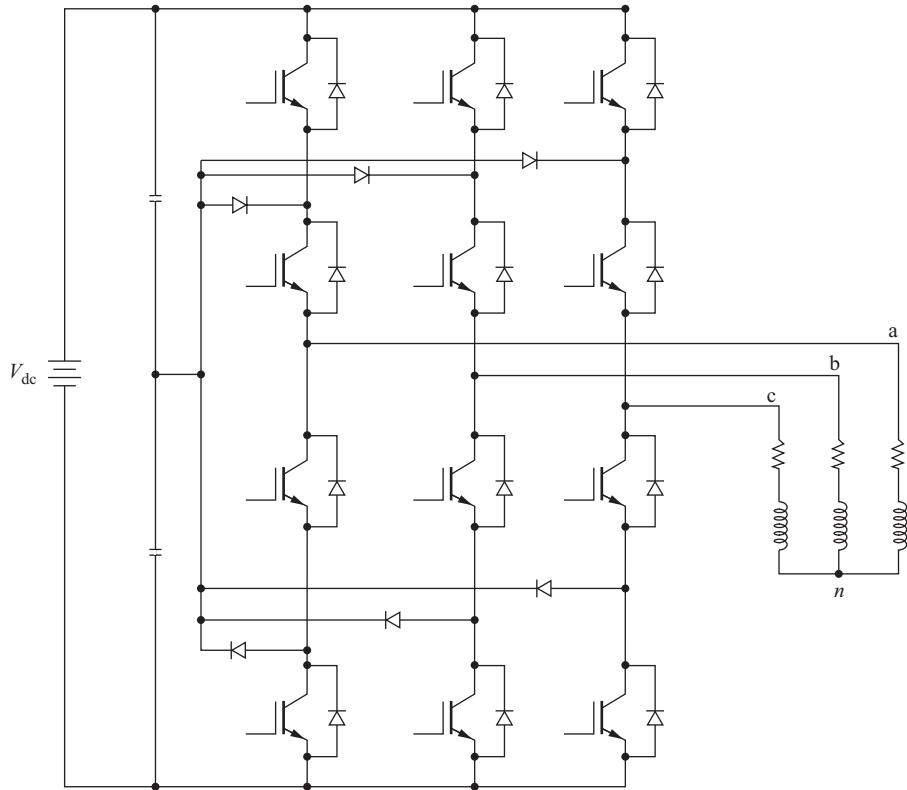


Figure 8-30 A three-phase diode-clamped multilevel inverter.

8.17 INDUCTION MOTOR SPEED CONTROL

The speed of an induction motor can be controlled by adjusting the frequency of the applied voltage. The synchronous speed ω_s of an induction motor is related to the number of poles p and the applied electrical frequency ω by

$$\omega_s = \frac{2\omega}{p} \quad (8-45)$$

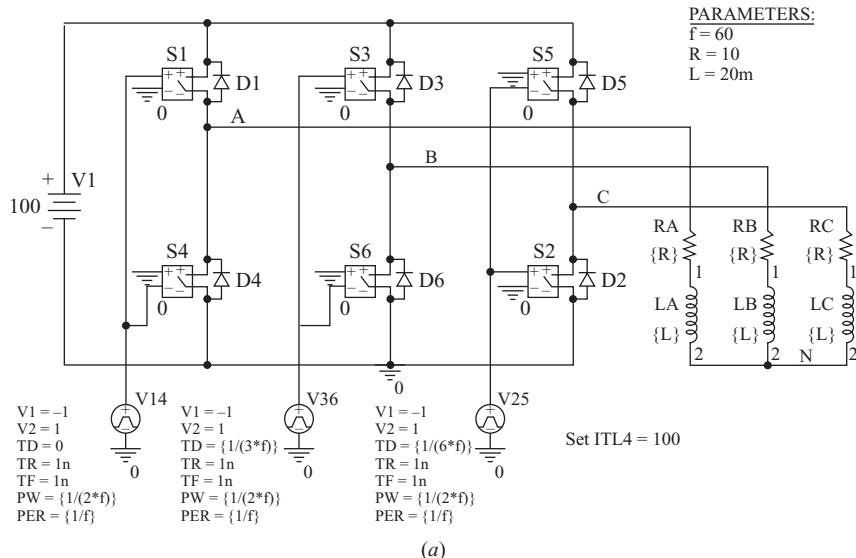
Slip s , is defined in terms of the rotor speed ω_r

$$s = \frac{\omega_s - \omega_r}{\omega_s} \quad (8-46)$$

and torque is proportional to slip.

If the applied electrical frequency is changed, the motor speed will change proportionally. However, if the applied voltage is held constant when the frequency is lowered, the magnetic flux in the air gap will increase to the point of

THREE-PHASE SIX-STEP INVERTER



SIX-STEP INVERTER EQUIVALENT

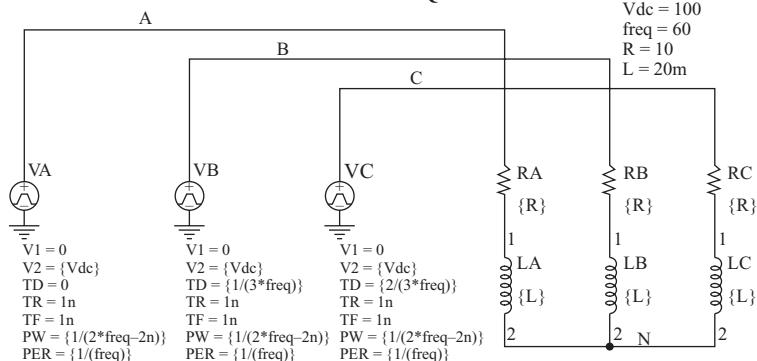


Figure 8-31 (a) A six-step inverter using switches and diodes (requires the full PSpice version); (b) A PSpice circuit for generating three-phase six-step converter voltages.

saturation. It is desirable to keep the air-gap flux constant and equal to its rated value. This is accomplished by varying the applied voltage proportionally with frequency. The ratio of applied voltage to applied frequency should be constant.

$$\frac{V}{f} = \text{constant} \quad (8-47)$$

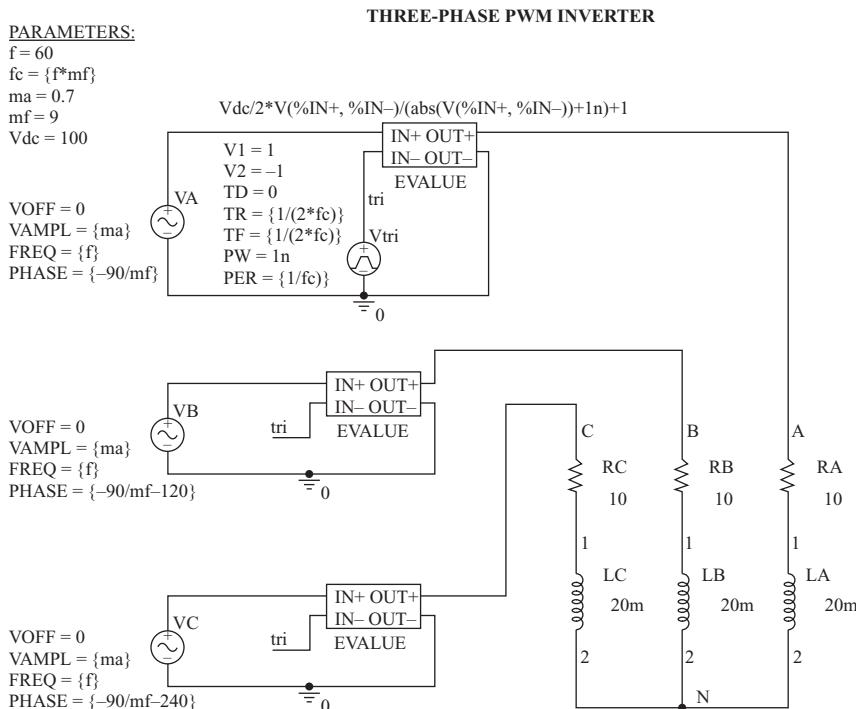


Figure 8-32 A PSpice functional circuit for generating three-phase PWM voltages.

The term *volts/hertz control* is often used for this situation. The induction motor torque-speed curves of Fig. 8-33 are for different frequencies and constant volts/hertz.

The six-step inverter can be used for this application if the dc input is adjustable. In the configuration of Fig. 8-34, an adjustable dc voltage is produced from a controlled rectifier, and an inverter produces an ac voltage at the desired

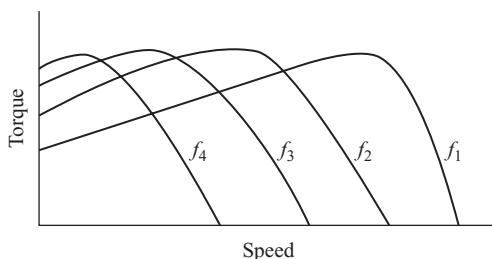


Figure 8-33 Induction motor torque-speed curves for constant volts/hertz variable-speed control.

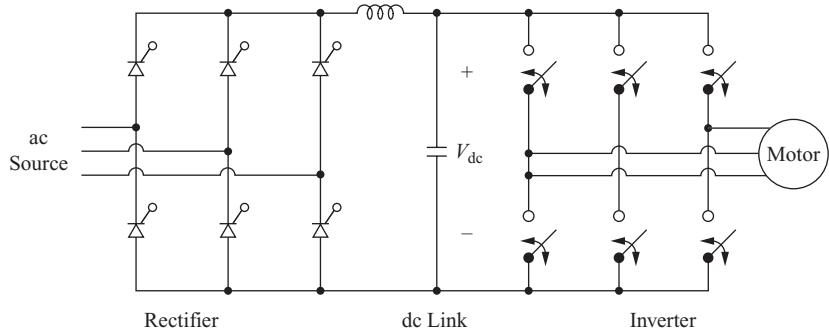


Figure 8-34 AC-AC converter with a dc link.

frequency. If the dc source is not controllable, a dc-dc converter may be inserted between the dc source and the inverter.

The PWM inverter is useful in a constant volts/hertz application because the amplitude of the output voltage can be adjusted by changing the amplitude modulation ratio m_a . The dc input to the inverter can come from an uncontrolled source in this case. The configuration in Fig. 8-34 is classified as an ac-ac converter with a dc link between the two ac voltages.

8.18 Summary

- The full- or half-bridge converters can be used to synthesize an ac output from a dc input.
- A simple switching scheme produces a square wave voltage output, which has a Fourier series that contains the odd harmonic frequencies of amplitudes

$$V_n = \frac{4V_{dc}}{n\pi}$$

- Amplitude and harmonic control can be implemented by allowing a zero-voltage interval of angle α at each end of a pulse, resulting in Fourier coefficients

$$V_n = \left(\frac{4V_{dc}}{n\pi} \right) \cos(n\alpha)$$

- Multilevel inverters use more than one dc voltage source or split a single voltage source with a capacitor voltage divider to produce multiple voltage levels on the output of an inverter.
- Pulse-width modulation (PWM) provides amplitude control of the fundamental output frequency. Although the harmonics have large amplitudes, they occur at high frequencies and are filtered easily.
- Class D audio amplifiers use PWM techniques for high efficiency.
- The six-step inverter is the basic switching scheme for producing a three-phase ac output from a dc source.
- A PWM switching scheme can be used with a three-phase inverter to reduce the THD of the load current with modest filtering.
- Speed control of induction motors is a primary application of three-phase inverters.

8.19 Bibliography

- J. Almazan, N. Vazquez, C. Hernandez, J. Alvarez, and J. Arau, "Comparison between the Buck, Boost and Buck-Boost Inverters," *International Power Electronics Congress*, Acapulco, Mexico, October 2000, pp. 341–346.
- B. K. Bose, *Power Electronics and Motor Drives: Advances and Trends*, Elsevier/Academic Press, 2006.
- J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and D. Zhong, "A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters," *IEEE Transactions on Power Electronics*, March 2004, pp. 478–490.
- K. A. Corzine, "Topology and Control of Cascaded Multi-Level Converters," Ph.D. dissertation, University of Missouri, Rolla, 1997.
- T. Kato, "Precise PWM Waveform Analysis of Inverter for Selected Harmonic Elimination," 1986 IEEE/IAS Annual Meeting, pp. 611–616.
- N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3d ed., Wiley, New York, 2003.
- L. G. Franquelo, "Multilevel Converters: Current Developments and Future Trends," *IEEE International Conference on Industrial Technology*, Chengdu, China, 2008.
- J. R. Hauser, *Numerical Methods for Nonlinear Engineering Models*, Springer Netherlands, Dordrecht, 2009.
- J. Holtz, "Pulsewidth Modulation—A Survey," *IEEE Transactions on Industrial Electronics*, vol. 39, no. 5, Dec. 1992, pp. 410–420.
- S. Miaozen, F. Z. Peng, and L. M. Tolbert, "Multi-level DC/DC Power Conversion System with Multiple DC Sources," *IEEE 38th Annual Power Electronics Specialists Conference*, Orlando, Fla., 2007.
- L. M. Tolbert, and F. Z. Peng, "Multilevel Converters for Large Electric Drives," *Applied Power Electronics Conference and Exposition*, anaheim, Calif., 1998.
- M. H. Rashid, *Power Electronics: Circuits, Devices, and Systems*, 3d ed., Prentice-Hall, Upper Saddle River, N.J., 2004.
- L. Salazar and G. Joos, "PSpice Simulation of Three-Phase Inverters by Means of Switching Functions," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, Jan. 1994, pp. 35–42.
- B. Wu, *High-Power Converters and AC Drives*, Wiley, New York, 2006.
- X. Yuan, and I. Barbi, "Fundamentals of a New Diode Clamping Multilevel Inverter," *IEEE Transactions on Power Electronics*, vol. 15, no. 4, July 2000, pp. 711–718.

Problems

Square-Wave Inverter

- 8-1.** The square-wave inverter of Fig. 8-1a has $V_{dc} = 125$ V, an output frequency of 60 Hz, and a resistive load of 12.5Ω . Sketch the currents in the load, each switch, and the source, and determine the average and rms values of each.
- 8-2.** A square-wave inverter has a dc source of 96 V and an output frequency of 60 Hz. The load is a series RL load with $R = 5 \Omega$ and $L = 100$ mH. When the load is first energized, a transient precedes the steady-state waveform described

by Eq. (8-5). (a) Determine the peak value of the steady-state current. (b) Using Eq. (8-1) and assuming zero initial inductor current, determine the maximum current that occurs during the transient. (c) Simulate the circuit with the PSpice input file of Fig. 8.4a and compare the results with parts (a) and (b). How many periods must elapse before the current reaches steady state? How many L/R time constants elapse before steady state?

- 8-3.** The square-wave inverter of Fig. 8-3 has a dc input of 150 V and supplies a series RL load with $R = 20 \Omega$ and $L = 40 \text{ mH}$. (a) Determine an expression for steady-state load current. (b) Sketch the load current and indicate the time intervals when each switch component ($Q_1, D_1; \dots, Q_4, D_4$) is conducting. (c) Determine the peak current in each switch component. (d) What is the maximum voltage across each switch? Assume ideal components.
- 8-4.** A square-wave inverter has a dc source of 125 V, an output frequency of 60 Hz, and an RL series load with $R = 20 \Omega$ and $L = 25 \text{ mH}$. Determine (a) an expression for load current, (b) rms load current, and (c) average source current.
- 8-5.** A square-wave inverter has an RL load with $R = 15 \Omega$ and $L = 10 \text{ mH}$. The inverter output frequency is 400 Hz. (a) Determine the value of the dc source required to establish a load current that has a fundamental frequency component of 8 A rms. (b) Determine the THD of the load current.
- 8-6.** A square-wave inverter supplies an RL series load with $R = 25 \Omega$ and $L = 25 \text{ mH}$. The output frequency is 120 Hz. (a) Specify the dc source voltage such that the load current at the fundamental frequency is 2.0 A rms. (b) Verify your results with PSpice. Determine the THD from PSpice.
- 8-7.** A square-wave inverter has a dc input of 100 V, an output frequency of 60 Hz, and a series RLC combination with $R = 10 \Omega$, $L = 25 \text{ mH}$, and $C = 100 \mu\text{F}$. Use the PSpice simplified square-wave inverter circuit of Fig. 8-4a to determine the peak and rms value of the steady-state current. Determine the total harmonic distortion of the load current. On a printout of one period of the current, indicate the intervals where each switch component in the inverter circuit of Fig. 8-3 is conducting for this load if that circuit were used to implement the converter.

Amplitude and Harmonic Control

- 8-8.** For the full-bridge inverter, the dc source is 125 V, the load is a series RL connection with $R = 10 \Omega$ and $L = 20 \text{ mH}$, and the switching frequency is 60 Hz. (a) Use the switching scheme of Fig. 8-5 and determine the value of α to produce an output with an amplitude of 90 V at the fundamental frequency. (b) Determine the THD of the load current.
- 8-9.** An inverter that produces the type of output shown in Fig. 8-5a is used to supply an RL series load with $R = 10 \Omega$ and $L = 35 \text{ mH}$. The dc input voltage is 200 V and the output frequency is 60 Hz. (a) Determine the rms value of the fundamental frequency of the load current when $\alpha = 0$. (b) If the output fundamental frequency is lowered to 30 Hz, determine the value of α required to keep the rms current at the fundamental frequency at the same value of part (a).
- 8-10.** Use the PSpice circuit of Fig. 8-7a to verify that (a) the waveform of Fig. 8-5a with $\alpha = 30^\circ$ contains no third harmonic frequency and (b) the waveform of Fig. 8-5a with $\alpha = 18^\circ$ contains no fifth harmonic.
- 8-11.** (a) Determine the value of α that will eliminate the seventh harmonic from the inverter output of Fig. 8-5a. (b) Verify your answer with a PSpice simulation.

- 8-12.** Determine the rms value of the notched waveform to eliminate the third and fifth harmonics in Fig. 8-6.
- 8-13.** Use PSpice to verify that the notched waveform of Fig. 8-6c contains no third or fifth harmonic. What are the magnitudes of the fundamental frequency and the first four nonzero harmonics? (The piecewise linear type of source may be useful.)

Multilevel Inverters

- 8-14.** For a multilevel inverter having three separate dc sources of 48 V each, $\alpha_1 = 15^\circ$, $\alpha_2 = 25^\circ$, and $\alpha_3 = 55^\circ$. (a) Sketch the output voltage waveform. (b) Determine the Fourier coefficients through $n = 9$. (c) Determine the modulation index M_i .
- 8-15.** For a three-source multilevel inverter, select values of α_1 , α_2 , and α_3 such that the third harmonic frequency ($n = 3$) in the output voltage waveform is eliminated. Determine the modulation index M_i for your selection.
- 8-16.** The five-source multilevel inverter of Fig. 8-11 has $\alpha_1 = 16.73^\circ$, $\alpha_2 = 26.64^\circ$, $\alpha_3 = 46.00^\circ$, $\alpha_4 = 60.69^\circ$, and $\alpha_5 = 62.69^\circ$. Determine which harmonics will be eliminated from the output voltage. Determine the amplitude of the fundamental-frequency output voltage.
- 8-17.** The concept of the two-source multilevel inverters of Figs. 8-9 and 8-11 is extended to have three independent sources and H bridges and three delay angles α_1 , α_2 , and α_3 . Sketch the voltages at the output of each bridge of a three-source multilevel converter such that the average power from each source is the same.

Pulse-Width-Modulated Inverters

- 8-18.** The dc source supplying an inverter with a bipolar PWM output is 96 V. The load is an RL series combination with $R = 32 \Omega$ and $L = 24 \text{ mH}$. The output has a fundamental frequency of 60 Hz. (a) Specify the amplitude modulation ratio to provide a 54-V rms fundamental frequency output. (b) If the frequency modulation ratio is 17, determine the total harmonic distortion of the load current.
- 8-19.** The dc source supplying an inverter with a bipolar PWM output is 250 V. The load is an RL series combination with $R = 20 \Omega$ and $L = 50 \text{ mH}$. The output has a fundamental frequency of 60 Hz. (a) Specify the amplitude modulation ratio to provide a 160-V rms fundamental frequency output. (b) If the frequency modulation ratio is 31, determine the total harmonic distortion of the load current.
- 8-20.** Use PSpice to verify that the design in Example 8-9 meets the THD specifications.
- 8-21.** Design an inverter that has a PWM output across an RL series load with $R = 10 \Omega$ and $L = 20 \text{ mH}$. The fundamental frequency of the output voltage must be 120 V rms at 60 Hz, and the total harmonic distortion of the load current must be less than 8 percent. Specify the dc input voltage, the amplitude modulation ratio m_a , and the switching frequency (carrier frequency). Verify the validity of your design with a PSpice simulation.
- 8-22.** Design an inverter that has a PWM output across an RL series load with $R = 30 \Omega$ and $L = 25 \text{ mH}$. The fundamental frequency of the output voltage must be 100 V rms at 60 Hz, and the total harmonic distortion of the load current must be less than 10 percent. Specify the dc input voltage, the amplitude modulation ratio m_a , and the switching frequency (carrier frequency). Verify the validity of your design with a PSpice simulation.

- 8-23.** Pulse-width modulation is used to provide a 60-Hz voltage across a series RL load with $R = 12 \Omega$ and $L = 20 \text{ mH}$. The dc supply voltage is 150 V. The amplitude of the 60-Hz voltage is to be 120 V. Use PSpice to obtain the current waveform in the load and the THD of the current waveform in the load. Use (a) bipolar PWM with $m_f = 21$, (b) bipolar PWM with $m_f = 41$, and (c) unipolar PWM with $m_f = 10$.

Three-Phase Inverters

- 8-24.** A six-step three-phase inverter has a 250-V dc source and an output frequency of 60 Hz. A balanced Y-connected load consists of a series $25\text{-}\Omega$ resistance and 20-mH inductance in each phase. Determine (a) the rms value of the 60-Hz component of load current and (b) the THD of the load current.
- 8-25.** A six-step three-phase inverter has a 400-V dc source and an output frequency that varies from 25 to 100 Hz. The load is a Y connection with a series $10\text{-}\Omega$ resistance and 30-mH inductance in each phase. (a) Determine the range of the rms value of the fundamental-frequency component of load current as the frequency is varied. (b) What is the effect of varying frequency on the THD of the load current and the THD of the line-to-neutral voltage?
- 8-26.** A six-step three-phase inverter has an adjustable dc input. The load is a balanced Y connection with a series RL combination in each phase, with $R = 5 \Omega$ and $L = 50 \text{ mH}$. The output frequency is to be varied between 30 and 60 Hz. (a) Determine the range of the dc input voltage required to maintain the fundamental-frequency component of current at 10 A rms. (b) Use PSpice to determine the THD of load current in each case. Determine the peak current and rms load current for each case.