Universidad de Costa Rica
Facultad de Ingeniería
Escuela de Ingeniería Eléctrica
IE-0624 –Laboratorio de Microcontroladores
II ciclo 2023

Laboratorio 5

STM32/Arduino: GPIO, Giroscopio, comunicaciones y TinyML

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1. Resumen

En este quinto laboratorio se busca desarrollar un controlador por voz, para esto es necesario utilizar el kit de Arduino Nano 33 BLE. Por lo tanto, se crea un programa para el microcontrolador que captura la información de audio y luego ésta es enviada a la computadora por el puerto USB, seguidamente por medio de la plataforma Edge Impulse se registran tres comandos de voz y también uno extra que no es considerado un comando sino que contiene ruido de fondo, de forma que se realiza lo siguiente: se carga la información de los comandos de voz, después se configura la red neuronal y se entrena esta red neuronal, por último se exporta el modelo obtenido al microcontrolador. Este modelo exportado es utilizado para poder realizar el reconocimiento del comando de voz, en el script de python utiliza el modelo de la red neuronal construida para detectar el tipo de comando, los comandos detectados son enviados a la PC con la palabra asociada al mismo, además en este script guarda la información recibida del micrófono del microcontrolador y etiqueta según el tipo de comando de voz mencionado, al final guarda la información en un archivo que se crea cuando finaliza el programa, y al final se envia a la plataforma de Iot los comandos y activar un widget que represente la acción, cabe destacar que esta plataforma fue la misma utilizada en el laboratorio anterior por lo que se tiene este conocimiento previo.

2. Nota Teórica

En la presente sección, se muestra el microcontrolador utilizado, además de los componentes y periféricos usados, con el diseño del circuito final.

2.1. Microcontrolador nRF52840

La compañía Nordic Semiconductor diseñó este microcontrolador nRF52840, como parte de la familiar de microcontroladores de nRF52, parte de las características más importantes que posee este microcontrolador son las siguientes [1]:

1. El dispositivo tiene protocolos Bluetooth 5, por lo permite transferencia de datos de 2 Mbps, además de una criptografía por hardware ARM TrusZone Cryptocell 310 security subsystem.

2. Este microcontrolador posee una arquitectura de 32 bits ARM Cortex-M4 y también puede trabajar con una velocidad de reloj de 64 MHz.

3. Con respecto a la memoria, tiene una memoria Flash de 1 MB, además de una memoria SRAM de 256 KB.

4. Ahora de periféricos, posee el de 48 puertos GPIO para la interfaz de componentes externos, convertidores analógico-digital con 8 canales para la lectura de los sensores e interfaces de comunicación como UART, I2C y SPI.

El diagrama de bloques para el microcontrolador nRF52840 se muestra en la siguiente Figura 1

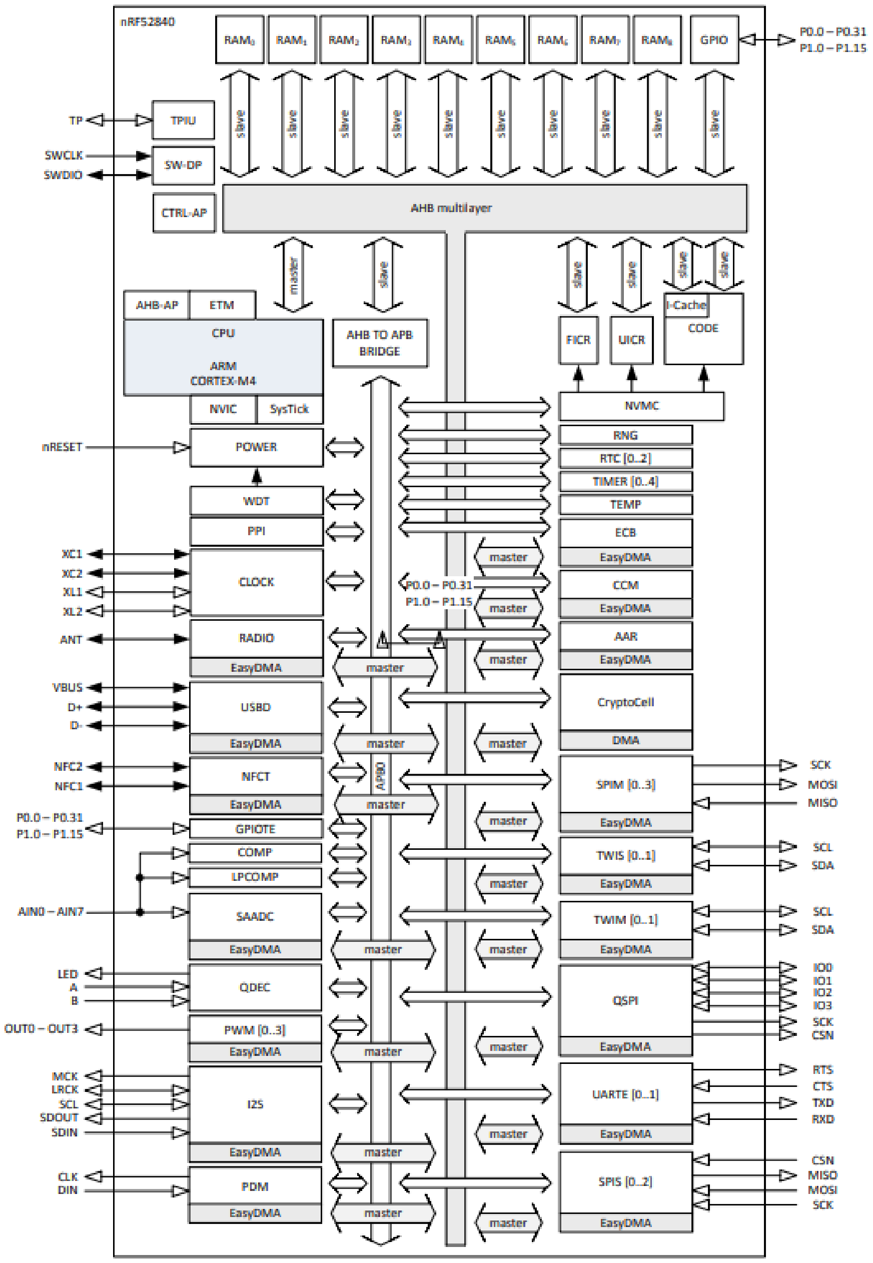


Figura 1: Diagrama de bloques nRF52840. Recuperado de [1]

2.2. Arduino Nano 33 BLE Sense

El arduino Nano 33 BLE Sense tiene placas de HW+SW libre con microcontrolador programable. Además la mayoría de microcontroladores pertenecen a la misma familia (AVR), además posee su IDE y tiene como lenguaje (C/C++), lo anterior inspiradas en Processing, por último su hardware esta inspirado en la placa libre Wiring. [2]
En la siguiente Figura 2 se muestra la placa del arduino nano 33 ble sense.

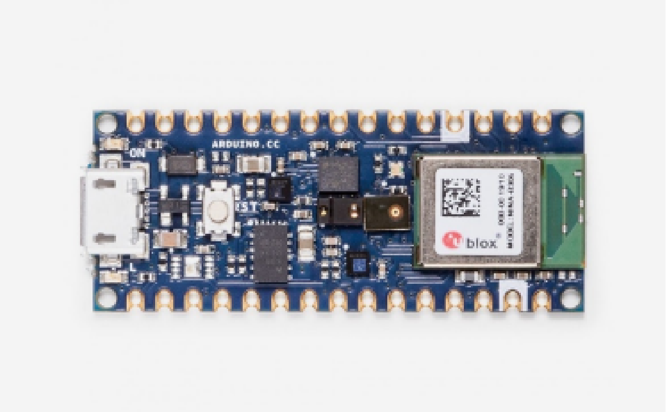


Figura 2: Placa Arduino Nano BLE 33 Sense. Recuperado de [2]

Ahora, para el Arduino Nano BLE 33 Sense TinyMLkit algunas de las características que lo conforma son las siguientes[2]:

1. La placa es versátil y compacta, con 11 sensores.
2. Está diseñada para aplicaciones de bajo consumo y posee una conectividad BLE. es decir Bluetooth Low Energy.
3. Se basa en el microcontrolador nRF52840 de Nordic Semiconductor.
4. Tiene un sensor de proximidad, color RGB, intensidad de luz y detección de gestos APDS9960, cámara OV7675 y micrófono digital.
5. Además, posee un giroscopio, magnetómetro en la placa (IMU LSM9DS1 de 9 ejes) y un acelerómetro.
6. Tiene soporte de MicroPython.
7. La versión Lite no tiene el sensor HTS221 de temperatura y humedad, pero si tiene el LPS22H, que es un sensor de presión y temperatura.

Ahora el diagrama de pines para este arduino se presenta en la Figura 3 y la topología que tiene en la Figura 4

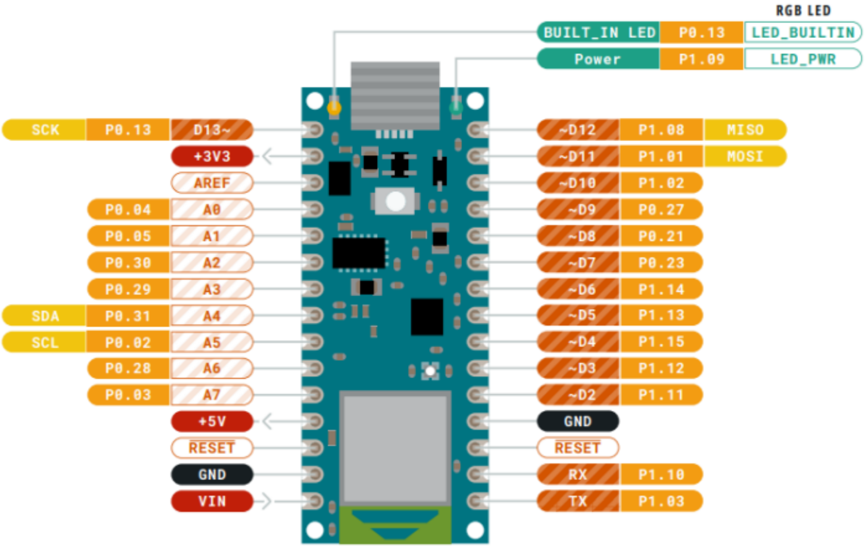


Figura 3: Pines del arduino nano ble 33 Sense . Recuperado de [2]

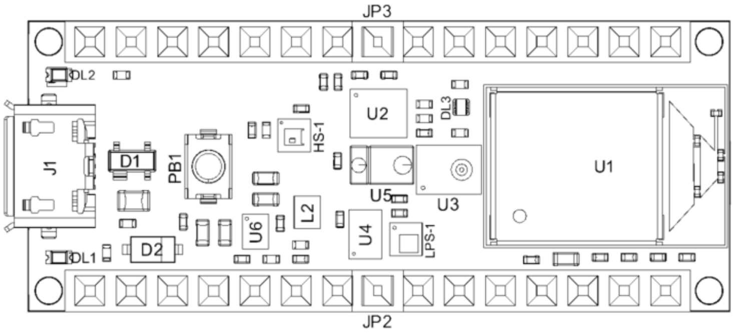


Figura 4: Topología del Arduino Nano BLE 33 Sense. Recuperado de [2]

2.3. LPS22HB

La compañía que diseñó el LPS22HB es STMicroelectronics, este es un sensor de medición de temperatura y presión, el cuál es de bajo consumo de energía y muy preciso [3]. Ahora algunas de sus características según la hoja de datos son las siguientes;

1. El sensor comunica también con otros dispositivos mediante la interfaz ISC de dos hilos, también posee registros internos para configurar y controlar diferentes modos de frecuencia de muestreo y de su funcionamiento.

2. Posee el sensor para medir la presión atmosférica.

3. Tiene un ternómetro de alta precisión que mide la temperatura ambiente.

El diagrama de bloques y el diagrama de pines para este dispositivo LPS22HB se presentan en las Figuras 5 y 6 de forma respectiva.

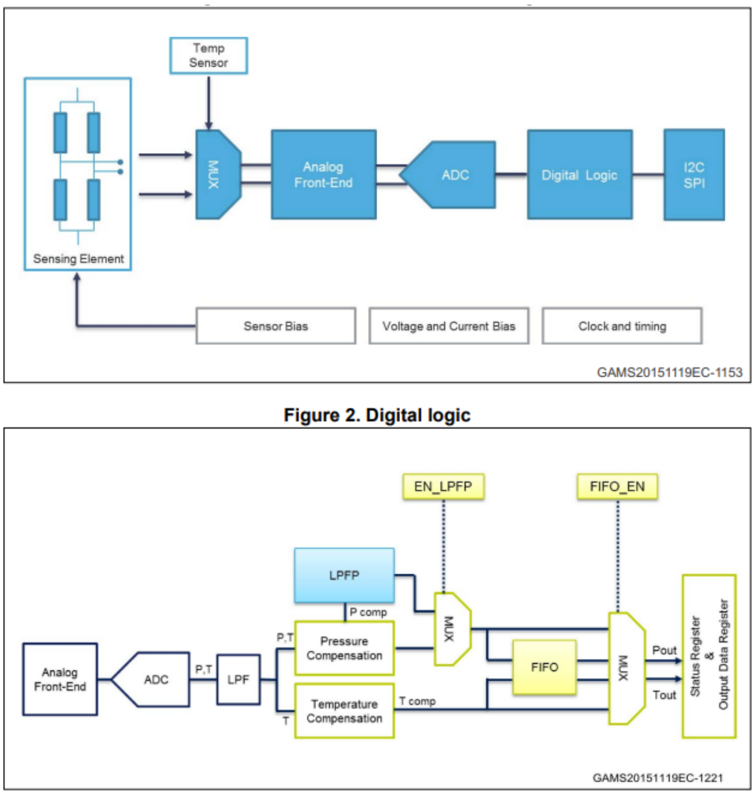


Figure 2. Digital logic

Figura 5: Diagrama de pines del sensor LPS22HB . Recuperado de [3]

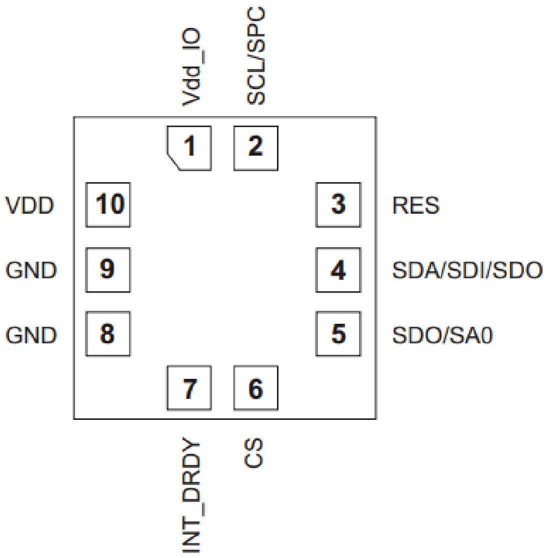


Figura 6: Diagrama de pines del sensor LPS22HB . Recuperado de [3]

2.4. APDS-9960

La compañia Broadcom diseñó el dispositivo APDS-9960 que es un sensor de detección, que logra capturar proximidad y gestos. Como parte de las características que posee este dispositivo según la hoja de datos, se destacan las siguientes [4]:

1. El detector de proximidad usa un emisor de luz infrarroja y un receptor para poder captar los objetos.
2. Utilizando el I2C puede configurarse el sensor para recibir datos de detección y controlar estas funciones.
3. Puede medir la luz ambiental y da información sobre la intensidad de luz, además puede medir el color de la luz ambiente.

En las siguientes Figuras 7 y 8 se muestra el diagrama de bloques del sensor y el dispositivo como tal de forma respectiva.

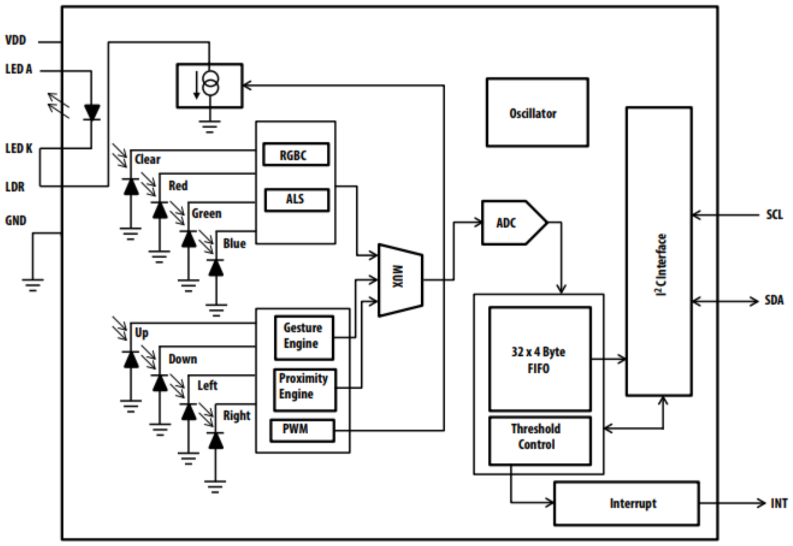


Figura 7: Diagrama de bloques del APDS-9960 . Recuperado de [4]

Figura 8: Sensor APDS-9960 . Recuperado de [4]

2.5. TensorFlow Lite

Tensorflow pertenece al área de aprendizaje automático con redes neuronales e inteligencia artificial, el cuál posee un biblioteca que es de software open source [5]. Entonces Tensorflow Lite fue diseñado para la interferencia en el dispositivo a partir de un marco de aprendizaje profundo de código abierto, en la librería se caracteriza porque proporciona las herramientas que permiten el aprendizaje automático en el dispositivo de forma que da una posibilidad de que los desarrolladores puedan ejecutar sus modelos entrenados en dispositivos o computadoras [5]. Con respecto a la compatibilidad, puede utilizarse con Linux, SO dispositivos móviles y MCU.

2.6. TinyML

TinyML está dirigido a un campo de crecimiento en tecnologías y aprendizaje automático. Donde se incluyen aspectos tanto de software, hardware y algoritmos capaces de realizar análisis de datos de sensores en dispositivos para diferentes áreas como biomédicos, visión, IMU entre otros más [6]. Se caracterizan por consumir una cantidad muy baja de potencia, de forma normal en rangos de mW.

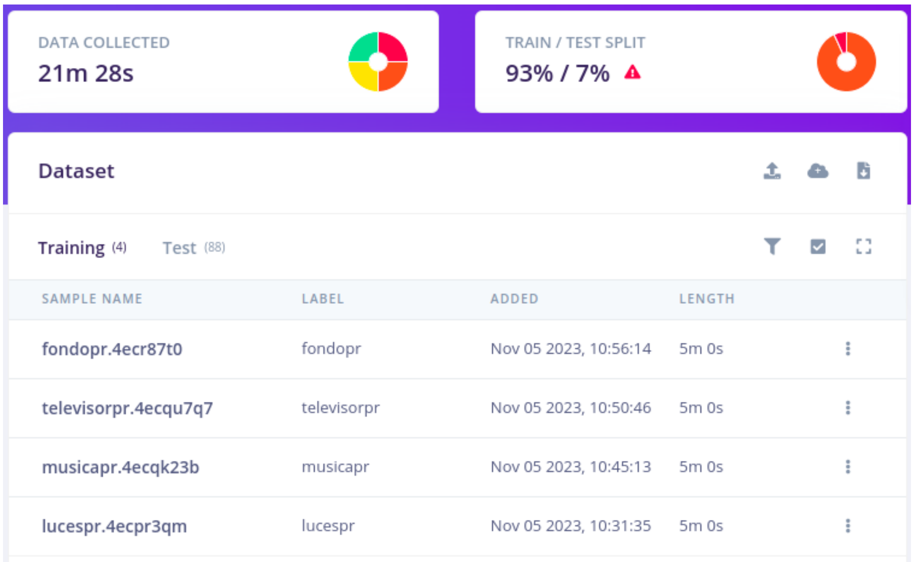
2.7. Lista de Componentes

Componente	Tipo	Cantidad	Precio por unidad	Lugar
Microcontrolador	Arduino TM Learning Kit	1	$60	Arduino Store

Tabla 1: Lista de Componentes

2.8. Diseño de red neuronal y código

Para esta sección primero se procedió a crear un proyecto en Edge Impulse, lo primero que se hizo fue la recolección de los datos, consistieron en 3 audios de 5 minutos cada uno en el que se repetían las palabras “ luces ”, “ música ”y “ televisor ”, respectivamente. Como se puede observar en la siguiente imagen:



DATA COLLECTED
21m 28s

TRAIN / TEST SPLIT
93% / 7%

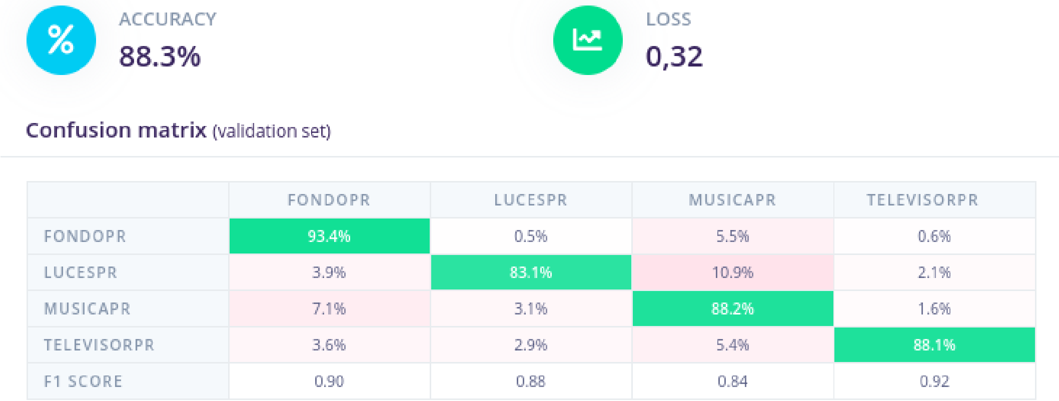
Dataset

Training (4) Test (88)

SAMPLE NAME	LABEL	ADDED	LENGTH
fondopr.4ecr87t0	fondopr	Nov 05 2023, 10:56:14	5m 0s
televisorpr.4ecqu7q7	televisorpr	Nov 05 2023, 10:50:46	5m 0s
musicapr.4ecqk23b	musicapr	Nov 05 2023, 10:45:13	5m 0s
lucespr.4ecpr3qm	lucespr	Nov 05 2023, 10:31:35	5m 0s

Figura 9: Recolección de datos para red neuronal

Después de esto se procedió a generar los valores necesarios para entrenar el modelo y después a entrenarlo, obteniendo los siguientes resultados, obteniendo un porcentaje de acierto de 88.3 % :



ACCURACY
88.3%

LOSS
0,32

Confusion matrix (validation set)

	FONDOPR	LUCESPR	MUSICAPR	TELEVISORPR
FONDOPR	93.4%	0.5%	5.5%	0.6%
LUCESPR	3.9%	83.1%	10.9%	2.1%
MUSICAPR	7.1%	3.1%	88.2%	1.6%
TELEVISORPR	3.6%	2.9%	5.4%	88.1%
F1 SCORE	0.90	0.88	0.84	0.92

Figura 10: Resultados de entrenamiento de red neuronal

3. Análisis de Resultados

En esta sección de análisis de resultados se explica más detalladamente lo creado con respecto a los programas en python y la conexión con thingsboard, como se explicó anteriormente se entrena la red neuronal en Edge Impulse, con el objetivo de poder exportarla en un .zip que se agregará a las librerías del Arduino IDE. Además se adjuntará un video en la carpeta de entrega del proyecto y el git, que contiene un video con el funcionamiento completo del programa.

3.1. Arduino

Entonces después de entrenar la red neuronal, ésta se exportó como una biblioteca de arduino para poder trabajar los resultados, el código implementado se puede entender en el siguiente diagrama:

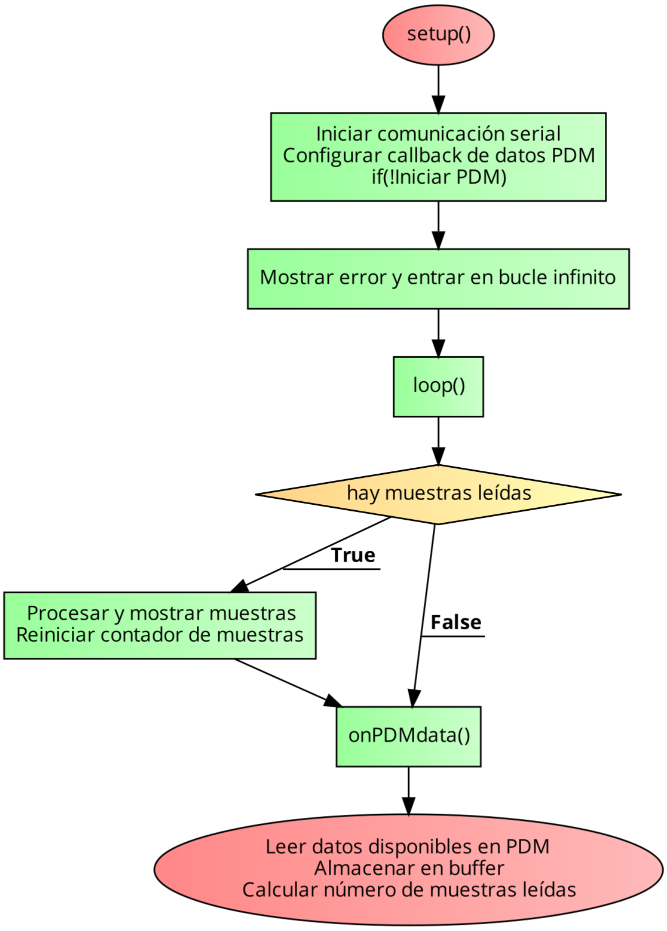

setup()
Iniciar comunicación serial
Configurar callback de datos PDM
if(!Iniciar PDM)
Mostrar error y entrar en bucle infinito
loop()
hay muestras leídas
True
False
Procesar y mostrar muestras
Reiniciar contador de muestras
onPDMdata()
Leer datos disponibles en PDM
Almacenar en buffer
Calcular número de muestras leídas

Figura 11: Diagrama del script implementado en Arduino

Este código está diseñado para la captura y procesamiento de audio mediante el Arduino Nano BLE 33, utilizando la librería PDM (Pulse Density Modulation). La configuración inicial establece el número de canales de audio y la frecuencia de muestreo, donde se utiliza un solo canal y una frecuencia de 16000 Hz, para que coincida con la de Edge Impulse. El programa se inicia con la función `setup()`, que configura la comunicación serial y prepara el sistema para recibir datos de audio. Si la inicialización del sistema PDM falla, el programa entra en un bucle infinito, indicando un fallo en el inicio.

En el bucle principal, definido en la función `loop()`, el programa espera a que se lean las muestras de audio. Una vez que las muestras están disponibles, se imprimen en el monitor serial. La función `onPDMdata()`, un callback, se activa con la disponibilidad de datos de audio, leyendo las muestras en un buffer y actualizando la cuenta de muestras leídas. Este enfoque demuestra la captura básica de audio y el procesamiento de datos utilizando un micrófono y la librería PDM en un entorno Arduino, enfocándose en la lectura y visualización de datos de audio en tiempo real.

3.2. Script de Python

Con respecto al script de python se crearon dos, de forma que se explicarán sus diferencias y tareas por realizar. Para el caso de **script.py** que establece una conexión serial con el arduino nano ble 33. a través por el puerto */dev/ttyACM0*, luego espera la entrada de los datos desde el arduino y procesa las líneas recibidas en busca de las etiquetas de los comandos de voz, luego guarda las palabras detectadas en un archivo de texto cuando se presiona Enter para finalizar el programa y crea el archivo con los comandos. Cabe destacar que para ejecutar este script es necesario compilar el anterior programa del arduino para que las librerías y demás configuraciones no causen errores. El otro sript de python **script_Iot,py** envía datos al servidor de thingsboard y se comunica con el arduino a través de un puerto serial para procesar los datos de los comandos de voz, y luego enviarlos a la plataforma thingsboard. El código sigue la siguiente estructura:

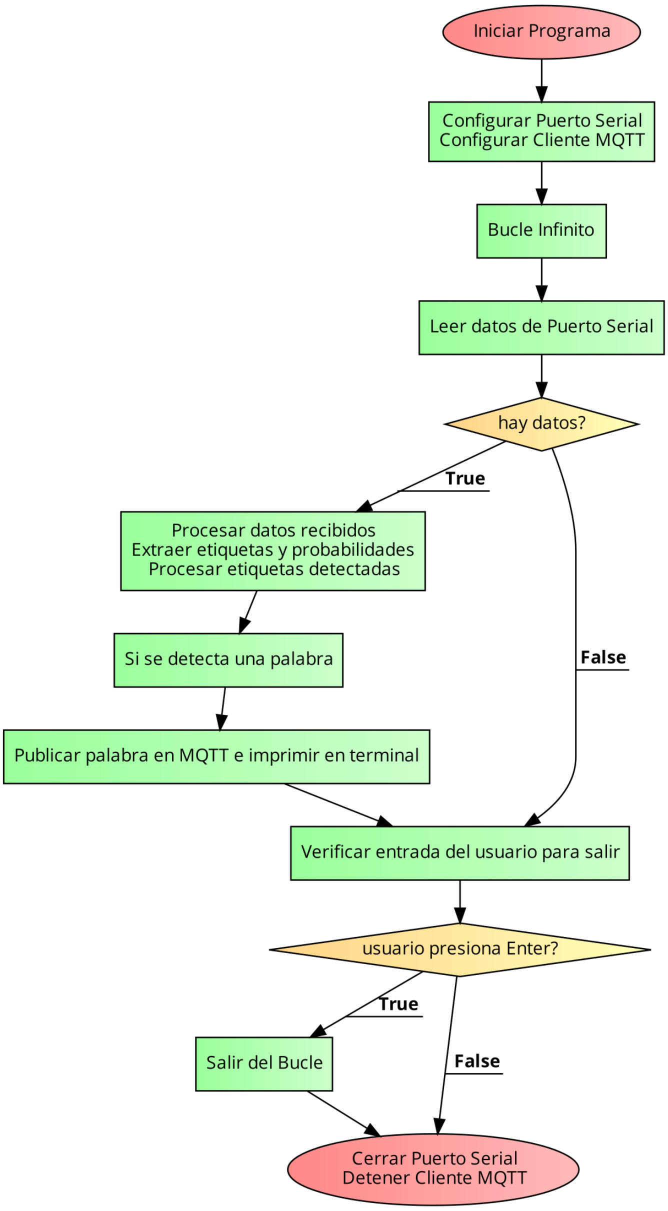


Figura 12: Diagrama del script implementado en Python

Del anterior diagrama, el programa configura un microcontrolador para recibir datos de audio a través de un micrófono, utilizando la librería PDM librería generada con el modelo entrenado para reconocer el sonido de entrada. La configuración incluye el número de canales y la frecuencia de muestreo del audio. Una vez configurado, el programa entra en un bucle infinito donde espera y lee muestras de audio, procesándolas y mostrándolas en un monitor serial. La función onPDMdata se utiliza como un callback para leer datos del buffer de audio cuando están disponibles.

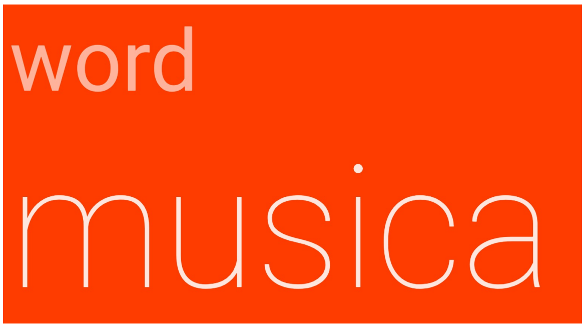
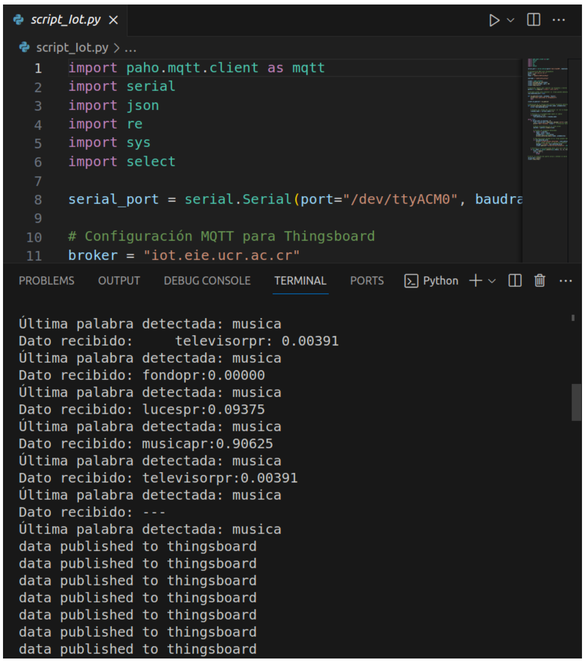


Figura 13: Resultado de la plataforma Thingsboard



```python
import paho.mqtt.client as mqtt
import serial
import json
import re
import sys
import select

serial_port = serial.Serial(port="/dev/ttyACM0", baudra

# Configuración MQTT para Thingsboard
broker = "iot.eie.ucr.ac.cr"
```

```
Última palabra detectada: musica
Dato recibido:     televisorpr: 0.00391
Última palabra detectada: musica
Dato recibido: fondopr:0.00000
Última palabra detectada: musica
Dato recibido: lucespr:0.09375
Última palabra detectada: musica
Dato recibido: musicapr:0.90625
Última palabra detectada: musica
Dato recibido: televisorpr:0.00391
Última palabra detectada: musica
Dato recibido: ---
Última palabra detectada: musica
data published to thingsboard
data published to thingsboard
data published to thingsboard
data published to thingsboard
data published to thingsboard
data published to thingsboard
data published to thingsboard
```

Figura 14: Script que capta comando de voz

Entonces en thingsboard se elije el diseño de un card para mostrar la clase o comando que reciba, la Figura 13 se muestra el card de thingsboard y en la Figura 14 el script donde dependiendo de la clase o comando detectada se envía a la plataforma.

Por lo tanto, se logra crear el programa para que detecte la palabra o comando de voz y luego envíe este dato a la computadora y cuando se finaliza el programa logra crear un archivo que guarda cada comando que se mencionó. Además de otro script que envía los datos a la plataforma thingsboard y se logra observar el comando que se mencione.

3.3. Repositorio Git

El repositorio de Github que contiene los archivos que muestran lo realizado se encuentra en el link: `https://github.com/SofiVillalta29/Laboratorio_De_Microcontroladores/tree/main`

4. Conclusiones y Recomendaciones

- Mediante la plataforma Edge Impulse se destaca la importancia que se carga la información de los comandos de voz, luego se realiza la configuración de la red neuronal, seguidamente se entrena esta red y después de las configuraciones respectivas se exporta el modelo obtenido al microcontrolador en una carpeta .zip como librería necesaria para instalar en el IDE de arduino.
-
-

Referencias

[1] Nordic Semiconductor (2018). nRF52840 Product Specification v1.4. Disponible en: `https://infocenter.nordicsemi.com/pdf/nRF52840_PS_v1.1.pdf`

[2] Arduino Nano 33 BLE Sense Datasheet (2022). Disponible en: `https://docs.arduino.cc/resources/datasheets/ABX00030-datasheet.pdf`

[3] STMicroelectronics (2022). LPS22HB MEMS pressure sensor: 260-1260 hPa absolute digital output barometer. Disponible en: `https://www.st.com/resource/en/datasheet/lps22hb.pdf`

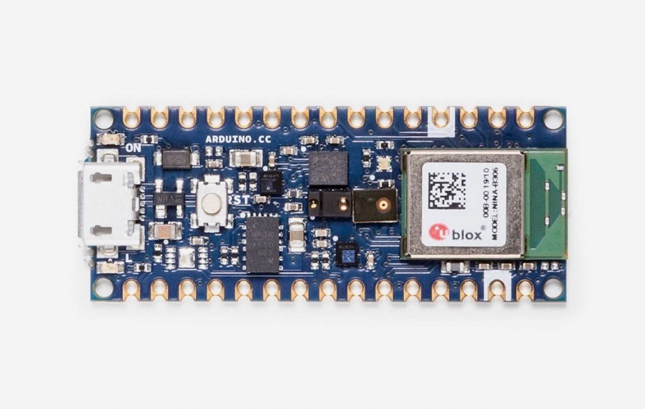
[4] Broadcom Limited (2016). APDS-9960 Proximity, Light, RGB, and Gesture Sensor. Disponible en: `https://docs.broadcom.com/doc/AV02-4191EN`

[5] Gaudenz Boesch. Tensorflow lite-real-time computer vision edge devices. Disponible en: `https://viso.ai/edge.ai/tensorflow-lite/`

[6] TinyML Foundation. About tinyml foundation. Disponible en: `https://www.tinyml.org/about/`

5. Apéndice

Product Reference Manual
SKU: ABX00031



Description

Nano 33 BLE Sense is a miniature sized module containing a NINA B306 module, based on Nordic nRF52480 and containing a Cortex M4F, a crypto chip which can securely store certificates and pre shared keys and a 9 axis IMU. The module can either be mounted as a DIP component (when mounting pin headers), or as a SMT component, directly soldering it via the castellated pads

Target areas:

Maker, enhancements, IoT application

Features

- **NINA B306 Module**
  - **Processor**
    - 64 MHz Arm® Cortex-M4F (with FPU)
    - 1 MB Flash + 256 KB RAM
  - **Bluetooth® 5 multiprotocol radio**
    - 2 Mbps
    - CSA #2
    - Advertising Extensions
    - Long Range
    - +8 dBm TX power
    - -95 dBm sensitivity
    - 4.8 mA in TX (0 dBm)
    - 4.6 mA in RX (1 Mbps)
    - Integrated balun with 50 Ω single-ended output
    - IEEE 802.15.4 radio support
    - Thread
    - Zigbee
  - **Peripherals**
    - Full-speed 12 Mbps USB
    - NFC-A tag
    - Arm CryptoCell CC310 security subsystem
    - QSPI/SPI/TWI/I²S/PDM/QDEC
    - High speed 32 MHz SPI
    - Quad SPI interface 32 MHz
    - EasyDMA for all digital interfaces
    - 12-bit 200 ksps ADC
    - 128 bit AES/ECB/CCM/AAR co-processor
- **LSM9DS1** (9 axis IMU)
  - 3 acceleration channels, 3 angular rate channels, 3 magnetic field channels
  - ±2/±4/±8/±16 g linear acceleration full scale
  - ±4/±8/±12/±16 gauss magnetic full scale
  - ±245/±500/±2000 dps angular rate full scale
  - 16-bit data output
- **LPS22HB** (Barometer and temperature sensor)
  - 260 to 1260 hPa absolute pressure range with 24 bit precision
  - High overpressure capability: 20x full-scale
  - Embedded temperature compensation
  - 16-bit temperature data output
  - 1 Hz to 75 Hz output data rateInterrupt functions: Data Ready, FIFO flags, pressure thresholds
- **HTS221** (relative humidity sensor)
  - 0-100% relative humidity range
  - High rH sensitivity: 0.004% rH/LSB
  - Humidity accuracy: ± 3.5% rH, 20 to +80% rH
  - Temperature accuracy: ± 0.5 °C,15 to +40 °C
  - 16-bit humidity and temperature output data

- **APDS-9960** (Digital proximity, Ambient light, RGB and Gesture Sensor)
  - Ambient Light and RGB Color Sensing with UV and IR blocking filters
  - Very high sensitivity – Ideally suited for operation behind dark glass
  - Proximity Sensing with Ambient light rejection
  - Complex Gesture Sensing
- **MP34DT05** (Digital Microphone)
  - AOP = 122.5 dbSPL
  - 64 dB signal-to-noise ratio
  - Omnidirectional sensitivity
  - –26 dBFS ± 3 dB sensitivity
- **ATECC608A** (Crypto Chip)
  - Cryptographic co-processor with secure hardware based key storage
  - Protected storage for up to 16 keys, certificates or data
  - ECDH: FIPS SP800-56A Elliptic Curve Diffie-Hellman
  - NIST standard P256 elliptic curve support
  - SHA-256 & HMAC hash including off-chip context save/restore
  - AES-128 encrypt/decrypt, galois field multiply for GCM
- **MPM3610** DC-DC
  - Regulates input voltage from up to 21V with a minimum of 65% efficiency @minimum load
  - More than 85% efficiency @12V

Contents

1 The Board

As all Nano form factor boards, Nano 33 BLE Sense does not have a battery charger but can be powered through USB or headers.

NOTE: Arduino Nano 33 BLE Sense only supports 3.3V I/Os and is **NOT** 5V tolerant so please make sure you are not directly connecting 5V signals to this board or it will be damaged. Also, as opposed to Arduino Nano boards that support 5V operation, the 5V pin does NOT supply voltage but is rather connected, through a jumper, to the USB power input.

1.1 Ratings

1.1.1 Recommended Operating Conditions

Symbol	Description	Min	Max
	Conservative thermal limits for the whole board:	-40 °C (40 °F)	85°C (185 °F)

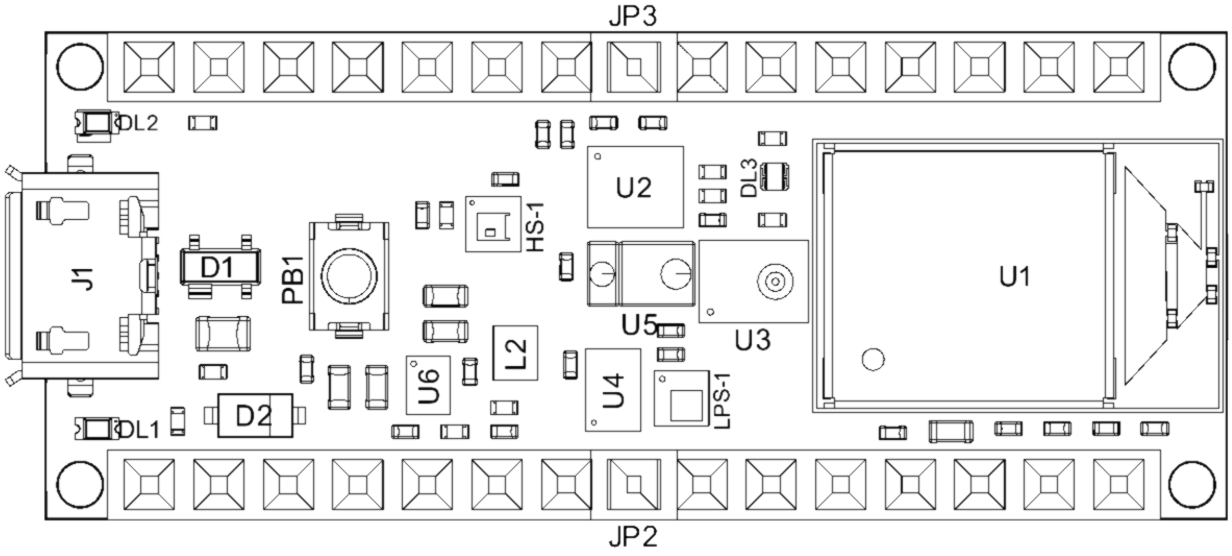
1.2 Power Consumption

Symbol	Description	Min	Typ	Max	Unit
PBL	Power consumption with busy loop		TBC		mW
PLP	Power consumption in low power mode		TBC		mW
PMAX	Maximum Power Consumption		TBC		mW

2 Functional Overview

2.1 Board Topology

Top:

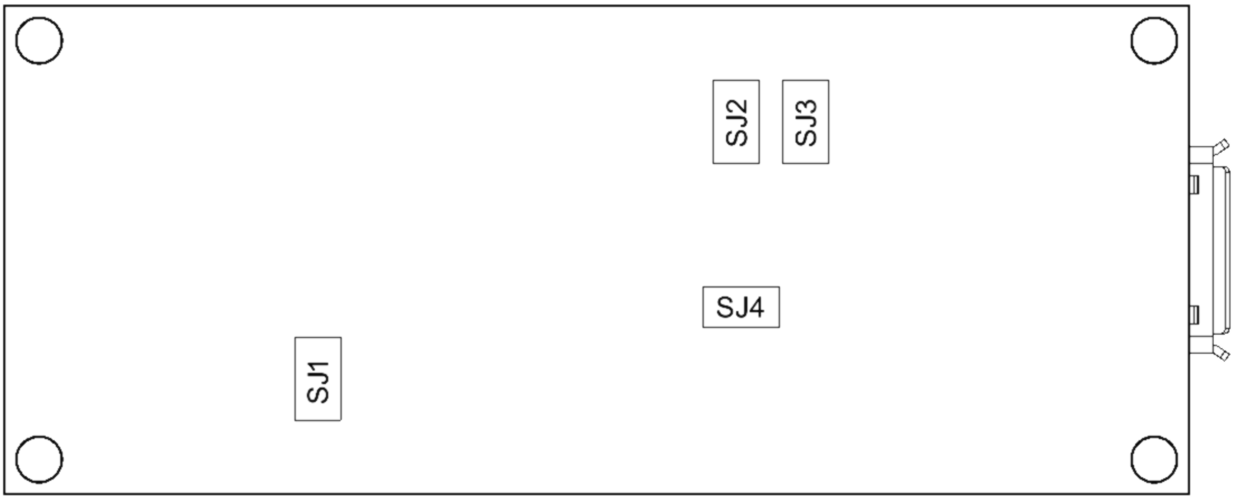


Board topology top

Ref.	Description	Ref.	Description
U1	NINA-B306 Module Bluetooth® Low Energy 5.0 Module	U6	MP2322GQH Step Down Converter
U2	LSM9DS1TR Sensor IMU	PB1	IT-1185AP1C-160G-GTR Push button
U3	MP34DT06JTR Mems Microphone	HS-1	HTS221 Humidity Sensor
U4	ATECC608A Crypto chip	DL1	Led L

Ref.	Description	Ref.	Description
U5	APDS-9660 Ambient Module	DL2	Led Power

Bottom:



Board topology bot

Ref.	Description	Ref.	Description
SJ1	VUSB Jumper	SJ2	D7 Jumper
SJ3	3v3 Jumper	SJ4	D8 Jumper

2.2 Processor

The Main Processor is a Cortex M4F running at up to 64MHz. Most of its pins are connected to the external headers, however some are reserved for internal communication with the wireless module and the on-board internal I^{2}C peripherals (IMU and Crypto).

NOTE: As opposed to other Arduino Nano boards, pins A4 and A5 have an internal pull up and default to be used as an I^{2}C Bus so usage as analog inputs is not recommended.

2.3 Crypto

The crypto chip in Arduino IoT boards is what makes the difference with other less secure boards as it provides a secure way to store secrets (such as certificates) and accelerates secure protocols while never exposing secrets in plain text.

Source code for the Arduino Library that supports the Crypto is available **[8]**

2.4 IMU

Arduino Nano 33 BLE has an embedded 9 axis IMU which can be used to measure board orientation (by checking the gravity acceleration vector orientation or by using the 3D compass) or to measure shocks, vibration, acceleration and rotation speed.

Source code for the Arduino Library that supports the IMU is available **[9]**

2.5 Barometer and Temperature Sensor

The embedded Barometer and temperature sensor allow measuring ambient pressure. The temperature sensor integrated with the barometer can be used to compensate the pressure measurement.

Source code for the Arduino Library that supports the Barometer is available **[10]**

2.6 Relative Humidity and Temperature Sensor

Relative humidity sensor measures ambient relative humidity. As the Barometer this sensor has an integrated temperature sensor that can be used to compensate for the measurement.

Source code for the Arduino Library that supports the Humidity sensor is available **[11]**

2.7 Digital Proximity, Ambient Light, RGB and Gesture Sensor

Source code for the Arduino Library that supports the Proximity/gesture/ALS sensor is available **[12]**

2.7.1 Gesture Detection

Gesture detection utilizes four directional photodiodes to sense reflected IR energy (sourced by the integrated LED) to convert physical motion information (i.e. velocity, direction and distance) to a digital information. The architecture of the gesture engine features automatic activation (based on Proximity engine results), ambient light subtraction, cross-talk cancellation, dual 8-bit data converters, power saving inter-conversion delay, 32-dataset FIFO, and interrupt driven I2C communication. The gesture engine accommodates a wide range of mobile device gesturing requirements: simple UP-DOWN-RIGHT-LEFT gestures or more complex gestures can be accurately sensed. Power consumption and noise are minimized with adjustable IR LED timing.

2.7.2 Proximity Detection

The Proximity detection feature provides distance measurement (E.g. mobile device screen to user’s ear) by photodiode detection of reflected IR energy (sourced by the integrated LED). Detect/release events are interrupt driven, and occur whenever proximity result crosses upper and/ or lower threshold settings. The proximity engine features offset adjustment registers to compensate for system offset caused by unwanted IR energy reflections appearing at the sensor. The IR LED intensity is factory trimmed to eliminate the need for end-equipment calibration due to component variations. Proximity results are further improved by automatic ambient light subtraction.

2.7.3 Color and ALS Detection

The Color and ALS detection feature provides red, green, blue and clear light intensity data. Each of the R, G, B, C channels have a UV and IR blocking filter and a dedicated data converter producing16-bit data simultaneously. This architecture allows applications to accurately measure ambient light and sense color which enables devices to calculate color temperature and control display backlight.

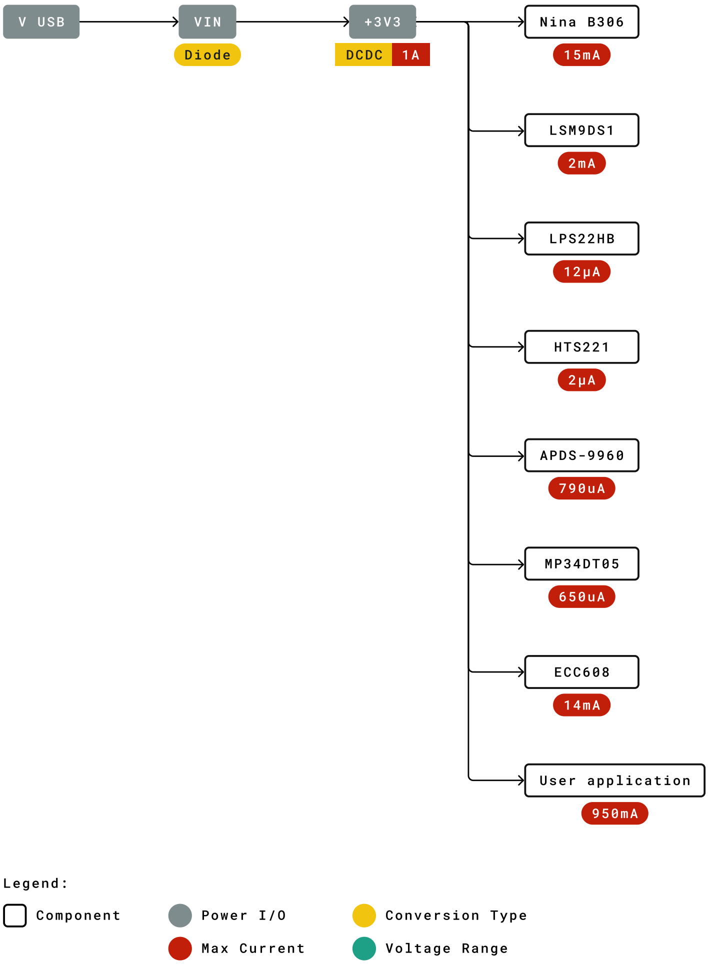
2.8 Digital Microphone

The MP34DT05 is an ultra-compact, low-power, omnidirectional, digital MEMS microphone built with a capacitive sensing element and an IC interface.

The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process dedicated to produce audio sensors

2.9 Power Tree

The board can be powered via USB connector, V_{IN} or V_{USB} pins on headers.



Power tree

NOTE: Since V_{USB} feeds V_{IN} via a Schottky diode and a DC-DC regulator specified minimum input voltage is 4.5V the minimum supply voltage from USB has to be increased to a voltage in the range between 4.8V to 4.96V depending on the current being drawn.

3 Board Operation

3.1 Getting Started - IDE

If you want to program your Arduino Nano 33 BLE while offline you need to install the Arduino Desktop IDE [1] To connect the Arduino Nano 33 BLE to your computer, you'll need a Micro-B USB cable. This also provides power to the board, as indicated by the LED.

3.2 Getting Started - Arduino Web Editor

All Arduino boards, including this one, work out-of-the-box on the Arduino Web Editor [2], by just installing a simple plugin.

The Arduino Web Editor is hosted online, therefore it will always be up-to-date with the latest features and support for all boards. Follow **[3]** to start coding on the browser and upload your sketches onto your board.

3.3 Getting Started - Arduino IoT Cloud

All Arduino IoT enabled products are supported on Arduino IoT Cloud which allows you to Log, graph and analyze sensor data, trigger events, and automate your home or business.

3.4 Sample Sketches

Sample sketches for the Arduino Nano 33 BLE can be found either in the "Examples" menu in the Arduino IDE or in the "Documentation" section of the Arduino Pro website [4]

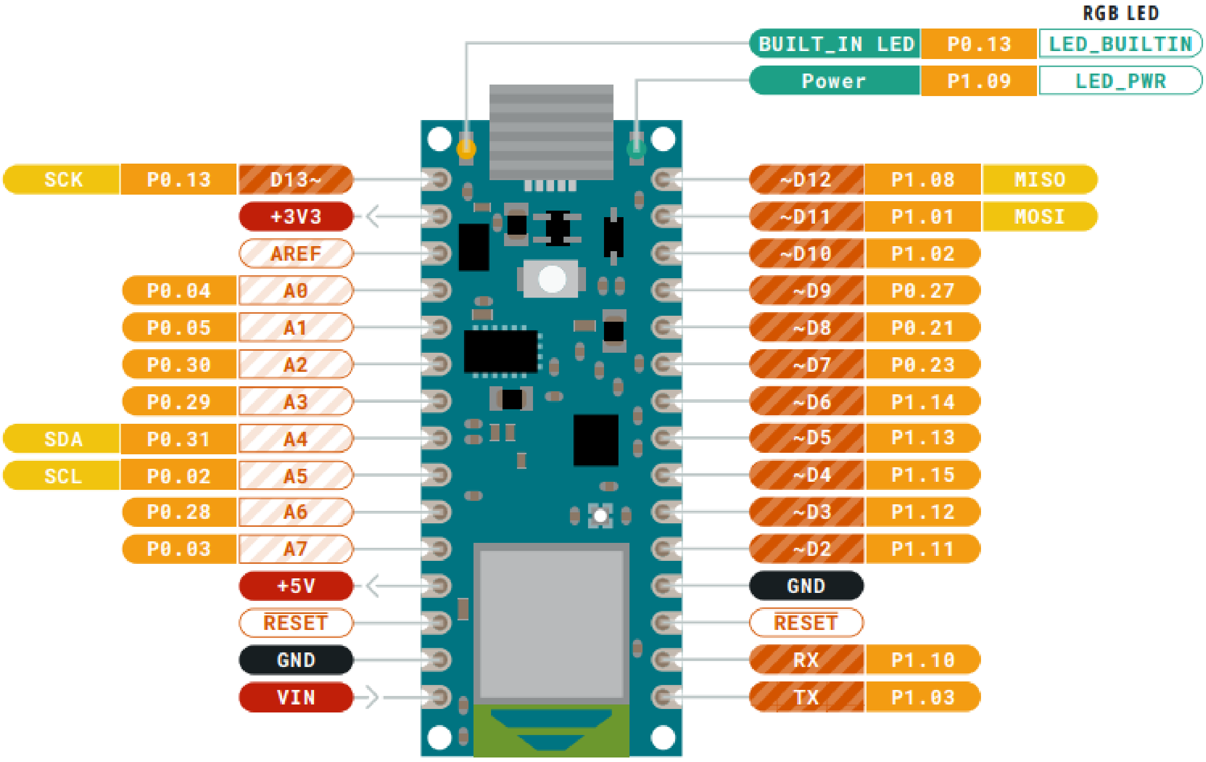
3.5 Online Resources

Now that you have gone through the basics of what you can do with the board you can explore the endless possibilities it provides by checking exciting projects on ProjectHub **[13]**, the Arduino Library Reference **[14]** and the on line store **[15]** where you will be able to complement your board with sensors, actuators and more.

3.6 Board Recovery

All Arduino boards have a built-in bootloader which allows flashing the board via USB. In case a sketch locks up the processor and the board is not reachable anymore via USB it is possible to enter bootloader mode by double-tapping the reset button right after power up.

4 Connector Pinouts



Pinout

4.1 USB

Pin	Function	Type	Description
1	VUSB	Power	Power Supply Input. If board is powered via VUSB from header this is an Output **(1)**
2	D-	Differential	USB differential data -
3	D+	Differential	USB differential data +
4	ID	Analog	Selects Host/Device functionality
5	GND	Power	Power Ground

4.2 Headers

The board exposes two 15 pin connectors which can either be assembled with pin headers or soldered through castellated vias.

Pin	Function	Type	Description
1	D13	Digital	GPIO
2	+3V3	Power Out	Internally generated power output to external devices
3	AREF	Analog	Analog Reference; can be used as GPIO
4	A0/DAC0	Analog	ADC in/DAC out; can be used as GPIO
5	A1	Analog	ADC in; can be used as GPIO
6	A2	Analog	ADC in; can be used as GPIO
7	A3	Analog	ADC in; can be used as GPIO
8	A4/SDA	Analog	ADC in; I2C SDA; Can be used as GPIO **(1)**
9	A5/SCL	Analog	ADC in; I2C SCL; Can be used as GPIO **(1)**
10	A6	Analog	ADC in; can be used as GPIO
11	A7	Analog	ADC in; can be used as GPIO
12	VUSB	Power In/Out	Normally NC; can be connected to VUSB pin of the USB connector by shorting a jumper
13	RST	Digital In	Active low reset input (duplicate of pin 18)
14	GND	Power	Power Ground

Pin	Function	Type	Description
15	VIN	Power In	Vin Power input
16	TX	Digital	USART TX; can be used as GPIO
17	RX	Digital	USART RX; can be used as GPIO
18	RST	Digital	Active low reset input (duplicate of pin 13)
19	GND	Power	Power Ground
20	D2	Digital	GPIO
21	D3/PWM	Digital	GPIO; can be used as PWM
22	D4	Digital	GPIO
23	D5/PWM	Digital	GPIO; can be used as PWM
24	D6/PWM	Digital	GPIO, can be used as PWM
25	D7	Digital	GPIO
26	D8	Digital	GPIO
27	D9/PWM	Digital	GPIO; can be used as PWM
28	D10/PWM	Digital	GPIO; can be used as PWM
29	D11/MOSI	Digital	SPI MOSI; can be used as GPIO
30	D12/MISO	Digital	SPI MISO; can be used as GPIO

4.3 Debug

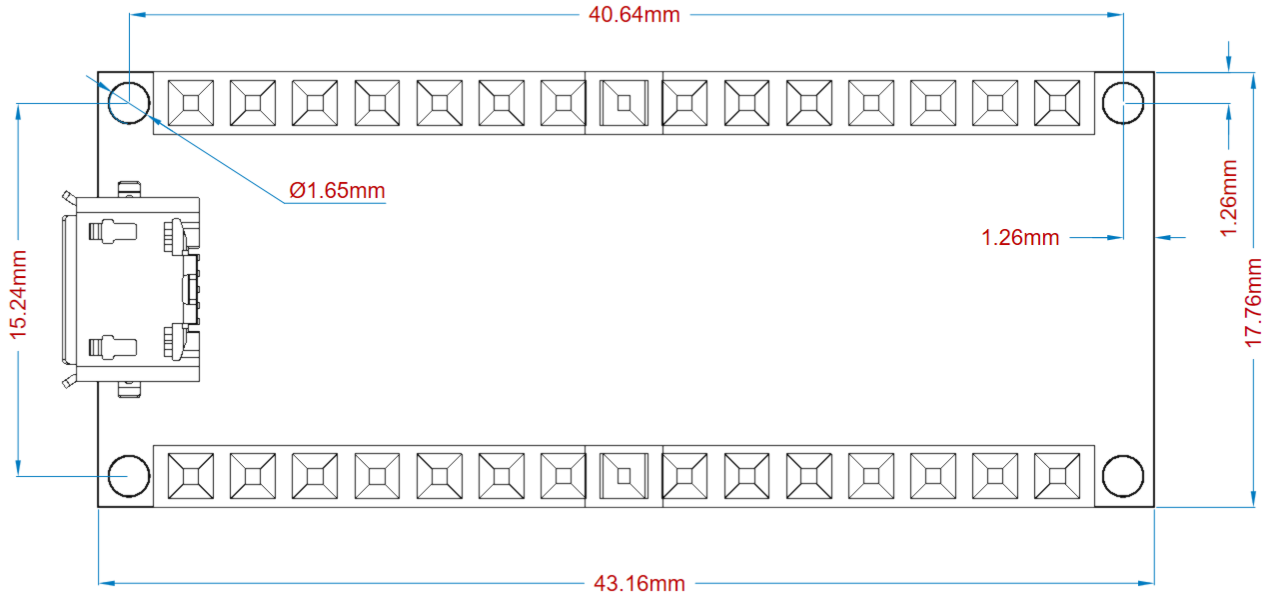
On the bottom side of the board, under the communication module, debug signals are arranged as 3x2 test pads with 100 mil pitch with pin 4 removed. Pin 1 is depicted in Figure 3 – Connector Positions

Pin	Function	Type	Description
1	+3V3	Power Out	Internally generated power output to be used as voltage reference
2	SWD	Digital	nRF52480 Single Wire Debug Data
3	SWCLK	Digital In	nRF52480 Single Wire Debug Clock
5	GND	Power	Power Ground
6	RST	Digital In	Active low reset input

5 Mechanical Information

5.1 Board Outline and Mounting Holes

The board measures are mixed between metric and imperial. Imperial measures are used to maintain 100 mil pitch grid between pin rows to allow them to fit a breadboard whereas board length is Metric



Board layout

6 Certifications

6.1 Declaration of Conformity CE DoC (EU)

We declare under our sole responsibility that the products above are in conformity with the essential requirements of the following EU Directives and therefore qualify for free movement within markets comprising the European Union (EU) and European Economic Area (EEA).

6.2 Declaration of Conformity to EU RoHS & REACH 211 01/19/2021

Arduino boards are in compliance with RoHS 2 Directive 2011/65/EU of the European Parliament and RoHS 3 Directive 2015/863/EU of the Council of 4 June 2015 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Substance	Maximum limit (ppm)
Lead (Pb)	1000
Cadmium (Cd)	100
Mercury (Hg)	1000
Hexavalent Chromium (Cr6+)	1000
Poly Brominated Biphenyls (PBB)	1000
Poly Brominated Diphenyl ethers (PBDE)	1000
Bis(2-Ethylhexyl} phthalate (DEHP)	1000
Benzyl butyl phthalate (BBP)	1000
Dibutyl phthalate (DBP)	1000
Diisobutyl phthalate (DIBP)	1000

Exemptions : No exemptions are claimed.

Arduino Boards are fully compliant with the related requirements of European Union Regulation (EC) 1907 /2006 concerning the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH). We declare none of the SVHCs (https://echa.europa.eu/web/guest/candidate-list-table), the Candidate List of Substances of Very High Concern for authorization currently released by ECHA, is present in all products (and also package) in quantities totaling in a concentration equal or above 0.1%. To the best of our knowledge, we also declare that our products do not contain any of the substances listed on the "Authorization List"

(Annex XIV of the REACH regulations) and Substances of Very High Concern (SVHC) in any significant amounts as specified by the Annex XVII of Candidate list published by ECHA (European Chemical Agency) 1907 /2006/EC.

6.3 Conflict Minerals Declaration

As a global supplier of electronic and electrical components, Arduino is aware of our obligations with regards to laws and regulations regarding Conflict Minerals, specifically the Dodd-Frank Wall Street Reform and Consumer Protection Act, Section 1502. Arduino does not directly source or process conflict minerals such as Tin, Tantalum, Tungsten, or Gold. Conflict minerals are contained in our products in the form of solder, or as a component in metal alloys. As part of our reasonable due diligence Arduino has contacted component suppliers within our supply chain to verify their continued compliance with the regulations. Based on the information received thus far we declare that our products contain Conflict Minerals sourced from conflict-free areas.

7 FCC Caution

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference

(2) this device must accept any interference received, including interference that may cause undesired operation.

FCC RF Radiation Exposure Statement:

1. This Transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
2. This equipment complies with RF radiation exposure limits set forth for an uncontrolled environment.
3. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

English: User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both. This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

French: Le présent appareil est conforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisée aux deux conditions suivantes :

(1) l’ appareil nedoit pas produire de brouillage

(2) l’utilisateur de l’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement.

IC SAR Warning:

English This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

French: Lors de l’ installation et de l’ exploitation de ce dispositif, la distance entre le radiateur et le corps est d ’au moins 20 cm.

Important: The operating temperature of the EUT can’t exceed 85℃ and shouldn’t be lower than -40℃.

Hereby, Arduino S.r.l. declares that this product is in compliance with essential requirements and other relevant provisions of Directive 2014/53/EU. This product is allowed to be used in all EU member states.

Frequency bands	Maximum output power (ERP)
863-870Mhz	5.47 dBm

8 Company Information

Company name	Arduino S.r.l
Company Address	Via Andrea Appiani 25 20900 MONZA Italy

9 Reference Documentation

Reference	Link
Arduino IDE (Desktop)	https://www.arduino.cc/en/software
Arduino IDE (Cloud)	https://create.arduino.cc/editor
Cloud IDE Getting Started	https://create.arduino.cc/projecthub/Arduino_Genuino/getting-started-with-arduino-web-editor-4b3e4a
Forum	http://forum.arduino.cc/
Nina B306	https://content.u-blox.com/sites/default/files/NINA-B3_DataSheet_UBX-17052099.pdf
ECC608	https://ww1.microchip.com/downloads/aemDocuments/documents/SCBU/ProductDocuments/DataSheets/ATECC608A-CryptoAuthentication-Device-Summary-Data-Sheet-DS40001977B.pdf
MPM3610	https://www.monolithicpower.com/pub/media/document/MPM3610_r1.01.pdf
ECC608 Library	https://github.com/arduino-libraries/ArduinoECCX08
LSM6DSL Library	https://github.com/adafruit/Adafruit_LSM9DS1
LPS22HB	https://github.com/stm32duino/LPS22HB
HTS221 Library	https://github.com/stm32duino/HTS221
APDS9960 Library	https://github.com/adafruit/Adafruit_APDS9960
ProjectHub	https://create.arduino.cc/projecthub?by=part&part_id=11332&sort=trending
Library Reference	https://www.arduino.cc/reference/en/

10 Revision History

Date	Revision	Changes
08/03/2022	2	Reference documentation links updates
04/27/2021	1	General datasheet updates

3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

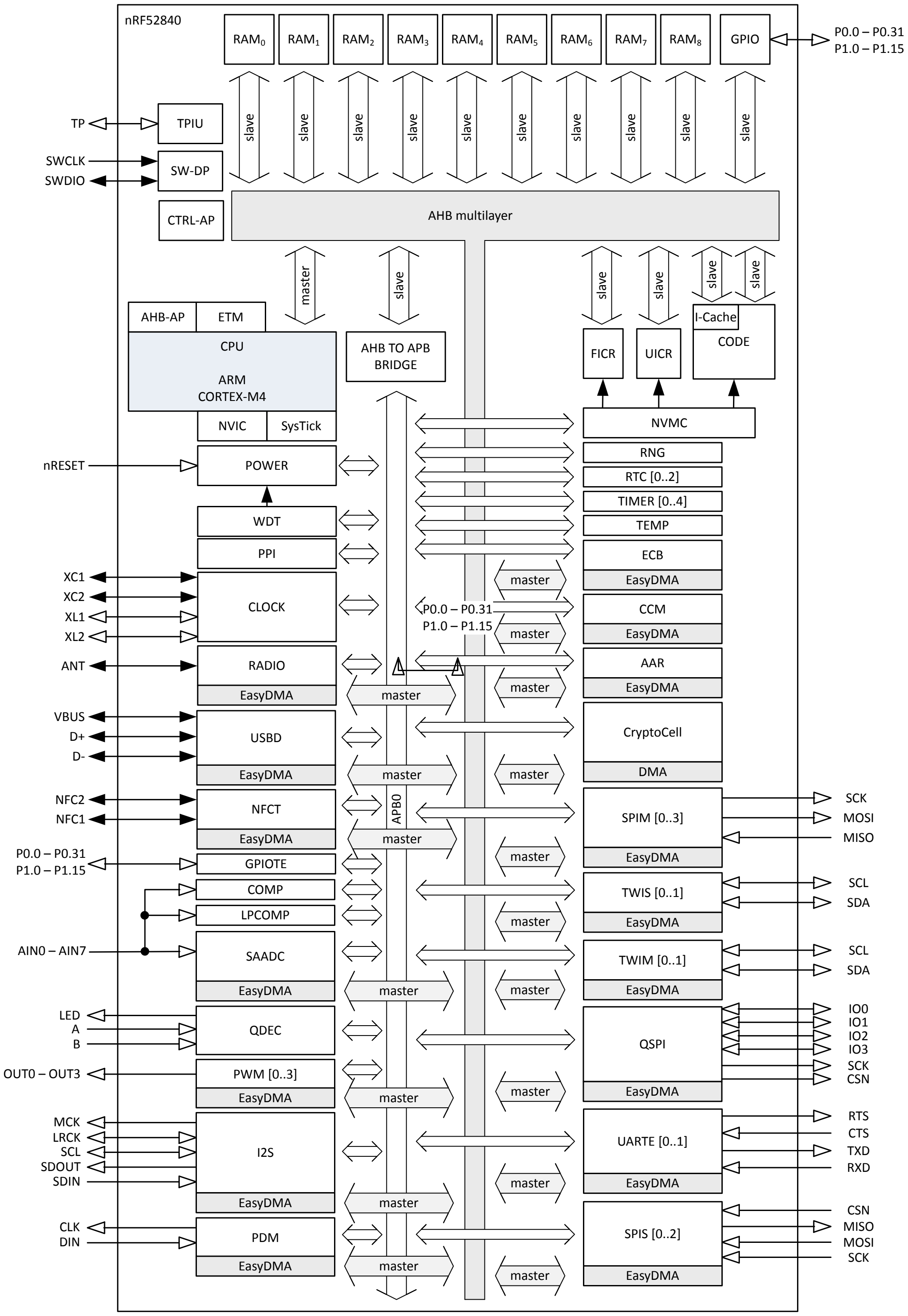


Figure 1: Block diagram

4 Core components

4.1 CPU

The ARM® Cortex-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16- and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing, including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8- and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM®Cortex® processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the nested vectored interrupt controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see Cache on page 26. The section Electrical specification on page 20 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

The ARM system timer (SysTick) is present on nRF52840. The SysTick's clock will only tick when the CPU is running or when the system is in debug interface mode.

4.1.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow, which in turn will trigger the FPU interrupt.

See Instantiation on page 23 for more information about the exceptions triggering the FPU interrupt.

To clear the IRQ (interrupt request) line when an exception has occurred, the relevant exception bit within the floating-point status and control register (FPSCR) needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

4.1.2 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested vector interrupt controller	48 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup interrupt controller	NO
Endianness	Memory system endianness	Little endian
Bit-banding	Bit banded memory	NO
DWT	Data watchpoint and trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating-point unit	YES
DAP	Debug access port	YES
ETM	Embedded trace macrocell	YES
ITM	Instrumentation trace macrocell	YES
TPIU	Trace port interface unit	YES
ETB	Embedded trace buffer	NO
FPB	Flash patch and breakpoint unit	YES
HTM	AMBA™ AHB trace macrocell	NO

4.1.3 Electrical specification

4.1.3.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark™ benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Typ.	Max.	Units
W_{FLASH}	CPU wait states, running CoreMark from flash, cache disabled			2	
$W_{FLASHCACHE}$	CPU wait states, running CoreMark from flash, cache enabled			3	
W_{RAM}	CPU wait states, running CoreMark from RAM			0	
CM_{FLASH}	CoreMark, running CoreMark from flash, cache enabled		212		CoreM
$CM_{FLASH/MHz}$	CoreMark per MHz, running CoreMark from flash, cache enabled		3.3		CoreMark/ MHz
$CM_{FLASH/mA}$	CoreMark per mA, running CoreMark from flash, cache enabled, DCDC 3V		64		CoreM mA

4.2 Memory

The nRF52840 contains 1 MB of flash and 256 kB of RAM that can be used for code and data storage.

The CPU and peripherals with EasyDMA can access memory via the AHB multilayer interconnect.

The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in Memory layout on page 21.

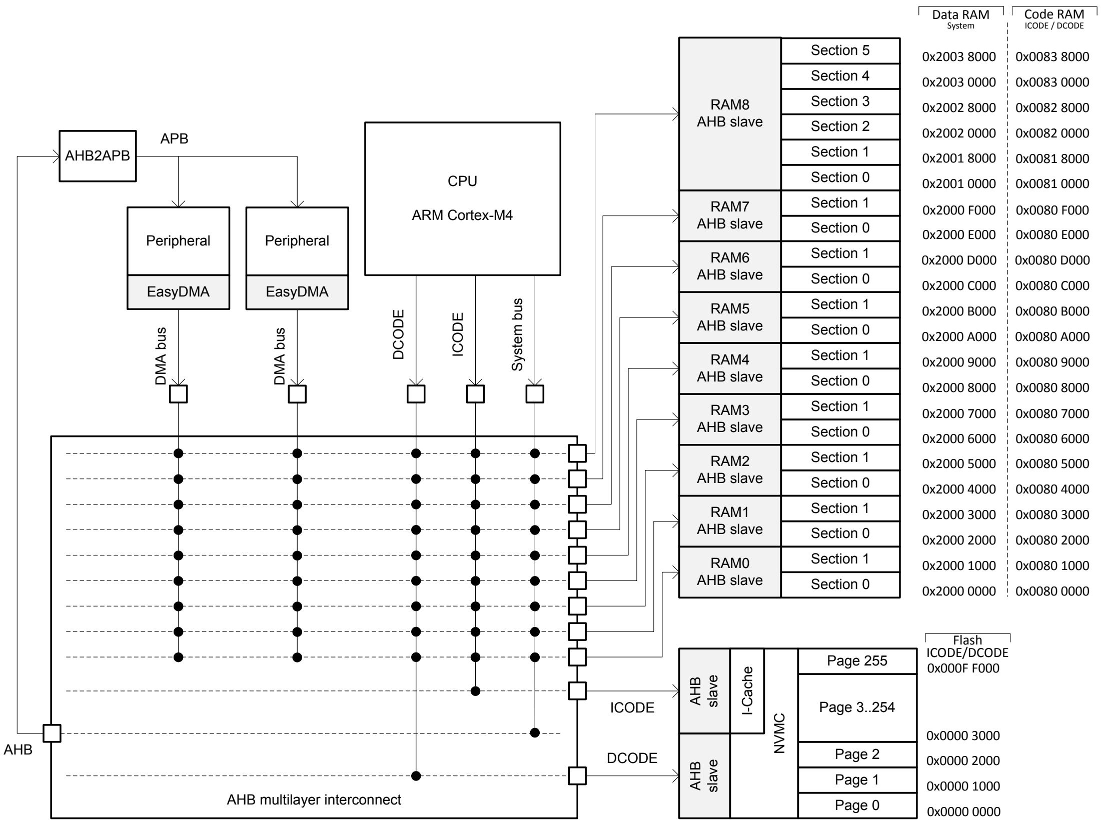


Figure 2: Memory layout

See AHB multilayer on page 49 and EasyDMA on page 46 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

4.2.1 RAM - Random access memory

The RAM interface is divided into 9 RAM AHB slaves.

RAM AHB slave 0-7 is connected to 2x4 kB RAM sections each and RAM AHB slave 8 is connected to 6x32 kB sections, as shown in Memory layout on page 21.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the POWER — Power supply on page 61).

4.2.2 Flash - Non-volatile memory

The flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.

Writing to flash is managed by the non-volatile memory controller (NVMC), see NVMC — Non-volatile memory controller on page 24.

The flash is divided into 256 pages of 4 kB each that can be accessed by the CPU via both the ICODE and DCODE buses as shown in Memory layout on page 21.

4.2.3 Memory map

The complete memory map for the nRF52840 is shown in Memory map on page 22. As described in Memory on page 20, Code RAM and Data RAM are the same physical RAM.

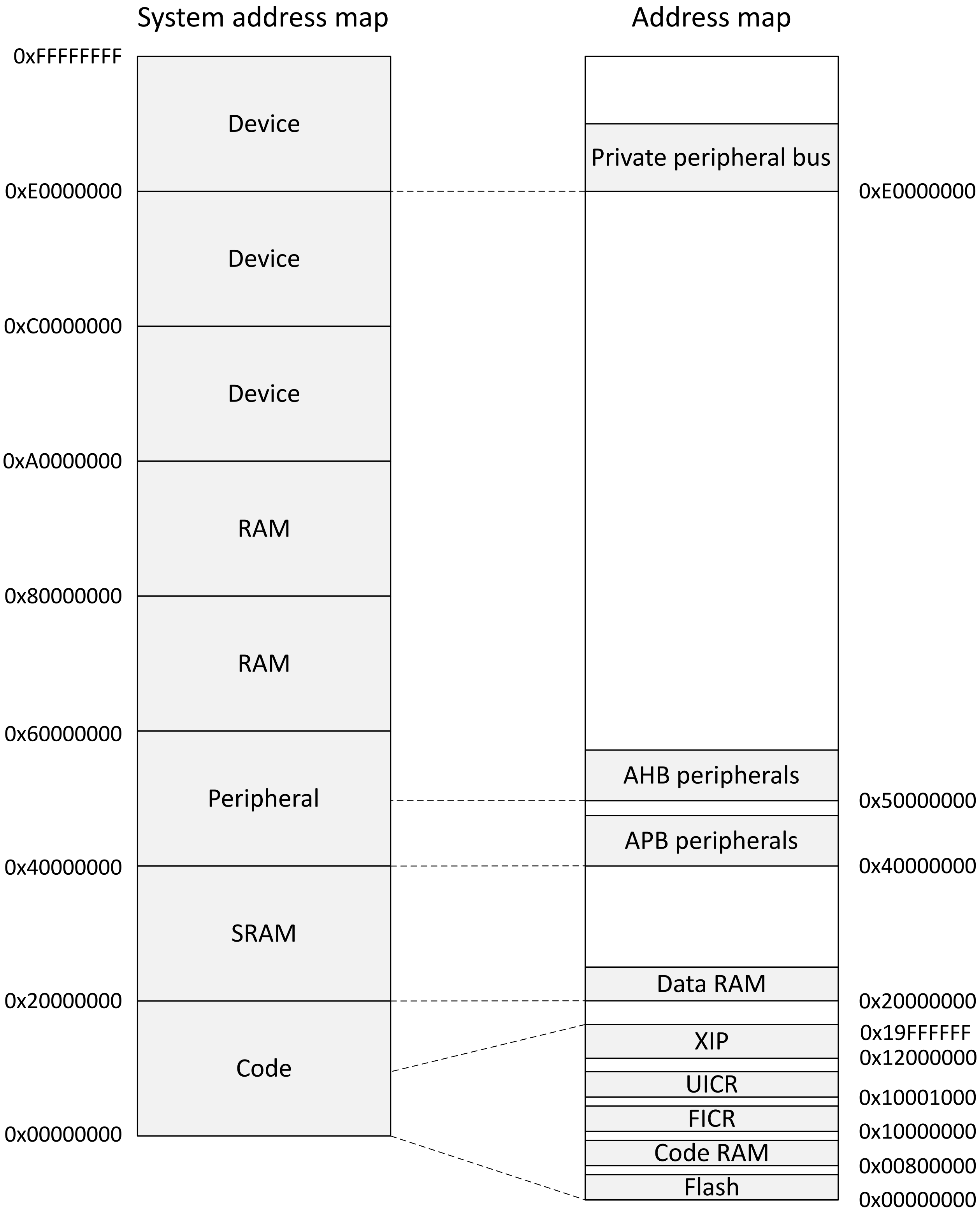


Figure 3: Memory map

4.2.4 Instantiation

ID	Base address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power control	
0	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
0	0x50000000	GPIO	P0	General purpose input and output, port 0	
0	0x50000300	GPIO	P1	General purpose input and output, port 1	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UART	UART0	Universal asynchronous receiver/transmitter	Deprecated
2	0x40002000	UARTE	UARTE0	Universal asynchronous receiver/transmitter with EasyDMA, unit 0	
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
4	0x40004000	SPIM	SPIM1	SPI master 1	
4	0x40004000	SPIS	SPIS1	SPI slave 1	
4	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
5	0x40005000	NFCT	NFCT	Near field communication tag	
6	0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	
7	0x40007000	SAADC	SAADC	Analog to digital converter	
8	0x40008000	TIMER	TIMER0	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real-time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature sensor	
13	0x4000D000	RNG	RNG	Random number generator	
14	0x4000E000	ECB	ECB	AES electronic code book (ECB) mode block encryption	
15	0x4000F000	AAR	AAR	Accelerated address resolver	
15	0x4000F000	CCM	CCM	AES counter with CBC-MAC (CCM) mode block encryption	
16	0x40010000	WDT	WDT	Watchdog timer	
17	0x40011000	RTC	RTC1	Real-time counter 1	
18	0x40012000	QDEC	QDEC	Quadrature decoder	
19	0x40013000	COMP	COMP	General purpose comparator	
19	0x40013000	LPCOMP	LPCOMP	Low power comparator	
20	0x40014000	EGU	EGU0	Event generator unit 0	
20	0x40014000	SWI	SWI0	Software interrupt 0	
21	0x40015000	EGU	EGU1	Event generator unit 1	
21	0x40015000	SWI	SWI1	Software interrupt 1	
22	0x40016000	EGU	EGU2	Event generator unit 2	
22	0x40016000	SWI	SWI2	Software interrupt 2	
23	0x40017000	EGU	EGU3	Event generator unit 3	
23	0x40017000	SWI	SWI3	Software interrupt 3	
24	0x40018000	EGU	EGU4	Event generator unit 4	
24	0x40018000	SWI	SWI4	Software interrupt 4	
25	0x40019000	EGU	EGU5	Event generator unit 5	
25	0x40019000	SWI	SWI5	Software interrupt 5	

ID	Base address	Peripheral	Instance	Description	
26	0x4001A000	TIMER	TIMER3	Timer 3	
27	0x4001B000	TIMER	TIMER4	Timer 4	
28	0x4001C000	PWM	PWM0	Pulse width modulation unit 0	
29	0x4001D000	PDM	PDM	Pulse Density modulation (digital microphone) interface	
30	0x4001E000	ACL	ACL	Access control lists	
30	0x4001E000	NVMC	NVMC	Non-volatile memory controller	
31	0x4001F000	PPI	PPI	Programmable peripheral interconnect	
32	0x40020000	MWU	MWU	Memory watch unit	
33	0x40021000	PWM	PWM1	Pulse width modulation unit 1	
34	0x40022000	PWM	PWM2	Pulse width modulation unit 2	
35	0x40023000	SPI	SPI2	SPI master 2	Deprecated
35	0x40023000	SPIM	SPIM2	SPI master 2	
35	0x40023000	SPIS	SPIS2	SPI slave 2	
36	0x40024000	RTC	RTC2	Real-time counter 2	
37	0x40025000	I2S	I2S	Inter-IC sound interface	
38	0x40026000	FPU	FPU	FPU interrupt	
39	0x40027000	USBD	USBD	Universal serial bus device	
40	0x40028000	UARTE	UARTE1	Universal asynchronous receiver/transmitter with EasyDMA, unit 1	
41	0x40029000	QSPI	QSPI	External memory interface	
42	0x5002A000	CC_HOST_RGF	CC_HOST_RGF	Host platform interface	
42	0x5002A000	CRYPTOCELL	CRYPTOCELL	CryptoCell subsystem control interface	
45	0x4002D000	PWM	PWM3	Pulse width modulation unit 3	
47	0x4002F000	SPIM	SPIM3	SPI master 3	
N/A	0x10000000	FICR	FICR	Factory information configuration	
N/A	0x10001000	UICR	UICR	User information configuration	

Table 3: Instantiation table

4.3 NVMC — Non-volatile memory controller

The non-volatile memory controller (NVMC) is used for writing and erasing of the internal flash memory and the UICR (user information configuration registers).

The CONFIG on page 27 is used to enable the NVMC for writing (CONFIG.WEN = Wen) and erasing (CONFIG.WEN = Een). The user must make sure that writing and erasing are not enabled at the same time. Having both enabled at the same time may result in unpredictable behavior.

The CPU must be halted before initiating a NVMC operation from the debug system.

4.3.1 Writing to flash

When write is enabled, full 32-bit words can be written to word-aligned addresses in the flash.

As illustrated in Memory on page 20, the flash is divided into multiple pages. The same 32-bit word in the flash can only be written n_{WRITE} number of times before a page erase must be performed.

The NVMC is only able to write `0` to bits in the flash that are erased (set to `1`). It cannot rewrite a bit back to `1`. Only full 32-bit words can be written to flash using the NVMC interface. To write less than 32 bits, write the data as a full 32-bit word and set all the bits that should remain unchanged in the word to `1`. Note that the restriction on the number of writes (n_{WRITE}) still applies in this case.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

The time it takes to write a word to flash is specified by t_{WRITE}. The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the flash.

NVM writing time can be reduced by using READYNEXT. If this status bit is set to '1', code can perform the next data write to the flash. This write will be buffered and will be taken into account as soon as the ongoing write operation is completed.

4.3.2 Erasing a page in flash

When erase is enabled, the flash memory can be erased page by page using the ERASEPAGE on page 27.

After erasing a flash page, all bits in the page are set to `1`. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the flash.

See Partial erase of a page in flash on page 25 for information on dividing the page erase time into shorter chunks.

4.3.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR can only be written n_{WRITE} number of times before an erase must be performed using ERASEUICR on page 29 or ERASEALL on page 28. The time it takes to write a word to UICR is specified by t_{WRITE}.
The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the UICR.

4.3.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the ERASEUICR on page 29.

After erasing UICR all bits in UICR are set to `1`. The time it takes to erase UICR is specified by $t_{ERASEPAGE}$. The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

4.3.5 Erase all

When erase is enabled, flash and UICR can be erased completely in one operation by using the ERASEALL on page 28. This operation will not erase the factory information configuration registers (FICR).

The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$ The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

4.3.6 Access port protection behavior

When access port protection is enabled, parts of the NVMC functionality will be blocked in order to prevent intentional or unintentional erase of UICR.

	CTRL-AP ERASEALL	**NVMC ERASEPAGE**	**NVMC ERASEPAGE PARTIAL**	**NVMC ERASEALL**	**NVMC ERASEUICR**
APPROTECT					
Disabled	Allowed	Allowed	Allowed	Allowed	Allowed
Enabled	Allowed	Allowed	Allowed	Allowed	Blocked

Table 4: NVMC Protection

4.3.7 Partial erase of a page in flash

Partial erase is a feature in the NVMC to split a page erase time into shorter chunks, so this can be used to prevent longer CPU stalls in time-critical applications. Partial erase is only applicable to the code area in the flash and does not work with UICR.

When erase is enabled, the partial erase of a flash page can be started by writing to ERASEPAGEPARTIAL on page 29. The duration of a partial erase can be configured in ERASEPAGEPARTIALCFG on page 29. A flash page is erased when its erase time reaches $t_{ERASEPAGE}$. Use ERASEPAGEPARTIAL N number of times so that N * ERASEPAGEPARTIALCFG ≥ $t_{ERASEPAGE}$, where N * ERASEPAGEPARTIALCFG gives the cumulative (total) erase time. Every time the cumulative erase time reaches $t_{ERASEPAGE}$, it counts as one erase cycle.

After the erase is done, all bits in the page are set to '1'. The CPU is halted if the CPU executes code from the flash while the NVMC performs the partial erase operation.

The bits in the page are undefined if the flash page erase is incomplete, i.e. if a partial erase has started but the total erase time is less than $t_{ERASEPAGE}$.

4.3.8 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See the Memory map in Memory map on page 21 for the location of flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from flash, depends on the processor frequency and is shown in CPU on page 19

Enabling the cache can increase CPU performance and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache will use some current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will reduce.

When disabled, the cache does not use current and does not retain its content.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the ICACHECNF register. When profiling is enabled, the IHIT and IMISS registers are incremented for every instruction cache hit or miss respectively. The hit and miss profiling registers do not wrap around after reaching the maximum value. If the maximum value is reached, consider profiling for a shorter duration to get correct numbers.

4.3.9 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	NVMC	NVMC	Non-volatile memory controller	

Table 5: Instances

Register	Offset	Description	
READY	0x400	Ready flag	
READYNEXT	0x408	Ready flag	
CONFIG	0x504	Configuration register	
ERASEPAGE	0x508	Register for erasing a page in code area	
ERASEPCR1	0x508	Register for erasing a page in code area. Equivalent to ERASEPAGE.	Deprecated
ERASEALL	0x50C	Register for erasing all non-volatile user memory	
ERASEPCR0	0x510	Register for erasing a page in code area. Equivalent to ERASEPAGE.	Deprecated
ERASEUICR	0x514	Register for erasing user information configuration registers	
ERASEPAGEPARTIAL	0x518	Register for partial erase of a page in code area	
ERASEPAGEPARTIALCFG	0x51C	Register for partial erase configuration	
ICACHECNF	0x540	I-code cache configuration register.	
IHIT	0x548	I-code cache hit counter.	

Register	Offset	Description
IMISS	0x54C	I-code cache miss counter.

Table 6: Register overview

4.3.9.1 READY

Address offset: 0x400

Ready flag

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

ID	Acce	Field	Value ID	Value	Description
A	R	READY			NVMC is ready or busy
			Busy	0	NVMC is busy (on-going write or erase operation)
			Ready	1	NVMC is ready

4.3.9.2 READYNEXT

Address offset: 0x408

Ready flag

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce	Field	Value ID	Value	Description
A	R	READYNEXT			NVMC can accept a new write operation
			Busy	0	NVMC cannot accept any write operation
			Ready	1	NVMC is ready

4.3.9.3 CONFIG

Address offset: 0x504

Configuration register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce	Field	Value ID	Value	Description
A	RW	WEN			Program memory access mode. It is strongly recommended to only activate erase and write modes when they are actively used. Enabling write or erase will invalidate the cache and keep it invalidated.
			Ren	0	Read only access
			Wen	1	Write enabled
			Een	2	Erase enabled

4.3.9.4 ERASEPAGE

Address offset: 0x508

Register for erasing a page in code area

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	ERASEPAGE			Register for starting erase of a page in code area The value is the address to the page to be erased. (Addresses of first word in page). Note that the erase must be enabled using CONFIG.WEN before the page can be erased. Attempts to erase pages that are outside the code area may result in undesirable behaviour, e.g. the wrong page may be erased.

4.3.9.5 ERASEPCR1 (Deprecated)

Address offset: 0x508

Register for erasing a page in code area. Equivalent to ERASEPAGE.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	ERASEPCR1			Register for erasing a page in code area. Equivalent to ERASEPAGE.

4.3.9.6 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	ERASEALL			Erase all non-volatile memory including UICR registers. Note that the erase must be enabled using CONFIG.WEN before the non-volatile memory can be erased.
			NoOperation	0	No operation
			Erase	1	Start chip erase

4.3.9.7 ERASEPCR0 (Deprecated)

Address offset: 0x510

Register for erasing a page in code area. Equivalent to ERASEPAGE.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	ERASEPCR0			Register for starting erase of a page in code area. Equivalent to ERASEPAGE.

4.3.9.8 ERASEUICR

Address offset: 0x514

Register for erasing user information configuration registers

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	ERASEUICR			Register starting erase of all user information configuration registers. Note that the erase must be enabled using CONFIG.WEN before the UICR can be erased.
			NoOperation	0	No operation
			Erase	1	Start erase of UICR

4.3.9.9 ERASEPAGEPARTIAL

Address offset: 0x518

Register for partial erase of a page in code area

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	ERASEPAGEPARTIAL			Register for starting partial erase of a page in code area The value is the address to the page to be partially erased (address of the first word in page). Note that the erase must be enabled using CONFIG.WEN before every erase page partial and disabled using CONFIG.WEN after every erase page partial. Attempts to erase pages that are outside the code area may result in undesirable behaviour, e.g. the wrong page may be erased.

4.3.9.10 ERASEPAGEPARTIALCFG

Address offset: 0x51C

Register for partial erase configuration

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																										A	A	A	A	A	A	A
Reset 0x0000000A	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	DURATION			Duration of the partial erase in milliseconds The user must ensure that the total erase time is long enough for a complete erase of the flash page.

4.3.9.11 ICACHECNF

Address offset: 0x540

I-code cache configuration register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																								B								A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	CACHEEN			Cache enable
			Disabled	0	Disable cache. Invalidates all cache entries.
			Enabled	1	Enable cache
B	RW	CACHEPROFEN			Cache profiling enable
			Disabled	0	Disable cache profiling
			Enabled	1	Enable cache profiling

4.3.9.12 IHIT

Address offset: 0x548

I-code cache hit counter.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	HITS			Number of cache hits

4.3.9.13 IMISS

Address offset: 0x54C

I-code cache miss counter.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	RW	MISSES			Number of cache misses

4.3.10 Electrical specification

4.3.10.1 Flash programming

Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
n_{WRITE}	Number of times a 32-bit word can be written before erase			2	
$n_{ENDURANCE}$	Erase cycles per page	10000			
t_{WRITE}	Time to write one 32-bit word			41[1]	µs
$t_{ERASEPAGE}$	Time to erase one page			85[1]	ms
$t_{ERASEALL}$	Time to erase all flash			169[1]	ms
$t_{ERASEPAGEPARTIAL,acc}$	Accuracy of the partial page erase duration. Total execution time for one partial page erase is defined as ERASEPAGEPARTIALCFG * $t_{ERASEPAGEPARTIAL,acc}$.			1.05[1]	

[1] Applies when HFXO is used. Timing varies according to HFINT accuracy when HFINT is used.

4.3.10.2 Cache size

Symbol	Description	Min.	Typ.	Max.	Units
$Size_{ICODE}$	I-Code cache size		2048		Bytes

4.4 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

4.4.1 Registers

Base address	Peripheral	Instance	Description	Configuration
0x10000000	FICR	FICR	Factory information configuration	

Table 7: Instances

Register	Offset	Description	
CODEPAGESIZE	0x010	Code memory page size	
CODESIZE	0x014	Code memory size	
DEVICEID[0]	0x060	Device identifier	
DEVICEID[1]	0x064	Device identifier	
ER[0]	0x080	Encryption root, word 0	
ER[1]	0x084	Encryption root, word 1	
ER[2]	0x088	Encryption root, word 2	
ER[3]	0x08C	Encryption root, word 3	
IR[0]	0x090	Identity Root, word 0	
IR[1]	0x094	Identity Root, word 1	
IR[2]	0x098	Identity Root, word 2	
IR[3]	0x09C	Identity Root, word 3	
DEVICEADDRTYPE	0x0A0	Device address type	
DEVICEADDR[0]	0x0A4	Device address 0	
DEVICEADDR[1]	0x0A8	Device address 1	
INFO.PART	0x100	Part code	
INFO.VARIANT	0x104	Build code (hardware version and production configuration)	
INFO.PACKAGE	0x108	Package option	
INFO.RAM	0x10C	RAM variant	
INFO.FLASH	0x110	Flash variant	
INFO.UNUSED8[0]	0x114		Reserved
INFO.UNUSED8[1]	0x118		Reserved
INFO.UNUSED8[2]	0x11C		Reserved
PRODTEST[0]	0x350	Production test signature 0	
PRODTEST[1]	0x354	Production test signature 1	
PRODTEST[2]	0x358	Production test signature 2	
TEMP.A0	0x404	Slope definition A0	
TEMP.A1	0x408	Slope definition A1	
TEMP.A2	0x40C	Slope definition A2	
TEMP.A3	0x410	Slope definition A3	
TEMP.A4	0x414	Slope definition A4	
TEMP.A5	0x418	Slope definition A5	
TEMP.B0	0x41C	Y-intercept B0	

Register	Offset	Description
TEMP.B1	0x420	Y-intercept B1
TEMP.B2	0x424	Y-intercept B2
TEMP.B3	0x428	Y-intercept B3
TEMP.B4	0x42C	Y-intercept B4
TEMP.B5	0x430	Y-intercept B5
TEMP.T0	0x434	Segment end T0
TEMP.T1	0x438	Segment end T1
TEMP.T2	0x43C	Segment end T2
TEMP.T3	0x440	Segment end T3
TEMP.T4	0x444	Segment end T4
NFC.TAGHEADER0	0x450	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST.
NFC.TAGHEADER1	0x454	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST.
NFC.TAGHEADER2	0x458	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST.
NFC.TAGHEADER3	0x45C	Default header for NFC tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST, and NFCID1_LAST.
TRNG90B.BYTES	0xC00	Amount of bytes for the required entropy bits
TRNG90B.RCCUTOFF	0xC04	Repetition counter cutoff
TRNG90B.APCUTOFF	0xC08	Adaptive proportion cutoff
TRNG90B.STARTUP	0xC0C	Amount of bytes for the startup tests
TRNG90B.ROSC1	0xC10	Sample count for ring oscillator 1
TRNG90B.ROSC2	0xC14	Sample count for ring oscillator 2
TRNG90B.ROSC3	0xC18	Sample count for ring oscillator 3
TRNG90B.ROSC4	0xC1C	Sample count for ring oscillator 4

Table 8: Register overview

4.4.1.1 CODEPAGESIZE

Address offset: 0x010

Code memory page size

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	Acce	Field	Value ID	Value	Description
A	R	CODEPAGESIZE			Code memory page size

4.4.1.2 CODESIZE

Address offset: 0x014

Code memory size

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	Acce	Field	Value ID	Value	Description
A	R	CODESIZE			Code memory size in number of pages Total code space is: CODEPAGESIZE * CODESIZE

4.4.1.3 DEVICEID[n] (n=0..1)

Address offset: 0x060 + (n × 0x4)

Device identifier

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

ID	Acce	Field	Value ID	Value	Description
A	R	DEVICEID			64 bit unique device identifier DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.

4.4.1.4 ER[n] (n=0..3)

Address offset: 0x080 + (n × 0x4)

Encryption root, word n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

ID	Acce	Field	Value ID	Value	Description
A	R	ER			Encryption root, word n

4.4.1.5 IR[n] (n=0..3)

Address offset: 0x090 + (n × 0x4)

Identity Root, word n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

ID	Acce	Field	Value ID	Value	Description
A	R	IR			Identity Root, word n

4.4.1.6 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

ID	Acce	Field	Value ID	Value	Description
A	R	DEVICEADDRTYPE			Device address type
			Public	0	Public address
			Random	1	Random address

4.4.1.7 DEVICEADDR[n] (n=0..1)

Address offset: 0x0A4 + (n × 0x4)

Device address n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	Acce	Field	Value ID	Value	Description
A	R	DEVICEADDR			48 bit device address DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.

4.4.1.8 INFO.PART

Address offset: 0x100

Part code

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00052840	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**

ID	Acce	Field	Value ID	Value	Description
A	R	PART			Part code
			N52840	0x52840	nRF52840
			Unspecified	0xFFFFFFFF	Unspecified

4.4.1.9 INFO.VARIANT

Address offset: 0x104

Build code (hardware version and production configuration)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	Acce	Field	Value ID	Value	Description
A	R	VARIANT			Build code (hardware version and production configuration). Encoded as ASCII.
			AAAA	0x41414141	AAAA
			BAAA	0x42414141	BAAA
			CAAA	0x43414141	CAAA
			AABA	0x41414241	AABA
			AABB	0x41414242	AABB
			AACA	0x41414341	AACA
			AAAB	0x41414142	AAAB
			Unspecified	0xFFFFFFFF	Unspecified

4.4.1.10 INFO.PACKAGE

Address offset: 0x108

Package option

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	Acce	Field	Value ID	Value	Description
A	R	PACKAGE			Package option
			QI	0x2004	QIxx - 73-pin aQFN
			CK	0x2005	CKxx - WLCSP
			Unspecified	0xFFFFFFFF	Unspecified

4.4.1.11 INFO.RAM

Address offset: 0x10C

RAM variant

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	Acce	Field	Value ID	Value	Description
A	R	RAM			RAM variant
			K16	0x10	16 kByte RAM
			K32	0x20	32 kByte RAM
			K64	0x40	64 kByte RAM
			K128	0x80	128 kByte RAM
			K256	0x100	256 kByte RAM
			Unspecified	0xFFFFFFFF	Unspecified

4.4.1.12 INFO.FLASH

Address offset: 0x110

Flash variant

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	Acce	Field	Value ID	Value	Description
A	R	FLASH			Flash variant
			K128	0x80	128 kByte FLASH
			K256	0x100	256 kByte FLASH
			K512	0x200	512 kByte FLASH
			K1024	0x400	1 MByte FLASH
			K2048	0x800	2 MByte FLASH
			Unspecified	0xFFFFFFFF	Unspecified

4.4.1.13 PRODTEST[n] (n=0..2)

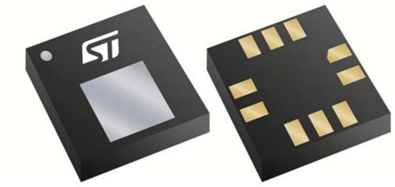
Address offset: 0x350 + (n × 0x4)

Production test signature n

LPS22HB

MEMS nano pressure sensor: 260-1260 hPa absolute digital output barometer

Datasheet - production data



HLGA-10L
(2.0 x 2.0 x 0.76 mm)

Features

- 260 to 1260 hPa absolute pressure range
- Current consumption down to 3 μA
- High overpressure capability: 20x full-scale
- Embedded temperature compensation
- 24-bit pressure data output
- 16-bit temperature data output
- ODR from 1 Hz to 75 Hz
- SPI and I²C interfaces
- Embedded FIFO
- Interrupt functions: Data Ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V
- High shock survivability: 22,000 *g*
- Small and thin package
- ECOPACK® lead-free compliant

Applications

- Altimeters and barometers for portable devices
- GPS applications
- Weather station equipment
- Sport watches

Description

The LPS22HB is an ultra-compact piezoresistive absolute pressure sensor which functions as a digital output barometer. The device comprises a sensing element and an IC interface which communicates through I^{2}C or SPI from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane manufactured using a dedicated process developed by ST.

The LPS22HB is available in a full-mold, holed LGA package (HLGA). It is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
LPS22HBTR	-40 to +85°C	HLGA-10L	Tape and reel

This is information on a product in full production.

Contents

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List of figures

1 Block diagrams

Figure 1. Device architecture block diagram

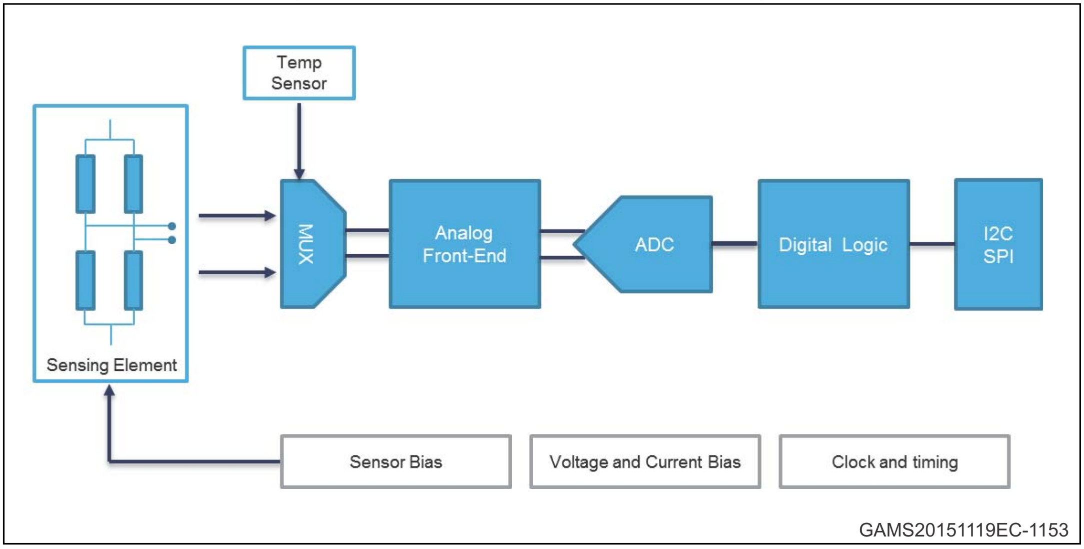
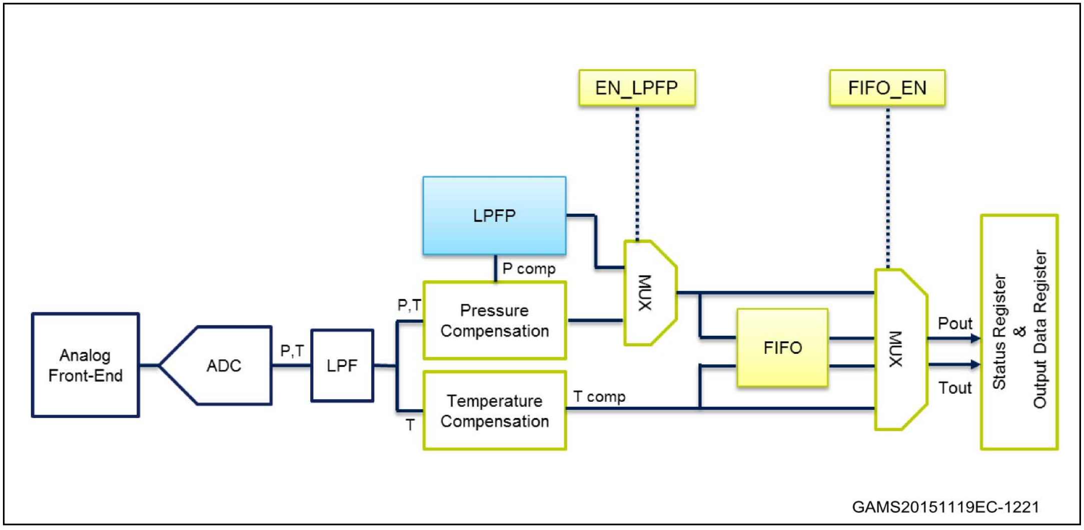


Figure 2. Digital logic



2 Pin description

Figure 3. Pin connections (bottom view)

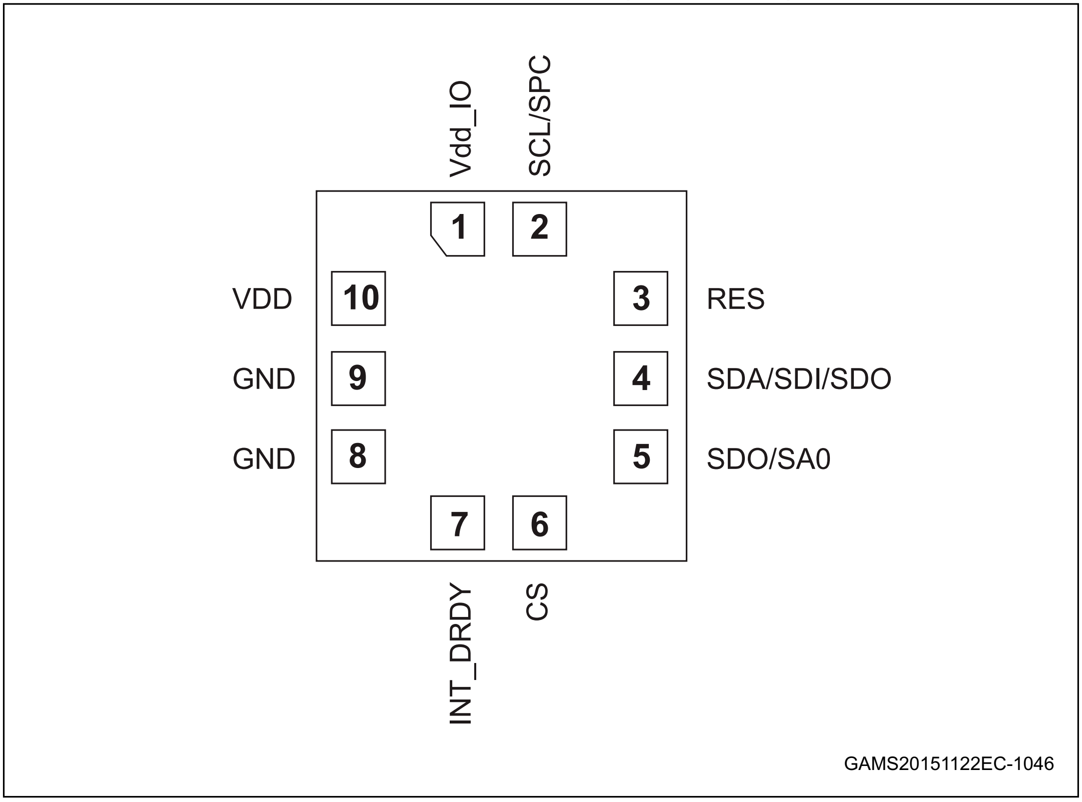


Table 2. Pin description

Pin number	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL SPC	I^{2}C serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I^{2}C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input/output (SDI/SDO)
5	SDO SA0	4-wire SPI serial data output (SDO) I^{2}C less significant bit of the device address (SA0)
6	CS	SPI enable I^{2}C/SPI mode selection (1: SPI idle mode / I^{2}C communication enabled; 0: SPI communication mode / I^{2}C disabled)
7	INT_DRDY	Interrupt or Data Ready
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply

3 Mechanical and electrical specifications

3.1 Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pressure sensor characteristics						
PT_{op}	Operating temperature range		-40		+85	°C
PT_{full}	Full accuracy temperature range		0		+65	°C
P_{op}	Operating pressure range		260		1260	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity			4096		LSB/ hPa
P_{AccRel}	Relative accuracy over pressure	P = 800 - 1100 hPa T = 25 °C		±0.1		hPa
P_{AccT}	Absolute accuracy over temperature	P_{op} T = 0 to 65 °C After OPC(2)		±0.1		hPa
		P_{op} T = 0 to 65 °C no OPC (2)		±1		
P_{noise}	RMS pressure sensing noise(3)	with embedded filtering		0.0075		hPa RMS
ODR_{Pres}	Pressure output data rate(4)			1 10 25 50 75		Hz
Temperature sensor characteristics						
T_{op}	Operating temperature range		-40		+85	°C
T_{sens}	Temperature sensitivity			100		LSB/°C
T_{acc}	Temperature absolute accuracy	T = 0 to 65 °C		±1.5		°C
ODR_T	Output temperature data rate(4)			1 10 25 50 75		Hz

1. Typical specifications are not guaranteed.
2. OPC: One-Point Calibration, see *RPDS_L (18h)*, *RPDS_H (19h)*.
3. Pressure noise RMS evaluated in a controlled environment, based on the average standard deviation of 50 measurements at highest ODR and with LC_EN bit = 0, EN_LPFP = 1, LPFP_CFG = 1.
4. Output data rate is configured acting on ODR[2:0] in *CTRL_REG1 (10h)*.

3.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
Vdd_IO	IO supply voltage		1.7		Vdd+0.1	V
Idd	Supply current	@ ODR 1 Hz LC_EN bit = 0		12		µA
		@ ODR 1 Hz LC_EN bit = 1		3		
IddPdn	Supply current in power-down mode			1		µA

[1] Typical specifications are not guaranteed.

Table 5. DC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DC input characteristics						
Vil	Low-level input voltage (Schmitt buffer)	-	-	-	0.2 * Vdd_IO	V
Vih	High-level input voltage (Schmitt buffer)	-	0.8 * Vdd_IO	-	-	V
DC output characteristics						
Vol	Low-level output voltage		-	-	0.2	V
Voh	High-level output voltage		Vdd_IO - 0.2	-	-	V

3.3 Communication interface characteristics

3.3.1 SPI - serial peripheral interface

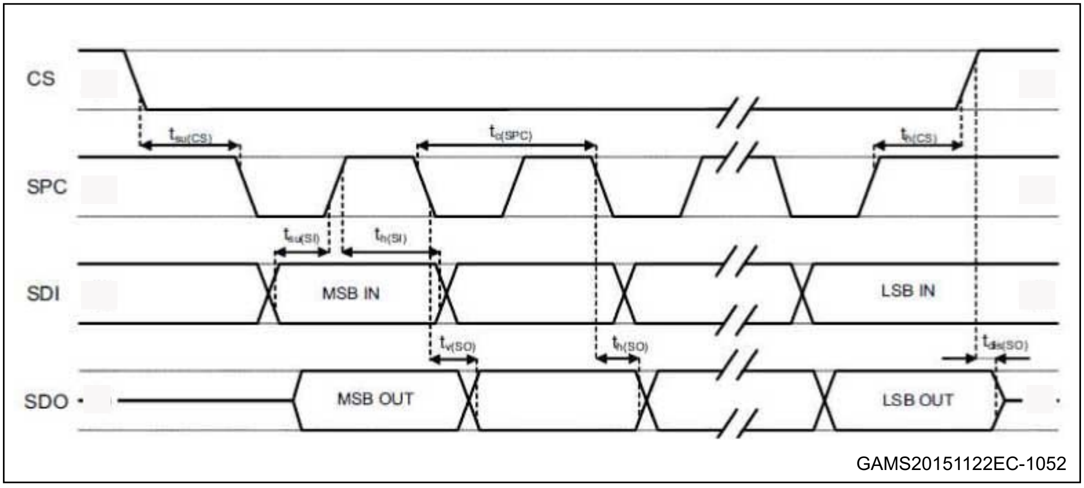
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

Symbol	Parameter	Value[1]		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 4. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

3.3.2 I²C - inter-IC control interface

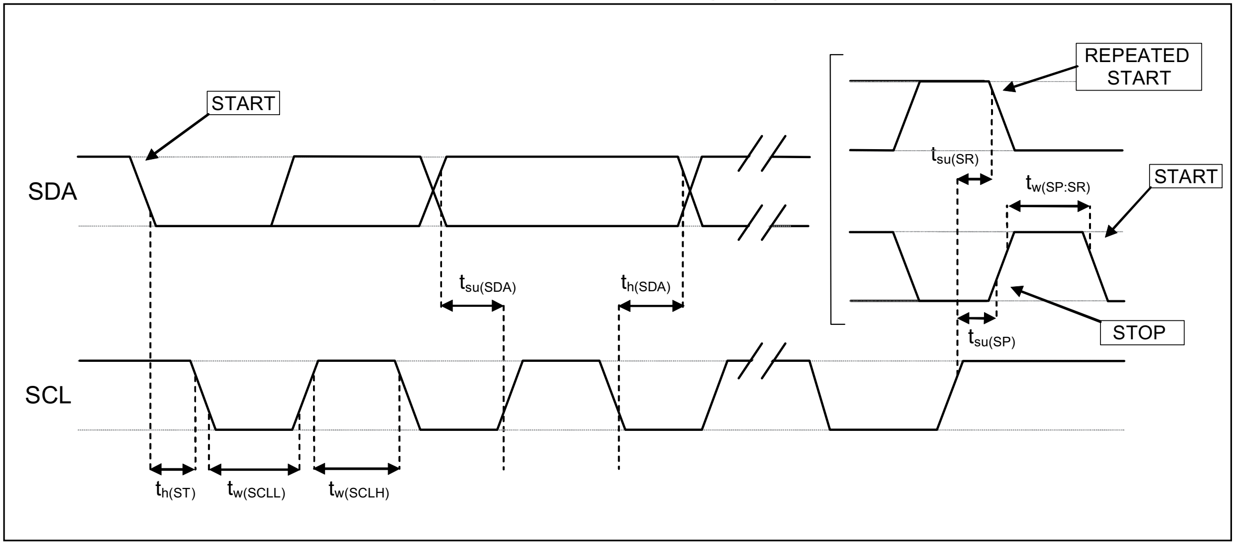
Subject to general operating conditions for Vdd and T_{OP}.

Table 7. I²C slave timing values

Symbol	Parameter (1)	I²C standard mode[(1)]		I²C fast mode[(1)]		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

[1] Data based on standard I²C protocol requirement, not tested in production.

Figure 5. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

3.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
P	Overpressure	2	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

APDS-9960

Digital Proximity, Ambient Light, RGB and Gesture Sensor

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

Description

The APDS-9960 device features advanced Gesture detection, Proximity detection, Digital Ambient Light Sense (ALS) and Color Sense (RGBC). The slim modular package, L 3.94 × W 2.36 × H 1.35 mm, incorporates an IR LED and factory calibrated LED driver for drop-in compatibility with existing footprints.

Gesture detection

Gesture detection utilizes four directional photodiodes to sense reflected IR energy (sourced by the integrated LED) to convert physical motion information (i.e. velocity, direction and distance) to a digital information. The architecture of the gesture engine features automatic activation (based on Proximity engine results), ambient light subtraction, cross-talk cancelation, dual 8-bit data converters, power saving inter-conversion delay, 32-dataset FIFO, and interrupt-driven I^{2}C-bus communication. The gesture engine accommodates a wide range of mobile device gesturing requirements: simple UP-DOWN-RIGHT-LEFT gestures or more complex gestures can be accurately sensed. Power consumption and noise are minimized with adjustable IR LED timing.

Description continued on next page...

Applications

- Gesture Detection
- Color Sense
- Ambient Light Sensing
- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement

Ordering Information

Part Number	Packaging	Quantity
APDS-9960	Tape & Reel	5000 per reel

Features

- Ambient Light and RGB Color Sensing, Proximity Sensing, and Gesture Detection in an Optical Module
- Ambient Light and RGB Color Sensing
  - UV and IR blocking filters
  - Programmable gain and integration time
  - Very high sensitivity – Ideally suited for operation behind dark glass
- Proximity Sensing
  - Trimmed to provide consistent reading
  - Ambient light rejection
  - Offset compensation
  - Programmable driver for IR LED current
  - Saturation indicator bit
- Complex Gesture Sensing
  - Four separate diodes sensitive to different directions
  - Ambient light rejection
  - Offset compensation
  - Programmable driver for IR LED current
  - 32 dataset storage FIFO
  - Interrupt driven I^{2}C-bus communication
- I^{2}C-bus Fast Mode Compatible Interface
  - Data Rates up to 400 kHz
  - Dedicated Interrupt Pin
- Small Package L 3.94 × W 2.36 × H 1.35 mm

Description (Cont.)

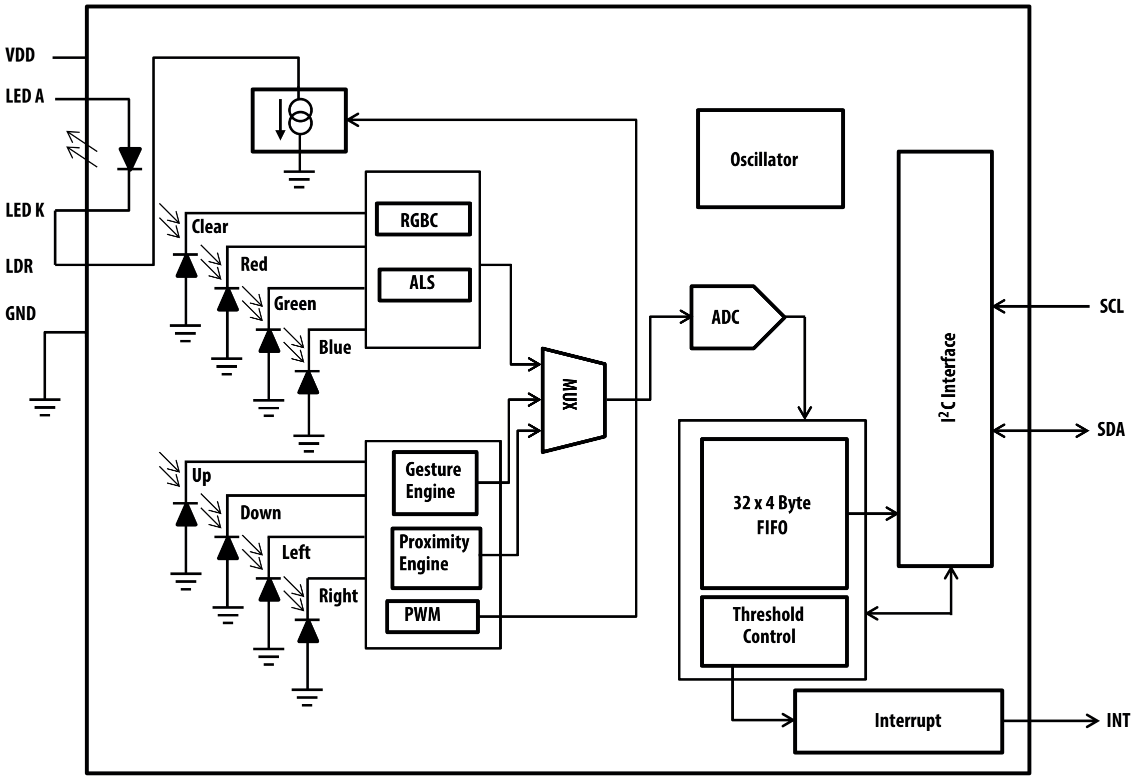
Proximity detection

The Proximity detection feature provides distance measurement (E.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated LED). Detect/release events are interrupt driven, and occur whenever proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for system offset caused by unwanted IR energy reflections appearing at the sensor. The IR LED intensity is factory trimmed to eliminate the need for end-equipment calibration due to component variations. Proximity results are further improved by automatic ambient light subtraction.

Color and ALS detection

The Color and ALS detection feature provides red, green, blue and clear light intensity data. Each of the R, G, B, C channels have a UV and IR blocking filter and a dedicated data converter producing16-bit data simultaneously. This architecture allows applications to accurately measure ambient light and sense color which enables devices to calculate color temperature and control display backlight.

Functional Block Diagram



I/O Pins Configuration

Pin	Name	Type	Description
1	SDA	I/O	I^{2}C serial data I/O terminal - serial data I/O for I^{2}C-bus
2	INT	O	Interrupt - open drain (active low)
3	LDR		LED driver input for proximity IR LED, constant current source LED driver
4	LEDK		LED Cathode, connect to LDR pin when using internal LED driver circuit
5	LEDA		LED Anode, connect to V_{LEDA} on PCB
6	GND		Power supply ground. All voltages are referenced to GND
7	SCL	I	I^{2}C serial clock input terminal - clock signal for I^{2}C serial data
8	V_{DD}		Power supply voltage

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)*

Parameter	Symbol	Min	Max	Units	Conditions
Power supply voltage [1]	V_{DD}		3.8	V	
Input voltage range	V_{IN}	-0.5	3.8	V	
Output voltage range	V_{OUT}	-0.3	3.8	V	
Storage temperature range	T_{stg}	-40	85	°C	

* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating ambient temperature	T_A	-30		85	°C
Power supply voltage	V_{DD}	2.4	3.0	3.6	V
Supply voltage accuracy, V_{DD} total error including transients		-3		+3	%
LED supply voltage	V_{LEDA}	3.0		4.5	V

Operating Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
IDD supply current [1]	I_{DD}		200	250	µA	Active ALS state PON = AEN = 1, PEN = 0
			790			Proximity, LDR pulse ON, PPulse = 8 (I_{LDR} not included)
			790			Gesture, LDR pulse ON, GPulse = 8 (I_{LDR} not included)
			38			Wait state PON = 1, AEN = PEN = 0
			1.0	10.0		Sleep state [2]
V_{OL} INT, SDA output low voltage	V_{OL}	0		0.4	V	3 mA sink current
I_{LEAK} leakage current, SDA, SCL, INT pins	I_{LEAK}	–5		5	µA	
I_{LEAK} leakage current, LDR P\pin	I_{LEAK}	–10		10	µA	
SCL, SDA input high voltage, V_{IH}	V_{IH}	1.26		V_{DD}	V	
SCL, SDA input low voltage, V_{IL}	V_{IL}			0.54	V	

Notes

1. Values are shown at the VDD pin and do not include current through the IR LED.
2. Sleep state occurs when PON = 0 and I2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will be high.

Optical Characteristics, V_{DD} = 3 V, T_A = 25 °C, AGAIN = 16×, AEN = 1 (unless otherwise noted)

Parameter	Red Channel		Green Channel		Blue Channel		Units	Test Conditions
	Min	Max	Min	Max	Min	Max		
Irradiance responsivity [1]	0	15	10	42	57	100	%	λ_D = 465 nm [2]
	4	25	54	85	10	45		λ_D = 525 nm [3]
	64	120	0	14	3	29		λ_D = 625 nm [4]

Notes:

1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda_{½}$ = 22 nm.
3. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda_{½}$ = 35 nm.
4. The 625 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 625 nm, spectral halfwidth $\Delta\lambda_{½}$ = 15 nm.

RGBC Characteristics, V_{DD} = 3 V, T_A = 25 °C, AGAIN = 16×, AEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Dark ALS count value		0	3	counts	E_e = 0, AGAIN = 64×, ATIME = 0×DB (100 ms)
ADC integration time step size		2.78		ms	ATIME = 0×FF
ADC number of integration steps	1		256	steps	
Full scale ADC counts per step			1025	counts	
Full scale ADC count value			65535	counts	ATIME = 0×C0 (175 ms)
Gain scaling, relative to 1× gain setting	3.6	4	4.4		4×
	14.4	16	17.6		16×
	57.6	64	70.4		64×
Clear channel irradiance responsivity	18.88	23.60	28.32	counts/(μW/cm2)	Neutral white LED, λ = 560 nm

Proximity Characteristics, V_{DD} = 3 V, T_A = 25 °C, PEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
ADC conversion time step size		696.6		μs	
ADC number of integration steps		1		steps	
Full scale ADC counts			255	counts	
LED pulse count [1]	1		64	pulses	
LED pulse width – LED on time [2]		4		μs	PPLEN = 0
		8			PPLEN = 1
		16			PPLEN = 2
		32			PPLEN = 3
LED drive current [3]		100		mA	LDRIVE = 0
		50			LDRIVE = 1
		25			LDRIVE = 2
		12.5			LDRIVE = 3
LED boost [3]		100		%	LED_BOOST = 0
		150			LED_BOOST = 1
		200			LED_BOOST = 2
		300			LED_BOOST = 3
Proximity ADC count value, no object [4]		10	25	counts	V_{LEDA} = 3 V, LDRIVE = 100 mA, PPULSE = 8, PGAIN = 4x, PPLEN = 8 μs, LED_BOOST = 100%, open view (no glass) and no reflective object above the module.

Table continued on next page...

Proximity Characteristics, V_{DD} = 3 V, T_A = 25 °C, PEN = 1 (unless otherwise noted) (continued)

Parameter	Min	Typ	Max	Units	Test Conditions
Proximity ADC count value, 100 mm distance object [5, 6]	96	120	144	counts	Reflecting object – 73 mm × 83 mm Kodak 90% grey card, 100 mm distance, V_{LEDA} = 3 V, LDRIVE = 100 mA, PPULSE = 8, PGAIN = 4x, PPLEN = 8 µs, LED_BOOST = 100%, open view (no glass) above the module.

Notes:
1. This parameter is ensured by design and characterization and is not 100% tested. 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.
2. Value may be as much as 1.36 µs longer than specified.
3. Value is factory-adjusted to meet the Proximity count specification. Considerable variation (relative to the typical value) is possible after adjustment. LED BOOST increases current setting (as defined by LDRIVE or GLDRIVE). For example, if LDRIVE = 0 and LED BOOST = 100%, LDR current is 100 mA.
4. Proximity offset value varies with power supply characteristics and noise.
5. ILEDA is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
6. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.

Gesture Characteristics, V_{DD} = 3 V, T_A = 25 °C, GEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
ADC conversion time step size [1]		1.39		ms	
LED pulse count [2]	1		64	pulses	
LED pulse width – LED on time [3]		4		µs	GPLEN = 0
		8			GPLEN = 1
		12			GPLEN = 2
		16			GPLEN = 3
LED drive current [4]		100		mA	GLDRIVE = 0
		50			GLDRIVE = 1
		25			GLDRIVE = 2
		12.5			GLDRIVE = 3
LED boost [4]		100		%	LED_BOOST = 0
		150			LED_BOOST = 1
		200			LED_BOOST = 2 [5]
		300			LED_BOOST = 3 [5]
Gesture ADC count value, no object [6]		10	25	counts	V_{LEDA} = 3 V, GLDRIVE = 100 mA, GPULSE = 8, GGAIN = 4x, GPLEN = 8 µs, LED_BOOST = 100%, open view (no glass) and no reflective object above the module, sum of UP & DOWN photodiodes.
Gesture ADC count value [7, 8]	96	120	144	counts	Reflecting object – 73 mm × 83 mm Kodak 90% grey card, 100 mm distance, V_{LEDA} = 3 V, GLDRIVE = 100 mA, GPULSE = 8, GGAIN = 4x, GPLEN = 8 µs, LED_BOOST = 100%, open view (no glass) above the module, sum of UP & DOWN photodiodes.
Gesture wait step size		2.78		ms	GTIME = 0x01

Notes:
1. Each U/D or R/L pair requires a conversion time of 696.6µs. For all four directions the conversion requires twice as much time.
2. This parameter ensured by design and characterization and is not 100% tested. 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.
3. Value may be as much as 1.36 µs longer than specified.
4. Value is factory-adjusted to meet the Gesture count specification. Considerable variation (relative to the typical value) is possible after adjustment.
5. When operating at these LED drive conditions, it is recommended to separate the VDD and VLEDA supplies.
6. Gesture offset value varies with power supply characteristics and noise.
7. ILEDA is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
8. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.

IR LED Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Peak Wavelength, λ_P		950		nm	I_F = 20 mA
Spectrum Width, Half Power, Δλ		30		nm	I_F = 20 mA
Optical Rise Time, T_R		20		ns	I_F = 100 mA
Optical Fall Time, T_F		20		ns	I_F = 100 mA

Wait Characteristics, V_{DD} = 3 V, T_A = 25 °C, WEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Wait Step Size		2.78		ms	WTIME = 0×FF

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted) *

Parameter	Symbol	Min.	Max.	Unit
Clock frequency (I^{2}C-bus only)	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	µs
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	µs
Data hold time	$t_{HD;DAT}$	30	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	ns
LOW period of the SCL clock	t_{LOW}	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	–	µs
Clock/data fall time	t_f	20	300	ns
Clock/data rise time	t_r	20	300	ns
Input pin capacitance	C_i	–	10	pF

* Specified by design and characterization; not production tested.

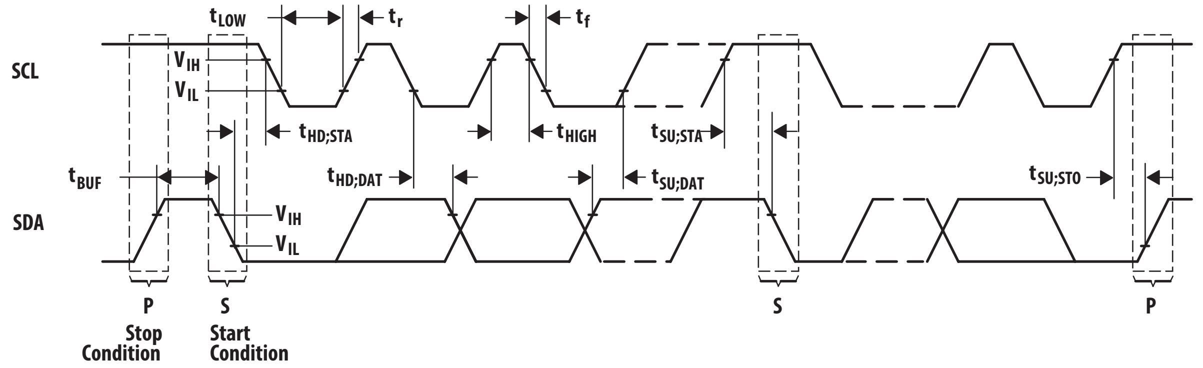


Figure 1. Timing Diagrams

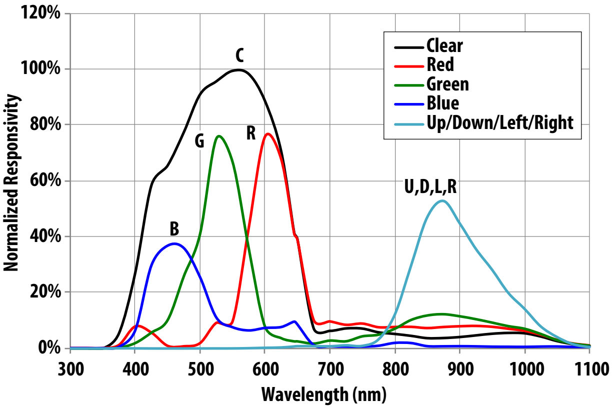


Figure 2. Spectral Response

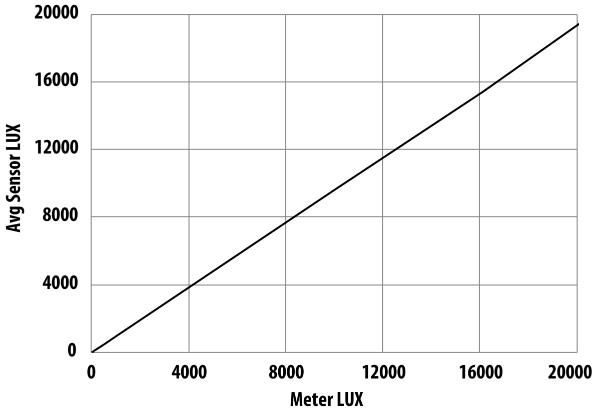


Figure 3a. ALS Sensor LUX vs Meter LUX using White Light

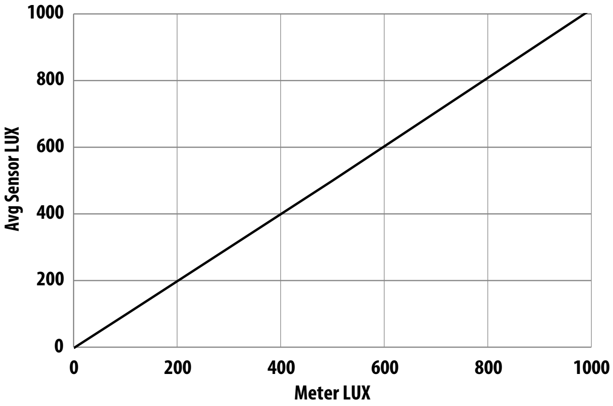


Figure 3b. ALS Sensor LUX vs Meter LUX using Incandescent Light

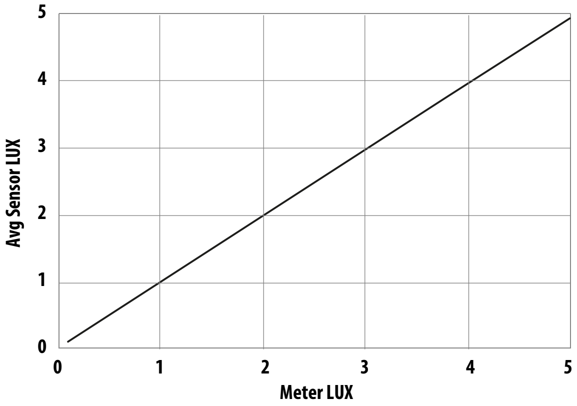


Figure 3c. ALS Sensor LUX vs Meter LUX using White Light

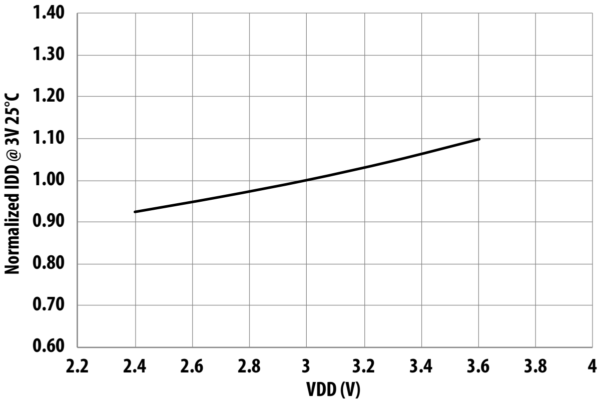


Figure 4a. Normalized IDD vs. VDD

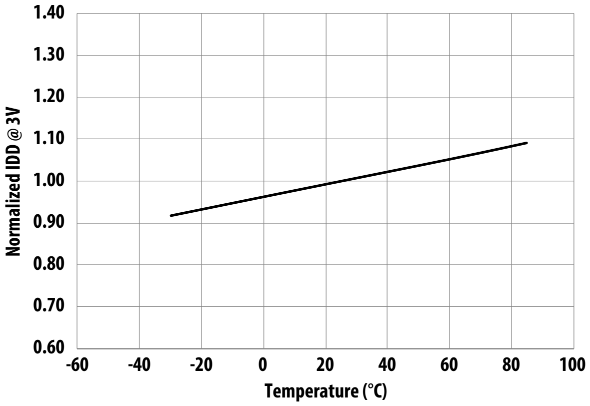


Figure 4b. Normalized IDD vs. Temperature