Keystone (Group 6)
dlofran2, mwdanie2, gentil2
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ECE 411 – MP3.2
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Roadmap

For the third checkpoint, we will finish the implementation of our 4-way set-associative L2 cache and fully integrate it to our design. To complete the checkpoint, we will also implement the hazard detection and data forwarding systems of the processor (see paper design and full diagram.)

Like for previous checkpoints, we will split those tasks among the three members. We will all start coding a part of the checkpoint and debug together. We will most likely keep our more specific tasks: Matt keeps track of the paper design as some changes are made during the implementation; Dominic modifies the files during the debugging phase, and I (Lisa) will maintain the bug log file in order to have all the information for the necessary reports. Finally, since checkpoint 3 goals include some designs of the next checkpoint, we will all work on creating the expected designs of the branch predictor, the eviction write buffer and the performance counters.