Keystone (Group 6)
dlofran2, mwdanie2, gentil2
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Roadmap

For the next and final checkpoint, we decided that it would be a good idea to have each member suggesting some advanced design options that could improve the performance of our LC-3b processor. By doing so, we came up with a lot of good ideas that we still have to choose from, depending on how complicated it may get but how more efficient the processor can get with these features.

In fact, we are thinking of changing our 2-way set-associative L1 D-cache to a 4-way set-associative cache, and perform the same changes to the L2 cache. On top of this specific feature that we started to think about at the very beginning of the MP, we are considering making the static branch predictor a dynamic weakly not taken branch predictor, implementing cache flushing, multiple issue, leapfrogging in the MEM stage, and hardware pre-fetching. Like I specified before, we still need to decide on which ones we will actually implement besides the 4-way set-associative cache.