Keystone (Group 6)
dlofran2, mwdanie2, gentil2
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Progress Report

//Intro

For this checkpoint, we had to complete the L2 cache implementation and integrate it to the rest of design by connecting it to the arbiter, itself connected to the L1 I-cache and L1 D-cache. We also had to create the hazard detection and forwarding units.

//L2 progress and bugs

While we planned on switching the L1 D-cache to a 4-way set-associative, and make the L2 cache a 4-way as well, we noticed that too many working units and decided to wait until the whole processor is working correctly, in order to have a better image of it before changing the cache.

//Hazard progress and bugs

Although it has not been possible to change our cache, we did accomplish a mandatory part of the third checkpoint: hazard detection and forwarding. During the implementation of the data forwarding, we encountered a few difficulties. In fact, several components of our design were in conflict with the way forwarding was to be done (e.g. the use of the ALU on an STR operation).

//Conclusion

Like every other checkpoint, we tried to split the work between the three of us: everyone codes, we debug together, and this time, all three of us maintained the paper design as updates were made in the code and added to the reports.