CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: Group 2

Team Members: Emil Kosic

Camden Fergen

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members. Examples may include:*

- Get an B or a better in the class
- Learn about computer architecture and how a processor works.
- Learn about how to make processors faster
- Understand how basic security works with computer architecture
- Use this class as a taste of what other more in depth classes interest our curiosity's
- Learn how to use VHDL and MIPS
- Understand how assembly gets converted to machine code

Team Expectations:

- **Conduct:** Be kind to each other. Both must keep up their work and get it done on time. Communicate well. Prepare to make sacrifices of time. Be very organized, meaning that all components and parts of the project are properly documented, named, and organized precisely into their specific categories.
- **Communication:** Snap chat is the best way of communication. Discord is the secondary for of communication (for voice calls and screen sharing). Expected response time on snap chat should be an hour or 2 (depending outside of class things).
- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*

We will name components to their relevant uses. Register and memory as is from the book and throughout class. If the name has multiple words name such as (onesComp) (no dashes). Test benches named as tb_blahBlah. i_ for input, s_ for signal, o_ for output, g_ for gates. Annotate waveforms, include specific specific components in waveforms and use dividers. Do files to have the same waveforms displayed when both team

members test a component. Variables will be documented and explained so when a team member tests a component, it should be rather easy to read. Github will be used for version control, commit whenever any change is made to a component. Add descriptive to the commit about what was changed, added, or removed.

- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person). Examples of other issues to consider include:*

  We will work together inside of each lab. We will also work outside of lab preferably in person otherwise online (last case scenario).Every week outside of lab we will work together Starting from 6-10 pm on Thursday or Friday 5-9pm and Saturday or Sunday from 2-6pm. We will show up to TA office hours every week on Tuesday from 11:30-12:30, Wednesday from 3-4pm, and Thursday from 3:30-4:30 pm.

- **Peer Evaluation Criteria:** Effort means that the group member is taking their work time for the project seriously and putting 100 percent of their focus in at that time. Contribution means group member is providing useful and valuable work to the group. If a group member has a busy week, they are expected to either get work done before that week (this is the priority) or pick up on that work after that week.

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Plan for an anticipated deadline (read the lab manual and ask your TAs for assistance in setting up a good timeline). Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part	Estimated Time	Design		Test	
		Lead	Deadline	Lead	Deadline
High-level design	1 hr	Emil	2/23/24	Camden	2/27/24
Test programs	4 hr	Emil	3/20/24	Camden	3/20/24
Control logic	2 hr	Camden	3/8/24	Emil	3/10/24
Fetch logic	3 hr	Emil	2/27/24	Camden	2/28/24
Barrel shifter	2 hr	Emil	3/4/24	Camden	3/5/24
ALU integration + Misc updates	2 hr	Camden	3/8/24	Emil	3/10/24
High-level integration	4 hr	Camden	3/18/24	Emil	3/20/24
Synthesis (human effort)	1.5 hr	Camden	3/21/24	Emil	3/23/24

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take*

disproportionately long or short. For your future planning, track this – for future prelabs you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Emil Kosic **Date** 2/21/24

Student Signature Camdem Fergen **Date** 2/21/24