SmartMedia™

# SmartMedia™ Electrical Specifications

# Web-Online Version 1.00

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SSFDC Forum Technical Committee

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Revision History

| Version | | | Date |
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| 1.00 | Web-Online Version | Formal release | May, 1999 |

# Contents

# 0. Introduction

This document defines the electrical characteristics of the SmartMedia™ (SSFDC or Solid State Floppy Disk Card) which is standardized by the SSFDC Forum.

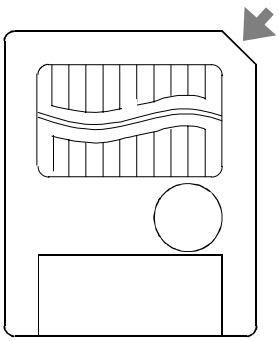
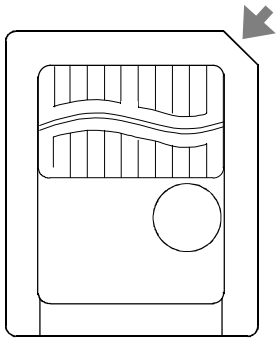
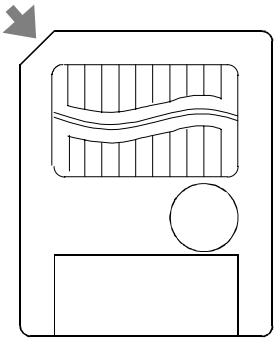
# 1. Applicable Models

There are many kinds of SmartMedia™, each with a different memory type (Flash Memory, MASK ROM), capacity, operating voltage (5 V, 3.3 V), etc. These specifications apply to the following SmartMedia™.

**Table 1-1 Device Code**

| Model | Flash Memory | | MASK ROM |
|---|---|---|---|
| | 3.3 V Model | 5 V Model | (3.3 V Model only) |
| 1 MBytes | 6Eh, E8h, ECh | 6Eh | — |
| 2 MBytes | EAh | 64h | 5Dh |
| 4 MBytes | E3h, E5h | 6Bh, E5h | D5h |
| 8 MBytes | E6h | — | D6h |

**Table 1-2 Package**

| Model | 3.3 V Model | | 5 V Model |
|---|---|---|---|
| Package | (1Chip SmartMedia™) | (2Chip SmartMedia™) | |
| |  |  |  |

# 2. Interface Specifications

## 2.1. Pin Assignments

**Table 2-1 Pin Names**

| No. | Pin Name | I/O | Pin Function | Note |
|---|---|---|---|---|
| 1 | GND | | Ground | |
| 2 | CLE | I | Command Latch Enable | |
| 3 | ALE | I | Address Latch Enable | |
| 4 | -WE | I | Write Enable | |
| 5 | -WP | I | Write Protect (Note 1) | Flash Memory only |
| 6 | D0 | I/O | Data 0 | |
| 7 | D1 | I/O | Data 1 | |
| 8 | D2 | I/O | Data 2 | |
| 9 | D3 | I/O | Data 3 | |
| 10 | GND | | Ground | |
| 11 | -CD | O | Card Detect | |
| 12 | VCC | | Vcc | |
| 13 | D4 | I/O | Data 4 | |
| 14 | D5 | I/O | Data 5 | |
| 15 | D6 | I/O | Data 6 | |
| 16 | D7 | I/O | Data 7 | |
| 17 | LVD | O | Low Voltage Detect | |
| 18 | GND | I | Ground (Note 2) | |
| 19 | R/-B | O (OD) | Ready/Busy (Note 3) | |
| 20 | -RE | I | Read Enable | |
| 21 | -CE | I | Card Enable | |
| 22 | VCC | | Vcc | |

(Note 1) Pin 5 is valid only with Flash Memories. In the case of MASK ROMs, this pin is NC (no connect).
(Note 2) For Pin 18, the ground level should be input.
(Note 3) Pin 19, O (OD) is an open drain output.
(Note 4) 'I' is the input signal to the SmartMedia™. 'O' is the output signal from the SmartMedia™. 'I/O' indicates a bi-directional signal.
(Note 5) The symbol '-' appearing before a signal name designates that signal as active low.
(Note 6) The same pin layout is used for all package types.

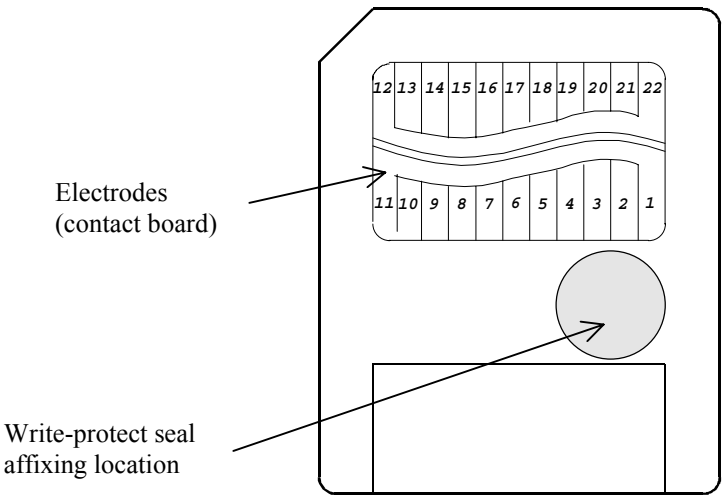



**Figure 2-1 Pin Assignment**

## 2.2. Explanation of Signals

**DO-7 DATA INPUT OUTPUT TERMINAL**

This port is for the input and output of addresses, commands, and data.

**CLE COMMAND LATCH ENABLE**

This signal enables commands to be sent to the internal command register of the device. By setting the level to 'H' when the -WE signal falls and rises, the data on the I/O terminals will be written into the command register.

**ALE ADDRESS LATCH ENABLE**

This signal controls whether data is sent to the internal address register or the internal data register in the device. By setting the level to 'H' when the -WE signal falls and rises, the data present at the I/O terminals is written into the address register as address data. By setting the level to 'L' when the -WE signal falls and rises, the data present at the I/O terminals is written into the data register as input data.

**-WE WRITE ENABLE**

This signal is used to write data present at the I/O terminals into the device.

**-RE READ ENABLE**

This signal enables the output of data serially from the I/O terminals. From the time -RE falls, valid output data will be present at the I/O terminals after tREA, and the internal column address counter advances (+1).

**-CE CARD ENABLE**

This is the device selection signal. If it is set to 'H' in the read state, the standby mode is assumed. Furthermore, in the Busy state during the execution of program and erase operations (R/-B = L), both 'H' and 'L' are accepted. (Standby will not be assumed when 'H'.)

**-WP WRITE PROTECT**

This signal forcibly prohibits writing and erasing. At 'L', the operation of the internal high voltage generating circuit is reset. Normally, the system is operated with this signal 'H', but if the power supply signals are irregular (ON/OFF, etc.), this signal should be 'L' in order to protect stored data from unexpected operations. In the event that the VCC voltage is outside the range in which correct operation is assured, it is recommended that the level be set to 'L'.

**R/-B READY / -BUSY**

This output signal is an open drain output that indicates the internal operating conditions of the device. During program, erase, and read operations, Busy (R/-B = L) is output. Then, Ready is automatically output when the operation is finished.

**-CD CARD DETECT**

This is the SmartMedia™ detection signal which outputs the ground level.

**LVD LOW VOLTAGE DETECT**

This signal is for the detection of the SmartMedia™ operating voltage. It is connected as described below.

| Flash Memory | | MASK ROM |
|---|---|---|
| 3.3 V Model | 5 V Model | |
| VCC | NC | VCC |

**VCC CARD POWER**

Power Supply Voltage.

**GND GROUND**

Ground.

## 2.3. Write Protect

When a write-protect seal (conductive seal) is attached in the write-protect seal position (see Fig. 2-1), the system detects the presence of the write-protect seal and prevents any data from being written to the SmartMedia™. In this way, the data cannot be altered accidently (by write and erase errors, etc.).

The write-protect seal only works on Flash Memories. In the case of MASK ROMs, data cannot be written, with or without a write-protect seal.

## 2.4. Ready/-Busy

The Ready/-Busy signal requires a pull-up resistor for this open-drain output. For the resistance, $Rp$ , refer to the following equation.

$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \sum I_L}$$

$\Sigma I_L$ is the sum of the input current of all devices connected to the Ready/-Busy pin.

# 3. Operating Environment

## 3.1. Absolute Maximum Rating

**Table 3-1 Absolute Maximum Rating**

| Symbol | Parameter | Flash Memory | | MASK ROM | Unit |
|---|---|---|---|---|---|
| | | 3.3 V Model | 5 V Model | | |
| $V_{CC}$ | Supply Voltage | -0.6 to 4.6 | -0.6 to 7.0 | -0.5 to 4.6 | V |
| $V_{AD}$ | Input/Output Voltage | -0.3 to Vcc+0.3 (≤4.6) | -0.3 to Vcc+0.5 (≤7.0) | -0.3 to Vcc+0.3 (≤4.6) | V |

## 3.2. Capacitance

**Table 3-2 Capacitance**

| Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Flash Memory MASK ROM | 1Chip SmartMedia™ | - | - | 10 | pF |
| | 2Chip SmartMedia™ | - | - | 70 | pF |

## 3.3. Operating Voltage

SmartMedia™(s) are available in two power-supply voltages: 3.3 V (low voltage), and 5 V (normal).

**Table 3-3 Operating Voltage**

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Flash Memory | Supply Low Voltage (3.3 V) | Vcc | 3.0 | 3.3 | 3.6 | V |
| | Supply Voltage (5 V) | Vcc | 4.5 | 5.0 | 5.5 | V |
| MASK ROM | Supply Low Voltage (3.3 V) | Vcc | 3.0 | 3.3 | 3.6 | V |

## 3.4. Input Levels

The input levels for SmartMedia™(s) with operating voltages of 3.3 V and 5 V are as follows:

**Table 3-4 Input Levels**

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Input High Voltage Level | $V_{IH}$ | Vcc = 3.3 V ± 0.3 V | 2.2 | Vcc +0.3 | V |
| Input Low Voltage Level | $V_{IL}$ | | -0.3 | 0.6 | V |
| Input High Voltage Level | $V_{IH}$ | Vcc = 5.0 V ± 0.5 V | 2.4 | Vcc +0.3 | V |
| Input Low Voltage Level | $V_{IL}$ | | -0.3 | 0.6 | V |

## 3.5. DC Electrical Characteristics

**Table 3-5 DC Electrical Characteristics (Ta = 0 to 55°C, Vcc=3.3V±0.3V / Vcc=5.0V±0.5V)**

| Symbol | Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | | $V_{IN}$ = 0 V–Vcc | | | ±10 | µA |
| $I_{LO}$ | Output Leakage Current | | $V_{OUT}$ = 0.4 V–Vcc | | | ±10 | µA |
| $I_{CCO1}$ | Operating Current | Serial Read | -CE = $V_{IL}$, , $I_{OUT}$ = 0 mA, $T_{cycle}$ = 80 ns | | | 30 | mA |
| $I_{CCO3}$ | | Command Input | $T_{cycle}$ = 80 ns | | | 30 | mA |
| $I_{CCO4}$ | | Data Input (Note) | $T_{cycle}$ = 80 ns | | | 70 | mA |
| $I_{CCO5}$ | | Address Input | $T_{cycle}$ = 80 ns | | | 30 | mA |
| $I_{CCO6}$ | | Program (Note) | — | | | 60 | mA |
| $I_{CCO7}$ | | Erase (Note) | — | | | 40 | mA |
| $I_{CCS1}$ | Stand-by Current (TTL) | | -CE = $V_{IH}$ | | | 1 | mA |
| $I_{CCS2}$ | Stand-by Current (CMOS) | | -CE = Vcc-0.2 V | | | 100 | µA |
| $V_{OH}$ | Output High Voltage Level | | $I_{OH}$ = -400 µA | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage Level | | $I_{OL}$ = 2.0 mA | | | 0.4 | V |
| $I_{OL}$ (R/-B) | Output Low Current (R/-B) | | $V_{OL}$ = 0.4 V | | 8 | | mA |

(Note) Operating current (data input, program, erase) applies to Flash Memories only.

# 4. Device Internal Configuration

## 4.1. Flash Memory

Program and read operations for Flash Memories are done page by page, and can be erased block by block. The internal configuration of the device is as described below.

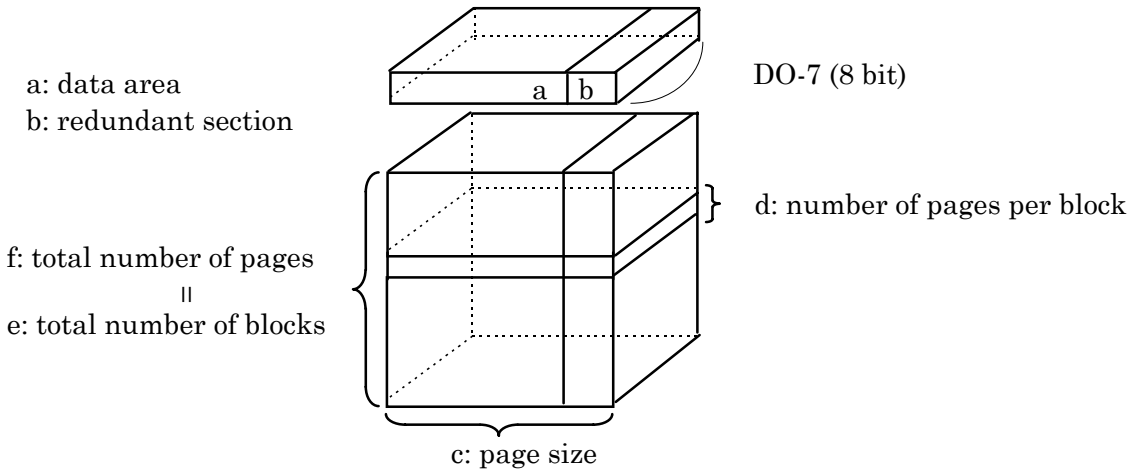



**Figure 4-1 Internal Configuration (Flash Memory )**

**Table 4-1 Memory Configuration (Flash Memory)**

| Model | Page Size (a + b = c) | Block Size (d) | Number of Blocks (e) | Number of Pages (f) |
|---|---|---|---|---|
| 1 MByte | 256 + 8 = 264 Bytes | 16 pages | 256 Blocks | 4,096 pages |
| 2 MBytes | | | 512 Blocks | 8,192 pages |
| 4 MBytes | 512 + 16 = 528 Bytes | | | 8,192 pages |
| 8 MBytes | | | 1,024 Blocks | 16,384 pages |

Flash Memories may contain some blocks that are unusable (failure blocks).
The minimum number of usable blocks for each memory capacity is as shown below.

**Table 4-2 Number of Usable Blocks**

| Model | Number of Zones | Number of Usable Blocks (Min.) |
|---|---|---|
| 1 MByte | — | 252 Blocks |
| 2 MBytes | | 502 Blocks |
| 4 MBytes | | |
| 8 MBytes | | 1,002 Blocks |

The 32 MBytes to 128 MBytes models are controlled in 16 MByte zones.
For details, see the “SmartMedia™ Physical Format Specification”.

## 4.2. MASK ROM

MASK ROMs can only be read one page at a time. The internal configuration of the device is as described below.

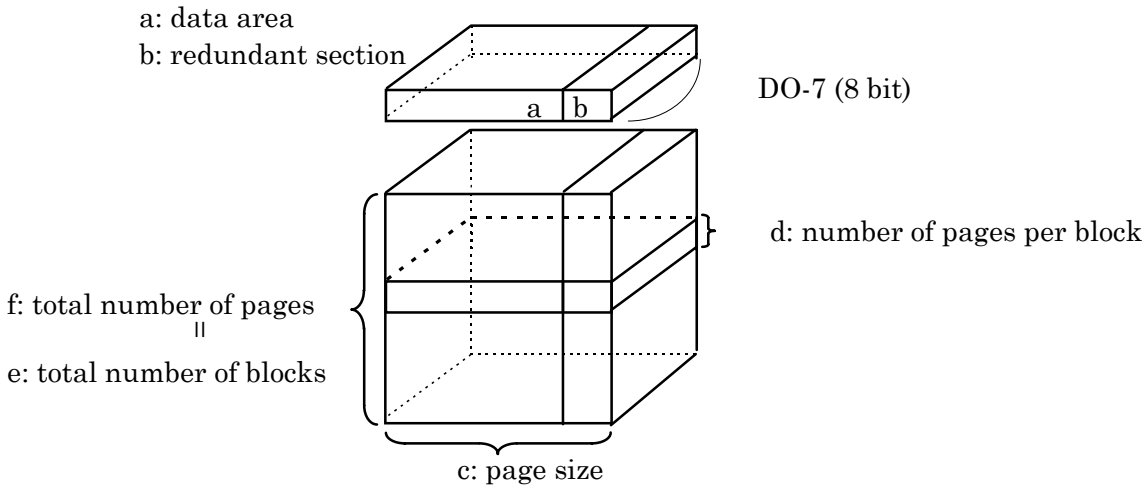



**Figure 4-2 Internal Configuration (MASK ROM)**

**Table 4-3 Memory Configuration (MASK ROM)**

| Model | Page Size (a + b = c) | Block Size (d) | Number of Blocks (e) | Number of Pages (f) |
|---|---|---|---|---|
| 2 MBytes | 512 + (16) = 528 Bytes | 16 pages | 256 Blocks | 4,096 pages |
| 4 MBytes | | | 512 Blocks | 8,192 pages |
| 8 MBytes | | | 1,024 Blocks | 16,384 pages |

(Note) For MASK ROMs, redundant section data (b) are all "FFh".

# 5. Address Settings

As SmartMedia™(s) do not have address terminals, addresses are incorporated during three or four clock cycles from the I/O terminals.

**Table 5-1 Address Configuration**

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1st cycle | CA7 | CA6 | CA5 | CA4 | CA3 | CA2 | CA1 | CA0 |
| 2nd cycle | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| 3rd cycle | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 |

CA0 to CA7: column address
PA0 to PA15: page address

The valid page addresses for each memory capacity are as shown below.

**Table 5-2 Valid Page Addresses (Flash Memory)**

| Model | Valid Page Address | 'L' Level(Note 1) | 'L' Level(Note 2) |
|---|---|---|---|
| 1 MBytes | PA0–PA11 | PA12–PA15 | — |
| 2 MBytes | PA0–PA12 | PA13–PA15 | |
| 4 MBytes | PA0–PA12 | PA13–PA15 | |
| 8 MBytes | PA0–PA13 | PA14, PA15 | |

**Table 5-3 Valid Page Addresses (MASK ROM)**

| Model | Valid Page Address | 'L' Level(Note 1) | 'L' Level(Note 2) |
|---|---|---|---|
| 2 MBytes | PA0–PA11 | PA12–PA15 | — |
| 4 MBytes | PA0–PA12 | PA13–PA15 | |
| 8 MBytes | PA0–PA13 | PA14, PA15 | |

(Note 1) In the 3rd cycle, the relevant I/O terminals for the page addresses mentioned above should be set to 'L'.

## < Flash Memory >

- 256 + 8 Byte/page ( 1 – 2 MBytes)

| 3rd Address Cycle | 2nd Address Cycle | | 1st Address Cycle |
|---|---|---|---|
| A23 ——— A16 | A15 — A12 | A11 — A8 | A7 ——— A0 |
| PA15 ——— PA8 | PA7 — PA4 | PA3 — PA0 | CA7 ——— CA0 |
| BA11 ——————— BA0 | | | |

- 512 + 16 Byte/page ( 4 – 8 MBytes)

| 3rd Address Cycle | 2nd Address Cycle | | | 1st Address Cycle |
|---|---|---|---|---|
| A24 ——— A17 | A16 — A13 | A12 — A9 | A8 | A7 ——— A0 |
| PA15 ——— PA8 | PA7 — PA4 | PA3 — PA0 | CA8 | CA7 ——— CA0 |
| BA11 ——————— BA0 | | | ↑ Note 1 | |

**Fig. 5-1 Address settings**

(Note 1) The input level for CA8 is automatically set within the circuitry by the commands '00' or '01'.

(Note 2) BA0 to BA11 show the block addresses.

## < MASK ROM >

- 512 + 16 Byte/page ( 2 – 8 MBytes)

| 3rd Address Cycle | 2nd Address Cycle | | | 1st Address Cycle |
|---|---|---|---|---|
| A24 ——— A17 | A16 — A13 | A12 — A9 | A8 | A7 A0 |
| PA15 ——— PA8 | PA7 — PA4 | PA3 — PA0 | CA8 | CA7 CA0 |
| BA11 ——————— BA0 | | | ↑ Note 1 | |

**Fig. 5-2 Address settings**

(Note 1) The input level for CA8 is automatically set within the circuitry by the commands '00' or '01'.

(Note 2) BA0 to BA11 show the block addresses.

# 6. Operating Modes

## 6.1. Operating Logic Table

Program, erase, read, and other operating modes are controlled by the following commands. Address input, command input, data I/O, etc., are controlled by the CLE, ALE, -CE, -WE, -RE, and -WP signals.

**Table 6-1 Operating Logic Table**

| Mode | CLE | ALE | -CE | -WE | -RE | -WP |
|---|---|---|---|---|---|---|
| Command Input | H | L | L | ↑ | H | * |
| Address Input | L | H | L | ↑ | H | * |
| Data Input (Note) | L | L | L | ↑ | H | * |
| Data Output | L | L | L | H | ↓ | * |
| During Program/Erase (Note) (During Busy State) | * | * | * | * | * | H |
| Write Protect (Note) | * | * | * | * | * | L |

H: $V_{IH}$ L: $V_{IL}$ *: $V_{IH}$ or $V_{IL}$

(Note) Flash Memories only.

## 6.2. Operating Command Table

**Fig. 6-2 Operating Command Table**

| Function | 1st cycle | 2nd cycle | Acceptable Command during Busy State |
|---|---|---|---|
| Serial Data Input (Note 1) | 80h | | |
| Read (1) | 00h | | |
| Read (2) (Note 2) | 01h | | |
| Read (3) (Note 3) | 50h | | |
| Reset | FFh | | O |
| Page Program (Note 1) | 10h | | |
| Block Erase (Note 1) | 60h | D0h | |
| Status Read | 70h | | O |
| ID Read | 90h | | |

(Note 1) Applies to Flash Memories only.

(Note 2) 512 + 16 Byte/page mode only is supported.

(Note 3) In the case of MASK ROMs, fixed data 'FFh' is output.

(Note 4) Once the read mode is set by using commands 00H, 01H, or 50H, there is no need for a read command to access subsequent pages.

(Note 5) Commands are expressed in hexadecimal code, and D0 to D7 are as described below.

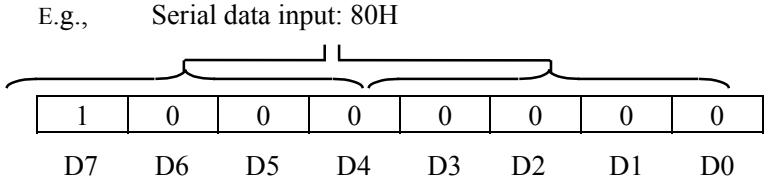



**Fig. 6-1 Correspondence between Commands and I/O Terminals.**

## 6.3. Operating Mode in the Read State.

**Table 6-3 Operating Mode in the Read State**

| Mode | CLE | ALE | -CE | -WE | -RE | D0-D7 | Power |
|---|---|---|---|---|---|---|---|
| Read Mode | L | L | L | H | L | Dout | Active |
| Output Deselect | L | L | L | H | H | High-Z | Active |
| Standby | L | L | H | H | * | High-Z | Standby |

H: $V_{IH}$ L: $V_{IL}$ *: $V_{IH}$ or $V_{IL}$

## 6.4. Status Output Table

When the status read command is being executed, the status can be read. Status outputs are allocated to D0 to D7 as shown below.

**Table 6-4 Status Output Table**

| | Status | Flash Memory | MASK ROM |
|---|---|---|---|
| D0 | Pass/Fail | "0": Pass, "1": Fail | "0": Pass (Ready), "1": Fail (Busy) |
| D1 | Reserved for Future Use | "0" | "0" |
| D2 | | "0" | "0" |
| D3 | | "0" | "0" |
| D4 | | "0" | "0" |
| D5 | | "0" | "0" |
| D6 | Ready/Busy | "0": Busy, "1": Ready | "0": Busy, "1": Ready |
| D7 | Write Protect | "0": Protected, "1": Not Protected | "0": Protected (Fixed) |

(Note) Pass/Fail status at D0 is valid when the device is in the Ready state. Before Pass or Fail is determined, the Ready state must be confirmed.
In MASK ROM, status at D0 is the inverted data of D6.

# 7. Timing Specifications

## 7.1. Cycle Time

$T_{cycle}$ : MIN. 80 ns

## 7.2. AC Characteristics

**Table 7-1 AC Characteristics (Ta= 0 to 55°C, Vcc=3.3V ±0.3V / Vcc=5.0V ±0.5V )**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{CLS}$ | CLE Set up Time | 20 | - | ns |
| $t_{CLH}$ | CLE Hold Time | 40 | - | ns |
| $t_{CS}$ | -CE Set up Time | 20 | - | ns |
| $t_{CH}$ | -CE Hold Time | 40 | - | ns |
| $t_{WP}$ | -WE Pulse Width | 40 | - | ns |
| $t_{ALS}$ | ALE Set up Time | 20 | - | ns |
| $t_{ALH}$ | ALE Hold Time | 40 | - | ns |
| $t_{DS}$ | Data Set up Time | 30 | - | ns |
| $t_{DH}$ | Data Hold Time | 20 | - | ns |
| $t_{WC}$ | Write Cycle Time | 80 | - | ns |
| $t_{WH}$ | -WE High Hold Time | 20 | - | ns |
| $t_{WW}$ | -WP High to -WE Low | 100 | - | ns |
| $t_{RR}$ | Ready to -RE Low | 20 | - | ns |
| $t_{RP}$ | Read Pulse Width | 60 | - | ns |
| $t_{RC}$ | Read Cycle Time | 80 | - | ns |
| $t_{REA}$ | -RE Access Time(Serial Data Access) | - | 45 | ns |
| $t_{CEH}$ | -CE High Hold Time(at the Last Serial Read) | 250 | - | ns |
| $t_{REAID}$ | -RE Access Time(ID Read) | - | 90 | ns |
| $t_{RHZ}$ | -RE High to Output Hi-Z | 5 | 30 | ns |
| $t_{CHZ}$ | -CE High to Output Hi-Z | - | 30 | ns |
| $t_{REH}$ | -RE High Hold Time | 20 | - | ns |
| $t_{IR}$ | Output Hi-Z to -RE Low | 0 | - | ns |
| $t_{RSTO}$ | -RE Access Time(Status Read) | - | 45 | ns |
| $t_{CSTO}$ | -CE Access Time(Status Read) | - | 55 | ns |
| $t_{RHW}$ | -RE High to -WE Low | 0 | - | ns |
| $t_{WHC}$ | -WE High to -CE Low | 50 | - | ns |
| $t_{WHR}$ | -WE High to -RE Low | 60 | - | ns |
| $t_{AR1}$ | ALE Low to -RE Low<br>(Address Register Read,ID Read) | 200 | - | ns |
| $t_{CR}$ | -CE Low to -RE Low<br>(Data Register Read,ID Read) | 200 | - | ns |
| $t_{WB}$ | -WE High to Busy | - | 200 | ns |
| $t_{AR2}$ | ALE Low to -RE Low (Read Cycle) | 150 | - | ns |
| $t_{RB}$ | Last -RE High to Busy(at Sequential Read) | - | 200 | ns |
| $t_{CRY}$ | -CE High to Ready (Note) | - | 1 | µs |

(Note): The length of the period between –CE High and Ready depends on the pull-up resistance at the Ready/–Busy terminal.

**Table 7.2 AC Test Conditions (Ta = 0 to +55°C)**

| Parameter | 3.3 V Model | 5 V Model |
|---|---|---|
| Supply Voltage | 3.3 V ± 0.3 V | 5.0 V ± 0.5 V |
| Input Pulse Level | 0.4 V – 2.4 V | 0.6 V – 2.4 V |
| Input comparison Level | 1.5 V / 1.5 V | 1.5 V / 1.5 V |
| Output Data comparison Level | 1.5 V / 1.5 V | 1.5 V / 1.5 V |
| Output Load | 1 TTL gate, CL = 100 pF | |

## 7.3. Program/Erase/Read/Reset

During program, erase, read, reset operations, it is necessary to monitor the Ready/Busy status. The Busy time during the execution of each operation is shown below.

**Table 7.3 1 MByte to 128 MByte SmartMedia™ Busy Time**

| Symbol | Parameter | | 1 Mbytes to 8 MBytes | | Unit |
|---|---|---|---|---|---|
| | | | Typ. | Max. | |
| $t_{PROG}$ | Program Time | | – | 20 | ms |
| $t_{BERASE}$ | Block Erase Time | | – | 400 | ms |
| $t_R$ | Data Transfer Time (from Cell to Register) | | – | 100 | µs |
| $t_{rst}$ | Device Resetting Time (Program/Erase/Read) | Program | – | 80 | µs |
| | | Erase | – | 6 | ms |
| | | Read | – | 40 | µs |

(Note) For details, see each company's technical data.

(Reference Data)

**Table 7.4 Toshiba SmartMedia™ Busy Time**

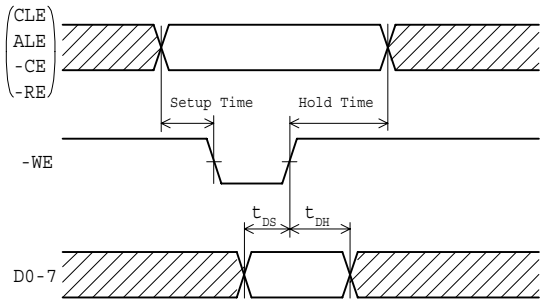
| Symbol | Parameter | TC5816ADC (2 MBytes) | | TC5832DC/TC58V32DC (4 MBytes) | | Unit |
|---|---|---|---|---|---|---|
| | | Typ. | Max. | Typ. | Max. | |
| $t_{PROG}$ | Program Time | 300–1000 | 5000 | 300 | 1500 | µs |
| $t_{BERASE}$ | Block Erase Time | 6 | 100 | 6 | 50 | ms |

**Table 7.5 Samsung SmartMedia™ Busy Time**

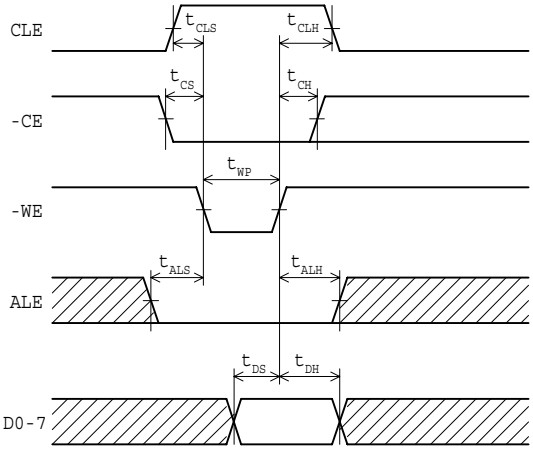
| Symbol | Parameter | SMFN002 (2 MBytes) | | SMFN004/SMFV004 (4 MBytes) | | Unit |
|---|---|---|---|---|---|---|
| | | Typ. | Max. | Typ. | Max. | |
| $t_{PROG}$ | Program Time | 250 | 1500 | 250 | 1500 | µs |
| $t_{BERASE}$ | Block Erase Time | 5 | 10 | 5 | 10 | ms |

## 7.4. Timing Diagram

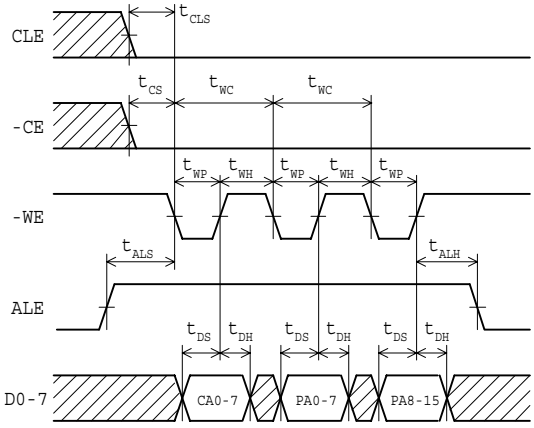
• **Basic Latch Timing for Command, Address and Data**



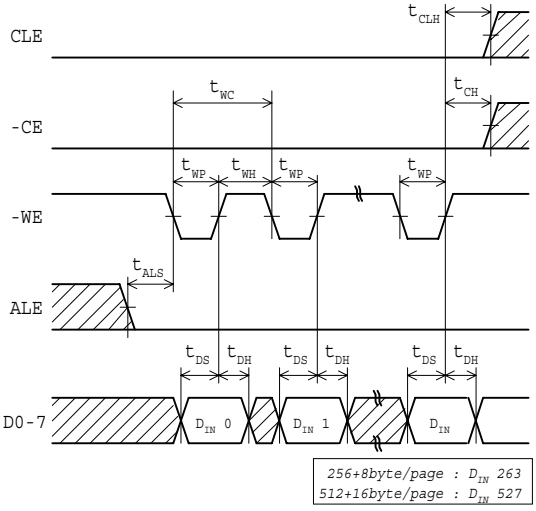

• **Command Input Cycle**




• **Address Input Cycle**

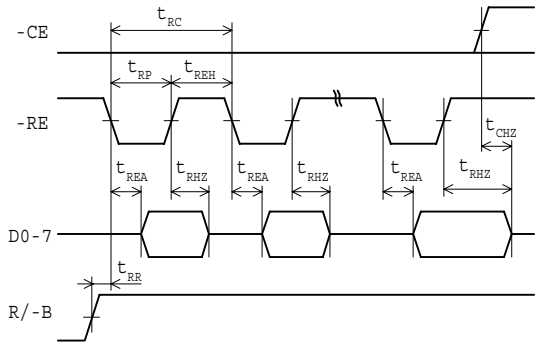



• **Data Input Cycle**

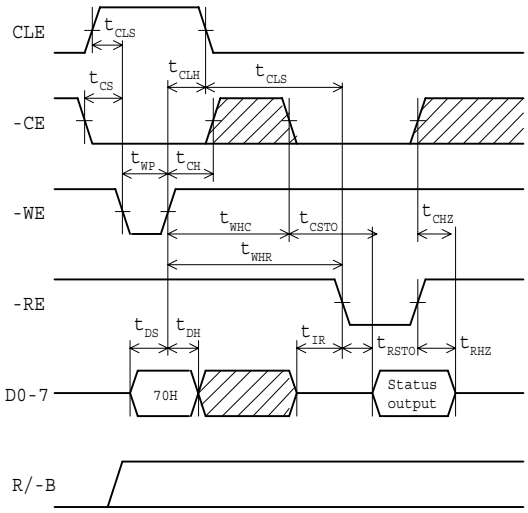



: $V_{IH}$ or $V_{IL}$

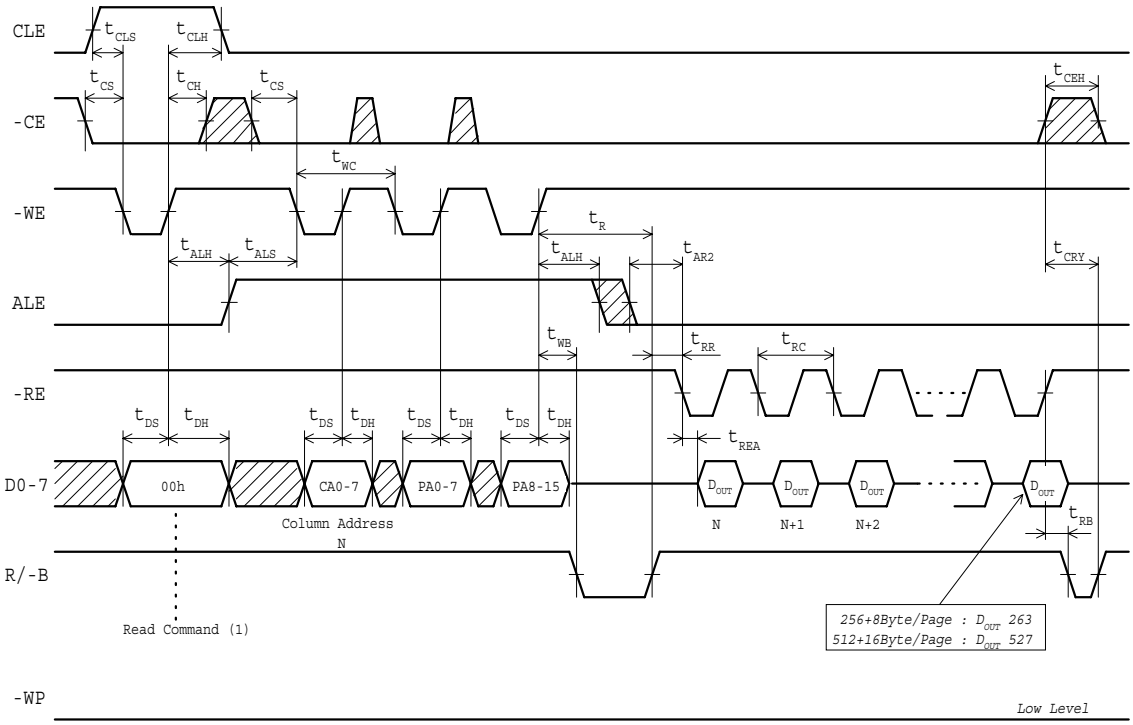
• **Serial Read Cycle**



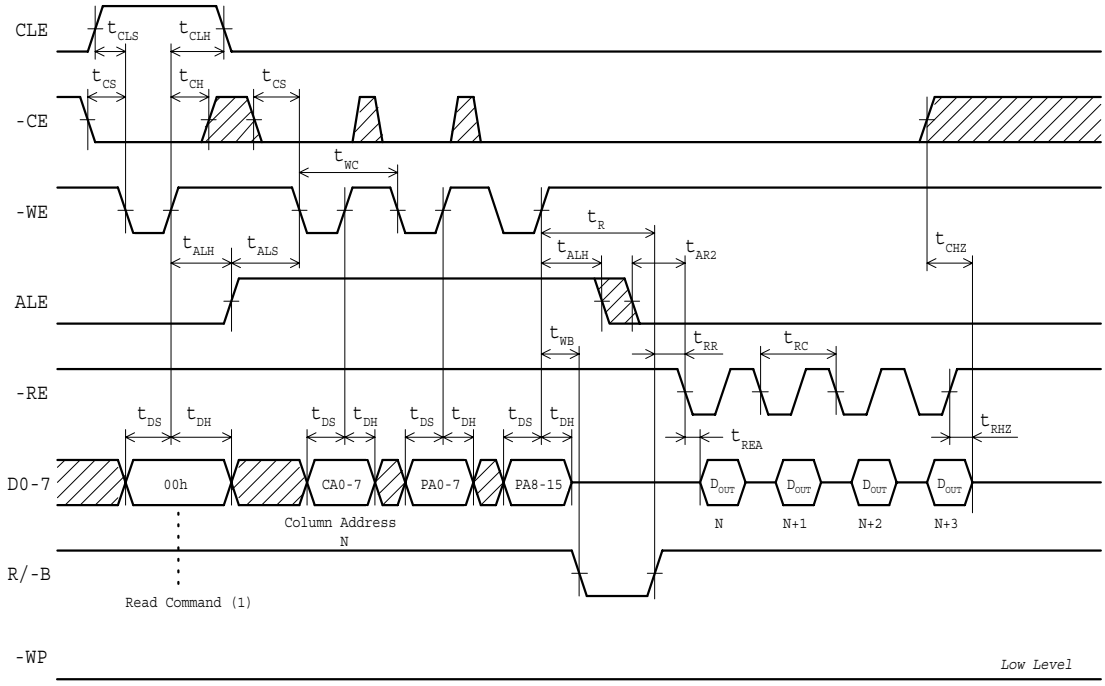

• **Status Read Cycle**



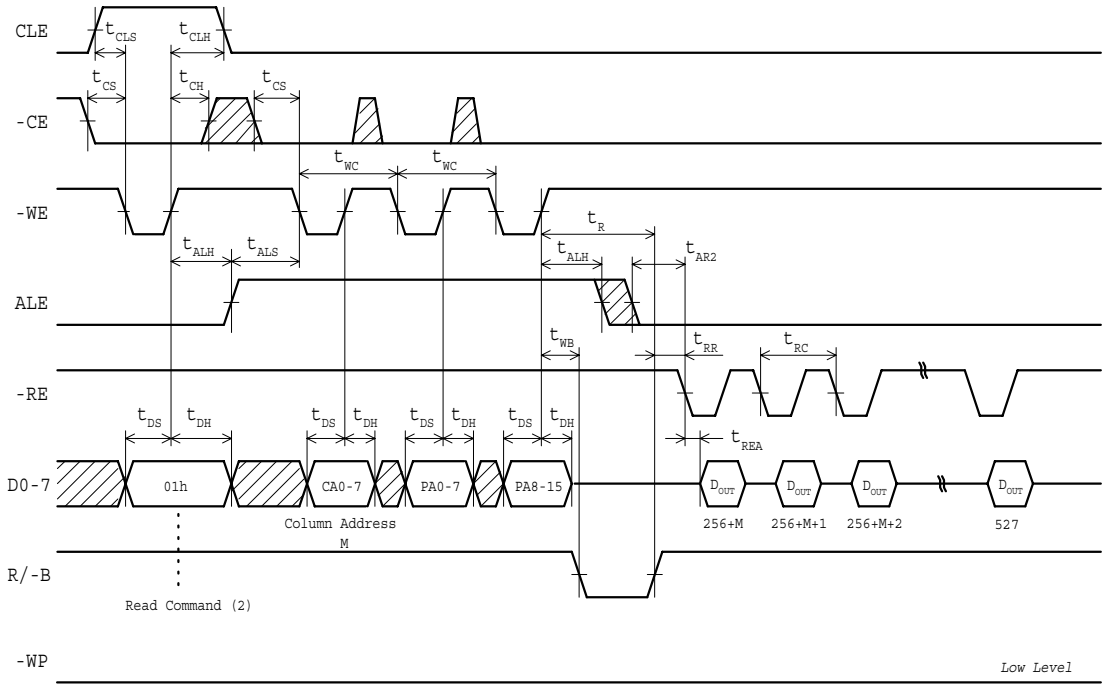

• **Read Cycle (1)**



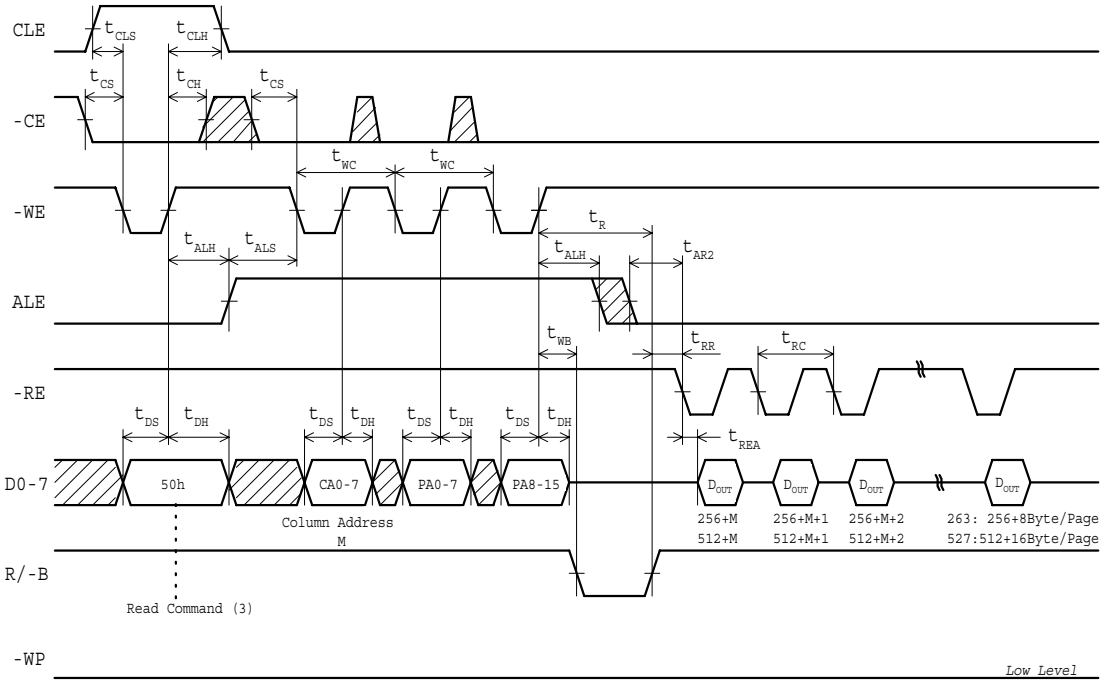
- **Read Cycle (1): when -CE is high during the cycle.**



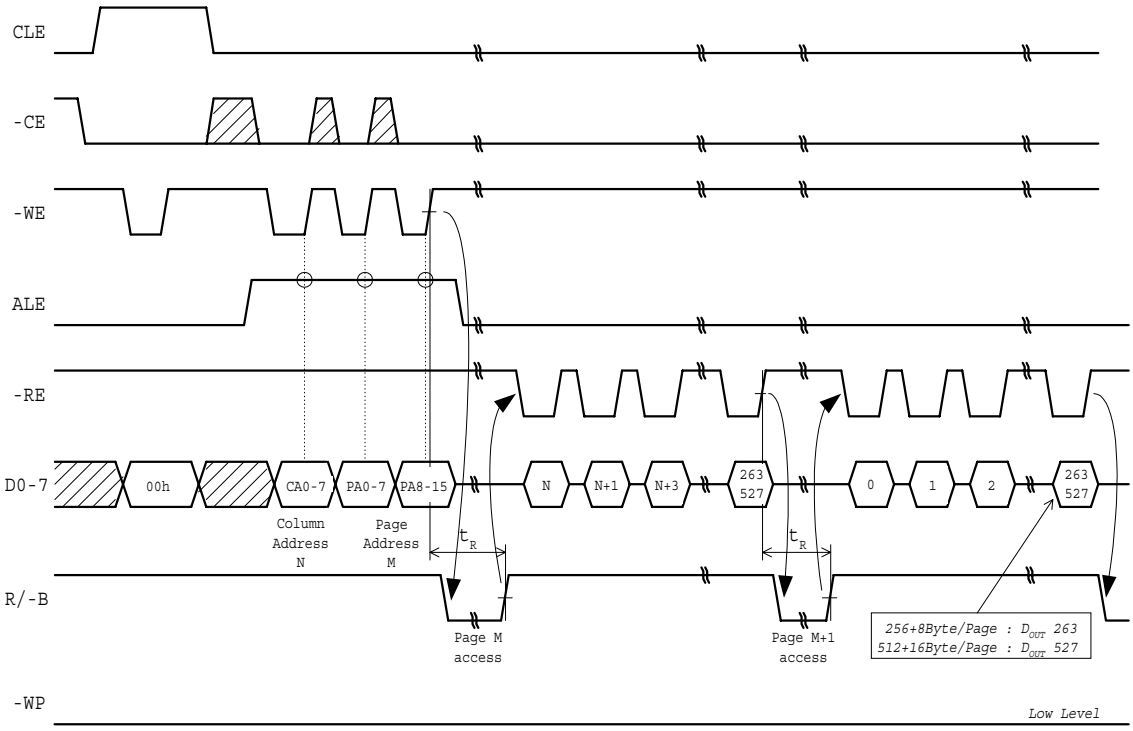

- **Read Cycle (2): (512 + 16 Byte/page models only)**



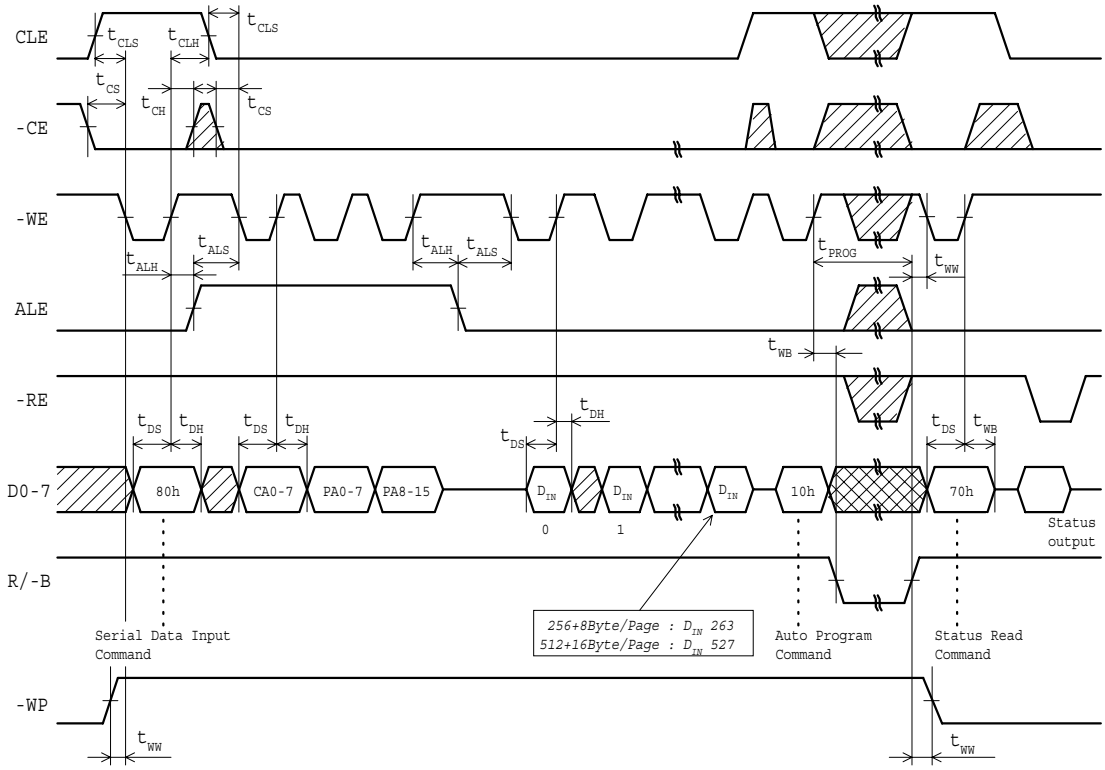
- **Read Cycle (3)**



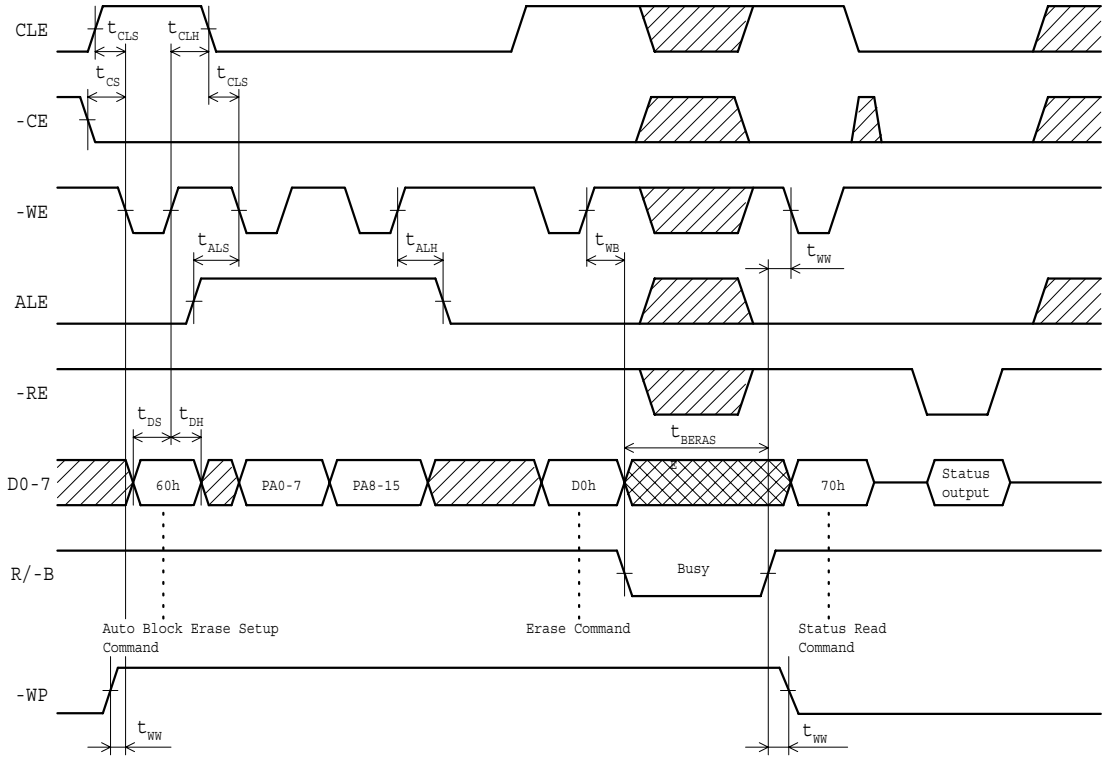

- **Sequential Read Timing**



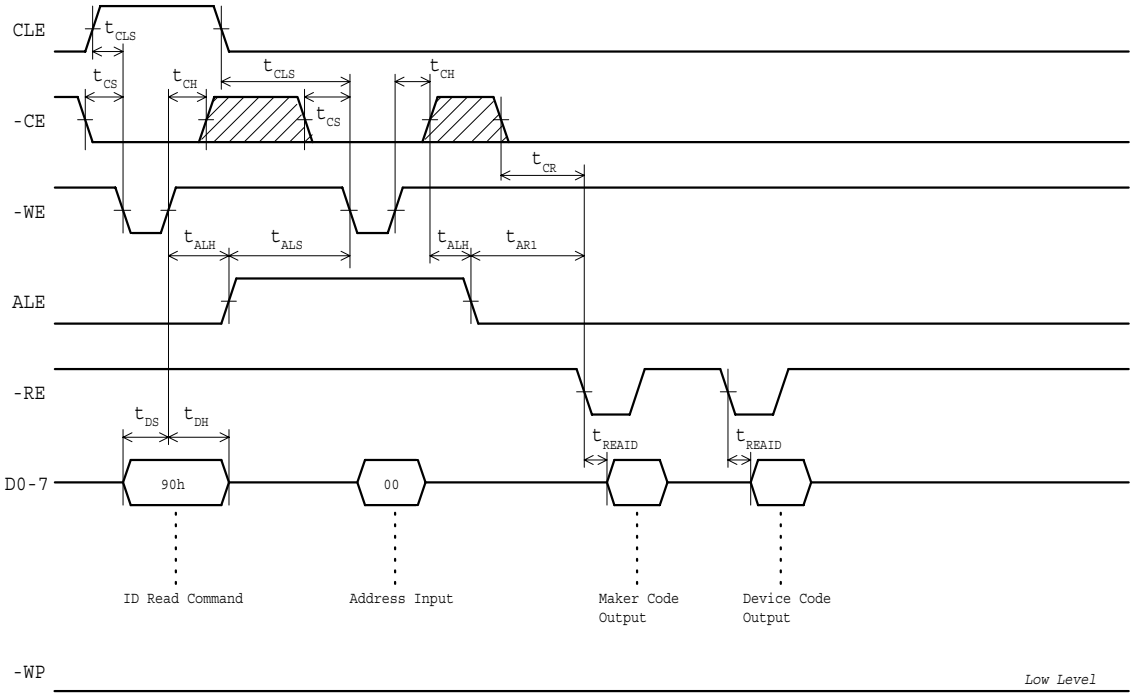
- **Auto Page Program Timing: (Flash Memories only)**



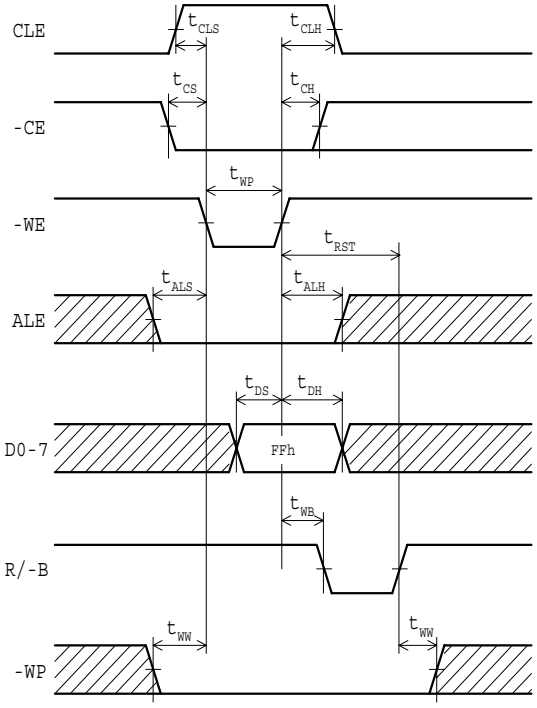

- **Auto Block Erase Timing: (Flash Memories only)**



- **ID Read Timing**




- **Reset Timing**



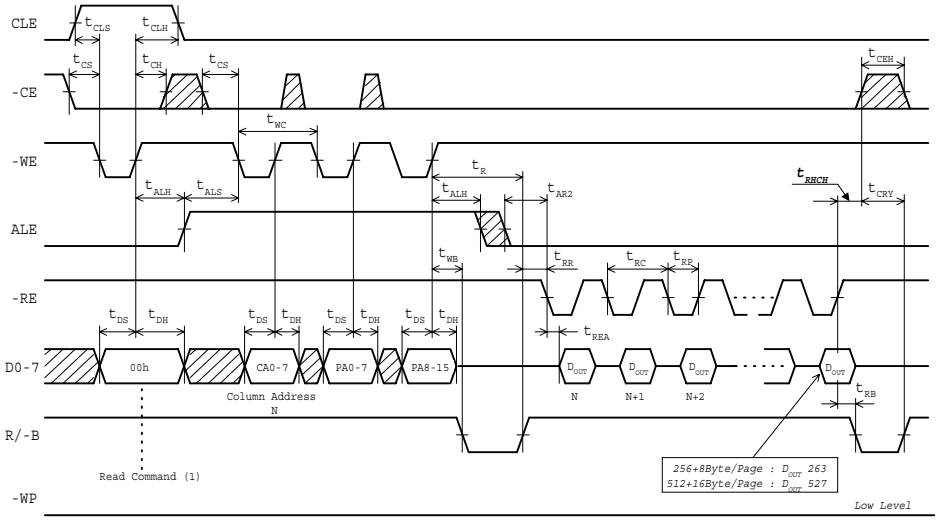
# 8. Device Operation and Precautions

## 8.1. Changing the timing when Data Read is executed

To release the Busy output after a Page Read is executed, set -CE to high for a certain length of time after accessing the final address of the page.

1. When -CE's delay (tRHCH) related to -RE is less than 30 ns, setting -CE to high for a certain time (tCEH) will enable the READY state to be maintained without outputting the Busy state.

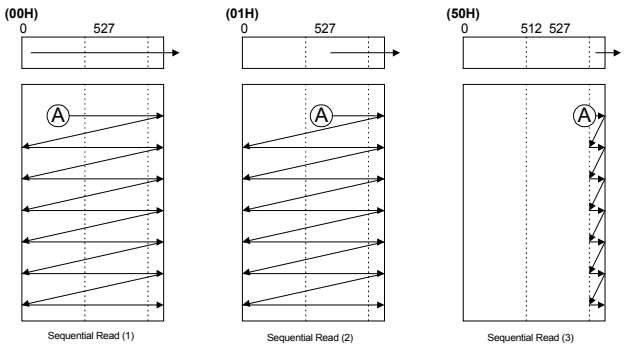
2. When -CE's delay (tRHCH) related to -RE is 30 ns or longer, keeping -CE high for a certain time (tCEH) will release the Busy output in tCRY after -CE is high.




## 8.2. Sequential Read

When a Data Read is executed, the initial address is specified at the start of the Data Read. Then, it is only necessary to input the -RE clock (without additional address input) in order to automatically increment the page address and continuously execute Read operation.

On the second page or later, all data in the main and redundant sections are output using Read commands (1) and (2). Only the redundant section is output using Read command (3). The sequential Read Mode can be used only within a single block.



## 8.3. Precautions when Programming Pages

1) Limit of the Write Operation to the Same Page

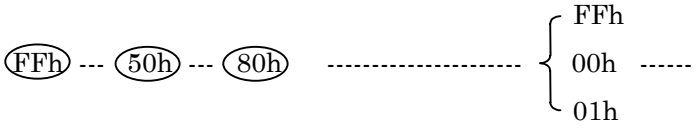
The data and redundant areas can only be written simultaneously once. If the system configuration requires it, writing to the redundant area may occur once more.

2) Writing to Pages within a Block

During the program operation, writing should be executed consecutively from a lower address page to an upper address page. Random page programming should be avoided.

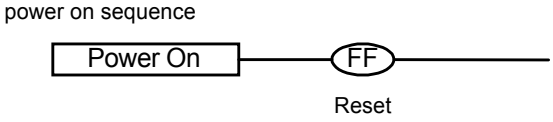
## 8.4. Precautions for writing in the redundant section only

Writing only to the redundant section requires the Reset command to be inputted and the Read command to be used to change data/pointer mode, as indicated in the following sequence. To program the data section after writing into the redundant section, the Reset command or Read commands (1) or (2) must be issued to reset the data pointer mode.




## 8.5. Resetting after power-on

After power-on, initialize the device using the following sequence.




## 8.6. Commands

(1) Command values other than those specified in the specifications cannot be inputted as a command.

(2) During the Busy state, inputting commands other than the Status Read command (70h) and Reset command (FFh) is not possible.

(3) After inputting the Serial Input command (80h), do not input command data other than the Program command (10) or Reset (FFh).

(4) Use the Ready/-Busy signal to determine the Busy state of the SmartMedia™.
The Status Read command is only available for abnormality judgement after the Erase command or Write command is issued. Execute the Status Read command after confirming that the state is Ready.