Date	Task	Who
9/28	Meet Up on teams	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
9/29-10/06	Worked on verilog code	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/07	Meeting on teams	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/09	Completed Multiplier	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/10	Completed Verilog code	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/11	Code ran successfuly on everybodies machine. Completed System Diagram and Every turn in part.	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/22	Teams meeting	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu

10/24	Teams meeting, Finite State Machine completed.	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/25	Fixed and Worked on the DFF, Gate logic code for all gates Xnor, Nand, NOT gate and all others.	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/28	Modified the DFF, Gate logic code for all gates Xnor, Nand, NOT gate and all others. System Diagram completed.	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/29	Made Accumulator and changed output. Also changed the code to better run for displaying the exact and correct output.	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/30	Fixed OutPuts and fixed spacing/display problems. Finished all other code.	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
10/31	Log completed, SystemDesign completed, Output completed.	Matthew Standeven, Rafael Raymos, Eric Cutherell, Evan McCauley, Jonas Salcedo, Paul Lupeituu
