```
C:\Users\Matthew\Desktop\Digital Logic>vvp a.out
InputA:    15:0000000000001111,InputB:   126:0000000001111110,ADD:0000,Result:   141:00000000000000000000000010001101,Error:00
InputA:    15:0000000000001111,InputB:   126:0000000001111110,SUB:0001,Result:65425:00000000000000001111111110010001,Error:01
InputA:    15:0000000000001111,InputB:   126:0000000001111110,MUL:0010,Result: 1890:00000000000000000000011101100010,Error:00
InputA:    15:0000000000001111,InputB:   126:0000000001111110,DIV:0011,Result:    0:00000000000000000000000000000000,Error:01
InputA:    15:0000000000001111,InputB:   126:0000000001111110,MOD:0100,Result:   15:00000000000000000000000000001111,Error:00
InputA:62463:1111001111111111,InputB:25726:0110010001111110,ADD:0000,Result:     22653:00000000000000000101100001111101,Error:01
InputA:62463:1111001111111111,InputB:25726:0110010001111110,SUB:0001,Result:     36737:00000000000000001000111110000001,Error:00
InputA:62463:1111001111111111,InputB:25726:0110010001111110,MUL:0010,Result:1606923138:01011111110001111011001110000010,Error:01
InputA:62463:1111001111111111,InputB:25726:0110010001111110,DIV:0011,Result:         2:00000000000000000000000000000010,Error:00
InputA:62463:1111001111111111,InputB:25726:0110010001111110,MOD:0100,Result     :11011:00000000000000000010101100000011,Error:01
project2code.txt:371: $finish called at 120 (1s)

C:\Users\Matthew\Desktop\Digital Logic>
```