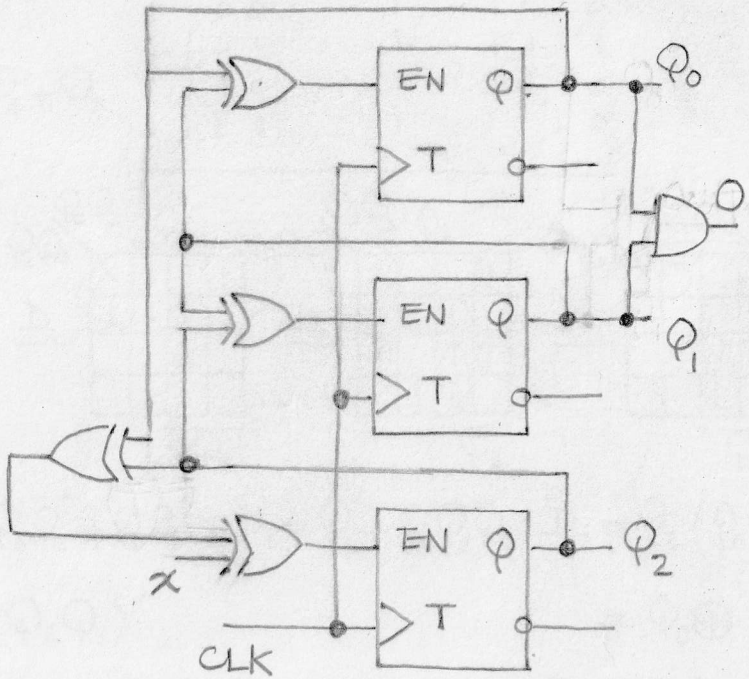
[3] [30 points]

A sequential system is described with the state table shown.

S	Input x=0	Input x=1	Output
A	A	E	0
B	E	A	0
C	B	F	0
D	F	B	1
E	C	G	0
F	G	C	0
G	D	H	0
H	H	D	1
	S*		

Design a synchronous state machine that implements the sequential system using Enabled T Flip-Flops. Rename the states using a three-bit binary code, so that **A** becomes 000, **B** becomes 001, etc.

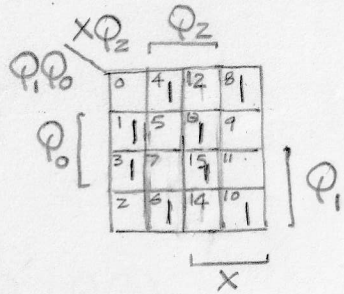
Bonus [10 points]
Implement the next-state logic (**NSL**) of the synchronous state machine using **ROM**s. Show the **ROM**s' logic diagrams and the tables of their addresses (inputs) and contents (data outputs).



S	X	Q_2 Q_1 Q_0	S^*	Q_2^* Q_1^* Q_0^*	EN_2	EN_1	EN_0
A	0	0 0 0	A	0 0 0	0	0	0
B	0	0 0 1	E	1 0 0	1	0	1
C	0	0 1 0	B	0 0 1	0	1	1
D	0	0 1 1	F	1 0 1	1	1	0
E	0	1 0 0	C	0 1 0	1	1	0
F	0	1 0 1	G	1 1 0	0	1	1
G	0	1 1 0	D	0 1 1	1	0	1
H	0	1 1 1	H	1 1 1	0	0	0
A	1	0 0 0	E	1 0 0	1	0	0
B	1	0 0 1	A	0 0 0	0	0	1
C	1	0 1 0	F	1 0 1	1	1	1
D	1	0 1 1	B	0 0 1	0	1	0
E	1	1 0 0	G	1 1 0	0	1	0
F	1	1 0 1	C	0 1 0	1	1	1
G	1	1 1 0	H	1 1 1	0	0	1
H	1	1 1 1	D	0 1 1	1	0	0

$EN_0 = Q_0 \oplus Q_1$

$EN_1 = Q_1 \oplus Q_2$



$EN_2 = x'(Q_0 \oplus Q_2) + x(Q_0 \oplus Q_2)'$

$= x \oplus Q_0 \oplus Q_2$