Himax

WiseEye™

DATA SHEET

(DOC No. HX6538-A-DS)

HX6538-A

WE2 AI Processor

Preliminary version 01 July 2023

Himax Technology, Inc.
http://www.himax.com.tw

Revision History

July 2023

Version	Date	Description of changes
01	2023/07/06	New setup.

List of Contents

July 2023

List of Contents

List of Figures

List of Tables

Important Notice

July 2023

Disclaimer

Himax reserves the right to modify this documentation without prior notice. The information appearing in this publication is believed to be accurate and reliable. However, Himax makes no warranty for any errors which may appear in this document. Contact Himax to obtain the latest version of product specifications before placing your order. No responsibility is assumed by Himax Group for any infringement of patent or other rights of third parties which may result from its use. Products described herein are intended for use in normal commercial applications. Please note that application circuits illustrated in this document are for reference purposed only.

All Rights Reserved

1. General Description

The HX6538-A is an extreme-low power, high performance microcontroller designed for battery powered Endpoint AI applications.

The HX6538-A embedded powerful dual ARM Cortex-M55 processors with Helium vector and floating-point extensions and an ARM Ethos-U55 microNPU core to accelerate convolution operation of neural network model. There are internal 2.5MB ultra-low-leakage SRAMs for system and program usage. With the benefit of Ethos-U55 microNPU and Helium vectored extended Cortex-M55 architecture, the HX6538-A provides maximum computing capability with the lowest power consumption and latency.

Besides traditional interrupt-based trigger wakeup mechanism from power-down or sleep mode, the HX6538-A provides a new multi-layer power management scheme to wakeup image sensor periodically for battery-powered applications. The multi-layer power management is controlled by hardware PMU state machine that support various trigger events for power state transition. The Cortex-M55 and Ethos-U55 cores are placed in 2nd power layer to save power consumption. Normally, Cortex-M55 and Ethos-U55 cores are in power shut-off state until 1st layer detection completed. There are hardware image accelerators in 1st layer to provide pre-processing of imaging tasks and provide a wake-up trigger when event is detected. Besides multi-layer power management, the HX6538-A also provides internal 0.8/0.9V Dynamic Voltage Frequency Scaling **(DVFS)** scheme to reduce dynamic power consumption. Both design schemes optimize power consumption and maintain required response time and accuracy in Endpoint AI applications.

Security is another key consideration for Internet of Things **(IoT)** or other embedded applications. In combing with hardware CryptoCell-312 crypto and Physical Unclonable Function **(PUF)** engines, the HX6538-A provides a complete system-level security solution including secure boot, secure OTA firmware update, and secure meta data output with minimum processing latency. A Physical Unclonable Function **(PUF)** hardware offers a unique identification **(UID)** or a hardware root of trust **(RoT)** for the establishment of a trusted foundation, from which all security operations need. PUF engine also provide high-quality TRNG number for crypto engine and security application usage. The HX6538-A also supports TrustZone security and TF-M software stack for application usage.

The HX6538-A provides rich peripheral interfaces for application need, including image MIPI CSI-2 transmitter and receiver, DVP and SDI interfaces, audio I^2S, PDM, interfaces, and peripheral interfaces of UART, I^2C, I^3C, SPI, GPIO, PWM, SD, SDIO and ADC.

2. Features

- ARM Cortex-M55 processor **(Big, high-performance core, version r1p1)**
  - Frequency up to 400MHz
  - Half/Single precision Floating Point Unit **(FPU)**
  - Helium vector processing extension for machine-learning
  - TrustZone security extension
  - 16KB of instruction cache, 16KB of data cache
  - 256KB of ITCM memory, 256KB of DTCM memory
  - Serial Wire Debug **(SWD)** with 8 breakpoints and 4 watch points
- ARM Cortex-M55 processor **(Little, high-efficiency core, version r1p1)**
  - Frequency up to 150MHz
  - Half/Single precision Floating Point Unit **(FPU)**
  - Helium vector processing extension for machine-learning
  - TrustZone security extension
  - 16KB of instruction cache, 16KB of data cache
  - Serial Wire Debug **(SWD)** with 8 breakpoints and 4 watch points
- ARM Ethos-U55 microNPU **(version r2p0)**
  - Frequency up to 400MHz
  - 64MACs/cycle
  - Support a variety of CNNs and RNNs network
  - Support weight compression
- Internal system memory
  - Configurable system memory, up to 2432KB
  - 64KB boot ROM
- External Flash
  - Support external 1 to 32MB QSPI Flash, up to 100MHz
  - Support Execute-In-Place **(XIP)** direct read mode
- Hardware accelerators
  - Motion detection
  - 2x2 sub-sampler and filter
  - 5x5 de-mosaic and filter
  - Image crop, sub-sampling, and binning
  - JPEG codec
  - Hardware-based voice active detector **(HWVAD)**
- Security
  - PUF based hardware Root-of-Trust **(RoT)**, and unique device ID
  - PUF based True Random Number Generator **(TRNG)**
  - CryptoCell-312 crypto engine
  - TrustZone security
  - Secure debug with certificated authentication
  - Secure boot, secure OTA, secure meta data output
- Image sensor interfaces
  - 2-lane MIPI CSI-2 RX, up to 1.8Gbps on each lane
  - 2-lane MIPI CSI-2 TX for image pass-through only, up to 1.8Gbps on each lane
  - Up to 1x DVP interface, 1/4/8-bit mode, up to 72MHz
  - Up to 1x SDI interface, 1-bit mode shared with DVP interface, up to 72MHz
- Audio interfaces
  - Up to 8-channel PDM RX
  - Up to 2-channel PDM TX for audio pass-through only
  - Up to 1x I^2S master or slave

- Peripheral interfaces
  - Up to 1x SPI master, up to 50MHz
  - Up to 1x SPI slave, up to 40MHz
  - Up to 2x I^2C master, up to 1MHz
  - Up to 2x I^2C slave, up to 1MHz
  - Up to 2x I^3C slave, support SDR and HDR-DDR, up to 12.5MHz
  - Up to 3x UARTs, 1 UART supports RS232/RS485 and IrDA
  - Up to 3x PWMs
  - Up to 37x GPIOs
- Memory card interface
  - Up to 1x SD and SDIO host, support DS mode, up to 25MHz
- ADC interface
  - Up to 4-channel
  - 1x 12-bit 1MSPS ADC
- Power management
  - Low power modes – active, sleep, power-down and deep-power-down
  - Hardware Power Management Unit **(PMU)**
  - Ultra-low leakage SRAMs with retention
  - Core 0.8/0.9V, up to 400MHz, Dynamic Voltage Frequency Scaling **(DVFS)**
  - On-chip high efficiency DC-DC for 0.8/0.9V core voltage generation
- Debug mode
  - Up to 1x Serial Wire Debug interface **(SWD)** with SRSTN
- Clock, reset and supply management
  - 1.8V supply for analog/mixed-signal blocks and SIF domain GPIOs
  - 1.8V or 3.3V supply for PIF and AON domain GPIOs
  - 24MHz crystal oscillator
  - 32.768KHz crystal oscillator
  - Internal 1/24/48/96MHz factory-trimmed RC oscillator
  - Internal 1/32.768KHz factory-trimmed RC oscillator
- Packages
  - LQFP128: 16.0mm x 16.0mm
    - HX6538-A04TLDG
    - HX6538-A07TLGG **(inc. 8MB HyperRAM)**
  - WLCSP65: 2.3mm x 5.6mm
  - QFN88: 8.0mm x 12.0mm
  - BGA64: 3.2mm x 7.0mm

3. Block Diagram

Figure 3.1 shows the functional modules in the HX6538-A.

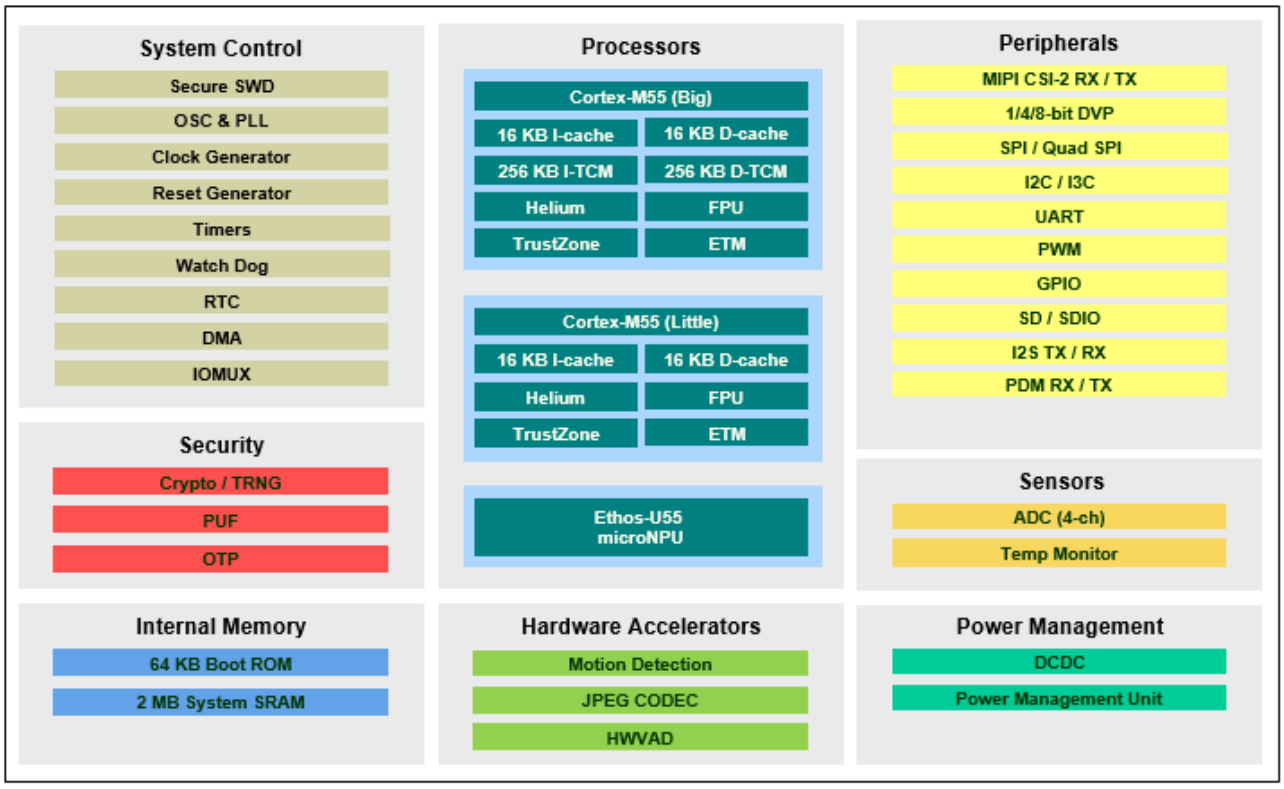


Figure 3.1: HX6538-A block diagram

4. Pin Assignment

4.1. LQFP128

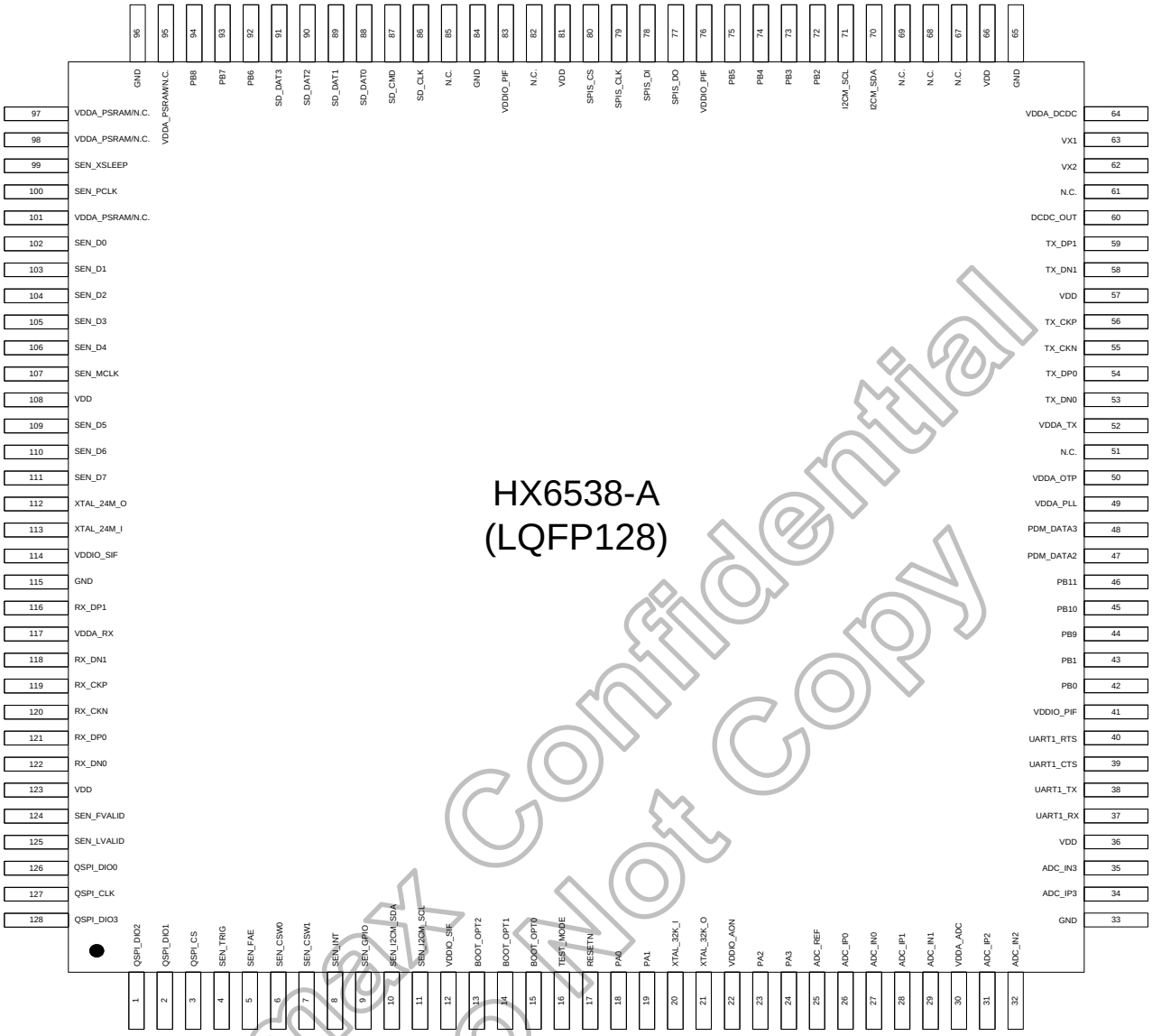


Figure 4.1: LQFP128 pin assignment (top view)

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground, **FS**=Fail-Safe
Reset States: **PH**=Pull High, **PL**=Pull Low
Pin Domains: **SIF**=1.8V only, **PIF**=1.8V or 3.3V, **AON**=1.8V or 3.3V **(always-on)**

Pin name	Pin no.	Type	Reset	Domain	Description
QSPI_DIO2	1	I/O, FS	O	SIF	QSPI data 2 for Flash.
QSPI_DIO1	2	I/O, FS	I, PL	SIF	QSPI data 1 for Flash.
QSPI_CS	3	O, FS	O	SIF	QSPI chip select for Flash.
SEN_TRIG	4	O, FS	O	SIF	Sensor trigger.
SEN_FAE	5	O, FS	O	SIF	Sensor frame auto exposure.
SEN_CSW0	6	O, FS	O	SIF	Sensor content switch0.
SEN_CSW1	7	O, FS	O	SIF	Sensor content switch1.
SEN_INT	8	I, FS	I; PL	SIF	Sensor interrupt.
SEN_GPIO	9	I/O, FS	O	SIF	Power down and reset control for image sensor.
SEN_I2CM_SDA	10	I/O, FS	I	SIF	I^2C master data for image sensor.
SEN_I2CM_SCL	11	I/O, FS	I	SIF	I^2C master clock for image sensor.
VDDIO_SIF	12,114	P	-	1.8V	I/O supply **(Image sensor GPIOs, SIF)**.
BOOT_OPT2	13	I	I; PL	AON	Boot option selection pin2.
BOOT_OPT1	14	I	I; PL	AON	Boot option selection pin1.
BOOT_OPT0	15	I	I; PL	AON	Boot option selection pin0.
TEST_MODE	16	I	I; PL	AON	Test mode.
RESETN	17	I, FS	I; PH	AON	Reset pin.
PA0 PA1	18 19	I/O, FS	I; PL	AON	General-purpose IO, group A.
XTAL_32K_I	20	I	I	AON	Crystal 32K.768Hz input.
XTAL_32K_O	21	O	O	AON	Crystal 32K.768Hz output.
VDDIO_AON	22	P	-	1.8/3.3V	I/O supply **(AON GPIOs)**.
PA2 PA3	23 24	I/O, FS	I; PH	AON	General-purpose IO, group A.
ADC_REF	25	AI	-	-	ADC reference voltage input.
ADC_IP0	26	AI	-	-	ADC input Ch0_P.
ADC_IN0	27	AI	-	-	ADC input Ch0_N.
ADC_IP1	28	AI	-	-	ADC input Ch1_P.
ADC_IN1	29	AI	-	-	ADC input Ch1_N.
VDDA_ADC	30	P	-	1.8/3.3V	Power supply **(ADC)**.
ADC_IP2	31	AI	-	-	ADC input Ch2_P.
ADC_IN2	32	AI	-	-	ADC input Ch2_N.
ADC_IP3	34	AI	-	-	ADC input Ch3_P.
GND	33,65 84,96 115	G	-	Ground	Ground.
ADC_IN3	35	AI	-	-	ADC input Ch3_N.
VDD	36,57 66,81 108,123	P	-	0.8/0.9V	Power supply from DC-DC output.
UART1_RX	37	I, FS	I; PL	PIF	UART1 RX pin.
UART1_TX	38	I/O, FS	I; PL	PIF	UART1 TX pin.
UART1_CTS	39	I, FS	I; PL	PIF	UART1 clear to send.
UART1_RTS	40	I/O, FS	I; PL	PIF	UART1 require to send.
VDDIO_PIF	41,76,83	P	-	1.8/3.3V	I/O supply **(peripheral GPIOs, PIF)**.
PB0 PB1 PB2 PB3	42 43 72 73	I/O, FS	I; PL	PIF	General-purpose IO, group B.

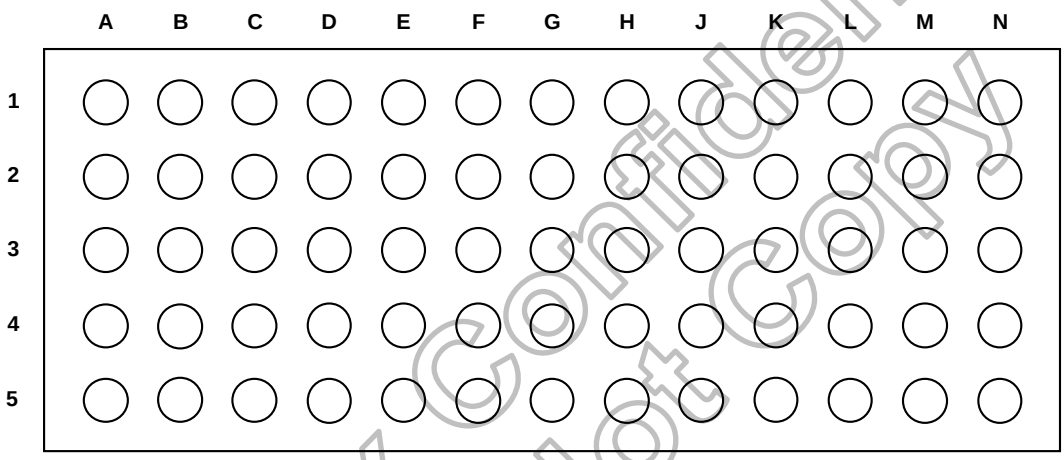
Pin name	Pin no.	Type	Reset	Domain	Description
PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11	74 75 92 93 94 44 45 46				
PDM_DATA2	47	I/O, FS	I; PL	PIF	PDM input data channel 2.
PDM_DATA3	48	I/O, FS	I; PL	PIF	PDM input data channel 3.
VDDA_PLL	49	P	-	1.8V	Power supply **(PLL)**.
VDDA_OTP	50	P	-	1.8V	Power supply **(OTP)**.
N.C.	51,61 67,68 69,82 85	-	-	-	No connection pin. It should be floating.
VDDA_TX	52	P	-	1.8V	Power supply **(MIPI TX)**.
TX_DN0	53	AO	-	-	MIPI TX data lane 0 negative output.
TX_DP0	54	AO	-	-	MIPI TX data lane 0 positive output.
TX_CKN	55	AO	-	-	MIPI TX clock negative output.
TX_CKP	56	AO	-	-	MIPI TX clock positive output.
TX_DN1	58	AO	-	-	MIPI TX data lane 1 negative output.
TX_DP1	59	AO	-	-	MIPI TX data lane 1 positive output.
DCDC_OUT	60	PO	-	-	DC-DC output **(0.8/0.9V)**.
VX2	62	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor output side.
VX1	63	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor input side.
VDDA_DCDC	64	P	-	1.8/3.3V	Power supply **(DC-DC)**.
I2CM_SDA	70	I/O, FS	I; PH	PIF	I²C master data.
I2CM_SCL	71	I/O, FS	I; PH	PIF	I²C master clock.
SPIS_DO	77	I/O, FS	I; PL	PIF	SPI slave data output.
SPIS_DI	78	I, FS	I; PL	PIF	SPI slave data input.
SPIS_CLK	79	I, FS	I; PL	PIF	SPI slave clock.
SPIS_CS	80	I, FS	I; PL	PIF	SPI slave chip select.
SD_CLK	86	I/O, FS	I; PL	PIF	SD/SDIO clock.
SD_CMD	87	I/O, FS	I; PL	PIF	SD/SDIO command.
SD_DAT0	88	I/O, FS	I; PL	PIF	SD/SDIO data 0.
SD_DAT1	89	I/O, FS	I; PL	PIF	SD/SDIO data 1.
SD_DAT2	90	I/O, FS	I; PL	PIF	SD/SDIO data 2.
SD_DAT3	91	I/O, FS	I; PL	PIF	SD/SDIO data 3.
VDDA_PSRAM/N.C.	95,97 98,101	P	-	1.8V	For HX6538-A07TLGG: Power supply **(HyperRAM)**. For HX6538-A04TLDG: No connection pin. It should be floating.
SEN_XSLEEP	99	O, FS	O	SIF	Sensor XSLEEP.
SEN_PCLK	100	I, FS	I	SIF	Sensor PCLK.
SEN_D0	102	I, FS	I	SIF	Sensor data Bit0.
SEN_D1	103	I, FS	I	SIF	Sensor data Bit1.
SEN_D2	104	I, FS	I	SIF	Sensor data Bit2.
SEN_D3	105	I, FS	I	SIF	Sensor data Bit3.
SEN_D4	106	I, FS	I	SIF	Sensor data Bit4.
SEN_MCLK	107	O, FS	O	SIF	Sensor MCLK.
SEN_D5	109	I, FS	I	SIF	Sensor data Bit5.
SEN_D6	110	I, FS	I	SIF	Sensor data Bit6.
SEN_D7	111	I, FS	I	SIF	Sensor data Bit7.
XTAL_24M_O	112	O	O	SIF	Crystal 24MHz output.
XTAL_24M_I	113	I	I	SIF	Crystal 24MHz input.

Pin name	Pin no.	Type	Reset	Domain	Description
RX_DP1	116	AI	-	-	MIPI RX data lane 1 positive input.
VDDA_RX	117	P	-	1.8V	Power supply **(MIPI RX)**.
RX_DN1	118	AI	-	-	MIPI RX data lane 1 negative input.
RX_CKP	119	AI	-	-	MIPI RX clock positive input.
RX_CKN	120	AI	-	-	MIPI RX clock negative input.
RX_DP0	121	AI	-	-	MIPI RX data lane 0 positive input.
RX_DN0	122	AI	-	-	MIPI RX data lane 0 negative input.
SEN_FVALID	124	I, FS	I	SIF	Sensor frame valid.
SEN_LVALID	125	I, FS	I	SIF	Sensor line valid.
QSPI_DIO0	126	I/O, FS	O	SIF	QSPI data 0 for Flash.
QSPI_CLK	127	O, FS	O	SIF	QSPI clock for Flash.
QSPI_DIO3	128	I/O, FS	O	SIF	QSPI data 3 for Flash.

Table 4.1: LQFP128 pin assignment

4.2. WLCSP65

	A	B	C	D	E	F	G	H	J	K	L	M	N	
1	QSPI_DIO2	QSPI_DIO0	RX_DP0	RX_DN1	RX_DP1	XTAL_24M_O	SEN_D1	SEN_D0	SEN_PCLK	SEN_XSLEEP	PB8	PB7	PB6	1
2	SEN_INT	QSPI_CS	QSPI_CLK	RX_DN0	RX_CKN	RX_CKP	XTAL_24M_I	SEN_MCLK	SEN_D3	SEN_D2	VDDIO_SIF	GND	VDDIO_PIF	2
3	SEN_I2CM_SCL	SEN_I2CM_SDA	SEN_GPIO	QSPI_DIO1	QSPI_DIO3	VDDIO_SIF	VDDA_RX	GND	PB11	TX_CKP	GND	PB3	PB5	3
4	PA2	PA3	PA1	PA0	TEST_MODE	BOOT_OPT	GND	TX_DN0	TX_CKN	TX_DP1	DCDC_OUT	GND	PB4	4
5	PB0	PB1	GND	VDDIO_AON	RESETN	PB9	PB10	VDDA_TX	TX_DP0	TX_DN1	VX1	VDDA_DCDC	PB2	5
	A	B	C	D	E	F	G	H	J	K	L	M	N	



Bottom View

Figure 4.2: WLCSP65 ball map

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground, **FS**=Fail-Safe
Reset States: **PH**=Pull High, **PL**=Pull Low
Pin Domains: **SIF**=1.8V only, **PIF**=1.8V or 3.3V, **AON**=1.8V or 3.3V **(always-on)**

Pin name	Pin no.	Type	Reset	Domain	Description
RX_DP1	E1	AI	-	-	MIPI RX data lane 1 positive input.
RX_DN1	D1	AI	-	-	MIPI RX data lane 1 negative input.
RX_DP0	C1	AI	-	-	MIPI RX data lane 0 positive input.
RX_DN0	D2	AI	-	-	MIPI RX data lane 0 negative input.
RX_CKP	F2	AI	-	-	MIPI RX clock positive input.
RX_CKN	E2	AI	-	-	MIPI RX clock negative input.
TX_DP1	K4	AO	-	-	MIPI TX data lane 1 positive output.
TX_DN1	K5	AO	-	-	MIPI TX data lane 1 negative output.
TX_DP0	J5	AO	-	-	MIPI TX data lane 0 positive output.
TX_DN0	H4	AO	-	-	MIPI TX data lane 0 negative output.
TX_CKP	K3	AO	-	-	MIPI TX clock positive output.
TX_CKN	J4	AO	-	-	MIPI TX clock negative output.
SEN_MCLK	H2	O, FS	O	SIF	Master clock output for image sensor.
SEN_PCLK	J1	I, FS	I	SIF	Pixel clock input from image sensor.
SEN_D0	H1	I, FS	I	SIF	Sensor data Bit0.
SEN_D1	G1	I, FS	I	SIF	Sensor data Bit1.
SEN_D2	K2	I, FS	I	SIF	Sensor data Bit2.
SEN_D3	J2	I, FS	I	SIF	Sensor data Bit3.
SEN_XSLEEP	K1	O, FS	O	SIF	Sensor XSLEEP.
SEN_INT	A2	I, FS	I; PL	SIF	Sensor interrupt.
SEN_GPIO	C3	I/O, FS	I	SIF	Power down and reset control for image sensor.
SEN_I2CM_SDA	B3	I/O, FS	I	SIF	I^2C master data for image sensor.
SEN_I2CM_SCL	A3	I/O, FS	I	SIF	I^2C master clock for image sensor.
PA0 PA1	D4 C4	I/O, FS	I; PL	AON	General-purpose IO, group A.
PA2 PA3	A4 B4	I/O, FS	I; PH	AON	General-purpose IO, group A.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11	A5 B5 N5 M3 N4 N3 N1 M1 L1 F5 G5 J3	I/O, FS	I; PL	PIF	General-purpose IO, group B.
XTAL_24M_O	F1	O	O	SIF	Crystal 24MHz output.
XTAL_24M_I	G2	I	I	SIF	Crystal 24MHz input.
BOOT_OPT	F4	I	I; PL	AON	Boot option selection pin.
TEST_MODE	E4	I	I; PL	AON	Test mode.
RESETN	E5	I, FS	I; PH	AON	Reset pin.
QSPI_CLK	C2	O, FS	O	SIF	QSPI clock for Flash.
QSPI_CS	B2	O, FS	O	SIF	QSPI chip select for Flash.
QSPI_DIO0	B1	I/O, FS	O	SIF	QSPI data 0 for Flash.
QSPI_DIO1	D3	I/O, FS	I, PL	SIF	QSPI data 1 for Flash.
QSPI_DIO2	A1	I/O, FS	O	SIF	QSPI data 2 for Flash.
QSPI_DIO3	E3	I/O, FS	O	SIF	QSPI data 3 for Flash.
VDDIO_SIF	F3, L2	P	-	1.8V	I/O supply **(Image sensor GPIOs, SIF)**.

Pin name	Pin no.	Type	Reset	Domain	Description
VDDIO_PIF	N2	P	-	1.8/3.3V	I/O supply **(Peripheral GPIOs, PIF)**.
VDDIO_AON	D5	P	-	1.8/3.3V	I/O supply **(AON GPIOs)**.
VDDA_DCDC	M5	P	-	1.8/3.3V	Power supply **(DC-DC)**.
VDDA_TX	H5	P	-	1.8V	Power supply **(MIPI TX, OTP and PLL)**.
VDDA_RX	G3	P	-	1.8V	Power supply **(MIPI RX)**.
VX1	L5	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor input side.
DCDC_OUT	L4	PO	-	-	DC-DC output **(0.8/0.9V)**. Connect to external inductor output side.
GND	C5, G4 H3, L3 M2, M4	G	-	Ground	Ground.

Table 4.2: WLCSP65 pin assignment

4.3. QFN88

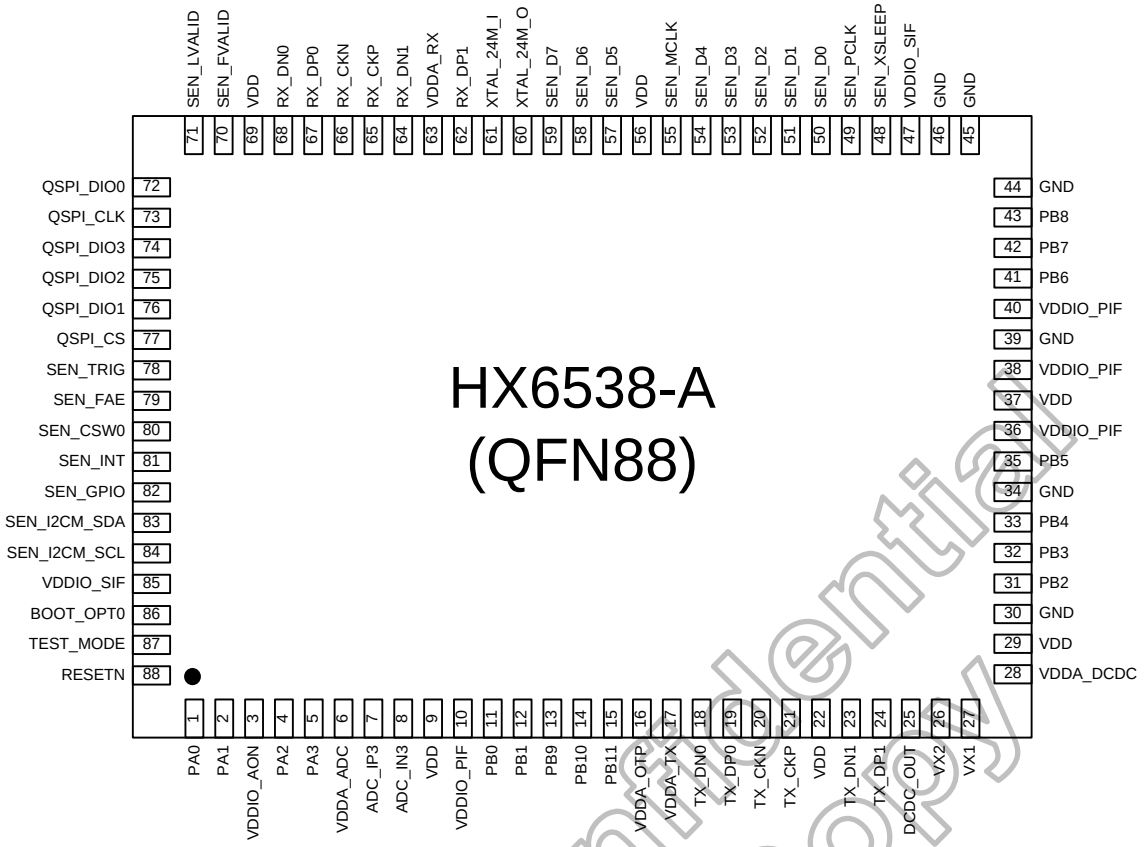


Figure 4.3: QFN88 pin assignment (top view)

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground, **FS**=Fail-Safe
Reset States: **PH**=Pull High, **PL**=Pull Low
Pin Domains: **SIF**=1.8V only, **PIF**=1.8V or 3.3V, **AON**=1.8V or 3.3V **(always-on)**

Pin name	Pin no.	Type	Reset	Domain	Description
PA0 PA1	1 2	I/O, FS	I; PL	AON	General-purpose IO, group A.
VDDIO_AON	3	P	-	1.8/3.3V	I/O supply **(AON GPIOs)**.
PA2 PA3	4 5	I/O, FS	I; PH	AON	General-purpose IO, group A.
VDDA_ADC	6	P	-	1.8/3.3V	Power supply **(ADC)**.
ADC_IP3	7	AI	-	-	ADC input Ch3_P.
ADC_IN3	8	AI	-	-	ADC input Ch3_N.
VDD	9,22 29,37 56,69	P	-	0.8/0.9V	Power supply from DC-DC output.
VDDIO_PIF	10,36 38,40	P	-	1.8/3.3V	I/O supply **(peripheral GPIOs, PIF)**.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11	11 12 31 32 33 35 41 42 43 13 14 15	I/O, FS	I; PL	PIF	General-purpose IO, group B.
VDDA_OTP	16	P	-	1.8V	Power supply **(OTP and PLL)**.
VDDA_TX	17	P	-	1.8V	Power supply **(MIPI TX)**.
TX_DN0	18	AO	-	-	MIPI TX data lane 0 negative output.
TX_DP0	19	AO	-	-	MIPI TX data lane 0 positive output.
TX_CKN	20	AO	-	-	MIPI TX clock negative output.
TX_CKP	21	AO	-	-	MIPI TX clock positive output.
TX_DN1	23	AO	-	-	MIPI TX data lane 1 negative output.
TX_DP1	24	AO	-	-	MIPI TX data lane 1 positive output.
DCDC_OUT	25	PO	-	-	DC-DC output **(0.8/0.9V)**.
VX2	26	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor output side.
VX1	27	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor input side.
VDDA_DCDC	28	P	-	1.8/3.3V	Power supply **(DC-DC)**.
GND	30,34 39,44 45,46	G	-	Ground	Ground.
VDDIO_SIF	47,85	P	-	1.8V	I/O supply **(Image sensor GPIOs, SIF)**.
SEN_XSLEEP	48	O, FS	O	SIF	Sensor XSLEEP.
SEN_PCLK	49	I, FS	I	SIF	Sensor PCLK.
SEN_D0	50	I, FS	I	SIF	Sensor data Bit0.
SEN_D1	51	I, FS	I	SIF	Sensor data Bit1.
SEN_D2	52	I, FS	I	SIF	Sensor data Bit2.
SEN_D3	53	I, FS	I	SIF	Sensor data Bit3.
SEN_D4	54	I, FS	I	SIF	Sensor data Bit4.
SEN_MCLK	55	O, FS	O	SIF	Sensor MCLK.
SEN_D5	57	I, FS	I	SIF	Sensor data Bit5.
SEN_D6	58	I, FS	I	SIF	Sensor data Bit6.

Pin name	Pin no.	Type	Reset	Domain	Description
SEN_D7	59	I, FS	I	SIF	Sensor data Bit7.
XTAL_24M_O	60	O	O	SIF	Crystal 24MHz output.
XTAL_24M_I	61	I	I	SIF	Crystal 24MHz input.
RX_DP1	62	AI	-	-	MIPI RX data lane 1 positive input.
VDDA_RX	63	P	-	1.8V	Power supply **(MIPI RX)**.
RX_DN1	64	AI	-	-	MIPI RX data lane 1 negative input.
RX_CKP	65	AI	-	-	MIPI RX clock positive input.
RX_CKN	66	AI	-	-	MIPI RX clock negative input.
RX_DP0	67	AI	-	-	MIPI RX data lane 0 positive input.
RX_DN0	68	AI	-	-	MIPI RX data lane 0 negative input.
SEN_FVALID	70	I, FS	I	SIF	Sensor frame valid.
SEN_LVALID	71	I, FS	I	SIF	Sensor line valid.
QSPI_DIO0	72	I/O, FS	O	SIF	QSPI data 0 for Flash.
QSPI_CLK	73	O, FS	O	SIF	QSPI clock for Flash.
QSPI_DIO3	74	I/O, FS	O	SIF	QSPI data 3 for Flash.
QSPI_DIO2	75	I/O, FS	O	SIF	QSPI data 2 for Flash.
QSPI_DIO1	76	I/O, FS	I, PL	SIF	QSPI data 1 for Flash.
QSPI_CS	77	O, FS	O	SIF	QSPI chip select for Flash.
SEN_TRIG	78	O, FS	O	SIF	Sensor trigger.
SEN_FAE	79	O, FS	O	SIF	Sensor frame auto exposure.
SEN_CSW0	80	O, FS	O	SIF	Sensor content switch0.
SEN_INT	81	I, FS	I; PL	SIF	Sensor interrupt.
SEN_GPIO	82	I/O, FS	I	SIF	Power down and reset control for image sensor.
SEN_I2CM_SDA	83	I/O, FS	I	SIF	I^2C master data for image sensor.
SEN_I2CM_SCL	84	I/O, FS	I	SIF	I^2C master clock for image sensor.
BOOT_OPT	86	I	I; PL	AON	Boot option selection pin.
TEST_MODE	87	I	I; PL	AON	Test mode.
RESETN	88	I, FS	I; PH	AON	Reset pin.

Table 4.3: QFN88 pin assignment

4.4. BGA64

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	QSPI_DIO3		QSPI_CLK		RX_DN0		RX_CKN		RX_DN1		VDDA_RX		XTAL_24M_O		SEN_MCLK		VDDIO_SIF		SEN_PCLK		PB8		A
B		QSPI_CS		QSPI_DIO0		RX_DP0		RX_CKP		RX_DP1		XTAL_24M_I		SEN_D3		SEN_D1		SEN_D0		SEN_XSLEEP		PB6	B
C	QSPI_DIO1																				PB7		C
D		QSPI_DIO2		SEN_I2CM_SCL				SEN_INT				GND				GND				GND_DCDC		PB2	D
E	VDDIO_AON		PA0		SEN_I2CM_SDA		SEN_GPIO		GND		PB10		GND		SEN_D2		PB5		PB4		PB3		E
F		PA1		RESETN		TEST_MODE		PB0		PB9		GND		TX_DN0		TX_CKN		TX_DN1		VDDA_DCDC		DCDC_OUT	F
G	PA3		PA2		VDDIO_PIF		BOOT_OPT		PB1		PB11		VDDA_TX		TX_DP0		TX_CKP		TX_DP1		VX1		G
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

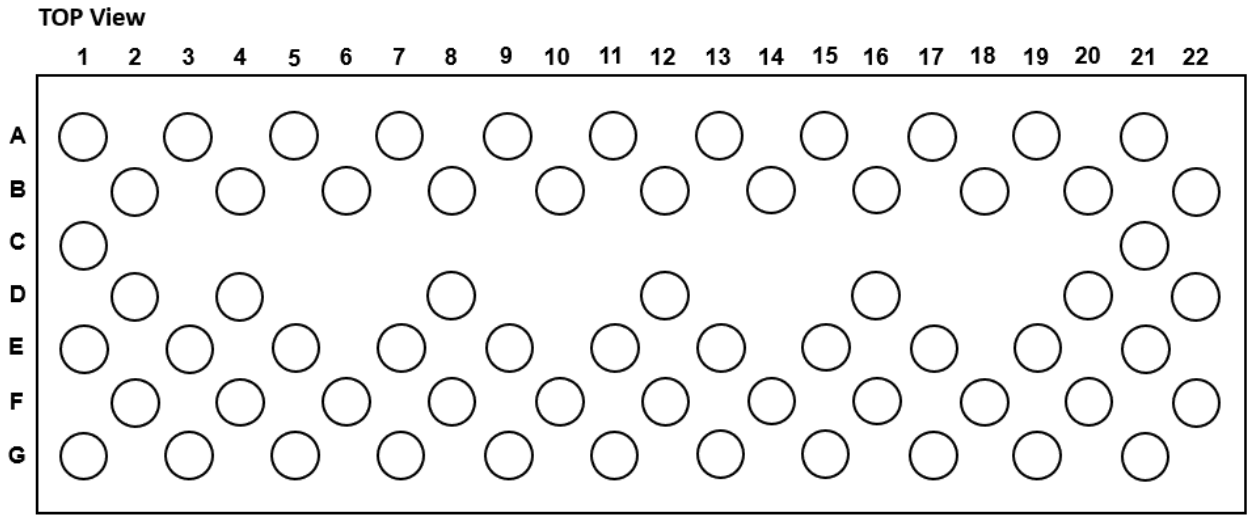


Figure 4.4: BGA64 ball map

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground, **FS**=Fail-Safe
Reset States: **PH**=Pull High, **PL**=Pull Low
Pin Domains: **SIF**=1.8V only, **PIF**=1.8V or 3.3V, **AON**=1.8V or 3.3V **(always-on)**

Pin name	Pin no.	Type	Reset	Domain	Description
RX_DP1	B10	AI	-	-	MIPI RX data lane 1 positive input.
RX_DN1	A9	AI	-	-	MIPI RX data lane 1 negative input.
RX_DP0	B6	AI	-	-	MIPI RX data lane 0 positive input.
RX_DN0	A5	AI	-	-	MIPI RX data lane 0 negative input.
RX_CKP	B8	AI	-	-	MIPI RX clock positive input.
RX_CKN	A7	AI	-	-	MIPI RX clock negative input.
TX_DP1	G19	AO	-	-	MIPI TX data lane 1 positive output.
TX_DN1	F18	AO	-	-	MIPI TX data lane 1 negative output.
TX_DP0	G15	AO	-	-	MIPI TX data lane 0 positive output.
TX_DN0	F14	AO	-	-	MIPI TX data lane 0 negative output.
TX_CKP	G17	AO	-	-	MIPI TX clock positive output.
TX_CKN	F16	AO	-	-	MIPI TX clock negative output.
SEN_MCLK	A15	O, FS	O	SIF	Master clock output for image sensor.
SEN_PCLK	A19	I, FS	I	SIF	Pixel clock input from image sensor.
SEN_D0	B18	I, FS	I	SIF	Sensor data Bit0.
SEN_D1	B16	I, FS	I	SIF	Sensor data Bit1.
SEN_D2	E15	I, FS	I	SIF	Sensor data Bit2.
SEN_D3	B14	I, FS	I	SIF	Sensor data Bit3.
SEN_XSLEEP	B20	O, FS	O	SIF	Sensor XSLEEP.
SEN_INT	D8	I, FS	I; PL	SIF	Sensor interrupt.
SEN_GPIO	E7	I/O, FS	I	SIF	Power down and reset control for image sensor.
SEN_I2CM_SDA	E5	I/O, FS	I	SIF	I²C master data for image sensor.
SEN_I2CM_SCL	D4	I/O, FS	I	SIF	I²C master clock for image sensor.
PA0 PA1	E3 F2	I/O, FS	I; PL	AON	General-purpose IO, group A.
PA2 PA3	G3 G1	I/O, FS	I; PH	AON	General-purpose IO, group A.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11	F8 G9 D22 E21 E19 E17 B22 C21 A21 F10 E11 G11	I/O, FS	I; PL	PIF	General-purpose IO, group B.
XTAL_24M_O	A13	O	O	SIF	Crystal 24MHz output.
XTAL_24M_I	B12	I	I	SIF	Crystal 24MHz input.
BOOT_OPT	G7	I	I; PL	AON	Boot option selection pin.
TEST_MODE	F6	I	I; PL	AON	Test mode.
RESETN	F4	I, FS	I; PH	AON	Reset pin.
QSPI_CLK	A3	O, FS	O	SIF	QSPI clock for Flash.
QSPI_CS	B2	O, FS	O	SIF	QSPI chip select for Flash.
QSPI_DIO0	B4	I/O, FS	O	SIF	QSPI data 0 for Flash.
QSPI_DIO1	C1	I/O, FS	I, PL	SIF	QSPI data 1 for Flash.
QSPI_DIO2	D2	I/O, FS	O	SIF	QSPI data 2 for Flash.
QSPI_DIO3	A1	I/O, FS	O	SIF	QSPI data 3 for Flash.
VDDIO_SIF	A17	P	-	1.8V	I/O supply **(Image sensor GPIOs, SIF)**.

Pin name	Pin no.	Type	Reset	Domain	Description
VDDIO_PIF	G5	P	-	1.8/3.3V	I/O supply **(Peripheral GPIOs, PIF)**.
VDDIO_AON	E1	P	-	1.8/3.3V	I/O supply **(AON GPIOs)**.
VDDA_DCDC	F20	P	-	1.8/3.3V	Power supply **(DC-DC)**.
VDDA_TX	G13	P	-	1.8V	Power supply **(MIPI TX, OTP and PLL)**.
VDDA_RX	A11	P	-	1.8V	Power supply **(MIPI RX)**.
VX1	G21	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor input side.
DCDC_OUT	F22	PO	-	-	DC-DC output **(0.8/0.9V)**. Connect to external inductor output side.
GND	E9,D12 F12,E13 D16	G	-	Ground	Ground.
GND_DCDC	D20	G	-	Ground	Ground of DC-DC

Table 4.4: BGA64 pin assignment

4.5. GPIO function selection

There is total 37 GPIOs that 16 GPIOs in AON and PIF domains and 21 GPIOs in SIF domain. Each individual GPIO pin can be connected to internal peripheral via pin-mux selection. Some internal peripheral connections appear in multiple GPIO pins for the flexibility of system application. The pin-mux selection is controlled by software register. Each GPIO pin selection has own register to control. For example, PB0 connects to UART0_RX, PB1 connects to UART0_TX, PB2 connects to I2CS1_SDA, PB3 connects to I2CS1_SCL, PB4 connects to GPIO, etc.

GPIO(1)	F1	F2	F3	F4	F5	F6	F7
PA0	GPIO(R)(2)	-	-	-	-	-	-
PA1	GPIO	VMUTE(R)(2)	-	-	-	-	-
PA2	GPIO	I2CS0_SCL(R)(2)	I3CS0_SCL	-	-	-	-
PA3	GPIO	I2CS0_SDA(R)(2)	I3CS0_SDA	-	-	-	-
PB0	GPIO	I2CS1_SDA	I3CS1_SDA	I2CM_SDA	SPIM_CLK	SPIS_CLK	UART0_RX
PB1	GPIO	I2CS1_SCL	I3CS1_SCL	I2CM_SCL	SPIM_CS	SPIS_CS	UART0_TX
PB2	GPIO	I2CS1_SDA	I3CS1_SDA	I2CM_SDA	SPIM_DO	SPIS_DO	UART1_RTS
PB3	GPIO	I2CS1_SCL	I3CS1_SCL	I2CM_SCL	SPIM_DI	SPIS_DI	UART1_CTS
PB4	GPIO	I2CS1_SDA	I3CS1_SDA	I2CM_SDA	SPIM_CLK	SPIS_CLK	UART1_RX
PB5	GPIO	I2CS1_SCL	I3CS1_SCL	I2CM_SCL	SPIM_CS	SPIS_CS	UART1_TX
PB6	GPIO	I2CS1_SDA	I3CS1_SDA	I2CM_SDA	SPIM_DI	SPIS_DI	UART1_RX
PB7	GPIO	I2CS1_SCL	-	I2CM_SCL	SPIM_DO	SPIS_DO	UART1_TX
PB8	GPIO	I2CS1_SDA	I3CS1_SDA	I2CM_SDA	SPIM_CLK	SPIS_CLK	UART1_CTS
PB9	GPIO	I2CS1_SCL	I3CS1_SCL	I2CM_SCL	-	-	UART2_RX
PB10	GPIO	I2CS1_SDA	I3CS1_SDA	I2CM_SDA	-	-	UART2_TX
PB11	GPIO	-	-	-	-	-	-
GPIO(1)	**F8**	**F9**	**F10**	**F11**	**F12**	**F13**	**F14**
PA0	-	-	-	-	-	-	-
PA1	-	-	-	-	-	-	-
PA2	-	-	-	-	-	-	-
PA3	-	-	-	-	-	-	-
PB0	SWCLK	SD_CMD	PWM0	-	-	-	-
PB1	SWDIO	SD_CLK	PWM1	-	-	-	-
PB2	SWDIO	SD_DAT1	PWM2	PDM_DATA2	I2SM_SDO	I2SS_SDO	PT_PDM_CLKI
PB3	SRSTN	SD_DAT0	PWM0	PDM_DATA1	I2SM_SDI	I2SS_SDI	PT_PDM_DATAO
PB4	SWCLK	SD_DAT2	PWM1	PDM_CLK	I2SM_SCLK	I2SS_SCLK	-
PB5	SWDIO	SD_DAT3	PWM2	PDM_DATA0	I2SM_WS	I2SS_WS	-
PB6	SRSTN	SD_CMD	PWM0	PDM_DATA3	-	-	-
PB7	SWCLK(R)(2)	SD_CLK	PWM1	-	-	-	-
PB8	SWDIO(R)(2)	-	PWM2	-	-	-	-
PB9	SWCLK	-	-	PDM_CLK	I2SM_SCLK	I2SS_SCLK	-
PB10	SWDIO	-	-	PDM_DATA0	I2SM_WS	I2SS_WS	-
PB11	SRSTN	-	-	PDM_DATA1	I2SM_SDI	I2SS_SDI	-

Note: (1) All packages support PA[3:0], PB[11:0] of AON/PIF domain GPIOs.
(2) (R) is GPIO function after reset.

Table 4.5: AON and PIF domains GPIO functions select

GPIO	F1	F2	F3	Package(2)
SEN_INT	SEN_INT (R)(1)	GPIO	SEN_FVALID	a, b, c, d
SEN_GPIO	SEN_GPIO (R)(1)	-	SEN_LVALID	a, b, c, d
SEN_I2CM_SDA	SEN_I2CM_SDA (R)(1)	GPIO	-	a, b, c, d
SEN_I2CM_SCL	SEN_I2CM_SCL (R)(1)	GPIO	-	a, b, c, d
SEN_XSLEEP	SEN_XSLEEP (R)(1)	GPIO	SEN_TRIG	a, b, c, d
SEN_D0	SEN_D0 (R)(1)	GPIO	-	a, b, c, d
SEN_D1	SEN_D1 (R)(1)	GPIO	-	a, b, c, d
SEN_D2	SEN_D2 (R)(1)	GPIO	-	a, b, c, d
SEN_D3	SEN_D3 (R)(1)	GPIO	-	a, b, c, d
SEN_PCLK	SEN_PCLK (R)(1)	GPIO	-	a, b, c, d
SEN_MCLK	SEN_MCLK (R)(1)	GPIO	SEN_XSLEEP	a, b, c, d
SEN_D4	SEN_D4 (R)(1)	GPIO	-	a, c
SEN_D5	SEN_D5 (R)(1)	GPIO	-	a, c
SEN_D6	SEN_D6 (R)(1)	GPIO	-	a, c
SEN_D7	SEN_D7 (R)(1)	GPIO	-	a, c
SEN_TRIG	SEN_TRIG (R)(1)	GPIO	-	a, c
SEN_FAE	SEN_FAE (R)(1)	GPIO	-	a, c
SEN_CSW0	SEN_CSW0 (R)(1)	GPIO	-	a, c
SEN_CSW1	SEN_CSW1 (R)(1)	GPIO	-	a, c
SEN_FVALID	SEN_FVALID (R (1)	GPIO	-	a, c
SEN_LVALID	SEN_LVALID (R)(1)	GPIO	-	a, c

Note: (1) (R) is GPIO function after reset.
(2) Package types of SIF domain GPIOs.
a. LQFP128
b. WLCSP65
c. QFN88
d. BGA64

Table 4.6: SIF domain GPIO functions select

5. Function Description

5.1. Memory mapping

All memory and registers are found in the same address space. The system memory includes two blocks of 1MB AXI SRAMs, one block of 384KB AHB SRAM. The Big Cortex-M55 core embedded 256KB ITCM and 256KB DTCM providing single-cycle access from processor. All AXI SRAMs, AHB SRAMs and TCM memory can be configurable during system initialization stage and power down unuse memory space to save power consumption.

Flash memory supports READ execute in place **(XIP)** mode that allows Cortex-M55 processor to execute program code directly from Flash memory via Quad Serial Peripheral Interface **(QSPI)**. Ethous-U55 also support to use XIP mode to read compressed Neuro Network (NN) weight data from Flash memory to extend executable NN model size.

The HX6538-A supports Arm TrustZone technologies. The system memory is partitioned into two regions, one is Secure memory, and another is Non-secure memory. Both Secure and Non-secure memory map are listed in the table below.

System memory map

Start address	End address	Size (MB)	Description
E0000000	FFFFFFFF	512	Cortex-M55 PPB.
57000000	DFFFFFFF	-	Reserved.
52000000	56FFFFFF	80	APB peripherals **(Secure)**.
50000000	51FFFFFF	32	AHB peripherals **(Secure)**.
47000000	4FFFFFFF	-	Reserved.
42000000	46FFFFFF	80	APB peripherals **(Non-secure)**.
40000000	41FFFFFF	32	AHB peripherals **(Non-secure)**.
3C000000	3FFFFFFF	-	Reserved.
3A000000	3BFFFFFF	32	Flash **(Secure)**.
36060000	39FFFFFF	-	Reserved.
36000000	3605FFFF	0.375	SRAM #2 **(Secure)**.
34200000	35FFFFFF	-	Reserved.
34100000	341FFFFF	1	SRAM #1 **(Secure)**.
34000000	340FFFFF	1	SRAM #0 **(Secure)**.
30040000	33FFFFFF	-	Reserved.
30000000	3003FFFF	0.25	DTCM **(Secure)**.
2C000000	2FFFFFFF	-	Reserved.
2A000000	2BFFFFFF	32	Flash **(Non-secure)**.
26060000	29FFFFFF	-	Reserved.
26000000	2605FFFF	0.375	SRAM #2 **(Non-secure)**.
24200000	25FFFFFF	-	Reserved.
24100000	241FFFFF	1	SRAM #1 **(Non-secure)**.
24000000	240FFFFF	1	SRAM #0 **(Non-secure)**.
20040000	23FFFFFF	-	Reserved.
20000000	2003FFFF	0.25	DTCM **(Non-secure)**.
10040000	1FFFFFFF	-	Reserved.
10000000	1003FFFF	0.25	ITCM **(Secure)**.
00040000	FFFFFFF	-	Reserved.
00000000	0003FFFF	0.25	ITCM **(Non-secure)**.

Table 5.1: System memory map

AHB peripherals (Non-secure)

Start address	End address	Size (MB)	Description
41820000	41FFFFFF	-	Reserved.
41810000	4181FFFF	-	DMA 3.
41800000	4180FFFF	-	DMA 2.
41020000	417FFFFF	-	Reserved.
41010000	4101FFFF	-	Flash controller.
41000000	4100FFFF	-	DMA 1.
40820000	40FFFFFF	-	Reserved.
40810000	4081FFFF	-	SPI slave.
40800000	4080FFFF	-	SPI master.
40010000	407FFFFF	-	Reserved.
40000000	4000FFFF	-	DMA 0.

Table 5.2: AHB peripherals (Non-secure) memory map

AHB peripherals (Secure)

Start address	End address	Size (MB)	Description
51820000	51FFFFFF	-	Reserved.
51810000	5181FFFF	-	DMA 3.
51800000	5180FFFF	-	DMA 2.
51020000	517FFFFF	-	Reserved.
51010000	5101FFFF	-	Flash controller.
51000000	5100FFFF	-	DMA 1.
50820000	50FFFFFF	-	Reserved.
50810000	5081FFFF	-	SPI slave.
50800000	5080FFFF	-	SPI master.
50010000	507FFFFF	-	Reserved.
50000000	5000FFFF	-	DMA 0.

Table 5.3: AHB peripherals (Secure) memory map

APB peripherals (Non-secure)

Start address	End address	Size (MB)	Description
46004000	46FFFFFF	-	Reserved.
46003000	46003FFF	-	GPIO **(AON domain)**.
46002000	46002FFF	-	GPIO **(AON domain)**.
46001000	46001FFF	-	PMU.
45010000	46000FFF	-	Reserved.
4500A000	4500FFFF	-	Timer.
45007000	45009FFF	-	RTC.
45006000	45006FFF	-	Reserved.
45005000	45005FFF	-	Sensor control.
45004000	45004FFF	-	Image data path.
45002000	45003FFF	-	Reserved.
45000000	45001FFF	-	WDT.
44010000	44FFFFFF	-	Reserved.
4400F000	4400FFFF	-	PDM.
4400E000	4400EFFF	-	I^2C slave 1.
4400D000	4400DFFF	-	I^3C slave 0.
4400C000	4400CFFF	-	Reserved.
4400B000	4400BFFF	-	I^2S slave.
4400A000	4400AFFF	-	Mailbox.
44006000	44009FFF	-	GPIO.
44005000	44005FFF	-	Reserved.
44004000	44004FFF	-	UART 2.
44003000	44003FFF	-	UART 0.
44002000	44002FFF	-	I^2S master.
44001000	44001FFF	-	I^2C master.
44000000	44000FFF	-	I^2C slave 0.
43110000	43FFFFFF	-	Reserved.
430F8000	4310FFFF	-	MIPI RX.
43070000	430F7FFF	-	Reserved.
43060000	4306FFFF	-	MIPI TX.
43050000	4305FFFF	-	Reserved.
43030000	4304FFFF	-	CryptoCell-312 crypto.
43020000	4302FFFF	-	Ethos-U55.
43010000	4301FFFF	-	Reserved.
43000000	4300FFFF	-	SD and SDIO host.
4200D000	42FFFFFF	-	Reserved.
4200C000	4200CFFF	-	ADC.
4200A000	4200BFFF	-	Reserved.
42009000	42009FFF	-	VAD.
42005000	42008FFF	-	Reserved.
42004000	42004FFF	-	I^2C master **(for camera)**.
42003000	42003FFF	-	PWM.
42002000	42002FFF	-	I^3C slave 1.
42001000	42001FFF	-	Reserved.
42000000	42000FFF	-	UART 1.

Table 5.4: APB peripherals (Non-secure) memory map

APB peripherals (Secure)

Start address	End address	Size (MB)	Description
56004000	56FFFFFF	-	Reserved.
56003000	56003FFF	-	GPIO **(AON domain)**.
56002000	56002FFF	-	GPIO **(AON domain)**.
56001000	56001FFF	-	PMU.
55010000	56000FFF	-	Reserved.
5500A000	5500FFFF	-	Timer.
55007000	55009FFF	-	RTC.
55006000	55006FFF	-	Reserved.
55005000	55005FFF	-	Sensor control.
55004000	55004FFF	-	Image data path.
55002000	55003FFF	-	Reserved.
55000000	55001FFF	-	WDT.
54010000	54FFFFFF	-	Reserved.
5400F000	5400FFFF	-	PDM.
5400E000	5400EFFF	-	I^2C slave 1.
5400D000	5400DFFF	-	I3C slave 0.
5400C000	5400CFFF	-	Reserved.
5400B000	5400BFFF	-	I^2S slave.
5400A000	5400AFFF	-	Mailbox.
54006000	54009FFF	-	GPIO.
54005000	54005FFF	-	Reserved.
54004000	54004FFF	-	UART 2.
54003000	54003FFF	-	UART 0.
54002000	54002FFF	-	I^2S master.
54001000	54001FFF	-	I^2C master.
54000000	54000FFF	-	I^2C slave 0.
53110000	53FFFFFF	-	Reserved.
530F8000	5310FFFF	-	MIPI RX.
53070000	530F7FFF	-	Reserved.
53060000	5306FFFF	-	MIPI TX.
53050000	5305FFFF	-	Reserved.
53030000	5304FFFF	-	CryptoCell-312 crypto.
53020000	5302FFFF	-	Ethos-U55.
53010000	5301FFFF	-	Reserved.
53000000	5300FFFF	-	SD and SDIO host.
5200D000	52FFFFFF	-	Reserved.
5200C000	5200CFFF	-	ADC.
5200A000	5200BFFF	-	Reserved.
52009000	52009FFF	-	VAD.
52005000	52008FFF	-	Reserved.
52004000	52004FFF	-	I^2C master **(for camera)**.
52003000	52003FFF	-	PWM.
52002000	52002FFF	-	I3C slave 1.
52001000	52001FFF	-	Reserved.
52000000	52000FFF	-	UART 1.

Table 5.5: APB peripherals (Secure) memory map

5.2. Power and clock management

Features

- Hardware power management Unit **(PMU)**
- Power modes – active, sleep, power-down, deep-power-down modes
- Clock sources – RC oscillators, crystal oscillators, PLL

Function description

The HX6538-A supports a variety of power control features to achieve the best compromise between low-power consumption, short startup time and available wakeup sources.

The Power Management Unit **(PMU)** is a hardware state machine that controls the HX6538-A internal power domain switches on/off for power modes transitions. PMU supports various wake-up sources including external interrupts or internal timers interrupt for periodic wake-up in “always-on” applications.

Active mode

There are two active modes, dual-core active and signal core active modes. Internal DC-DC is set to ON mode in both active modes.

In dual-core active mode, the dual Cortex-M55 processors, and all peripherals are powered up, clocks are active. Processors can execute instructions to access selected peripherals for applications.
In single-core active mode, only Little Cortex-M55 processor is active. Big Cortex-M55 processor and Ethos-U55 microNPU are power shut off. Some peripherals are power shut off as well.

Sleep mode

This is an Arm-defined power mode. In sleep mode, internal DC-DC is set to ON mode and the Cortex-M55 processor is powered up, but internal processor clock is gated, and processor is idled. Once wakeup event happens, the gated clock will be released immediately. Processor back to normal and begin instruction execution process. For further information, see the *Arm Cortex-M55 Processor Devices Generic User Guide*.

Power-Down mode

In power-down mode, internal DC-DC is set to LIGHT LOADING mode and dual Cortex-M55 processors and Ethos-U55 microNPU are powered off, but Big Cortex-M55 processor TCM memories and system memories can be programmed in power retention state to retain software code and data. When an event triggers wake-up, PMU will transit power mode to active mode. The startup time is short because all instruction and data is kept in retention memory in power-down mode. There is no re-load programming and re-booting latency required.

Deep-Power-Down mode

In deep-power-down mode, internal DC-DC is set to OFF mode and the main core power is removed except PMU block. When an event triggers wake-up, PMU will transit power mode to active mode. Cortex-M55 processor will re-load program from external Flash memory and re-booting before execute instruction. PMU can be programmed to disable unused external power sources via GPIO output in this mode.

Clock sources

The HX6538-A supports three RC oscillators **(RCOSC)**, two crystal oscillators and one PLL.

- RC oscillators
  The 24MHz RCOSC provides the default clock at reset and provides a clean system clock after the power supply reach operating voltage.
  - Selectable 24MHz or 1MHz RCOSC oscillator, factory trimmed for accuracy, that can be optionally used for a system clock as well as other purposes. This RCOSC can be enabled or disabled by software. The default is enabled and select 24MHz.
  - Selectable 96MHz or 48MHz RCOSC oscillator, factory trimmed for accuracy, that can be optionally used for a system clock as well as other purposes. This RCOSC can be enabled or disabled by software. The default is enabled and select 96MHz.
  - Selectable 32.768KHz or 1KHz RCOSC oscillator, factory trimmed for accuracy, that can be optionally used for a system clock as well as other purposes. This RCOSC can be enabled or disabled by software. The default is enabled and select 32.768KHz.

- Crystal oscillators
  There are two independent oscillators for 32.768KHz and 24MHz that can be optionally used for a system clock as well as other purposes. Following reset, the HX6538-A will operate from the internal 24MHz FRO until switched by software. This allows system to operate without any external crystal and the boot loader code to operate at a known frequency. These two crystal oscillators can be enabled or disabled by software. The default two oscillators are enabled.

- PLL
  The input sources of PLL are from FROs or crystal oscillator. PLL accepts an input clock frequency in the range of 10MHz to 36MHz. The PLL output frequency in the range of 40MHz to 400MHz that can be optionally used for a system clock as well as other purposes. These PLL can be enabled or disabled by software. The default PLL is disabled.

5.3. Cortex-M55 processor

The Cortex-M55 processor implements the Armv8.1‑M Mainline architecture and also supports previous Armv8‑M architectural features. For more information on Armv8‑M and Armv8.1‑M features and variants information, see the *Armv8‑M variants section in the Armv8-M Architecture Reference Manual*.

Cortex-M55 processor core

The Cortex-M55 processor core has an Instruction Fetch Unit **(IFU)** that is closely coupled with the Data Processing Unit **(DPU)**.

The DPU contains the logic to:
- Decode and execute scalar integer instructions
- Handle the register transfer operations required for exception entry and exit

Extension processing unit

The Extension Processing Unit **(EPU)** includes support for all the instructions in the M‑profile Vector Extension **(MVE)** and half, single-precision scalar FPv5 architecture.

The EPU has the following features:
- MVE is implemented using a 64-bit arithmetic and load/store data-path in a two beats per tick configuration. A beat is the execution of 1/4 of an MVE instruction. Instructions can overlap to allow full utilization of the logic with a sustained bandwidth of 64-bit Multiply ACcumulate **(MAC)** and 64-bit load/store per cycle.
- Extended register file, which is optimized for efficient vector operations.
- Floating-point MAC unit capable of a throughput of up to two single-precision or four-half precision MAC instructions every cycle when MVE is included in the Cortex-M55 processor.

Memory components

The memory components consist of
- Memory Authentication Unit **(MAU)**: control access to the memory.
- Memory Protection Unit **(MPU)**: provide programmable support for memory protection using many software controllable regions. This unit defines the memory attributes that are associated with a particular memory region and the access permissions of addresses. Memory regions can be programmed to generate faults when accessed inappropriately, for example, by unprivileged software, reducing the scope of incorrectly written application code. The architecture includes fault status registers to allow an exception handler to determine the source of the fault and to apply corrective action or notify the system. The entire MPU logic can be split into Secure and Non-secure MPU regions.
- Security Attribution Unit **(SAU)**: define and authenticates access to memory based on the Security states **(Non-secure, Secure and Non-secure Callable, Secure)**.
- TCM Gate Unit: control software to access TCMs based on the Security attribute of the access.

- Memory system: include interface to and ITCM and four interfaces to DTCM, an L1 instruction cache and an L1 data cache, internal bus to access system memory and peripherals.

Interrupt components

The interrupt components consist of

- Nested Vectored Interrupt Controller **(NVIC)**: achieve low-latency interrupt processing
- Wakeup Interrupt Controller **(WIC)**: allow processor to enter low-power state

TrustZone security

TrustZone technology uses the Security Extension. Memory and peripherals in the system can be marked as Secure, making them accessible only to code that is running in the Secure state. Interrupts can be marked as Secure indicating that they are handled by Secure handler code in the Secure world. Hardware protects all Secure resources, including firmware and sensitive data values from being visible to Non-secure code and debug.

5.4. Ethos-U55 microNPU

The Ethos-U55 microNPU improves inference performance of neural networks. The microNPU targets 8-bit and 16-bit integer quantized Convolutional Neural Networks **(CNN)** and Recurrent Neural Networks **(RNN)**. The NPU supports 8-bit weights.

A neural network must be compiled offline using the open-source compiler to produce a command stream. The application invokes the driver, which communicates with the microNPU to tell it where the command stream is and initiates the network traversal. The command stream describes the steps necessary for the NPU to execute the operators compiled into the command stream autonomously. When complete, the NPU raises an IRQ to the driver.

The Ethos-U55 microNPU supports open-source *TensorFlow Lite for Microcontrollers* tool, which runs on an external host application processor. It uses the compiler offline to compile and optimize the neural network graph for the microNPU. Its API generates a command stream for the microNPU to process.

The compiler decides which parts of a network graph can be optimized and executed on the microNPU. The Ethos-U55 microNPU drivers manage the workloads that execute inferences on the microNPU. The others process layers will be performed by Cortex-M55 processor.

5.5. Security

5.5.1. PUF and OTP

PUF provides the primitive functions of robust on-chip secret, trusted secure storage, and endless supply of true random bits generation.

- PUF ID: offer 8 unique 256-bit keys. These keys can be used as a source for a unique ID, root key or entropy source, which is different for each chip.
- PUF Key Storage: a PUF-based data encryption technique for secure storage.
- PUF TRNG: a true random number generator with a PUF-based refinement engine.
- One Time Programming **(OTP)**: 1KB OTP storage for security and analog trimming.

5.5.2. CryptoCell-312 crypto

CryptoCell-312 offers platform security services and a rich set of cryptographic services that target multiple threats. The services that CryptoCell-312 offers are needed across various IoT applications.

CryptoCell-312 supports the following features:
- Cryptographic acceleration for the protection of data-in-transit and data-at-rest.
- Multiple modes and algorithms.
- Protection of various assets **(for example, code or data)**, belonging to various stakeholders **(for example, ICV, OEM, or service provider)**. It includes Image verification at boot or during runtime, Authenticated debug, Security life-cycle-state management, and Asset Provisioning.

CryptoCell-312 supports a variety of cryptographic algorithms and modes as below.

Algorithm	Mode	Key size
AES	ECB, CEC, CTR, OFB,	128, 192, and 256-bit
	CMAC, CBC-MAC	128, 192, and 256-bit
	CCM	128, 192, and 256-bit
	GCM	128, 192, and 256-bit
Hash	SHA1, SHA2 **(SHA224, SHA256)**	N/A
HMAC	SHA1, SHA2 **(SHA224, SHA256)**	N/A
RSA PKCS#1	Encryption, signature schemes: • PKCS #1 v2.1 Public-Key Cryptography Standards RSA Cryptography Specifications Using SHA1, SHA224, SHA256	2048, 3072, and 4096-bit
RSA key generation	N/A	2048 and 3072-bit
ECC key generation	N/A	NIST curves and 25519 curves.
Elliptic curve digital signature	N/A	NIST curves.
Key derivation	CMAC • NIST SP800-108 Recommendation for Key Derivation Using Pseudorandom Functions	N/A
TRNG	Compliant with NIST SP 800-90B Recommendation for the Entropy Sources Used for Random Bit Generation.	N/A

Table 5.6: CryptoCell-312 supported algorithms

For more information, see the Cryptocell-312 hardware-accelerated algorithms in the *Arm CryptoCell-312 Software Integrators Manual*.

5.5.3. TrustZone

The TrustZone technology for Armv8-M is a Security Extension that is designed to partition the hardware into secure and non-secure worlds

In the Arm architecture, there are two memory mapped Security states: Secure and Non-secure. After software setting the security attribution, all system resources including Flash memory, SRAM, peripherals, and interrupts are partitioned to either secure or non-secure world. Non-secure world only accesses non-secure resources. Secure world can access all resources in both worlds, including secure and non-secure resources. The HX6538-A follows Arm Trusted Firmware-M **(TF-M)** secured software architecture including Secure Processing Environment **(SPE)** and Non-secure Processing Environment **(NSPE)**. TF-M relies on an isolation boundary between the NSPE and the SPE.

For more information, see the *TrustZone technology for the ARMv8-M architecture*.

5.5.4. Secure debug channel

Secure debug engine provides a dedicated channel for authentication to the HX6538-A target platform by using an unlocking mechanism. Authentication certificate can be verified by secure debug engine through this channel.

The secure debug performs the following tasks:
- Performs boot-time verification of debug certificates that enable authenticated debugging of secure domains.
- Allows an authorizing party to shift the device into RMA LCS by using the same certificate mechanism.

The debugged target and the servicing agent are typically the same processor or processor subsystem, but they can be separate entities as well. The authentication process can involve a hardware-based cryptographic engine on the target.

The cryptographic engine verifies the debug certificate that is passed to the servicing agent through the secure debug engine. The debugger and the servicing agent run a protocol on top of the secure debug engine, which:
- Identifies the HX6538-A chip.
- Injects the appropriate debug certificate to the debug target for processing by the cryptographic engine.

5.5.5. Secure system

Features

- Secure boot
- Secure On-The-Air **(OTA)** firmware update
- Secure key generation and storage in PUF

Function description

The HX6538-A security system solution including signature authentication for the running firmware, firmware update and software protected in TrustZone.

Secure boot is to prevent the loading of malicious or unauthorized firmware on the HX6538-A. Secure OTA provides the basis for secure firmware update and validate by digital signature.

Secure boot

The secure boot provides a secure foundation for customer firmware. The HX6538-A bootloader is started from SPE to provides authentication, decryption, integrity verification, and version checking for customer firmware on installation and boot/reset. And set secure resource permission in TF-M.

The secure boot flow chart is as below.

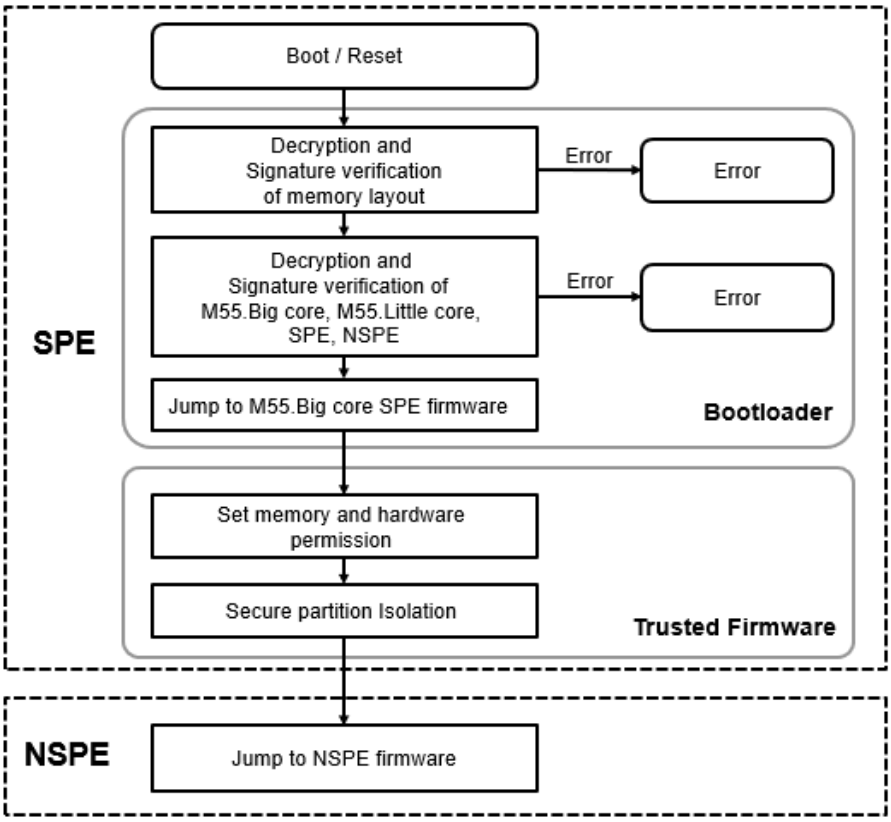


Figure 5.1: Secure boot flow

Secure OTA

The secure OTA is executed in the HX6538-A firmware and loader. The secure OTA uploader provides the authentication, decryption, integrity verification and firmware version checking for customer firmware before upgrade firmware to Flash memory.

Below are the tasks for secure OTA:

- OTA APP in NSPE invokes PSA firmware update **(FWU)** service in SPE to initial and setup OTA process in SPE.
- OTA process does firmware version checking, firmware decryption and signature verification.
- OTA process can do the re-encryption with hardware unique key **(HUK) (optional)**.
- OTA process updates firmware to Flash memory.

The secure OTA flow chart is as below.

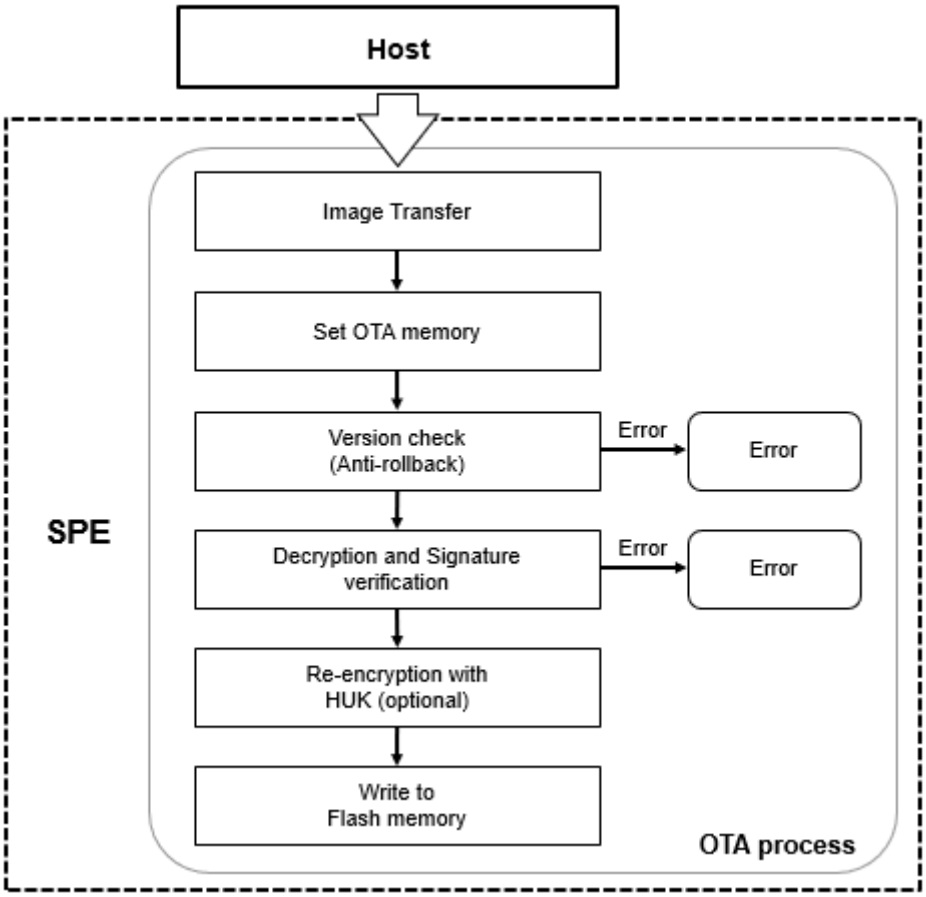


Figure 5.2: Secure OTA flow

5.6. Camera interfaces and subsystem

5.6.1. MIPI receiver and image pass-through

MIPI interface is commonly used in camera. The HX6538-A provides 2-lane MIPI CSI-2 v1.2 RX interface to connect with camera. The supported max resolution is 3840x2160, and 8-,10-bit RAW image data format.

MIPI CSI-2 v1.2 TX interface supports image pass-through mode only. The supported max resolution is 3840x2160, 8- or 10-bit RAW image data format, and 2 virtual channels for HDR application. In this mode, MIPI TX output clock and data are transparent from MIPI RX input directly. Image mute function is also supported in this mode by VMUTE input GPIO control.

5.6.2. DVP and SDI

Digital Video Port **(DVP)** supports 1-,4-,8-bit parallel image data signals based on camera module configuration. 1-bit DVP signal also supports Himax Serial Digital Interface **(SDI)** mode that is a 2-wire image data and clock without SEN_FVALD and SEN_LVALID signals. Besides DVP signals, the HX6538-A also supports “hardware trigger” side band signals that is a novel low-power communication mechanism with Himax always-on vision **(AONV)** sensors. In most of use cases, the AONV sensor and the AI processor stay in standby mode to save power. When a system wakeup event occurs, the AI processor asserts a “hardwire trigger” signal to the AONV sensor and trigger the sensor to resume exposure and data readout. This “hardwire trigger” communication is purely controlled by the hardware and is not MCU software assisted. This mechanism reduces camera wakeup time and provide the optimum system power consumption.

5.6.3. Image subsystem

Features

- Motion detection with de-noise pre-processing **(max. resolution 480x270)**
- Crop function to select Region of Interest **(ROI)**
- 2x2 down-scaling in vertical and horizontal
- 5x5 low pass filter or demosaic for Bayer image
- 2/3/4/5/6/7/8 sub-sampling in channel or quad mode
- 2/3/4/5/6/7/8 binning in channel or quad mode
- JPEG decode and encode **(fixed 4x or 10x compression ratio)**
- RGB to YUV converter
- DMA

Function description

The image subsystem includes camera interfaces and hardware accelerators that provide image pre-processing function, and most used functions in feature extraction of Computer Vision **(CV)** algorithm. It can off-load Cortex-M55/Ethos-U55 and achieve higher “Vision” performance with low power consumption. The image data is from either MIPI RX or DVP or SDI interface. The maximum input resolution of front-end INP block is 3840x2160 from MIPI RX interface. The maximum output resolution of INP is 640x640 by image sub-sampling, or binning or crop at single region of interest (ROI), then the INP processed data will enter image subsystem for pre-processing before ML.

The front-end INP block provided below sub-sampling and binning modes.

- Sub-sampling: Sub-2/3/4/5/6/7/8 in channel or quad modes
- Binning: Bin-2/3/4/5/6/7/8 in channel or quad modes

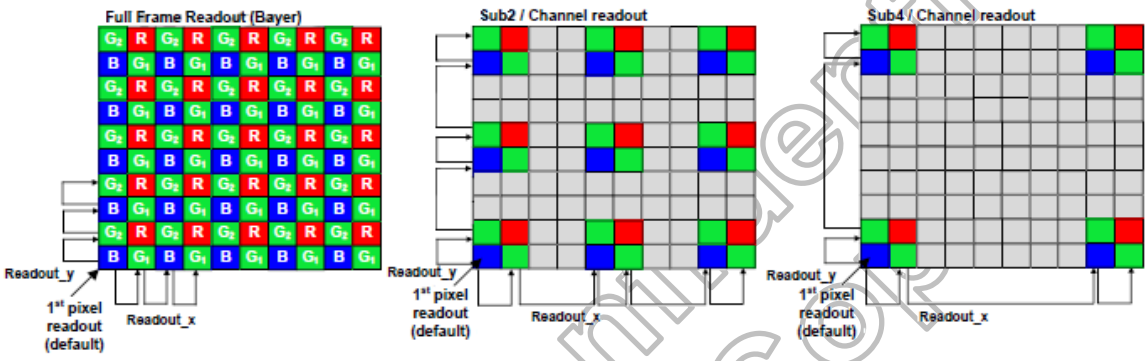


Figure 5.3: Sub-sampling in channel mode

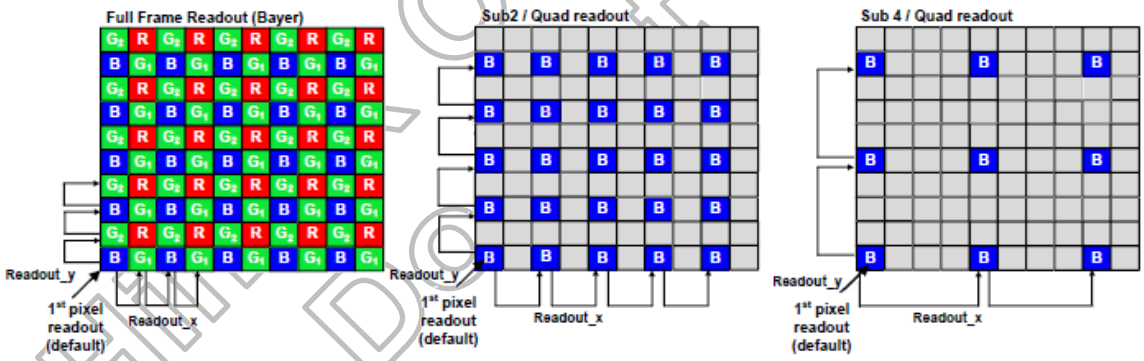


Figure 5.4: Sub-sampling in quad mode

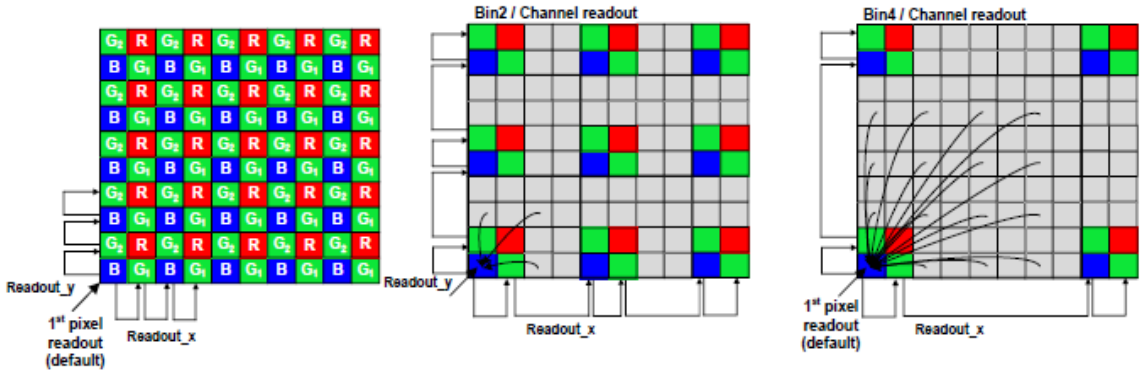


Figure 5.5: Binning in channel mode

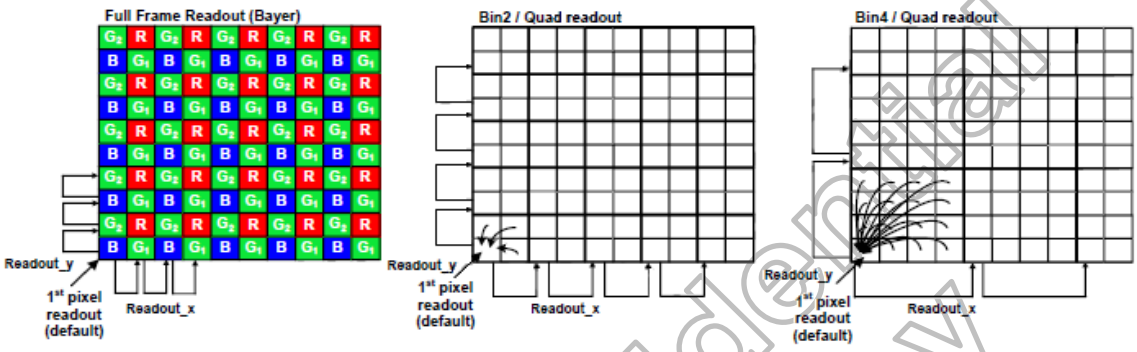


Figure 5.6: Binning in quad mode

A programmable virtual channel data selection is provided for MIPI RX input. It supports 2 virtual channels for line-interlaced long-short exposure. Only one MIPI RX virtual channel data enter image subsystem for ML, and filler out another one.

The image datapath flow control provides individual accelerator enable/disable control and various datapath routing setting by software programming. Motion Detection **(MD)** is one of wakeup sources for PMU or MCU in power-down mode or sleep mode. JPEG CODEC is used for image data compression to reduce storage space of system memory. The image datapath also includes DMA engines to transfer processed image data into system memory or get system memory data for hardware processing. It supports image pre-roll when MCU in power-down mode or sleep mode.

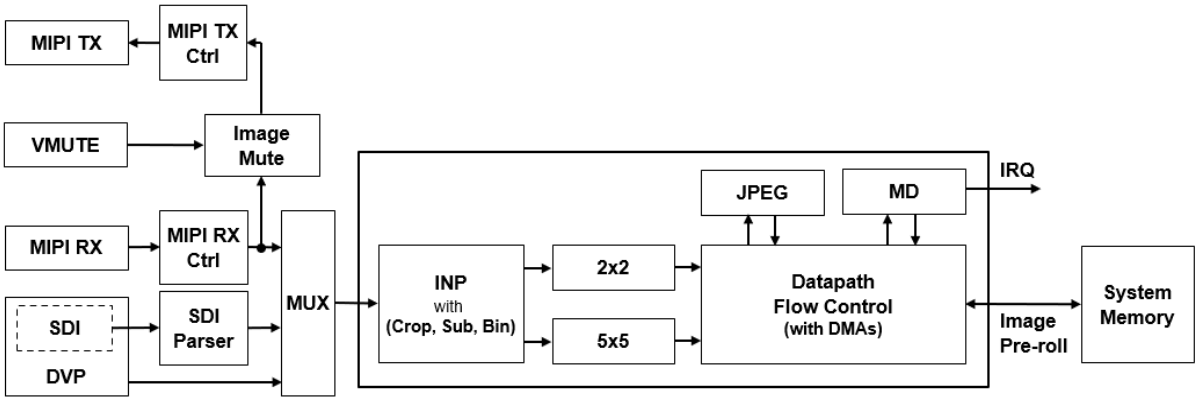


Figure 5.7: Image subsystem block diagram

5.7. Audio interfaces and subsystem

5.7.1. PDM receiver and audio pass-through

Pulse-Density Modulation **(PDM)** interface is commonly used in digital microphone input. The HX6538-A provides up to 8 channels PDM microphone inputs for far field audio applications. It supports up to 3.25MHz input PDM frequencies to convert to 8K to 48KHz 16-bit PCM output data.

PDM TX interface supports audio pass-through mode only. In this mode, 2-channels PDM TX output data is pass-through from PDM RX input pin directly, and PDM RX output clock is pass-through from PDM TX input pin directly.

5.7.2. I^2S

I^2S interface provides a standard communication for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual **(mono or stereo)** audio data transfer. The HX6538-A provides up to 2 channels, programable master or slave I^2S interface. It supports 12-,16-, 20-,24-, and 32-bit audio data resolution.

5.7.3. Audio subsystem

Features

- Hardware-based voice activity detector **(HWVAD)** with input gain control
- DMA

Function description

The audio subsystem includes audio interfaces and hardware-based voice activity detector **(HWVAD)**. The HWVAD can be active during sleep mode and therefore provide lowest power operation comparing with software-based implementation. HWVAD output an interrupt to wakeup Little Cortex-M55 processor when the delta between the two detectors is larger than a predefined value. The input source of HWVAD is PCM format that comes from anyone of PDM channels or I^2S channels.

In combing with system DMA services, audio subsystem can transfer audio data into system memory during sleep mode for further data analysis after Coetex-M55 processor wakeup. It supports audio pre-roll when MCU in sleep mode.

This subsystem also provides 2-channel audio pass-through mode for PDM Microphone application. In this mode, PDM TX audio output data is from PDM RX input.

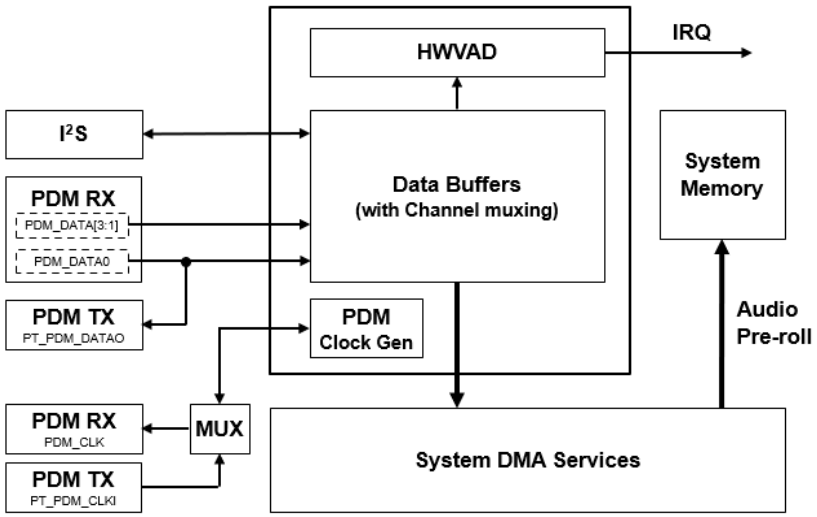


Figure 5.8: Audio subsystem block diagram

5.8. Peripherals

5.8.1. DMA

The DMA controller provides peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA service provides descriptor-based unidirectional DMA transfers for a single source and destination.

5.8.2. Timers and RTC

The general purpose 32-bit Timers is designed to count cycles of the system derived clock with interrupt. Real Time Clock **(RTC)** provides date and time functions that allow the user to set and retrieve calendar date and time with alarm function **(epoch of January 1, 2000 00:00:00 (hh:mm:ss))**. RTC block is in the always-on power domain. No re-initial date and time needed after system back from power-down or deep-power-down mode. Therefore, RTC data can be used for system time stamp information as well.

5.8.3. Watch-dog

The Watch-dog is designed to count cycles of the system derived clock. It can optionally generate interrupts and reset. Watch-dog block is in the always-on power domain. The counter is still active in power-down or deep-power-down mode.

5.8.4. I^2C

The I^2C supports features as below:
- Master or slave operation
- Programable 7- or 10-bit addressing
- Support for clock stretching
- Transmission modes
  - Standard mode **(0 to 100Kb/s)**
  - Fast mode **(up to 400Kb/s)**
  - Fast mode plus **(up to 1000Kb/s)**

5.8.5. I^3C

The I^3C supports features as below:
- Slave operation only **(MIPI I^3C spec v1.0)**
- In-band interrupt
- Transmission modes
  - Standard mode **(0 to 100Kb/s)**
  - Fast mode **(up to 400Kb/s)** / Fast mode plus **(up to 1000Kb/s)**
  - Single data rate messaging **(SDR, SDR mode, up to 12.5Mb/s)**
  - High data rate messaging **(HDR, HDR-DDR mode, up to 25Mb/s)**

5.8.6. SPI

The SPI supports features as below:
- Master or slave operation
- Programmable data frame size from 4 to 32-bit
- Programmable serial interface operation
  - Motorola Serial Peripheral Interface (SPI)
  - Texas instruments Synchronous Serial Protocol **(SSP)**
  - National Semiconductors Microwire

5.8.7. UART

The UART supports features as below:
- 9-bit serial data support
- False start bit detection
- Programmable fractional baud rate support
- Support Auto Flow Control mode **(UART1 only)**
- Support multi-drop RS485 interface **(UART1 only)**
- Support IrDA 1.0 SIR mode **(UART1 only)**

5.8.8. GPIO

The GPIO controls the output data and direction of external I/O pads with interrupt capability. It can also read back the data on external pads using memory-mapped registers. The read back data can be inverted by programming register.

5.8.9. SD and SDIO host

The SD and SDIO host interface supports modes as below:
- Secure Digital memory **(SD v1.1/2.0)**
- Secure Digital I/O **(SDIO v2.0)**
- Supports up to 25 MHz DS mode of interface frequency

6. Electrical Characteristics

6.1. Absolute maximum ratings(1)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply voltage	VDDA_ADC VDDA_PLL VDDA_OTP VDDA_TX VDDA_RX VDDIO_SIF VDDA_PSRAM(2)	-0.5	-	2.07	V
	VDD	-0.5	-	1.03	V
	VDDIO_PIF VDDIO_AON VDDA_DCDC	-0.5	-	3.63	V
CMOS/TTL input voltage	V_{IN}	-0.5	-	VDDIO	V
CMOS/TTL output voltage	V_{OUT}	-0.5	-	VDDIO	V
Storage temperature	T_{STG}	-40	-	125	°C
ESD Human body model(3)	V_{ESD_HBM}	-	-	2000	V
ESD Machine model(4)	V_{ESD_MM}	-	-	100	V
Latch-up current(5)	I_{LU}	-	-	100	mA

Note: (1) Device will probably be damaged permanently in case that the stresses are over the absolute maximum ratings listed above.
(2) For HX6538-A07TLGG only.
(3) HBM condition: T_A=25°C, Standard EIA /JEDEC JESD22-A114.
(4) MM condition: T_A=25°C, Standard EIA /JEDEC JESD22-A115.
(5) Latch-up condition: T_A=25°C, Standard JEDEC STANDARD NO.78 March 1997.

6.2. Recommended operating conditions

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Supply voltage	VDDA_ADC VDDA_PLL VDDA_OTP VDDA_TX VDDA_RX VDDIO_SIF VDDA_PSRAM(1)	-	1.7	1.8	1.9	V
	VDD	M55.Big core at 400MHz U55 core at 400MHz M55.Little core at 150MHz	0.85	0.9	0.95	V
		M55.Big core at 150MHz U55 core at 150MHz M55.Little core at 75MHz	0.75	0.8	0.95	V
	VDDIO_PIF VDDIO_AON VDDA_DCDC(2)	-	1.7	1.8(3)	1.9	V
		-	3.1	3.3(3)	3.5	V
Operating temperature	T_A	-	-40	25	85	°C
Junction temperature	T_J	-	-40	-	105	°C

Note: (1) For HX6538-A07TLGG only.
(2) VDDA_DCDC supply voltage must be the same with VDDIO_AON.
(3) According to the host controller's I/O voltage.

6.3. Power consumption

Mode	Condition	Supply voltage(1)	Current			Unit
			Min.	Typ.(2)	Max.	
Active **(Dual core)**	VDD=0.9V M55.Big=U55=400MHz **(Facial Landmark)** M55.Little=100MHz **(Idle)** 24MHz XTAL is enabled PLL is enabled	VDDIO_PIF=1.8V VDDIO_AON=1.8V VDDIO_DCDC=1.8V	-	40	-	mA
		VDDIO_PIF=3.3V VDDIO_AON=3.3V VDDIO_DCDC=3.3V	-	TBD	-	mA
Active **(Single core)**	VDD=0.9V M55.Big=U55=power gating mode M55.Little=24MHz **(Drystone)** 24MHz XTAL is disabled PLL is disabled 24MHz RCOSC is enabled	VDDIO_PIF=1.8V VDDIO_AON=1.8V VDDIO_DCDC=1.8V	-	TBD	-	mA
		VDDIO_PIF=3.3V VDDIO_AON=3.3V VDDIO_DCDC=3.3V	-	TBD	-	mA
Active **(Single core)**	VDD=0.8V M55.Big=U55=power gating mode M55.Little=24MHz **(Drystone)** 24MHz XTAL is disabled PLL is disabled 24MHz RCOSC is enabled	VDDIO_PIF=1.8V VDDIO_AON=1.8V VDDIO_DCDC=1.8V	-	TBD	-	mA
		VDDIO_PIF=3.3V VDDIO_AON=3.3V VDDIO_DCDC=3.3V	-	TBD	-	mA
Sleep **(Single core)**	VDD=0.8V M55.Big=U55=power gating mode M55.Little=24MHz **(WFI)** 24MHz XTAL is disabled PLL is disabled 1MHz RCOSC is enabled	VDDIO_PIF=1.8V VDDIO_AON=1.8V VDDIO_DCDC=1.8V	-	TBD	-	mA
		VDDIO_PIF=3.3V VDDIO_AON=3.3V VDDIO_DCDC=3.3V	-	TBD	-	mA
Power-Down	VDD=0.6V M55.Big=U55=power gating mode M55.Little=power gating mode AXI/AHB/TCM SRAMs are retention 24MHz XTAL is disabled PLL is disabled 32.768KHz RCOSC is enabled PMU is active, wait for RCOSC wake up	VDDIO_PIF=1.8V VDDIO_AON=1.8V VDDIO_DCDC=1.8V	-	TBD	-	mA
		VDDIO_PIF=3.3V VDDIO_AON=3.3V VDDIO_DCDC=3.3V	-	TBD	-	mA
Deep-Power-Down	VDD=OFF M55.Big=U55=OFF M55.Little=OFF 24MHz XTAL is OFF PLL is OFF 32.768KHz RCOSC is disabled PMU is active, wait for GPIO wake up	VDDIO_PIF=OFF VDDIO_AON=1.8V VDDIO_DCDC=1.8V	-	1.0	-	μA
		VDDIO_PIF=OFF VDDIO_AON=3.3V VDDIO_DCDC=3.3V	-	TBD	-	μA

Note: (1) VDDA_* and VDDIO_SIF supply voltage are 1.8V. These supply sources are OFF in deep-power-down mode.
(2) Typical ratings are not guaranteed. Typical values are characterized through measurements at room temperature **(25°C)** using typical samples.

6.4. DC electrical characteristics

6.4.1. I/O Pins

(3.3V mode I/O parameters for AON/PIF domain GPIOs)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High level input voltage	V_{IH}	-	2.0	-	VDDIO	V
Low level input voltage	V_{IL}	-	GND	-	0.8	V
High level output voltage	V_{OH}	I_{OH}=-2mA	2.4	-	VDDIO	V
Low level output voltage	V_{OL}	I_{OL}=2mA	GND	-	0.4	V

Table 6.1: 3.3V mode I/O DC parameters

(1.8V mode I/O parameters for AON/PIF/SIF domain GPIOs)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High level input voltage	V_{IH}	-	0.7 x VDDIO	-	VDDIO	V
Low level input voltage	V_{IL}	-	GND	-	0.3 x VDDIO	V
High level output voltage	V_{OH}	I_{OH}=-2mA	0.8 x VDDIO	-	VDDIO	V
Low level output voltage	V_{OL}	I_{OL}=2mA	GND	-	0.2 x VDDIO	V

Table 6.2: 1.8V mode I/O DC parameters

6.4.2. MIPI transmitter

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High speed transmit static common mode voltage(1)	V_{CMTX}	-	150	200	250	mV
V_{CMTX} mismatch when output is differential-1 or differential-0(2)	$\lvert\Delta V_{CMTX}\rvert_{(1,0)}$	-	-	-	5	mV
High speed transmit differential voltage(1)	$\lvert V_{OD}\rvert$	-	140	200	270	mV
V_{OD} mismatch when output is differential-1 or differential-0(2)	$\lvert\Delta V_{OD}\rvert$	-	-	-	14	mV
High speed output high voltage(1)	V_{OHHS}	-	-	-	360	mV
Single ended output impedance	Z_{OS}	-	40	50	62.5	Ω
Single ended output impedance mismatch	ΔZ_{OS}	-	-	-	10	%

Note: (1) Value when driving into load impedance anywhere in the Z_{ID} range.
(2) It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity.

Table 6.3: MIPI HS-TX DC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Thevenin output high level	V_{OH}	-	1.1	1.2	1.3	V
Thevenin output low level	V_{OL}	-	-50	-	50	mV
Output impedance of low power transmitter(1)	Z_{OLP}	-	110	-	-	Ω

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.

Table 6.4: MIPI LP-TX DC parameters

6.4.3. MIPI receiver

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Common-mode voltage HS receive mode(1)(2)	$V_{CMRX(DC)}$	-	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	-	70	mV
Differential input low threshold	V_{IDTL}		-70	-	-	mV
Single-ended input high voltage(1)	V_{IHHS}	-	-	-	460	mV
Single-ended input low voltage(1)	V_{ILHS}	-	-40	-	-	mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	-	450	mV
Differential input impedance	Z_{ID}	-	80	100	125	Ω

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance, and variations below 450MHz.

Table 6.5: MIPI HS-RX DC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IH}	-	800	-	-	mV
Logic 0 input voltage, not in ULP state	V_{IL}	-	-	-	550	mV
Logic 0 input voltage, ULP state	$V_{IL-ULPS}$	-	-	-	300	mV
Input hysteresis	V_{HYST}	-	25	-	-	mV

Table 6.6: MIPI LP-RX DC parameters

6.5. AC electrical characteristics

6.5.1. I²C interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	1	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	50	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	5	-	-	ns

Table 6.7: I²C AC parameters

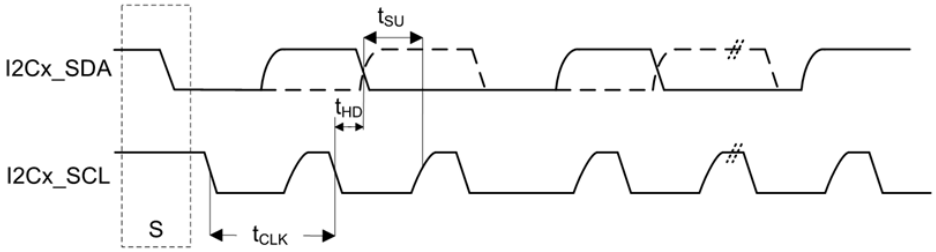


Figure 6.1: I²C bus timing

6.5.2. I³C interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	12.5	MHz
		VDD=0.8V	-	-	10	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	6	-	-	ns
Data input hold time	t_{HD}	VDD=0.9V	3	-	-	ns
		VDD=0.8V	5	-	-	ns

Table 6.8: I³C AC parameters

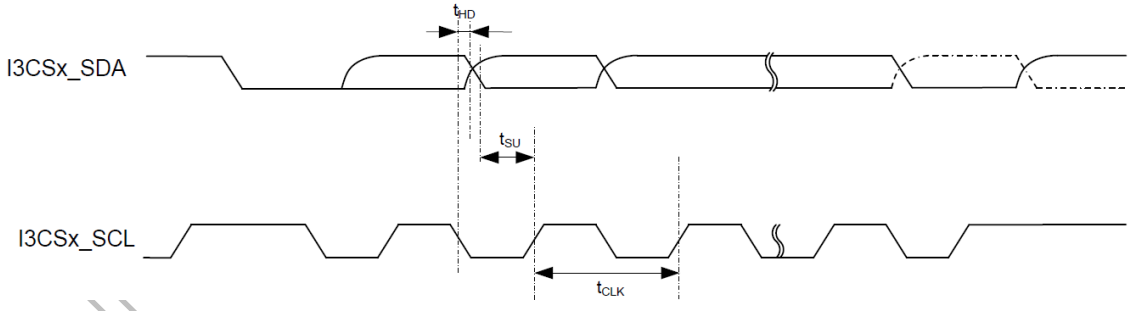


Figure 6.2: I³C bus timing

6.5.3. SPI interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	50	MHz
		VDD=0.8V	-	-	25	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	4	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	0	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-2(1)	-	8	ns

Note: (1) A negative time indicates the actual output data edge is earlier than clock appearing at pin.

Table 6.9: SPI master AC parameters

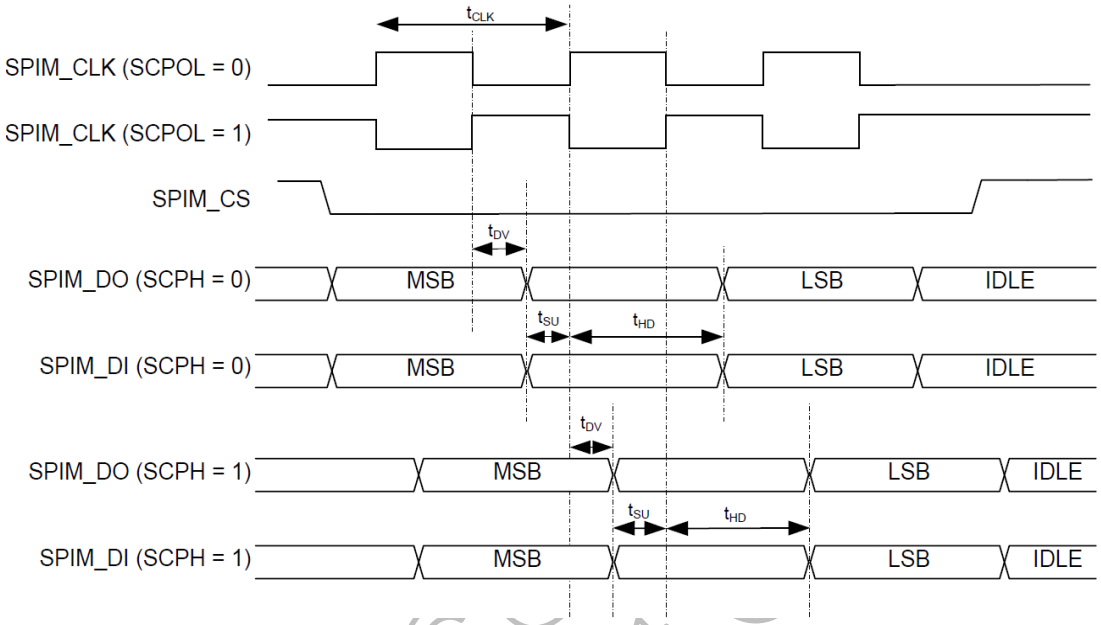


Figure 6.3: SPI master timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period(1)	t_{CLK}	VDD=0.9V	-	-	40	MHz
		VDD=0.8V	-	-	15	MHz
Data input setup time(1)	t_{SU}	VDD=0.9/0.8V	0	-	-	ns
Data input hold time(1)	t_{HD}	VDD=0.9V	10	-	-	ns
		VDD=0.8V	27	-	-	ns
Data output valid time(1)	t_{DV}	VDD=0.9V	10	-	22	ns
		VDD=0.8V	12	-	24	ns

Note: (1) SPIS_CLK, SPIS_DI, SPIS_DO signals are sampled by internal ssi_clk clock. The maximum clock period is one-tenth of ssi_clk frequency. The timing spec is based on ssi_clk frequency is 400MHz at 0.9V, and 150MHz at 0.8V.

Table 6.10: SPI slave AC parameters

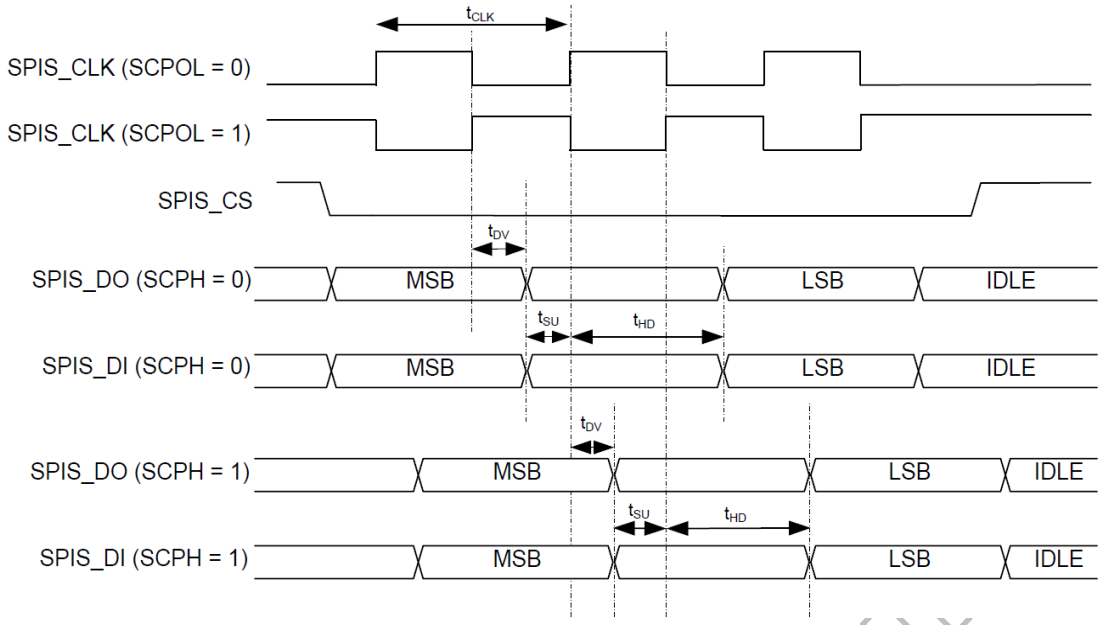


Figure 6.4: SPI slave timing

6.5.4. I²S interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.125	MHz
Clock HIGH	t_{WH}	VDD=0.9/0.8V	160	-	-	ns
Clock LOW	t_{WL}	VDD=0.9/0.8V	160	-	-	ns
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	10	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-	-	30	ns

Table 6.11: I²S master AC parameters

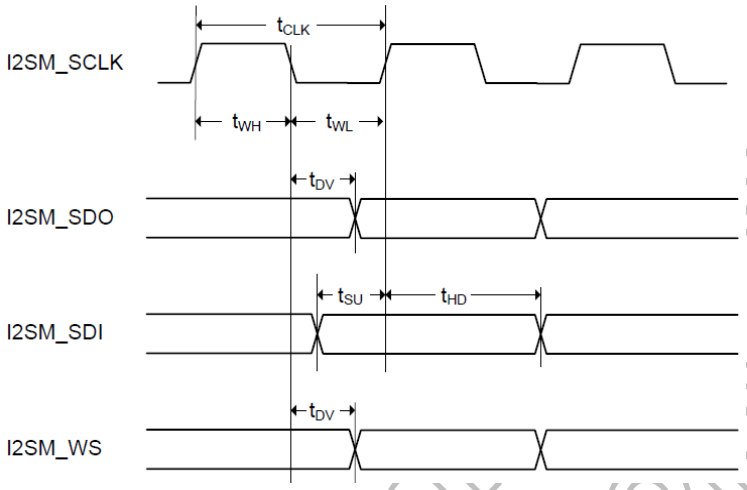


Figure 6.5: I²S master timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.125	MHz
Clock HIGH	t_{WH}	VDD=0.9/0.8V	160	-	-	ns
Clock LOW	t_{WL}	VDD=0.9/0.8V	160	-	-	ns
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	0	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-	-	30	ns

Table 6.12: I²S slave AC parameters

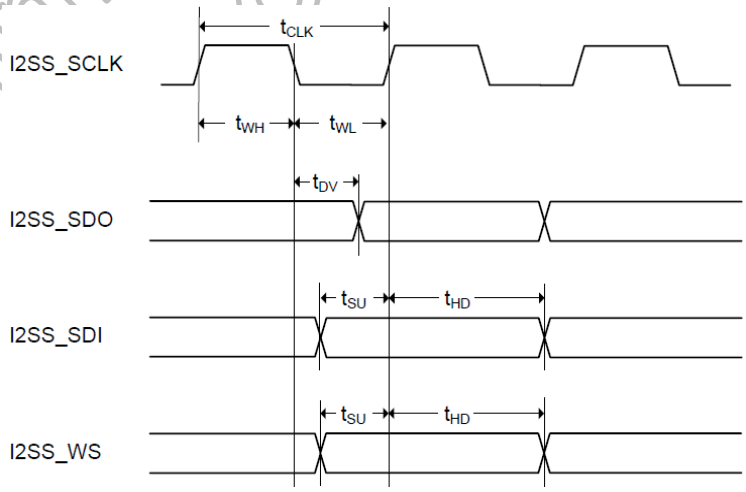


Figure 6.6: I²S slave timing

6.5.5. PDM interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.25	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	5	-	-	ns

Table 6.13: PDM RX AC parameters

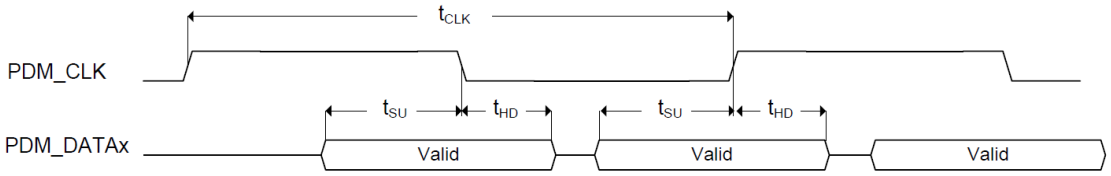


Figure 6.7: PDM RX timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.25	MHz
Clock path delay	t_{CLK_D}	VDD=0.9/0.8V	-	-	15	ns
Data path delay(1)	t_{DATA_D}	VDD=0.9/0.8V	-	-	15	ns

Note: (1) Only PDM_DATA0 input supports PDM pass-through mode.

Table 6.14: PDM pass-through AC parameters

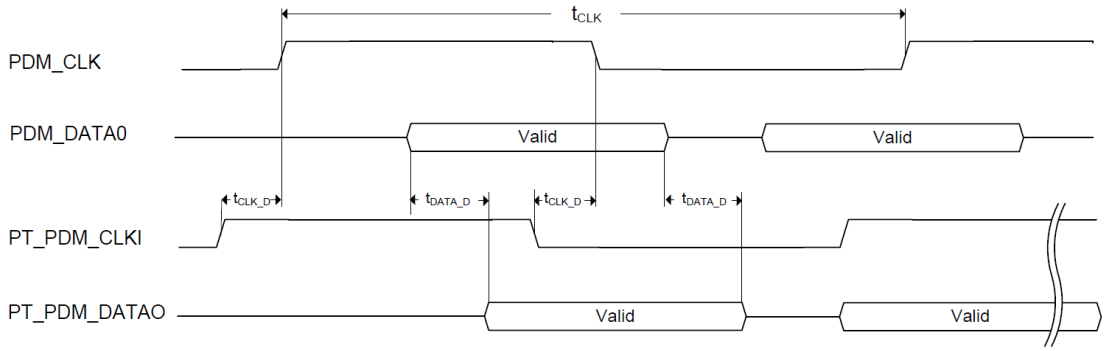


Figure 6.8: PDM pass-through timing

6.5.6. SD and SDIO host interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	25	MHz
		VDD=0.8V	-	-	12.5	MHz
Data input setup time	t_{SU}	VDD=0.9V	10	-	-	ns
		VDD=0.8V	13	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	3	-	-	ns
Data output valid time	t_{DV}	VDD=0.9V	-	-	14	ns
		VDD=0.8V	-	-	34	ns
Data output hold time	t_{OH}	VDD=0.9/0.8V	2	-	-	ns

Table 6.15: SD and SDIO host AC parameters

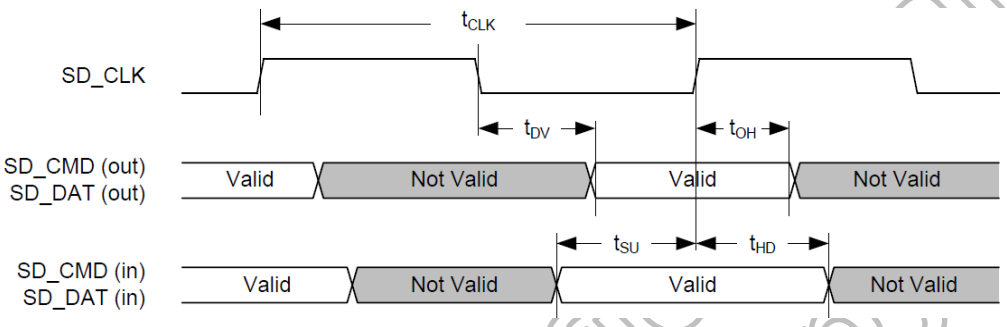


Figure 6.9: SD and SDIO host timing

6.5.7. DVP and SDI interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	72	MHz
		VDD=0.8V	-	-	40	MHz
Data input setup time	t_{SU}	VDD=0.9V	5	-	-	ns
		VDD=0.8V	11	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	6	-	-	ns

Table 6.16: DVP AC parameters

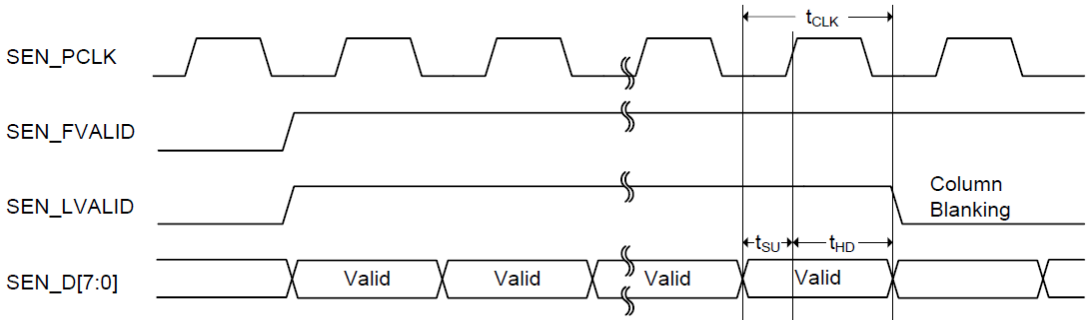


Figure 6.10: DVP interface timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	72	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	3	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	6	-	-	ns

Table 6.17: SDI AC parameters

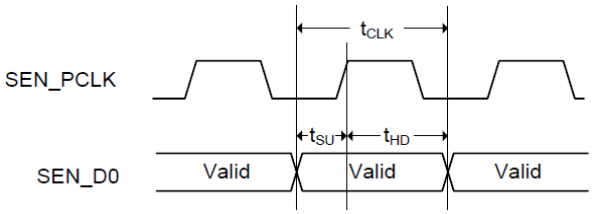


Figure 6.11: SDI interface timing

6.5.8. QSPI Flash interface(1)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	100	MHz
		VDD=0.8V	-	-	50	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	-1(2)	-	-	ns
Data input hold time	t_{HD}	VDD=0.9V	6	-	-	ns
		VDD=0.8V	11	-	-	ns
Data output valid time	t_{DV}	VDD=0.9V	-	-	3	ns
		VDD=0.8V	-	-	15	ns
Data output hold time	t_{OH}	VDD=0.9/0.8V	-2(3)	-	-	ns

Note: (1) The timing values above are based on default software settings for QSPI sampling registers.
(2) A negative time indicates the actual capture edge inside the device is later than clock appearing at pin.
(3) A negative time indicates the actual output data edge is earlier than clock appearing at pin.

Table 6.18: QSPI Flash AC parameters

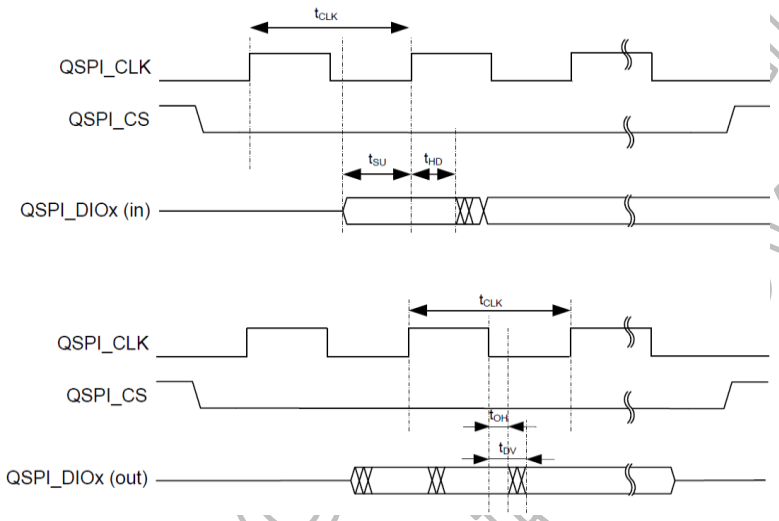


Figure 6.12: QSPI Flash interface timing

6.5.9. SWD debug interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	15	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	15	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-	-	45	ns

Table 6.19: SWD debug AC parameters

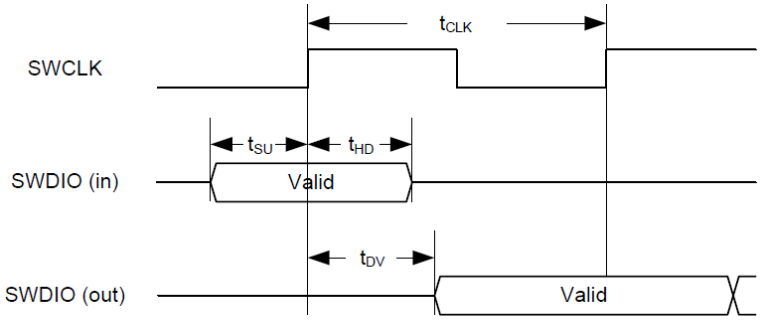


Figure 6.13: SWD debug interface timing

6.5.10. MIPI transmitter interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Common-level variations	$\Delta V_{CMTX(HF)}$	above 450MHz	-	-	15	mV_{RMS}
Common-level variations	$\Delta V_{CMTX(LF)}$	50-450MHz	-	-	25	mV_{PEAK}
Rise time and fall time	t_R and t_F	20% to 80%	-	-	0.3(1)(2)	UI
			-	-	0.35(1)(3)	UI
			-	-	0.4(4)	UI
			100(5)	-	-	ps

Note: (1) UI is equal to 1/(2*fh). See Ch. 8.3 of MIPI D-PHY specification for the definition of fh.
(2) Applicable when operating at HS bit rates ≤ 1Gbps **(UI ≥ 1ns)**.
(3) Applicable when operating at HS bit rates > 1Gbps **(UI < 1ns)**.
(4) Application for all HS Bit rate when supporting > 1.5Gbps.
(5) Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1Gbps **(UI ≥ 1ns)**, should not use values below 150ps.

Table 6.20: MIPI HS-TX AC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Rise time and fall time(1)	T_{RLP} /T_{FLP}	15% to 85%	-	-	25	ns
Rise time and fall time(1)(2)(3)	T_{REOT}	30% to 85%	-	-	35	ns
Pulse width of the LP exclusive-OR clock(4)	$T_{LP-PULSE-TX}$	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	-	-	ns
		All other pulses	20	-	-	ns
Period of the LP exclusive-OR clock	$T_{LP-PER-TX}$	-	90	-	-	ns
Slew Rate(1)(5)(6)(7)(8)(9)	$\delta V/\delta t_{SR}$	C_{LOAD}=0 pF	30	-	500	mV/ns
		C_{LOAD}=5 pF	30	-	300	mV/ns
		C_{LOAD}=20 pF	30	-	250	mV/ns
		C_{LOAD}=70 pF	30	-	150	mV/ns
Load capacitance(1)	C_{LOAD}	20% to 80%	0	-	70	pF

Note: (1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
(3) With an additional load capacitance CCM between 0 and 60pF on the termination center tap at RX side of the lane.
(4) This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between DP and DN LP transmitters. Any LP exclusive-OR pulse observed during HS EoT **(transition from HS level to LP-11)** is glitch behavior.
(5) Measured as average across any 50mV segment of the output signal transition.
(6) This value represents a corner point in a piecewise linear curve.
(7) When the output voltage is in the range specified by VPIN **(absmax)**.
(8) When the output voltage is between 400mV and 930mV.
(9) When the output voltage is between 400mV and 700mV.

Table 6.21: MIPI LP-TX AC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Common-mode interference(1)	$\Delta V_{CMRX(HF)}$	above 450MHz	-	-	100	mV
Common-mode interference(2)(3)	$\Delta V_{CMRX(LF)}$	50-450MHz	-50	-	50	mV
Common-mode termination(4)	CCM	-	-	-	60	pF

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) Excluding 'static' ground shift of 50mV.
(3) Voltage difference compared to the DC average common-mode potential.
(4) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 6.22: MIPI HS-RX AC parameters

6.5.11. MIPI receiver interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input pulse rejection(1)(2)(3)	e_{SPIKE}	-	-	-	300	V.ps
Minimum pulse width response(4)	T_{MIN-RX}	-	20	-	-	ns
Peak Interference amplitude	V_{INT}	-	-	-	200	mV
Interference frequency	f_{INT}	-	450	-	-	MHz

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state.
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 6.23: MIPI LP-RX AC parameters

6.5.12. ADC interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input voltage	V_{ADIN}	Differential	-1	-	1	V
		Single-end	-	-	1	V
ADC_REF reference voltage input	V_{REF}	-	-	1.2	-	V
Sampling rate	F_{SAMPLE}	-	-	-	1	MS/s
Differential nonlinearity	DNL	-	-	±0.9	-	LSB
Integral nonlinearity	INL	-	-	±1	-	LSB
Offset error	E_{OFFSET}	-	-	1	-	% FS
Effective number of bits	ENOB	Differential	-	9.5	-	Bit
		Single-end	-	8.5	-	Bit
Signal to noise ratio	SNR	Differential	-	70	-	dB
		Single-end	-	60	-	dB

Table 6.24: ADC characteristics

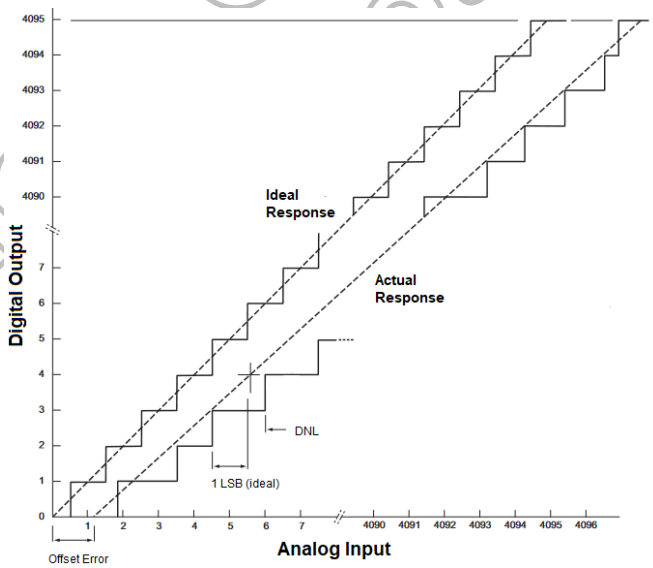
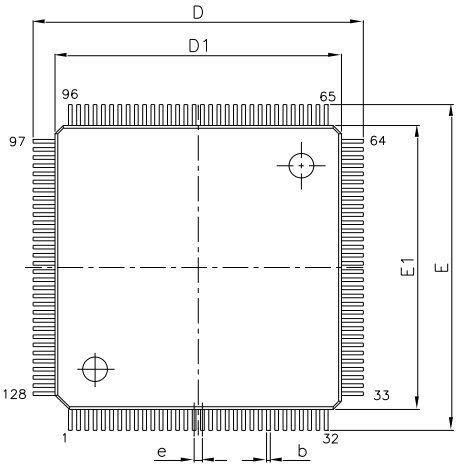
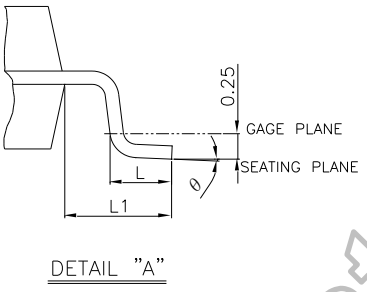


Figure 6.14: ADC characteristics

7. Package Outline Dimension

7.1. LQFP128

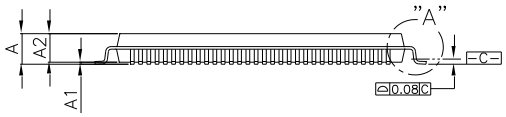




DETAIL "A"

Symbol	Min	Nom	Max
A	–	–	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
D	15.85	16.00	16.15
D1	13.90	14.00	14.10
E	15.85	16.00	16.15
E1	13.90	14.00	14.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

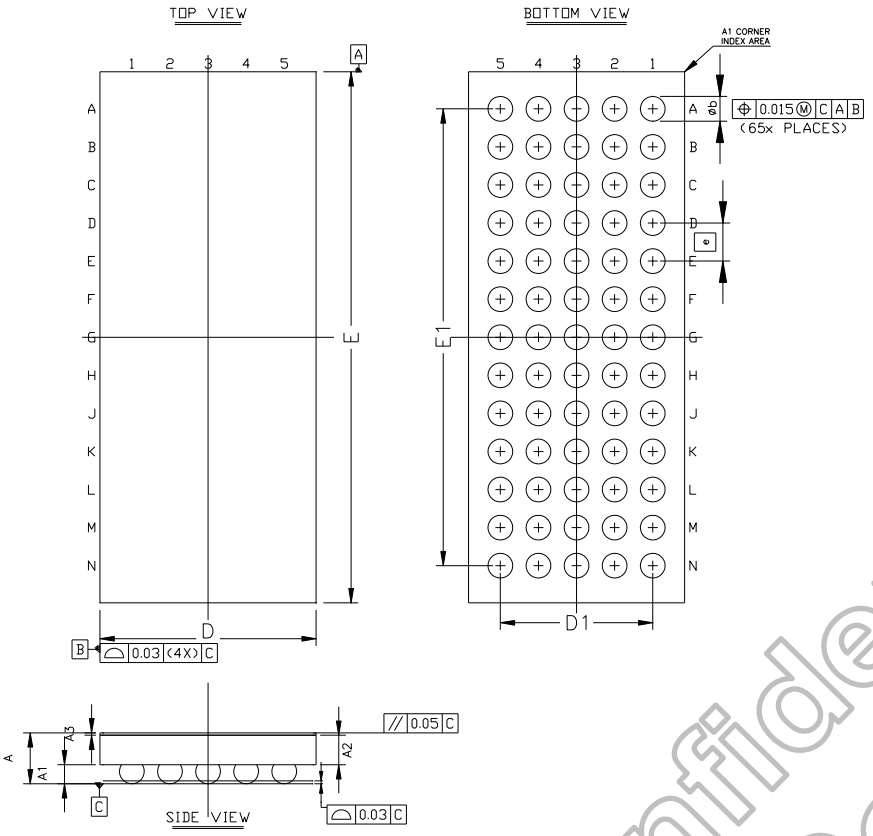
UNIT: MM



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
   INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE
   TO THE LOWEST POINT OF THE PACKAGE BODY.
6. REFERENCE DOCUMENT : JEDEC MS-026.

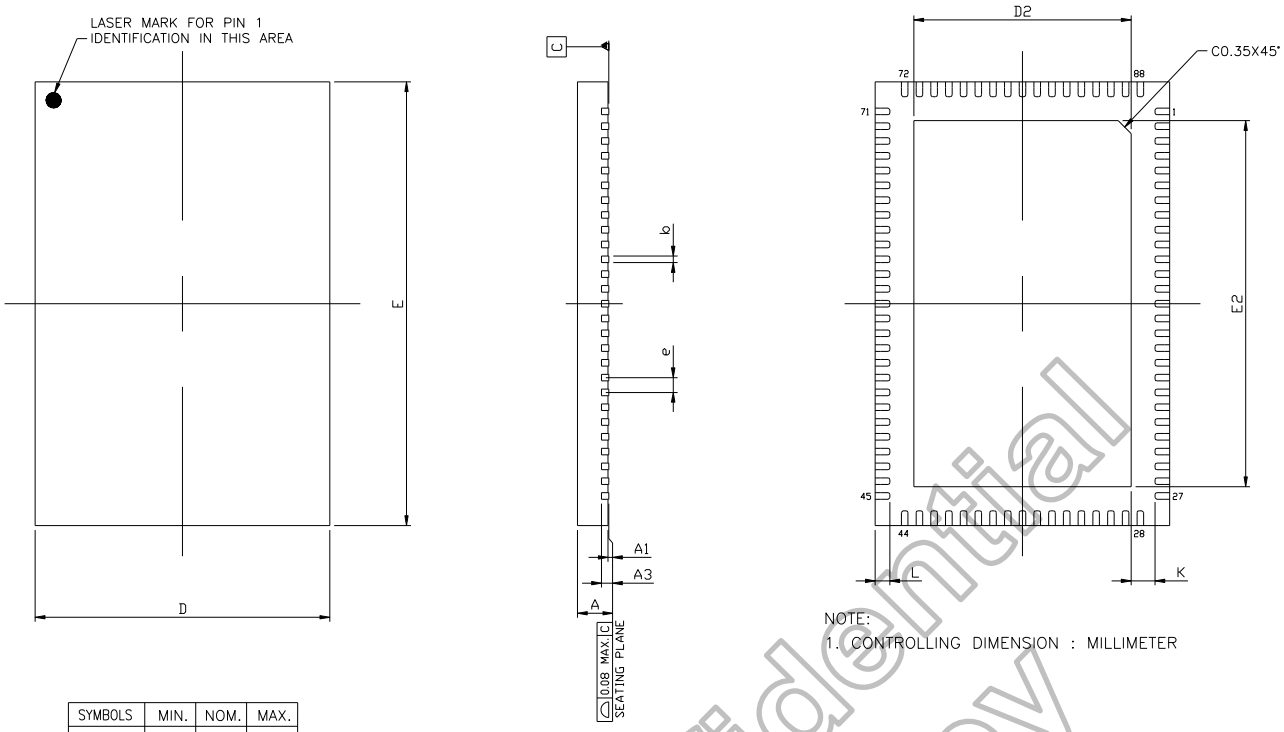
7.2. WLCSP65



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.505	0.535	0.565
A1	0.18	0.2	0.22
A2	0.29	0.31	0.33
A3	0.025 BSC		
øb	0.24	0.26	0.28
D	2.240	2.273	2.306
D1	1.6 BSC		
E	5.551	5.584	5.617
E1	4.8 BSC		
e	0.4 BSC		

UNIT: MM

7.3. QFN88

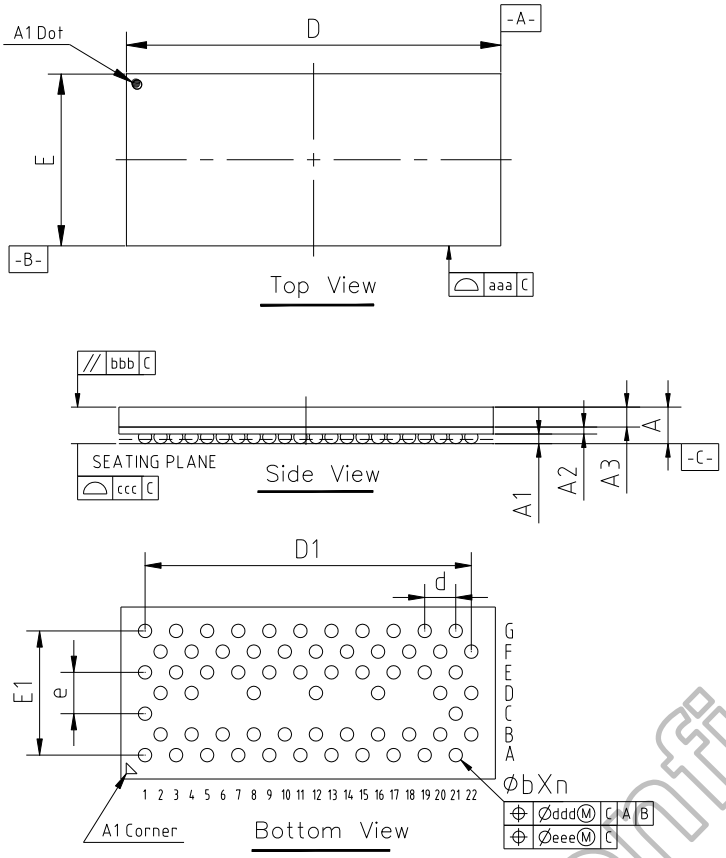


NOTE:
1. CONTROLLING DIMENSION : MILLIMETER

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	—	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
D	7.90	8.00	8.10
E	11.90	12.00	12.10
b	0.15	0.20	0.25
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

Exposed pad size				
L/F	D2		E2	
	MIN.	MAX.	MIN.	MAX.
①	5.60	6.20	9.60	10.20

7.4. BGA64



	Symbol	Dimension in mm		
		Min	Norm	Max
TOTAL THICKNESS	A	---	---	0.75
STAND OFF	A1	0.13	---	0.
SUBSTRATE THICKNESS	A2	0.10	0.13	0.16
MOLD THICKNESS	A3	0.36	0.37	0.38
BALL DIAMETER(BEFORE)	--		0.25	
BALL OPENING	--		0.25	
Test Pad OPENING	Φg		--	
BALL WIDTH (AFTER)	Φb	0.	---	0.
BALL PITCH	d		0.581	
	e		0.770	
BALL COUNT	n			
BODY SIZE	D	6.90	7.00	7.10
	E	3.10	3.20	3.30
EDGE BALL CENTER TO CENTER	D1			
	E1			
PROFILE OF A SURFACE	aaa		0.10	
MOLD FLATNESS	bbb		0.	
COPLANARITY	ccc		0.08	
BALL OFFSET(PACKAGE)	ddd		0.15	
BALL OFFSET(BALL)	eee		0.	

UNIT: MM

8. Ordering Information

Part no.	Package	Application	Description
HX6538-A04TLDG	LQFP128	AIoT, surveillance	WE2 AI processor
HX6538-A07TLGG	LQFP128	AIoT, surveillance	WE2 AI processor **(SIP with 8MB HyperRAM)**
HX6538-A01TWA	WLCSP65	AIoT, Laptop, wearable	WE2 AI processor
HX6538-A05TBEG	BGA64	AIoT, Laptop, wearable	WE2 AI processor
HX6538-A06TDFG	QFN88	AIoT, surveillance	WE2 AI processor