University of Asia Pacific

Department of Computer Science & Engineering

Lab Report

Course Title: *Digital Logic & System Design Lab.*

Course Code:CSE 210
Experiment No:05.

Experiment Name : Implement and verify SR Latch with NAND and NOR gate.

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PROBLEM STATEMENT:

Implement and verify SR Latch with NAND and NOR gate.

INSTRUMENTS:

- **NAND GATE**
- **NOR GATE**

VARIABLE:

INPUTS:S, R

OUTPUT:Q,Q`

TRUTH TABLE:

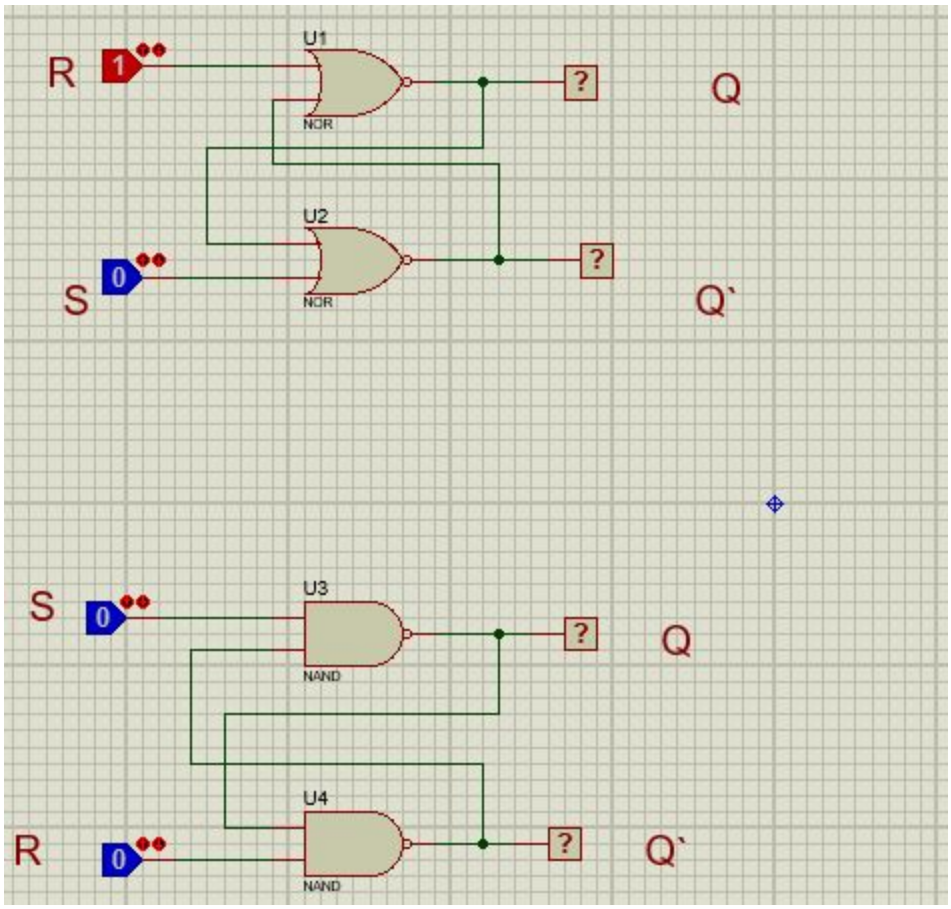
S	R	Q
0	0	Qo
0	1	0
1	0	1
1	1	Q=Q`=0

NO CHANGE
RESET
SET
INVALID

S	R	Q
0	0	Q=Q`=0
0	1	1
1	0	0
1	1	Qo

INVALID
SET
RESET
NO CHANGE

LOGIC DIAGRAM:



DISCUSSION:

We know that a flip-flop circuit consists of two inputs set(S) and reset(R), two outputs Q and Q'. A cross coupled connection is given between output of one gate and the input of the other gate. Such type of cross coupled connection constitutes the feedback path for the flip-flops. These flip-flops are called direct coupled RS Flip flops (or) SR latch.

Now before analyzing the circuit using two NOR gates, we must know the truth table of the NOR gate.

From the truth table it is evident that the output of a NOR gate is zero if any of the inputs is 1 and the output is 1 only if both the inputs of the gate is 0.

Now to analyze the circuit let us assume that the

1. SET input = 1 and RESET input = 0.

For convenience let the Set input be S and Reset input be R.

We know that if any input of NOR gate is 1 then its output is 0.

Therefore when S=1, the output of the gate corresponding to S (Gate 2 in figure) becomes 0. So Q' becomes 0. This Q' is given as an input (Cross coupled connection) along with R to the other gate. So the output of the second gate, Q becomes 1(since both R and Q' are 0).