Sohaib El-Araby Ali
Digital Desgin & Verification Engineer

+201094646362
sohibalaraby9.com
es-SohaibElaraby2025@alexu.edu.eg
GitHub Profile
LinkedIn Profile

Education

•Faculty Of Engineering Alexandria University, Alexandria *2025-2020*
Communication and Electronics Department CGPA/Percentage: 3.3
High Education

•Gamal Abd-El-Naser Secondary School, Alexandria *2020-2019*
Secondary Education CGPA/Percentage: 97.9%

Experience

•MIA Technical Team *2023-2022*
Electronics Engineer Alexandria

•Chipions Program *2024-2023*
Digital IC Member Alexandria

•IEEE SSCS Alex SC *2025-2024*
Digital IC Member Alexandria

Personal Projects

•MIPS Processor

In Verilog

- Tools & technologies used: Modelsim
- In this project, I have built all the blocks necessary for MIPS functionality and verified each block through direct testing by building a test bench for each block to ensure they meet the specifications. Finally, I built a test bench for the entire design and tested it using two programs, obtaining correct outputs.

•FIFO Memory

In Systemverilog

- Tools & technologies used: Questasim
- FIFO is a very important memory type used in many applications like UART. In this project, I built a circular FIFO with two variables to keep track of the head and the tail of the FIFO. If the head or tail reaches the end of the memory, it returns to the beginning and vice versa. There are also two variables that monitor the FIFO status: if the FIFO is empty, it prevents any read operation, and if it is full, it prevents writing to it. I also built a test bench to verify the design through direct testing.

•UART

In Systemverilog

- Tools & technologies used: Questasim, EDA Playgroun
- UART (Universal Asynchronous Receiver/Transmitter) is a hardware communication protocol used for asynchronous serial communication between devices. In this project, I built the transmitter and receiver, then built a test bench for each of them. Afterward, I connected them together and built a test bench to verify the complete system.

•ALU Testbench Based In UVM

In Systemverilog

- Tools & technologies used: Questasim, EDA Playgroun, UVM
- In this project, I applied OOP concepts and utilized the UVM structure. I transitioned from design to verification, building a comprehensive UVM test bench with a focus on reusability. In the end, it worked excellently, achieving 100% coverage.

Technical Skills and Interests

Languages: Arabic, English
Developer Tools: Modelsim, Questasim, EDA-playground
HDL: Verilog, Systemverilog
Verification Methodology: UVM(basic knowledge)
Soft Skills: Team Work, Communication Skills, Passion For Learning, Time Management
Programming Languages: C, Python
Areas of Interest: Design & Verification Of Integrated Circuits