Sohaib El-Araby Ali

Digital Design Engineer

Education

•Faculty Of Engineering Alexandria University, Alexandria *2025-2020*

Communication and Electronics Department CGPA/Percentage: 3,28

High Education Military Status: Final exemption from The army

Communication info

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Github

Graduation Project

PCIe Gen 5 MAC Layer Functional Verification (Grade: A+)

Alexandria University 2025

- Developing a UVM-based verification environment for PCIe Gen 5 physical (MAC) layer.
- Have been fully involved in the development of many components and objects in the verification environment, like Scoreboards, Monitors, Error injection sequences.
- Working on many features like Linkup, Recovery, Error injection.
- Collaborated with a team to identify and solve both design and environment bugs.
- Performing synthesis on the design.

Technical Projects

•ALU Verification Based on UVM

In SystemVerilog, UVM

– The project involved the application of OOP concepts and the utilization of UVM structure and verification principles. A complete UVM environment was developed for testing ALU functionality, incorporating all UVM structural components and a coverage collector to address all corner cases, achieving 100% functional coverage.

•UART Verification Based on UVM

In SystemVerilog, UVM

– The project involved the development of a complete UVM environment to verify the two primary components of a UART protocol design: the transmitter and the receiver. A bug was identified in the receiver's FSM that prevented correct data reception. The issue was resolved by modifying the FSM, followed by retesting to confirm functionality. The verification process achieved 99.4% coverage. This project is 100% on me

•UVM Agent For PCIe GEN 5 RX PIPE Interface

In SystemVerilog, UVM

– The project involved building a UVM agent to monitor Traning sequece one and two, analyze them, then predict the receiver's current state based on these packets and use these results to verify the the RX LTSSM FSM . This was part of my graduation project and required significant effort, studying, analytical skills, debugging skills, and a deep understanding of the specifications. This agent covers most of the state transitions of the RX LTSSM of PCIe. This project is 100% on me

•Two UVM Scoreboard For UPstream And Downstream PCIe GEN5 devices

In SystemVerilog, UVM

– These 2 scoreboards check the type and number of ordersets TS1, TS2, IDLE, EIOS sent and whether they are compatible with the current state and whether the next state to which it will be transferred is correct according to the above. All possible possibilities such as time out and other cases were considered. Each scoreboard serves both the receiver and the transmiter. This project is 100% on me.

•Single Cycle 32-bit RISC V (RV32I) Microprocessor

In SystemVerilog

– The project focused on studying the RISC-V instruction set architecture, designing an architecture to support all integer instructions, developing RTL code for the RV32I architecture, and verifying its functionality through direct testing. This project enhanced personal knowledge of Computer Architecture. This project is 100% on me

•Single Cycle 32-bits MIPS Microprocessor Design

In Verilog

– The project involved designing and implementing all blocks required for MIPS functionality, with each block verified through direct testing using individual testbenches to ensure compliance with specifications. In this project, studying Computer Architecture was essential. A comprehensive testbench was then developed for the entire design, and functionality was validated using two programs, producing correct outputs. This project is 100% on me

•UART Design

In SystemVerilog

– UART (Universal Asynchronous Receiver/Transmitter) is a hardware communication protocol used for asynchronous serial communication between devices. The project involved designing and implementing the transmitter and receiver, followed by the development of individual testbenches for each. Subsequently, the transmitter and receiver were interconnected, and a comprehensive testbench was created to verify the complete system. This project is 100% on me

•Circular FIFO Memory Design

In SystemVerilog

– FIFO is a critical memory type used in various applications, such as UART. The project involved building a circular FIFO with two variables to track the head and tail positions. When the head or tail reaches the end of the memory, it wraps around to the beginning. Two additional variables monitor the FIFO status: one prevents read operations when the FIFO is empty (underflow), and the other prevents write operations when the FIFO is full (overflow). A testbench was developed to verify the design through direct testing. This project is 100% on me

Academic Courses

1- Programming 1 2- Digital Logic 1 3- Digital Logic 2 4- Electronics 1 5- Electronics 2
6- Solid Devices 7- Digital IC 8- VLSI 9- Computer Architecture 10- Operating Systems
11- Data Structures 12- Micro Processors

Technical Skills and Interests

Languages: Arabic (Native Speaker), English (Very Good)
Developer Tools: Modelsim, Questasim, EDA-playground
Good Knowledge at HDL: Verilog, Systemverilog, VHDL
Good Knowledge at Verification Methodology: UVM
Good knowledge at: SVA, CDC, STA, OOP, Computer Architecture, PCIe, MIPs Architecture, RISC V Architecture, UART, Operating System, VLSI
Good Knowledge at: Supervised Machine Learning, Neural Network, Convolutional Neural Network
Soft Skills: Team Work, Communication Skills, Passion For Learning, Time Management
Operating Systems: Linux Operating System, Windows
Programming Languages: C Programming, Python
Areas of Interest: Design & Verification Of Digital Integrated Circuits

Experience

•MIA Technical Team *1 year*

Electronics Engineer Alexandria

– Responsible for creating Python scripts to automate regular software tasks, as well as developing Python machine learning models and computer vision models.
– Also responsible for designing the entire hardware system of the ROV and all related PCB circuits.
– Additionally, participated in the MATE ROV regional competition, where The team won 3rd place.

•IEEE SSCS Alex SC *1 year*

Member Alexandria

– A member of the IEEE SSCS Alex SC Digital IC subteam.

•Verification Diploma

2 months

– Studied for 2 months a verification diploma under the supervision of Eng.Sherif Hosny. Through this diploma I studied SystemVerilog, SystemVerilog OOP, SVA, and UVM.