Soham Nivargi

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Electrical Engineering, Dual Degree
Indian Institute of Technology Bombay

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Pursuing a **minor** degree in **Computer Science and Engineering**, IIT Bombay

Scholastic Achievements

- Acquired an **All India Rank 769** out of 150 thousand candidates who appeared for **JEE Advanced** exam *[2021]*
- Secured an **All India Rank 454** out of **1.5** million candidates who appeared for **JEE Mains** exam *[2021]*
- Awarded Kisore Vaigyanik Protsahan Yojana **(KVPY)** fellowship by IISC with **All India Rank 374** *[2021]*
- Attained **Maharashtra State Rank 37** (**99.98** percentile) in MHT-CET engineering entrance exam *[2021]*
- Cleared NSEP and qualified and appeared for the **second level** of **InPHO** (International Physics Olympiad) *[2021]*

Professional Experience

Embedded Software Intern | Texas Instruments Inc. *[May'24 - July'24]*

Summer Intern | Guide: Vaishnav Achath

SMMU Support on Xen Hypervisor

- Analysed the **boot process** of bootloader and linux kernel on **ARM processors** on **j721e-evm processor boards**
- Assesed the boot flow of **U-boot bootloader** and **Ti-linux-kernel** and integrated **Xen hypervisor** boot process after U-boot to implement **parallel boot** of two **paravirtualized linux domains** based on the **device tree** parsed
- Achieved the same setup on **Synopsys VDK Elite Simulator** which consists of a **TDA5 SoC** with **ARM System Memory Management Unit**, by modifying the **configuration source** to include Xen hypervisor and linux domains
- Summarized **ARM SMMUv3 architecture** and its use case in Xen hypervisor and kernel **DMA transactions**

JIRA Cross-Referencing Tool

- Developed a tool in **Python** for cross-referencing JIRA issues to its **test results**, for internal use, for **organized analysis** of **requirement status** and its **testcases** per **platform release** scalable with **multiple platforms' support**
- Grouped all **requirements linked to a feature** which is a **subset of an IP** and the tool **summarizes** in a **structured format** where it elaborates all **requirements' test status** linked to the feature, for **every feature** of **each IP**
- Designed algorithm to **import all issues** from JIRA, and **auto-map** the currently **untracked requirements** to their **respective feature and IP**, to the **platform(s)** of the requirement, by **matching sequences** of requirement titles

Key Projects

Image Cartoonifier | WnCC Summer of Code *[May'23 - July'23]*

Summer of Code, 2024 | Web and Coding Club, IIT Bombay

- Trained a deep learning model with multiple hidden layers to **recognize digits** using the **digit recognizer dataset**, applying **forward propagation, backward propagation** and **gradient descent** using only **NumPy** & **Pandas**
- Reviewed the research paper on **Neural Algorithm of Artistic Style** which focuses on **content reconstruction** and **style reconstruction**, employing deep learning techniques that utilizes a **cost function** that blends both reconstructions

EEG Recording System | EE344 Electronic Design Lab Project *[Feb'24 - April'24]*

Guide: Prof. Siddharth Tallur | IIT Bombay

- Steered a team of four to design a **16-channel EEG** recording system consisting of passive filters and electro-static discharge circuit for **filtering**, voltage regulators for generation of required voltage levels and a **8-channel Analog-to-Digital Converter (ADC) integrated chip**, with in-built **amplifier**, **low-noise filtering** and **bias correction** capibilities
- Assembled the **circuit schematic** and completed **routing** connections in **KiCAD** for the **breakout board**
- Used **SPI protocol** to **send/receive commands** and **data** between the ADC and **STM32 Nucleo** development board

IITB-RISC-Superscalar | EE739 Course Project *[Nov'23 - Dec'23]*

Guide: Prof. Virendra Singh | IIT Bombay

- Designed a multi-purpose, versatile **16-bit out-of-order processor**, leveraging a 2-way fetch pipeline within **superscalar architecture** to exploit **parallelism** and advanced out-of-order execution capabilities for efficient **resource utilization**
- Engineered an efficient **reservation station** that **holds instruction-specific data**, dynamically based on availability
- Devised a resilient design for the **register file** and **register alias table**, adeptly managing any WAR, RAW, WAW dependencies that emerge due to the **out-of-order dispatch** and subsequent **in-order reorder buffer** execution
- Integrated a streamlined **datapath** that incorporates the **2-way fetch process**, **reservation station**, **reorder buffer**, **register file**, and **execution pipelines**, capitalizing on the inherent parallelism offered by the superscalar architecture

Multi-Band Pass Filter Design | EE338 Course Project *[Feb'24 - April'24]*

Guide: Prof. Vikram Gadre | IIT Bombay

- Designed a series of **discrete time filters** for extraction of **specific frequency bands** of an analog signal with prescribed filter **output specifications** of sampling rate, transition band width, passband tolerance, and stopband tolerance
- Employed either the **Butterworth, Chebyshev or Elliptic approximation** to design the **IIR discrete time filters**
- Utilized the **Kaiser Window Function** with optimum parameters to design the **FIR discrete time filters**

Lung Cancer Detection | EE769 Course Project *[March'24 - April'24]*

Guide: Prof. Amit Sethi | IIT Bombay

- Developed a deep **convolutional neural network classifier** with a **pre-trained model** as the **backbone**, trained on a lung cancer type dataset with 3 classes while **freezing** the higher level weights of the pre-trained model
- Analysed **model accuracies** on **ResNet50, VGG16, and MobileNet** as pre-trained model backbones in **TensorFlow**

IITB-RISC-Pipelined | EE309 Course Project *[Apr'23 - May'23]*

Guide: Prof. Virendra Singh | Course: Microprocessors | IIT Bombay

- Designed a functional, multi-purpose **16-bit RISC processor** with **pipelined architecture** and **MIPS ISA**
- Developed a **6-stage pipeline**, including stages such as Instruction Fetch, Instruction Decode, Register Read, Execute, Memory Access, and Writeback, to enhance instruction processing **throughput** and maximise **cycle frequency**
- Implemented advanced features, such as a 2-level **data forwarding logic** and a **history bit-based branch predictor**, to **minimize data hazards** and **improve branch prediction** accuracy, ensuring smooth operation without stalls

Modified-Mini-8085 | EE309 Course Project *[Apr'23]*

Guide: Prof. Virendra Singh | Course: Microprocessors | IIT Bombay

- Employed hardware flow-chart methodology to meticulously design a **16-bit CISC** microprocessor similar to **Intel 8085**
- Designed the **data-path** for a comprehensive set of **18 instructions**, crafting control store through microcode architecture

Bubble Trouble | CS101 Course Project *[Mar'22]*

Guide: Prof. Parag Chaudhari | Course: Computer Programming | IIT Bombay

- Utilized **Object Oriented Programming** using efficient **C++** libraries to analyze the score and time variables
- Implemented 3 levels of difficulty and a user friendly interface using **Simplecpp** to enhance the gaming experience

Position of Responsibility

Media Secretary | Electrical Engineering Students' Association *[Oct'22 - Apr'23]*

Department of Electrical Engineering | IIT Bombay

- Responsible for the **photography and videography** duties along with photoshop & **collage-making** requirements
- Coordinated with the department council to ensure seamless execution of numerous **EESA** events

Media Manager | Core Team Member, Impulse, IIT Bombay *[Mar'23]*

Department of Electrical Engineering | IIT Bombay

- Handled the **digital marketing** responsibilities of the first ever **Impulse**, the Electrical Engineering Department Fest
- Managed the **social media** accounts of **Instagram** & **LinkTree** of Impulse and EESA to effectively market the fest

Key Courses Undertaken

Electrical Engg	Digital Systems, Microprocessor, Advanced processor Design, VLSI Design, Analog Circuits, Control Systems, Digital Signal Processing, Power Engineering, Electronic Devices & Circuits, Communication Systems, EM Waves
Computer Science	Computer Programming, Data Structures & Algorithms, Design & Analysis of Algorithms, Automata Theory
Mathematics & ML	Calculus, Linear Algebra, Probability & Random Processes, Differential Equations, Complex Analysis, Markov Chains & Queuing Systems, Online Learning & Optimization, Introducing to Machine Learning

Technical Skills

Programming	Python | C++ | LaTeX | VHDL | Verilog | Assembly | C | Bash
Python Libraries	Tensorflow | Pytorch | Pandas | Matlplotlib | Scikit-Learn | Numpy | OpenCV
Software	Quartus | GNU Radio | Keil μVision Studio | NGSpice | Arduino | Matlab

Extracurriculars

- Mentored 6 students on **Data Structures and Algorithms** for **Summer of Science** organized by MnP Club *(2023)*
- Secured **2nd Runner-Up** trophy in RC Plane Competition held by the **Aeromodelling Club**, IIT Bombay *(2022)*
- Completed **1** year of **professional** basketball training under **NSO** (National Sports Organisation), IIT Bombay *(2021-22)*
- Represented **district basketball** team under Solapur District Basketball Association for 3 consecutive years *(2017-19)*
- Clinched **1st** position in the **District** level Basketball Championship (Inter School) in a team of 12 players *(2017)*
- Innovated a **RC Car** in the **Robotics summer camp** conducted by Robotics and Aeromodelling Club, Solapur *(2016)*