COMPARATIVE ANALYSIS OF LOW POWER FULL ADDERS

Project report submitted in partial fulfilment of the requirements for the degree of Bachelor of Electronics and Telecommunication Engineering

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Certificate

This is to certify that the project report entitled "**Comparative analysis of low power full adder "** submitted by **Soham Mondal** , **Mukesh Kumar Shaw** and **Suraj Bhagat** for the partial fulfilment of the degree of Bachelor of Electronics and Telecommunication Engineering of Jadavpur University is based on their assigned project work during the session 2018-2019 under the guidance of **Dr. Chandrima Mondal** of **Electronics and Telecommunication Engineering Department** of **Jadavpur University**, Kolkata, West Bengal, India.

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ABSTRACT

Addition is one of the common and widely used fundamental arithmetic operation in many VLSI systems. Other similar arithmetic operations are subtraction, multiplication, division, address calculation etc. Using binary adders, the full adder is designed and improving 1-bit full adder performance plays an important role in VLSI. Different varieties of full adders exploit completely different logic designs and technologies, which are reported. Nanometre range devices face the problem of hot carrier effects and other short-channel effects. In order to maintain speed, threshold voltage must be scaled down, but doing so standby current increases, which in turn implies that static power is the main contributor to total power and thus should be taken care of properly. A brief study is done about the existing 28T,16T,14T,10T transistors using 180nm technology node in T-spice and Power, Delay and Power Delay Product (PDP) is analysed using 1.8V as supply voltage. In terms of Power Delay Product, we observe 28T full adder has more power and delay and PDP compared to 16T, 14T, 10T full adders, because a greater number of transistors results in high input loads, more power consumption. Next, we explore complementary MOS logic in 90nm technology node, complementary pass transistor full adder involving pass transistor logic, the hybrid CMOS logic full adder, ultra-low power full adder using Ultra low power diode and XOR and XNOR gates, hybrid full adder using semi XOR and XNOR logic and Gate Diffusion Input-multiplexer full adder. Power delay product (PDP) is analyzed for these transistors at various supply voltages starting from 0.9 volt to 1.2 volt. Hybrid full adder using semi XOR and XNOR logic has the highest power delay product because of high power dissipation. The complementary pass transistor and ultra-low power full adder logic styles has more or less the same power delay product profile for the entire range of supply voltages. The complementary MOS logic full adder and gate diffusion input multiplexer full adder has the overall least power delay product profile. For supply voltages from 0.9 volt to 1 volt we can go for gate diffusion input multiplexer logic full adder and for supply voltages from 1 volt to 1.2 volt we can go for conventional complementary MOS logic.

TABLE OF CONTENTS

Chapter 1

INTRODUCTION & RELATED WORK

1.1) Overview

Addition is one of the common and widely used fundamental arithmetic operation in many VLSI systems. Other similar arithmetic operations are subtraction, multiplication, division, address calculation etc. Using binary adders, the full adder is designed and improving 1-bit full adder performance plays an important role in VLSI. In this chapter we have introduced why we need low power adders in general.

1.2) Introduction

The explosive growth in laptops and portable systems and in cellular networks has intensified the research efforts in low power microelectronics. In present day there is an ever-increasing number of portable applications requiring low-power than ever before. For example, note book and laptop computers, representing the fastest growing segment of the computer industry, are demanding the same computation capabilities as found in desktop machines. Therefore, circuits with low-power consumption become the major candidates for design of systems.

Most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. Addition, subtraction, multiplication, and multiply and accumulate (MAC) are examples of the most commonly used operations. The 1-bit full-adder cell is the building block of all these modules. Thus, enhancing its performance is critical for enhancing the overall module performance. The most important performance parameters for future VLSI systems are speed and power consumption.

There are three main components of power consumption in digital CMOS VLSI circuits. 1) Switching Power: consumed in charging and discharging of the circuit capacitances during transistor switching. 2) Short-Circuit Power: consumed due to short-circuit current flowing from power supply to ground during transistor switching. 3) Static Power: consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits [2], [3]. It depends on the input pattern applied to the circuit, which will either cause the transistors to switch (circuit capacitances consume power) or to keep their previous state (no power consumption) at each clock cycle. The third component is usually negligible in a well-designed CMOS circuit [3].

The total power is given by the following equation [4]:

$P_{total} = V_{dd} * f_{clk} * \Sigma_i V_{swing} * C_{load} * p_i + V_{dd} * \Sigma_i I_{i\,sc} + V_{dd} * I_l$

where

V_{dd} - power supply voltage;

V_{swing} - voltage swing of the output which is ideally equal to V_{dd};

C_{load} -load capacitance at node i;

F_{clk} system clock frequency; pi switching activity at node i;

$I_{i\,sc}$ short-circuit current at node i;

I_l leakage current.

The summation is over all the node capacitances of the circuit. With the constant increase in systems' clock frequency, designing systems with low power consumption is not a straightforward task, as it involves different system abstraction levels. Beginning from system behavioural description and ending with fabrication process and packaging, all the steps can be tailored toward low power design.

1.3) Related Work

A 16-transistor CMOS 1-bit full-adder cell is presented in [1]. It uses the low-power designs of the XOR and XNOR gates, pass transistors, and transmission gates. Energy savings up to 30% are achieved.

A low power and low transistor count static energy recovery full adder (SERF) is presented in [5]. It uses 10 transistors in total.

Two low-power 1-bit Full Adder cells are presented in [6]. Both of them are based on majority-not gates. The first cell is only composed of input capacitors and CMOS inverters, and the second one also takes advantage of a high-performance CMOS bridge circuit.

Novel direct designs for 3-input exclusive-OR (XOR) function at transistor level are presented in [7]. These designs are appropriate for low-power and high-speed applications. The critical path of the presented designs consists of only two pass-transistors, which causes low propagation delay.
Majority function-based 1-bit full adder is given in [8] that uses MOS capacitors (MOSCAP) in its structure. It can work reliably at low supply voltage. In this design, the time consuming XOR gates are eliminated.

In this paper [9] the main topologies of one-bit full adders, including the most interesting of those recently proposed, are analysed and compared for speed, power consumption, and power-delay product. The most interesting implementations in terms of trade-off between power and delay are the traditional CMOS and Mirror topologies. Moreover, the Dual-rail Domino and the CPL allow the best speed performance.

A new hybrid style full adder circuit is presented in [10]. The sum and carry generation circuits of the proposed full adder are designed with hybrid logic styles. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem.

In [11] the adder cell is anatomized into smaller modules. This type of approach is the first of its' kind. The modules are studied and evaluated extensively. A library of full-adder cells is developed and presented to the circuit designers to pick the full-adder cell that satisfies their specific applications.

This paper [12] presents a novel low-power multiplexer-based 1-bit full adder that uses 12 transistors (MBA-12T). In addition to reduced transition activity and charge recycling capability, the circuit has no direct connections to the power-supply nodes, leading to a noticeable reduction in short-current power consumption.

Comparisons are performed on more efficient CMOS circuit realizations and CPL logic styles in [13] and a wider range of different logic cells, as well as the use of realistic circuit arrangements demonstrate CMOS to be superior to CPL in most cases with respect to speed, area, power dissipation, and power-delay products.

Hybrid-CMOS design style utilizes various CMOS logic style circuits to build new full adders with desired performance. This provides the designer a higher degree of design freedom to target a wide range of applications, thus significantly reducing design efforts. Hybrid-CMOS full adders are classified into three broad categories based upon their structure in [15]. The full adder in this paper is based on a novel XOR–XNOR circuit that generates XOR and XNOR full-swing outputs simultaneously.

Exclusive-OR and exclusive-NOR gates are important in digital circuits. This paper [16] proposes a new set of low power 4-transistor XOR-XNOR gates.

In this paper [17], a new structure of a hybrid full adder, namely, the branch-based logic and pass-transistor (BBL-PT) cell is proposed, which is implemented by combining branch-based logic and pass-transistor logic. Evolution of the proposed cell from its original version to an ultralow-power (ULP) cell is described. Quantitative comparisons of the optimized version, namely, the ULP full adder (ULPFA), are carried out versus the BBL-PT full adder and its counterparts in two well-known and commonly used logic styles, i.e., conventional static CMOS logic and complementary pass logic (CPL), in a 0.13- m PD SOI CMOS with a supply voltage of 1.2 V, demonstrating power delay product (PDP) and static power performance that are more than four times better than CPL design.

In [18] SOI vs bulk technology MOSFET is studied and analysed. Basic architecture of ULP and ULP diode is given and also their basic applications in implementing basic analog functions. Then there is a brief study as to why we should be going for ULP.

Two new methods are proposed in [19] to implement the exclusive-OR and exclusive-NOR functions on the transistor level.

In [20] two new symmetric designs for Low-Power full adder cells featuring GDI (Gate-Diffusion Input) structure and hybrid CMOS logic style is presented. The main design objectives for these adder modules are not only providing Low-Power dissipation and high speed but also full-voltage swing. In the first design, hybrid logic style is employed. The hybrid logic style utilizes different logic styles in order to create new full adders with desired performance. This provides the designer with a higher degree of design freedom to target a wide range of applications, hence reducing design efforts. The second design is based on a different new approach which eliminates the need of XOR/XNOR gates for designing full adder cell and also by utilizing GDI (Gate-Diffusion-Input) technique in its structure, it provides Ultra Low-Power and high-speed digital component as well as a full voltage swing circuit.

Gate diffusion input (GDI)—a new technique of low-power digital combinatorial circuit design is described in general here [21]. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design.

1.4 Organization of Report

Thesis can be organized in the following manner.

- Chapter 2 includes theoretical background of 28 transistor ,16 transistor, 14 transistor, 10 transistor full adders. It also explains CMOS logic full adder, complementary pass transistor logic full adder, hybrid full adder, Ultra low power full adder, hybrid full adder using semi XOR and semi XNOR, their detailed theory and Gate diffusion input full adder.
- In Chapter 3 , the power dissipation, propagation delay and power delay product of 28T,16T,14T,10T transistor full adder designs are analysed and compared using simulation at 180nm technologies at a supply voltage of 1.8V. CMOS, CPL, hybrid CMOS, ULPFA, hybrid CMOS using semi XOR and semi XNOR logic and GDI Mux full adder are analysed and their power delay product are compared for supply voltages ranging from 0.9V to 1.2V in 90nm technology node.
- Chapter 4 contains observations and concluding remarks.

Chapter 2

THEORETICAL BACKGROUND

2.1) 28T FULL ADDER:

The conventional CMOS adder cell using 28 transistors based on standard CMOS topology is shown in below Fig. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. However, using inverters on the output nodes decreases the rise-time and fall-time and increases the driving ability. It functions well at low power supply voltages because it does not have threshold loss problem.

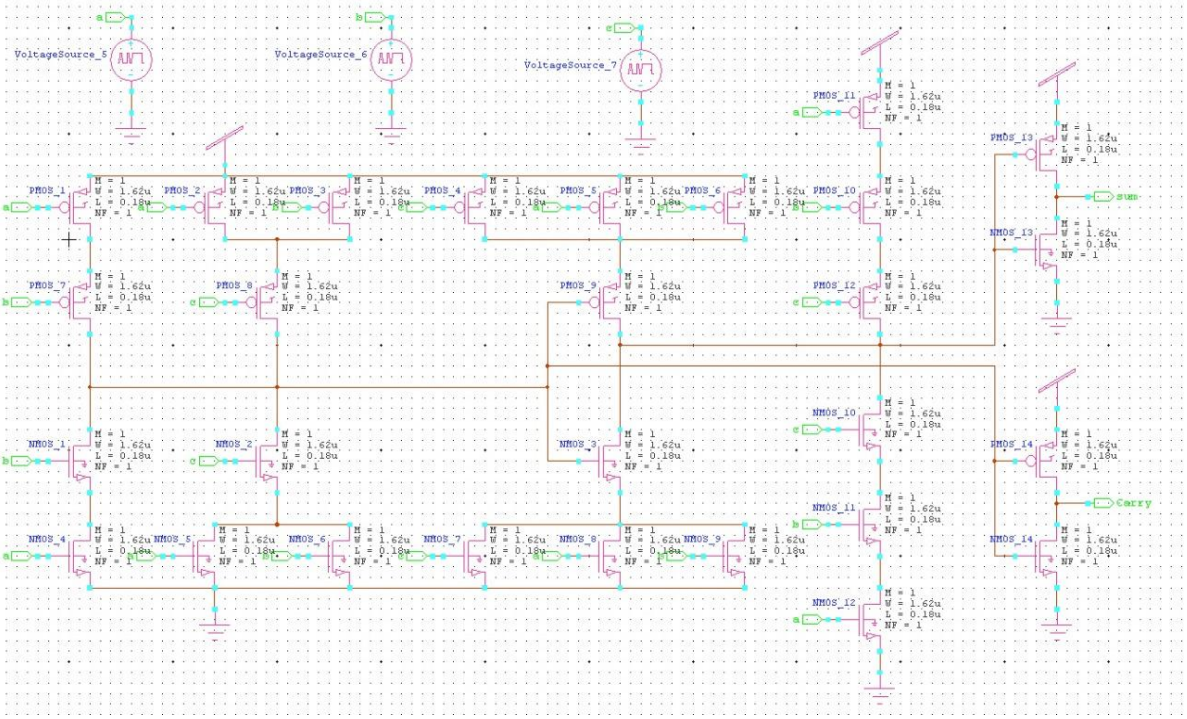

Fig-2.1 Schematic of 28T transistor

2.2) 16T FULL ADDER

The adder cell has 16 transistors. Lower power and delay have been obtained at the expense of 2 additional transistors [1]. It is based on the 4-transistor implementations of the XOR and XNOR functions pass transistor, and transmission gates. It has incomplete voltage swing at H when (A = 0, B = 0) and incomplete voltage swing at H' when (A = 1, B = 1) which account for less dynamic power consumption at those nodes. Also, it has less load capacitance at node H, since it is driving fewer loads than all other designs, which provides additional savings in dynamic power.

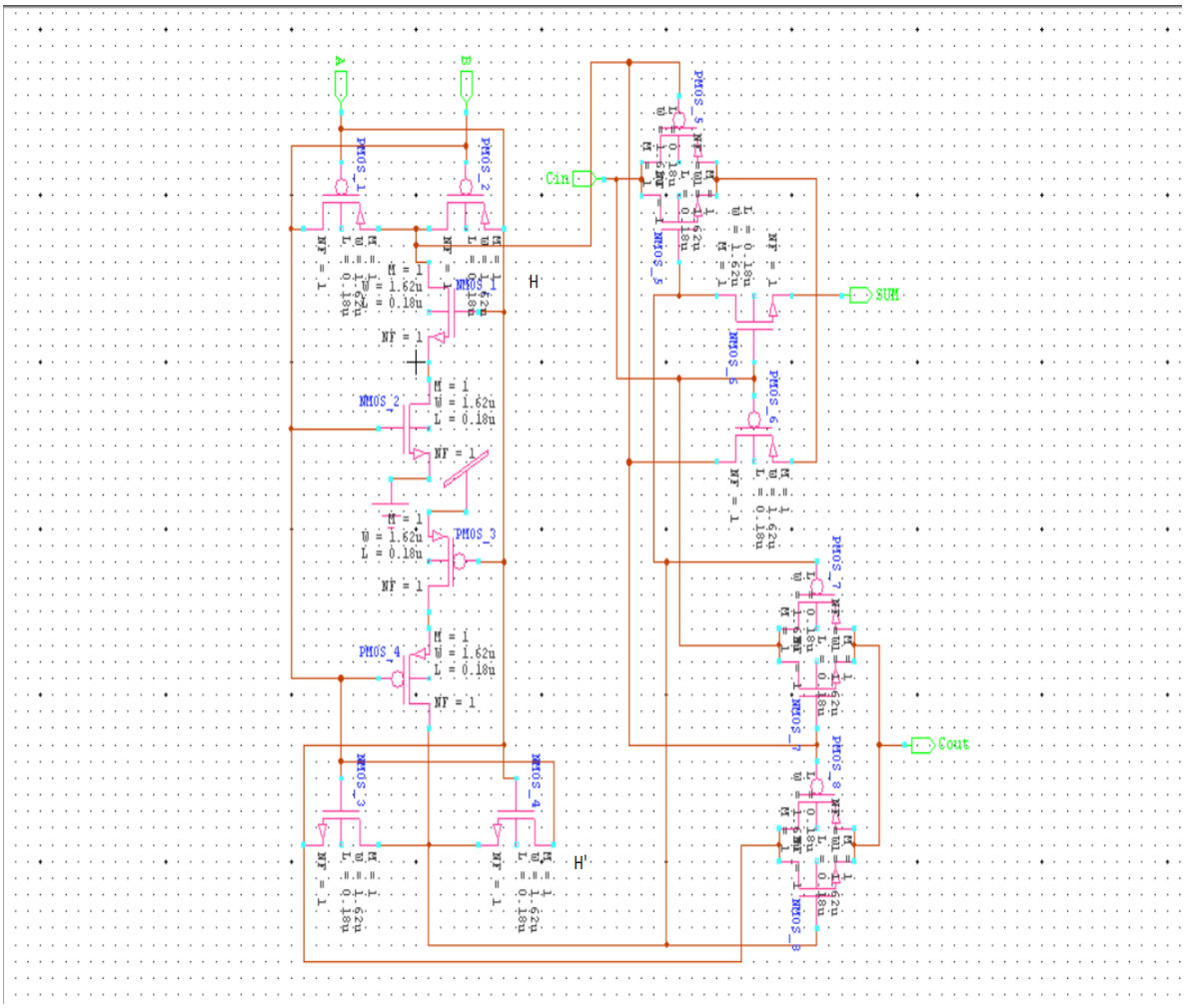

Fig-2.2 Schematic of 16T transistor

2.3) 14T FULL ADDER

One of the recent enhancements is the 14-transistors adder (14T). Power consumption has been reduced by using the 4-transistor XOR implementation presented in [16], which decreases the overall cell transistor count to 14. 14T uses only one inverter, but it has the same problem of glitches in the outputs. Also, it has the drawback of introducing a static power component at the inverter output. Due to the incomplete voltage swing of the XOR gate when A = B = 0, both the N and P transistors will be ON (N is weakly ON), which will lead to drawing current from the power supply although the circuit is in steady state. This drawback increases the power consumed by this cell, but still it remains a good candidate for low power applications due to having only 14 transistors. This circuit has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate sum and c_{out}. The signals c_{in} and c_{in}" are multiplexed which can controlled either by (a ⊗ b).

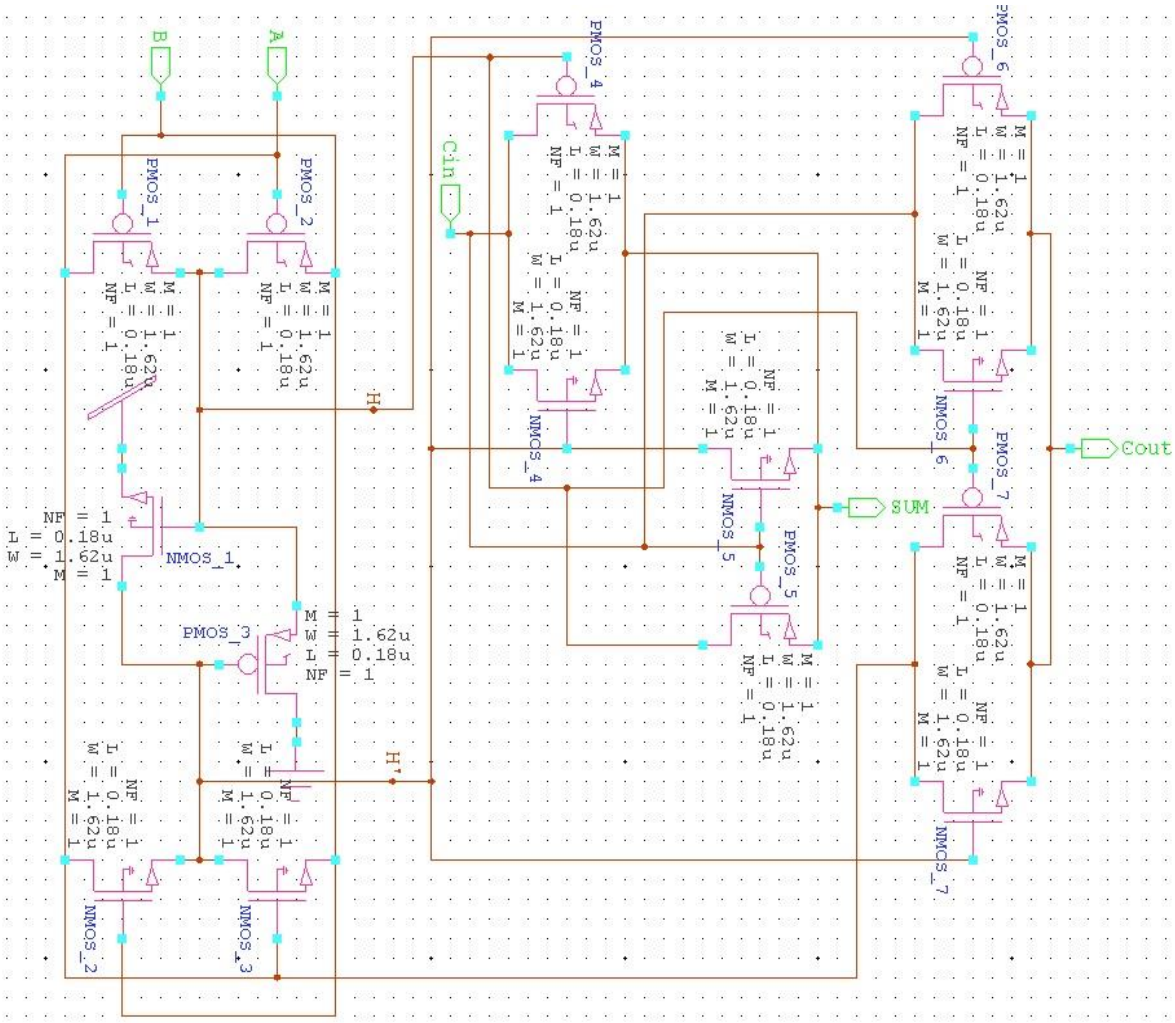

Fig-2.3 Schematic of 14T transistor

2.4) 10T FULL ADDER

SERF (Static Energy Recovery Full Adder) full adder is implemented by 10 transistors, as shown in schematic below, uses energy recovery technique to reduce power consumption . SERF use energy recovery technique to decrease the power consumption [5]. Energy recovery logics reuse charge. Therefore, it consumes less energy than the other full adders. There are some problems in this circuit. First SUM is generated from two cascaded XNOR gates (group1) which lead to long delay. Second, it cannot work correctly in low voltage. As shown in Fig.1 in the worst case, when A=B="1" there is 2Vtn threshold loss in output voltage. Therefore, logic 1 becomes equal to VDD-2Vtn in this case. The suitable operating supply voltage is limited to VDD> 2Vtn+|Vtp|. Second, there are five gate capacitances on node X. It causes to long delay in generating of intermediate A⊕ B signal and finally delay in generating SUM and COUT. This problem also increases the power.

In the 10T adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation mechanism results in faster XOR and XNOR outputs and also it balances the output delays from the SUM and CARRY output [5]. This leads to less spurious SUM and Carry signals. The output capacitance is also minimized as no inverter is connected at the output stage [5]. If the output suffers from threshold voltage loss then signal drivers can be used to reduce the degradation. The generated outputs using the driver will have same rise and fall time. This ensures better performance characteristics like faster speed, low power dissipation and driving capabilities of the circuit. If a driver is used at the output then the output voltage will have same voltage level as the supplied voltage.

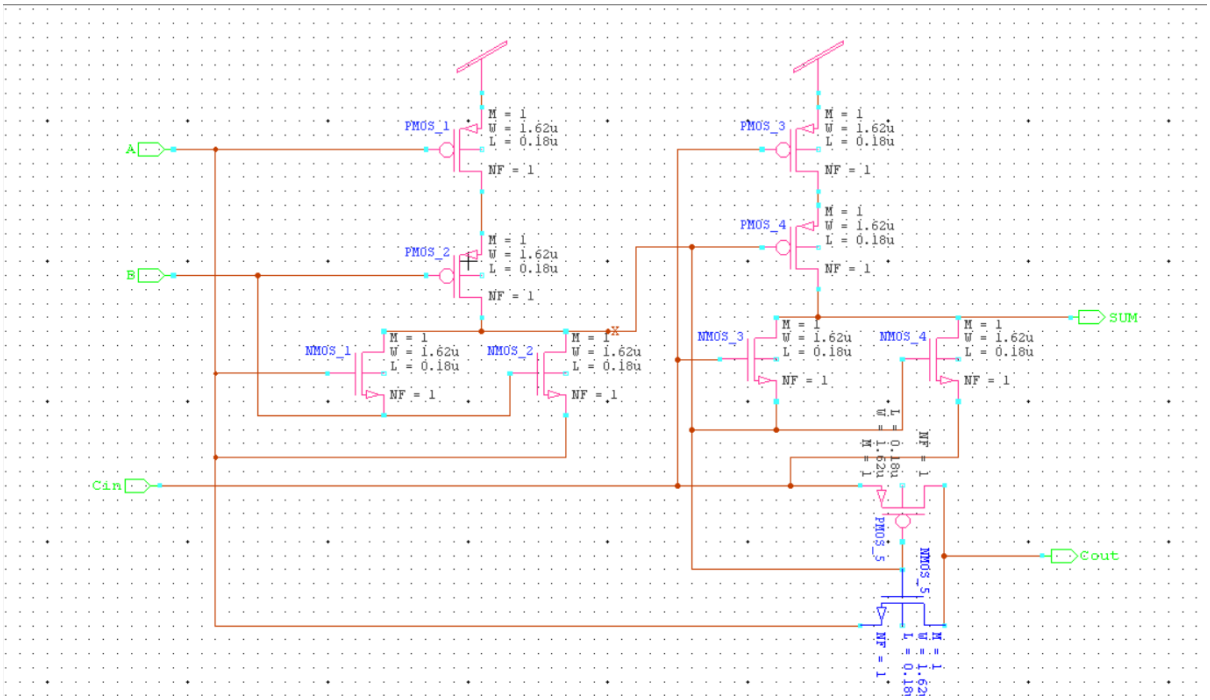

Fig-2.4 Schematic of 10T transistor

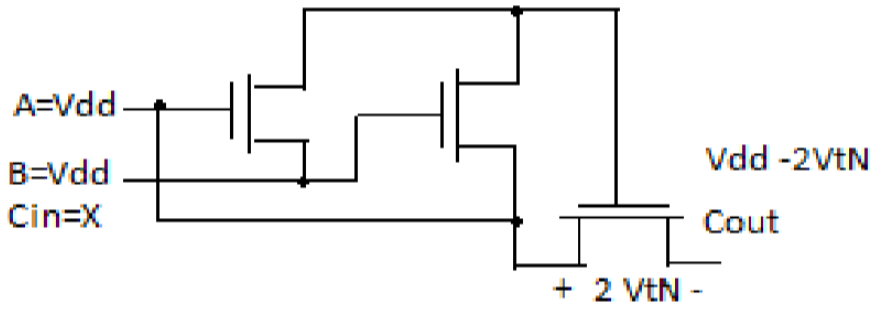

Fig-2.5 worst case of threshold loss problem in SERF full adder

2.5) Complementary CMOS Full Adder

Complementary CMOS structure is constructed using regular CMOS design consists of PMOS pull-up and NMOS pull-down transistors [10-13]. At the output stage transistors are present in series, which decrease the driving capability of the circuit. Therefore, extra buffers are required for suitable compensation. The benefit of C-CMOS style is improved quality of output in spite of transistor sizing and voltage scaling. It also gives a full voltage swing, which is needed in complex designs. More on, the layout of this design is area efficient and simple attributing to the PMOS NMOS transistor pairs and little variety of interconnecting wires.

2.5.1 Block diagram

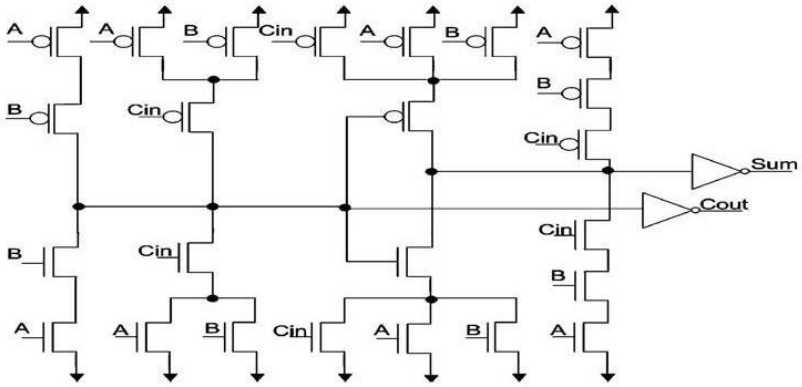

Fig-2.6 Blok diagram of C-CMOS

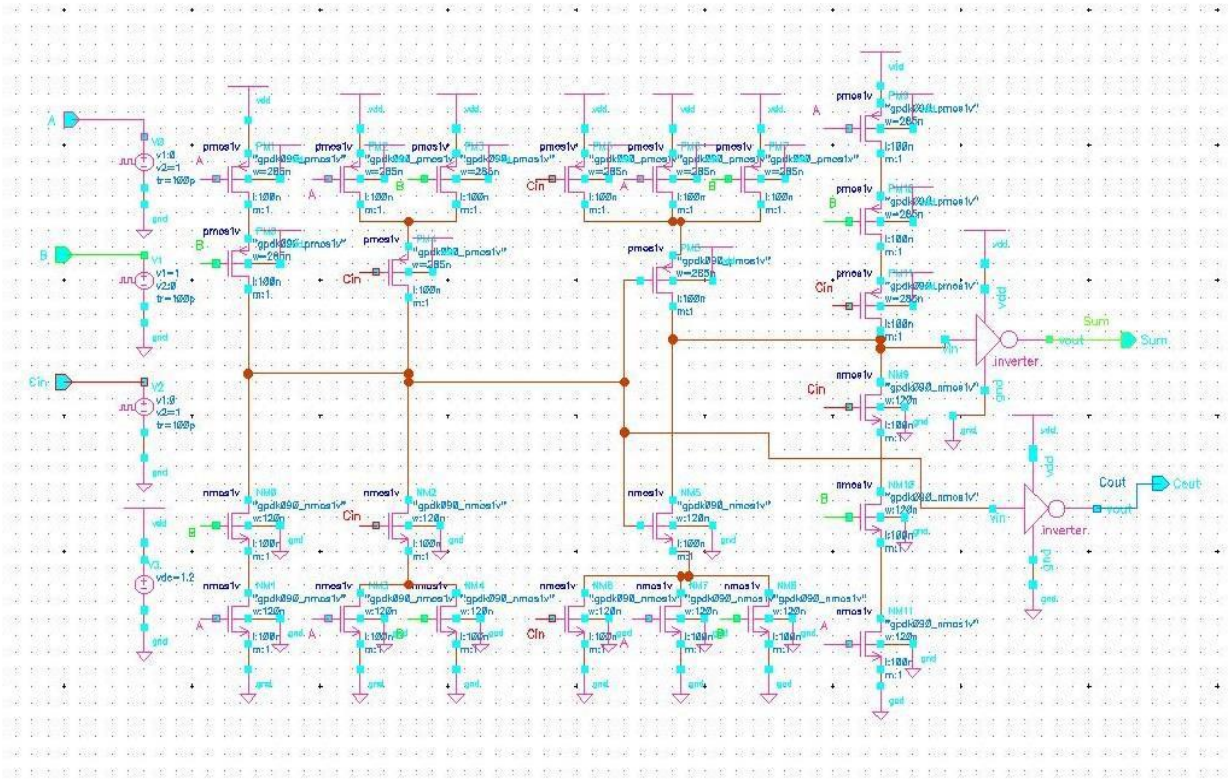

Fig-2.7 Schematic diagram of C-CMOS

2.6) COMPLEMENTARY PASS TRANSISTOR LOGIC

The complementary pass transistor logic (CPL) full adder with swing restoration [10,11,13,14] is shown below and it consists of 32 transistors with dual rail structure. The complementary transistor and pass transistor logic have some basic difference between them that is source terminal of pass transistor logic is not connected to power, instead it is connected to some input signals. Anyone of the pass transistor either PMOS or NMOS is enough to implement logic function and therefore which results in using of small input load and a smaller number of transistors. The pass transistor logic has weak driving capability because of that output inverters are used for control driving capability.

2.6.1) Block diagram

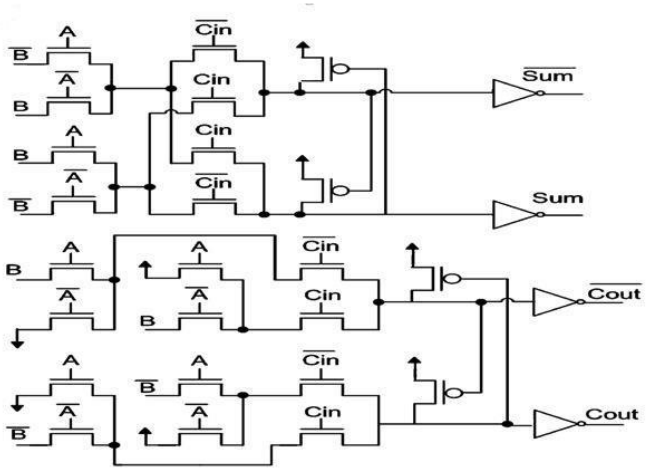

Fig-2.8 Block diagram of CPL Full Adder

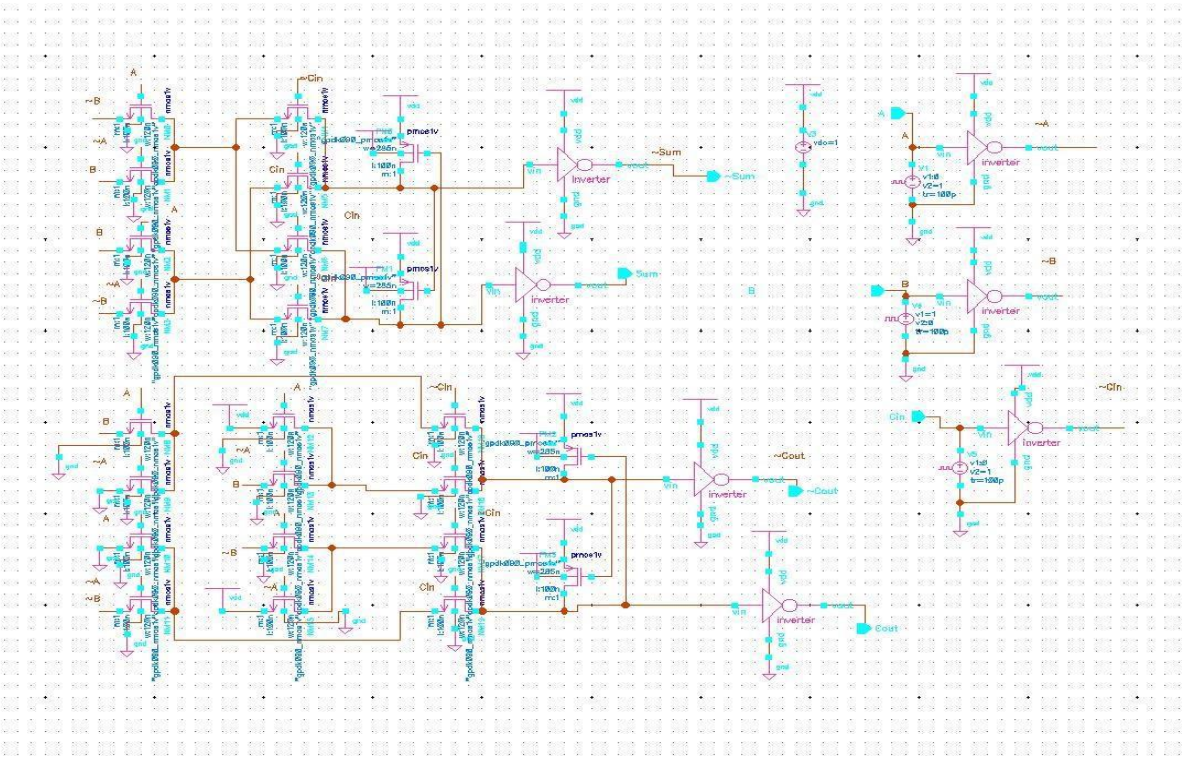

Fig-2.9 Schematic diagram of CPL Full Adder

2.7) HYBRID CMOS FULL ADDER

The design utilizes several types of CMOS logic styles to generate a design of higher efficiency shown below.
Module 1 gives fast response due to employment of only NMOS pass transistors, owing to their high mobility, for complementary pass transistor logic (CPL). However, a drawback exists to this design which is that it consumes more power due to employment of CPL designs [10, 13] and inverter. Inverter forms a sole reason for excess power consumption in static CMOS designs.

Module 3 uses an inverter and 4-transistors XOR gate. The design has been realized using pass transistor logic [16] and thus is inherently less power consuming, but decreases the driving capability [15] and hence an inverter is provided at the end to increase the drivability. But introducing an inverter implies that more power has be consumed for the working of this stage.

Module 2 gives out the sum of inputs. This module utilizes 10 transistors both in static CMOS style as well as transmission gate style, and this implies using large PMOS MOSFETs and thus consume large area. Also, the input capacitance increases because of PMOS transistors. Moreover, presence of series transistors decreases the drivability and hence an inverter has been introduced to counter this effect. But, it also increases the static power consumption.

2.7.1) Block diagram

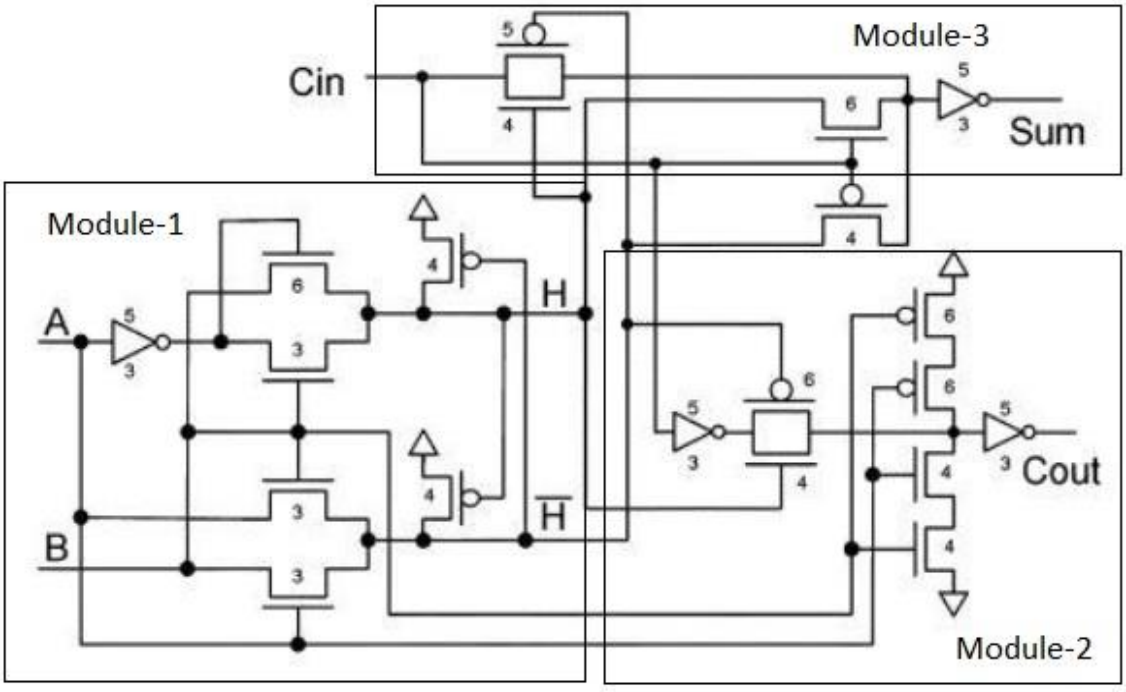

Fig-2.10 Block diagram Hybrid CMOS Full Adder

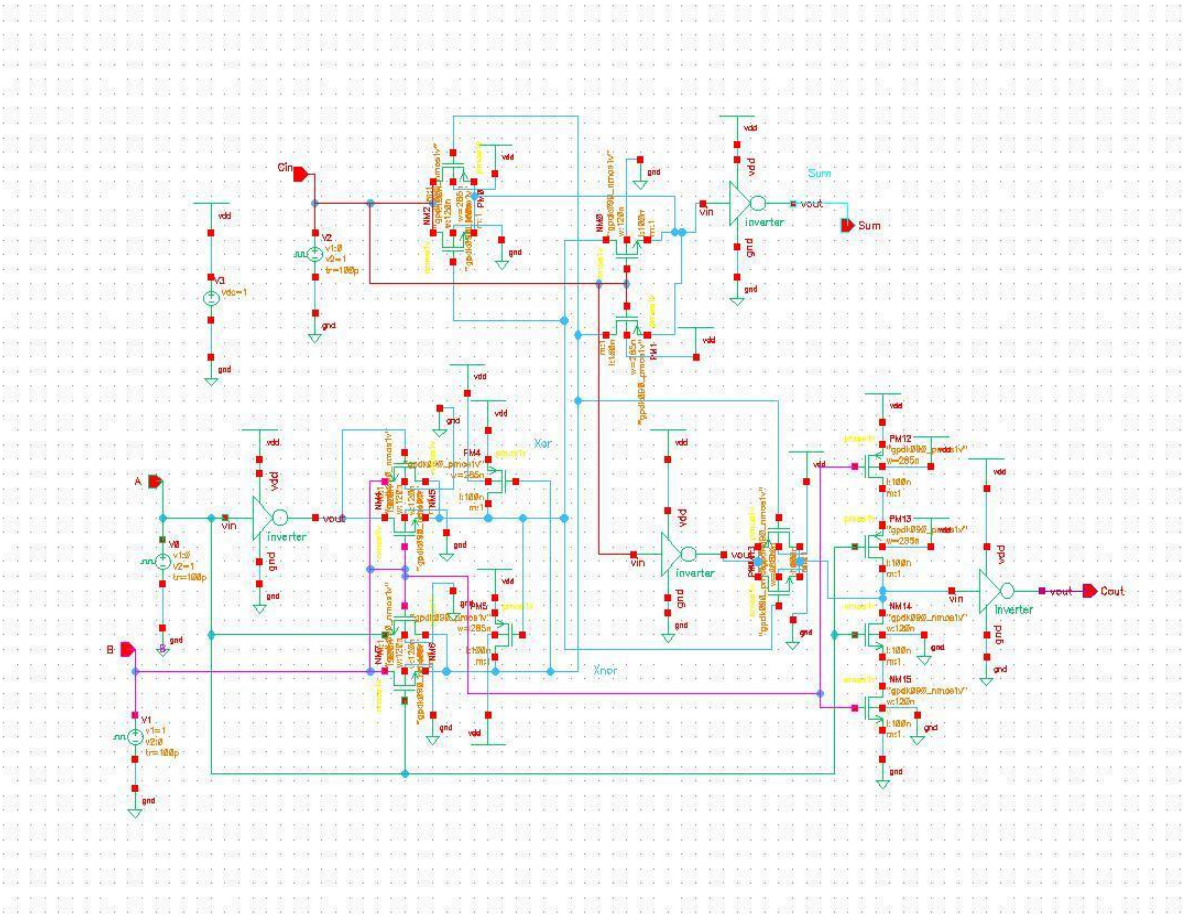

Fig-2.11 Schematic diagram of Hybrid CMOS Full Adder

2.8) ULPFA FULL ADDER

ULPFA design using CMOS logic style and pass transistor logic shown below. A unique voltage restorer ULPD has been employed in this full adder, which eliminates the need for speed compensations for full swing at outputs, provided in previous designs.
ULP diode is designed using one PMOS and one NMOS transistors, this diode provides a low leakage current when operated in reverse direction [18] .

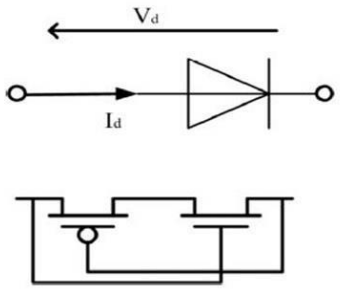

Fig-2.12 ULP diode

UPLD works as a voltage restorer due to the fact that when a large reverse bias is provided, the reverse current increases due to increased VDS, but again when a maximum value is reached, current decreases due to increased negative value of VGS. Thus, a negative resistance region is formed that can be used for level restoration. Depletion mode PMOS and NMOS transistors have to be used to ensure that in negative resistance region it give high opposite current peaks [17].
For designing a ULP full adder we need low power XOR and XNOR gates [19]. These two gates are used for implementing Sum output with pass transistor logic style and ULP diode voltage level restorer because of this the problems of delay, power dissipation and noise are eliminated. Static CMOS logic style is used for designing C_{out} circuit. This circuit design is robust against voltage scaling and sizing of transistors. Due to existence of large number of PMOS transistors it uses large space and has high input capacitance. And also, at the output series transistors create a weak driver. Moreover, to eliminate the extra inverters the inputs of the design to be inverted. This is one drawback of this design due to the combination of two different logics we get non-symmetrical and irregular layout for constructing the Sum and C_{out}.

2.8.1) block diagram

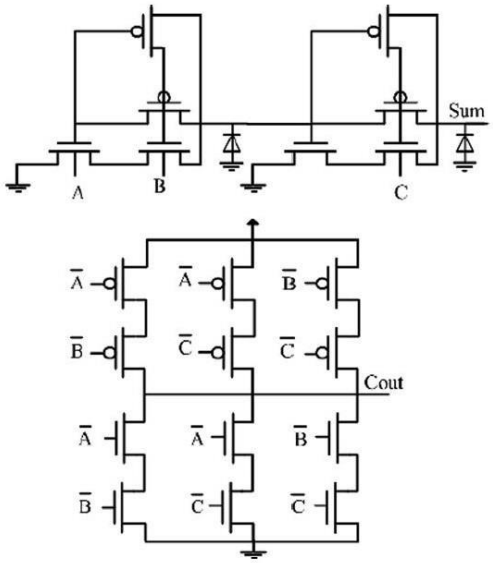

Fig-2.13 Block diagram of ULPFA Full Adder

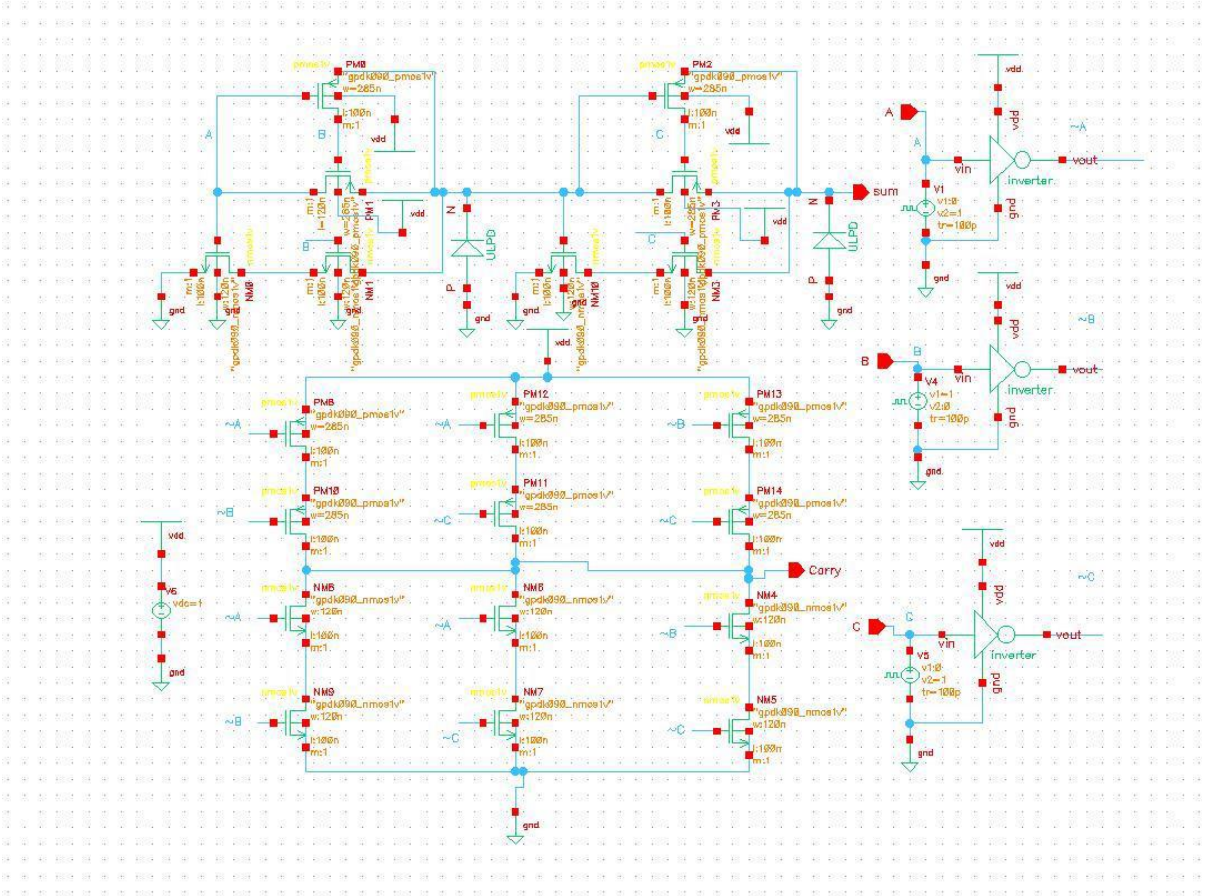

Fig-2.14 Schematic diagram of ULPFA Full Adder

2.9) HYBRID FULL ADDER USING SEMI XOR AND SEMI XNOR

This low power hybrid full adder utilizes a unique approach using Semi XOR-$XNOR$ gates . Design shows that Semi-XOR and Semi-$XNOR$ lacks to give possible outputs of normal XOR and $XNOR$ whose characteristics are provided below in table.

2.9.1) SEMI XOR-XNOR GATES

Here, a different circuit has been employed for Cout unlike the semi XOR-XNOR structure in [7] shown just below, which results in a robust and flexible low power full adder. These two gates Truth table has shown in Table-1.

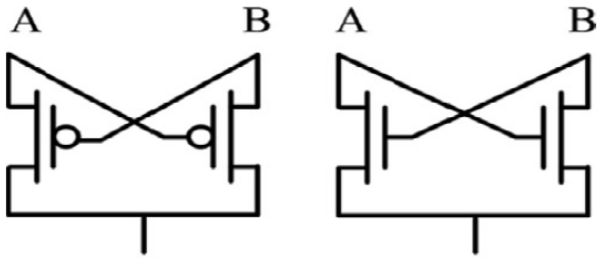

Fig-2.15 Semi XOR & Semi XNOR

Table-1:

A	B	Semi XOR	Semi XNOR
0	0	0	HZ
0	1	1	0
1	0	1	0
1	1	HZ	1

Table-2:
Truth table of sum and c_{out}

A	B	Cin	Sum	Cout	Semi-XOR	Semi-XNOR
0	0	0	0	0	0	HZ
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	HZ	1
1	0	0	1	0	0	HZ
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	HZ	1

The above-mentioned Table-2 shows that the first 4 states can be achieved by using Semi XOR gate and the remaining states can be obtained using Semi XNOR gate. Thus, using a selector, such that for C_{in} as 0, Semi XOR gate is chosen and for C_{in} as 1, Semi XNOR gate is chosen, a low power full adder using these gates can be realized.

The circuit shown below based on the explanation above works fine as long as the output does not tend towards either of the two high impedance cases. One such high impedance output can be prevented by adding an extra NMOS transistor whose source/drain is connected with input C_{in} and drain/source connected with SUM. This NMOS is switched on in the two situations when Semi XNOR gate gives an output 1, where value of SUM, in these states, becomes equal to C_{in}. Another high impedance can be removed by introducing a PMOS with its source/drain connected to SUM and drain/source to Cin. The final design for SUM is shown in below.

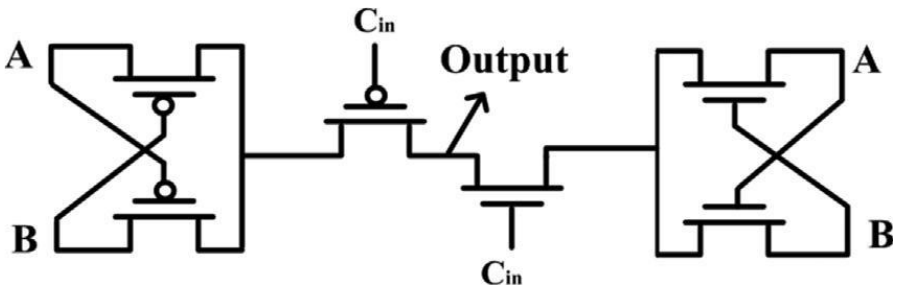

Fig-2.16 Sum generator cell with incomplete output

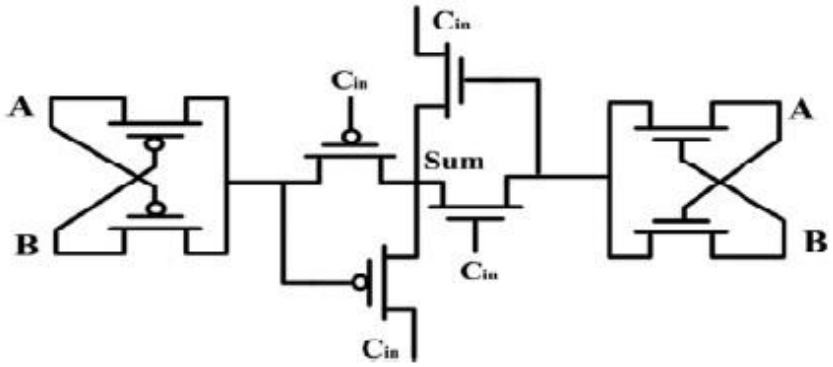

Fig-2.17 Sum generator with complete output

Now, for designing a circuit for determining Cout, Table 2 shows that first 4 states can be realized through Semi XNOR gate and the rest through Semi XOR gate, except for the two high impedance situations that arise when either both the inputs are 1s or both 0s. First in high impedance case, when both inputs are 1s can be rectified by introducing an extra NMOS with its source connected to Cout, drain to V_{dd} and gate to Semi XNOR output. The second-high impedance case, where both inputs are 0s, can be eliminated by connecting a PMOS such that its gate is connected to Semi XOR output, source to Cout and drain to Cin. Figure below shows the adder circuit without compensation for high impedance cases and the final schematic for the above explanation is shown later as complete full adder [20].

Figure below shows the utilization of ULPD at the input terminals [17,18]. This causes a full swing at the output without the requirement of output buffers, which form a main reason for static power consumption. Also, ULPD prevents any short-circuit currents owing to the fact that one part of the circuit remains off when the other part starts conducting, thereby removing any chance of direct path between V_{dd} and ground. ULPD not only prevents leakage currents but also provides good drivability which is essential in cascaded designs and other complex situations.

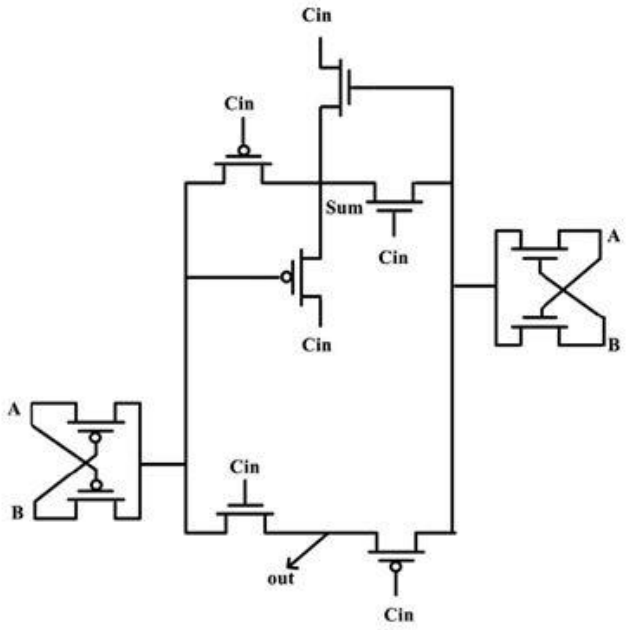

Fig-2.18 Incomplete full adder cell

This circuit is made of a smaller number of transistors that is 20 transistors compared to other circuits, and this design provides low dynamic power dissipation. This is because, lower number of transistors implies that there is less amount of switching capacitance and hence low power assimilation. Moreover, this circuit is way faster than its counterparts, because, here, the critical path contains only two transistors which drive the output.

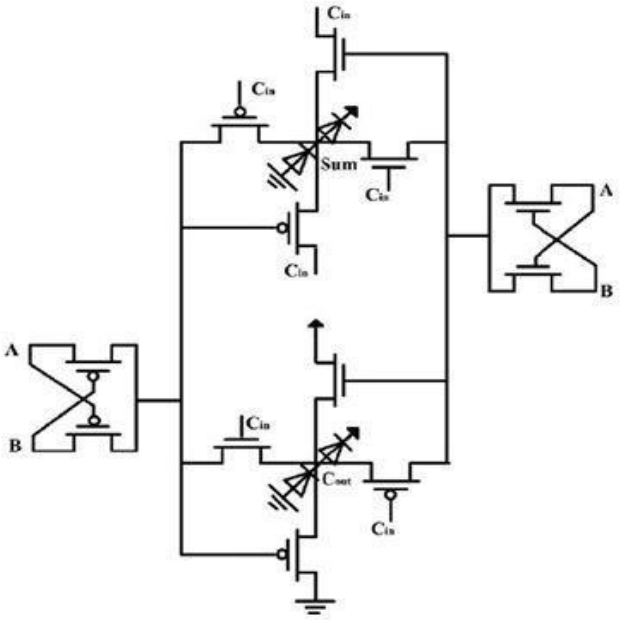

Fig-2.19 New hybrid full adder [20]

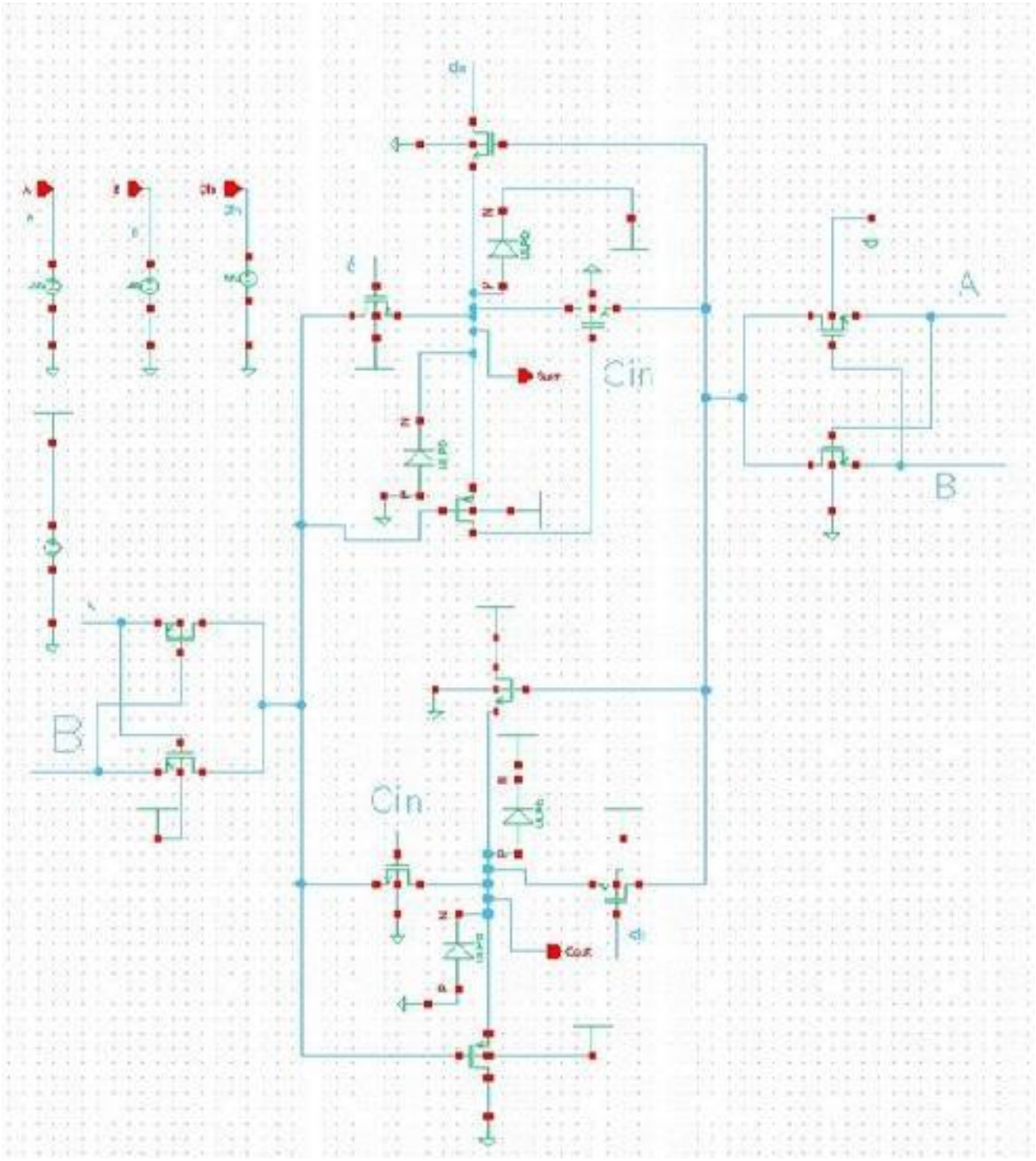

Fig-2.20 Schematic diagram of hybrid full adder

2.10) GDI-MUX FULL ADDER

An ultra-low power circuit using GDI method [20] is implemented and briefly discussed and is shown in figure below. GDI-MUX design is a new approach by eliminating the use of XOR and XNOR gates. Some alternate logic blocks like AND, OR and MUX are used to build a full adder. From Truth Table of a full adder, we can consider that when Cin=0, $Cout$ is same as the output of (A AND B) and both are equal, when Cin=1, $Cout$ is same as the output of (A OR B) and both are equal. Therefore, to get $Cout$ output, multiplexer is used. By following the same method when $Cout$=0 the Sum is same as output of (A OR B OR Cin) and both are equal, when $Cout$=1 the Sum is same as the output of (A AND B AND Cin) and both are equal. For required condition to select the following particular value $Cout$ is used, to drive a multiplexer.

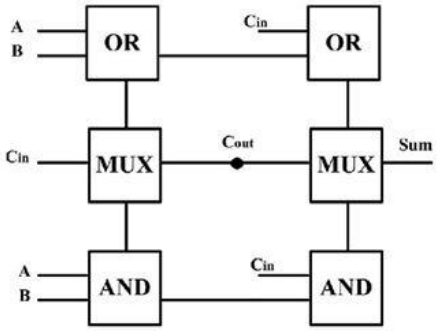

Fig-2.21 Another logical scheme for designing full adder cell [20]

2.10.1) GDI cell

The GDI cell is displayed in figure below which consists of one PMOS and one NMOS transistors [21], and Table-3 shows the Truth Table of cell. It has two extra input pins which will used. The cell contains total three inputs P(input to source/drain of PMOS), G(combined gate input of PMOS and NMOS) and N(input to source/drain of NMOS).Both PMOS and NMOS bulks are linked to P or N, so it based on the CMOS inverter. In order to implement GDI design SOI process is required [21]. It uses a smaller number of transistors as compared to CMOS and pass transistor logic designs.

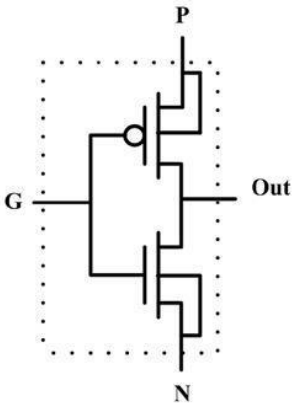

Fig-2.22 Basic GDI cell

Table-3:
Truth table of basic GDI cell

N	P	G	Out	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX
0	1	A	$\bar{A}$	NOT

The GDI-MUX full adder implementation is shown in figure below.
In Module-1 (A OR B) is implemented by connecting N input to V_{dd}, G input to A and P input to B. Second step is module-2- In this (A AND B) is implemented by connecting N to B, G to A and P to GND. Cin acts as selector which connected to input G of GDI for getting Cout and P is connected to (A AND B) and N is connected to (A OR B) .

Module-3 shows the designing of multiplexer, the above mentioned processor is followed here to implement (A OR B OR Cin) .

Module-4 is implemented by connecting P to C_{in},N to V_{dd} and G to (A OR B).

Module-5 is implemented by connecting P to GND,G to (A AND B) and N to Cin.
Finally, for getting Sum output G input is connected to Cout and P is connected to (A OR B OR Cin) and N is connected to (A AND B AND Cin) respectively.

This approach minimizes the Power dissipation (both static and Dynamic) and because of using UPLD level restorer it removes the current leakage problems and in cascaded series circuits it provides good driving capability. GDI-MUX design uses 20 transistors which give low switching capacitance and low dynamic power consumption.

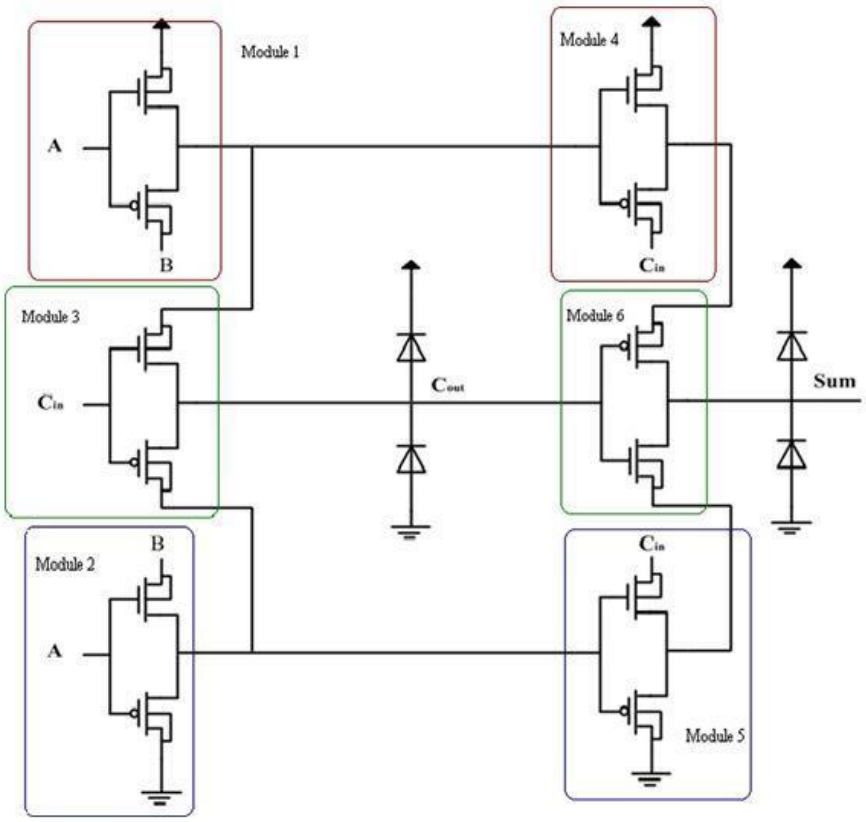

Fig-2.23 GDI-mux full adder [20]

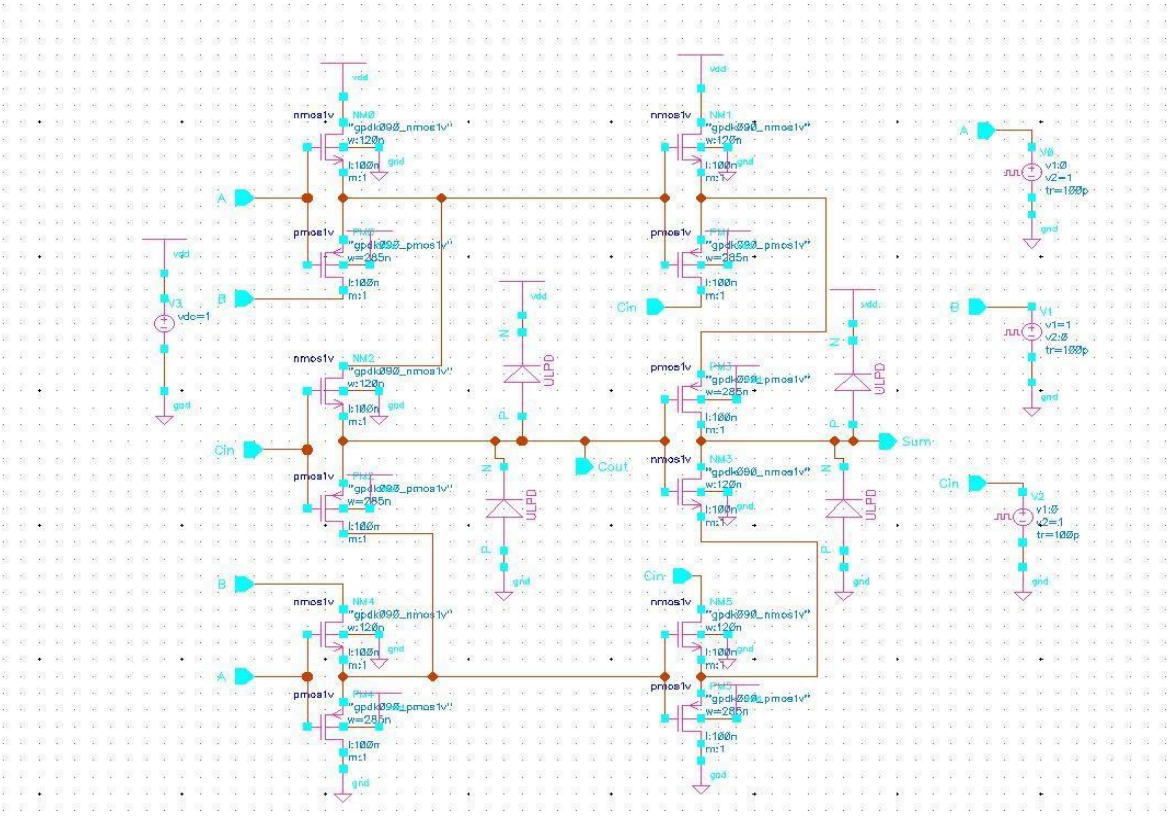

Fig-2.24 Schematic diagram of GDI-MUX full adder

Chapter 3

SIMULATION RESULTS AND ANALYSIS

3.1) SIMULATION ENVIRONMENT

In this chapter, we have introduced the waveforms and simulation results of 28T,16T,14T,10T full adders and also their power delay product comparisons. These full adders are made in TSPICE tool in 180nm technology at supply voltage of 1.8 volts. The figures below show their transient response respectively.

Next the simulation results for CMOS, hybrid CMOS, ULPFA, hybrid using semi XOR and semi XNOR logic, GDI-MUX full adders are given and compared their power delay product profiles. All these full adders' simulations are done using Cadence Virtuoso in 90nm gpdk CMOS technology with supply voltage varying from 0.9 to 1.2V. Power dissipation, delay and Power delay product (PDP) are measured for different design techniques.

3.2) SIMULATION RESULTS

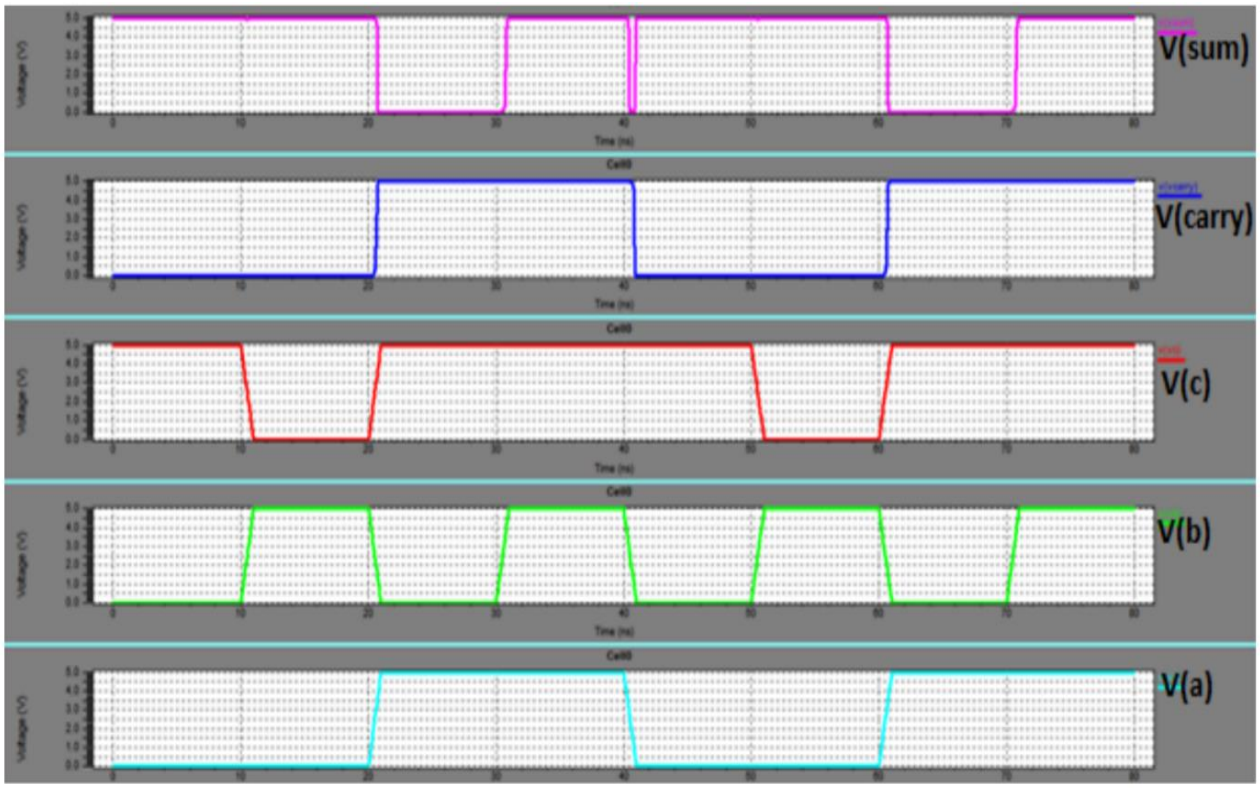

Fig-3.1 Transient response of 28T full adder

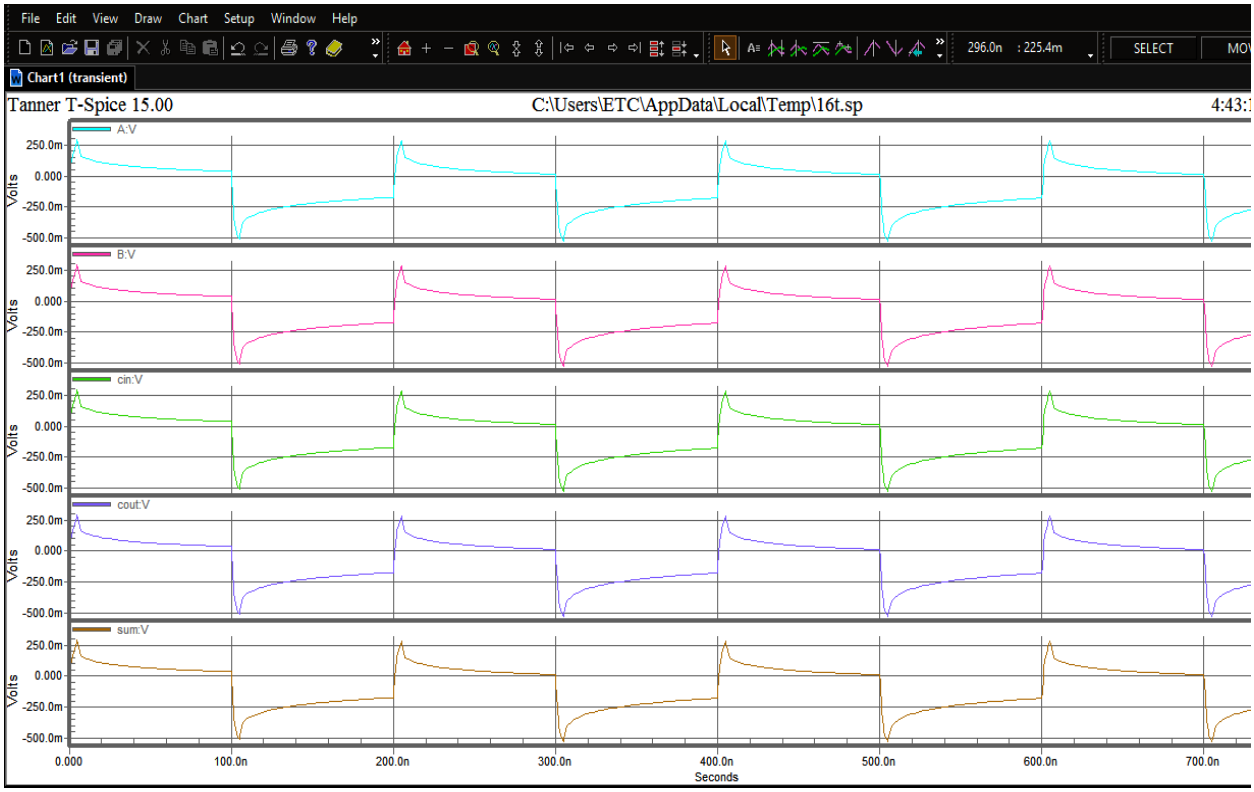

Fig-3.2 Transient response of 16T full adder

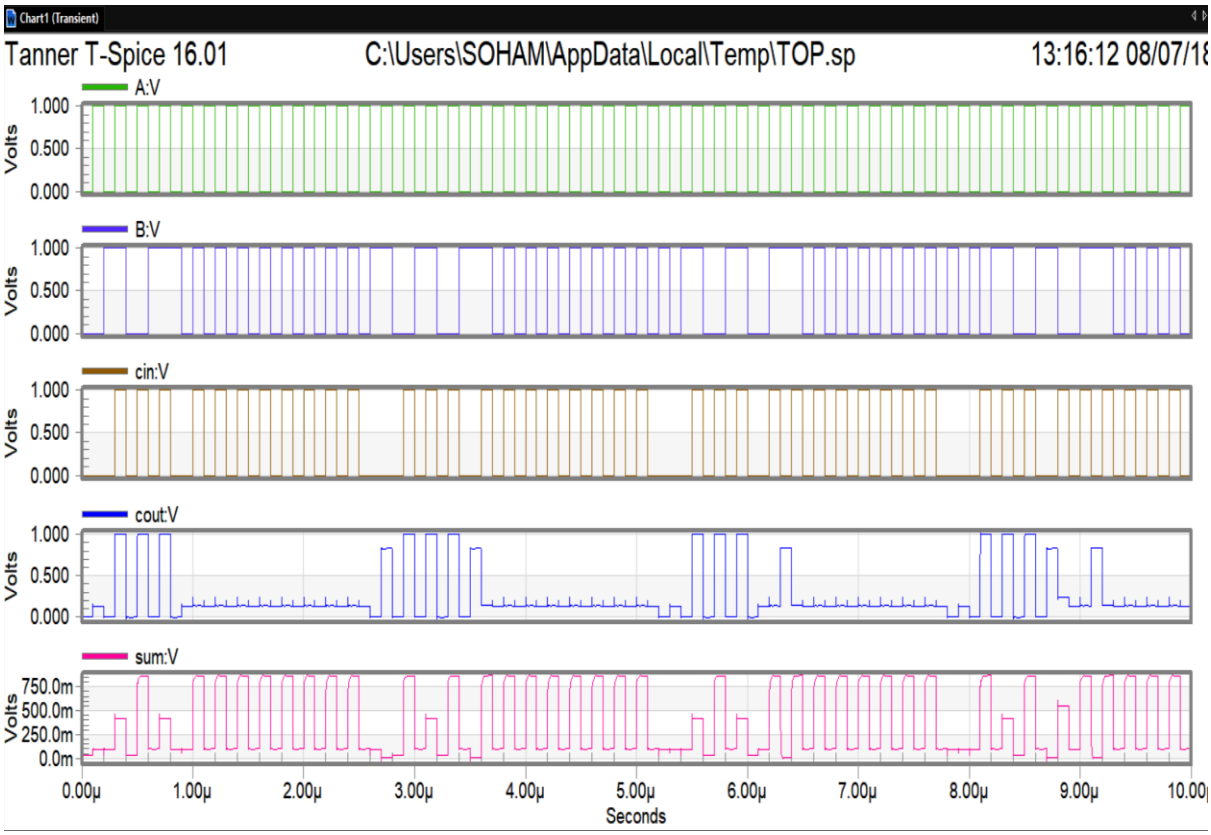

Fig-3.3 Transient response of 14T full adder

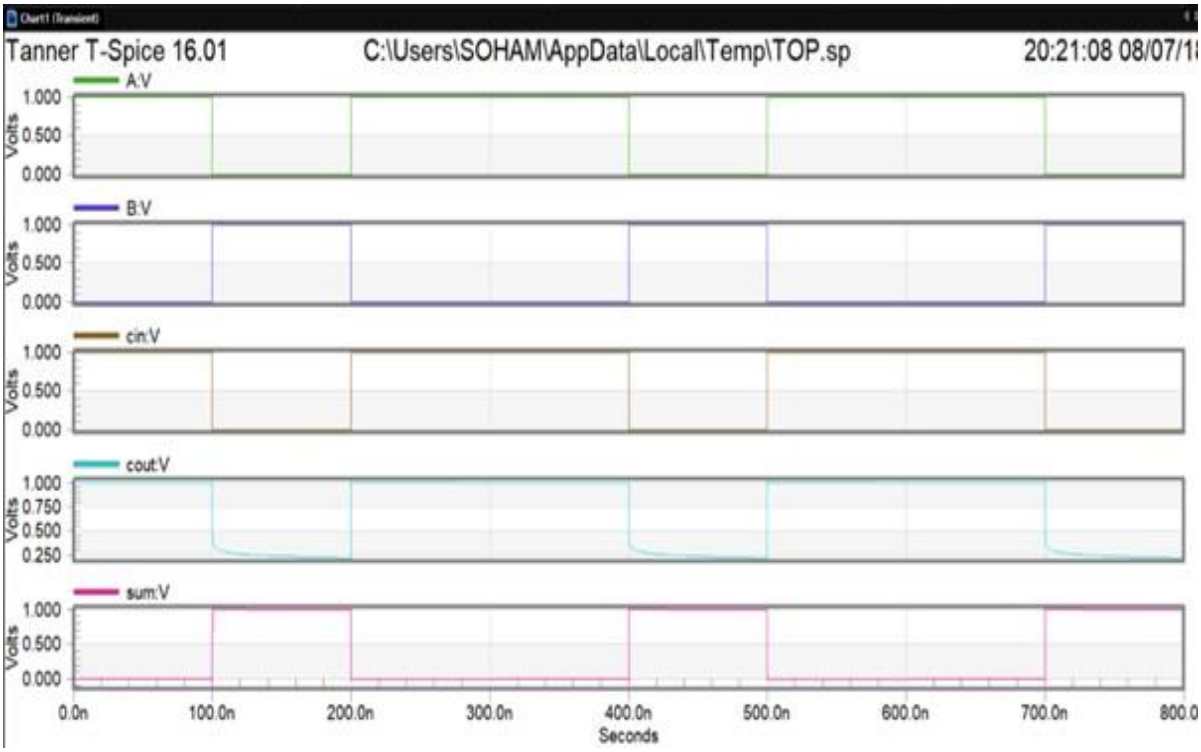

Fig-3.4 Transient response of 10T full adder

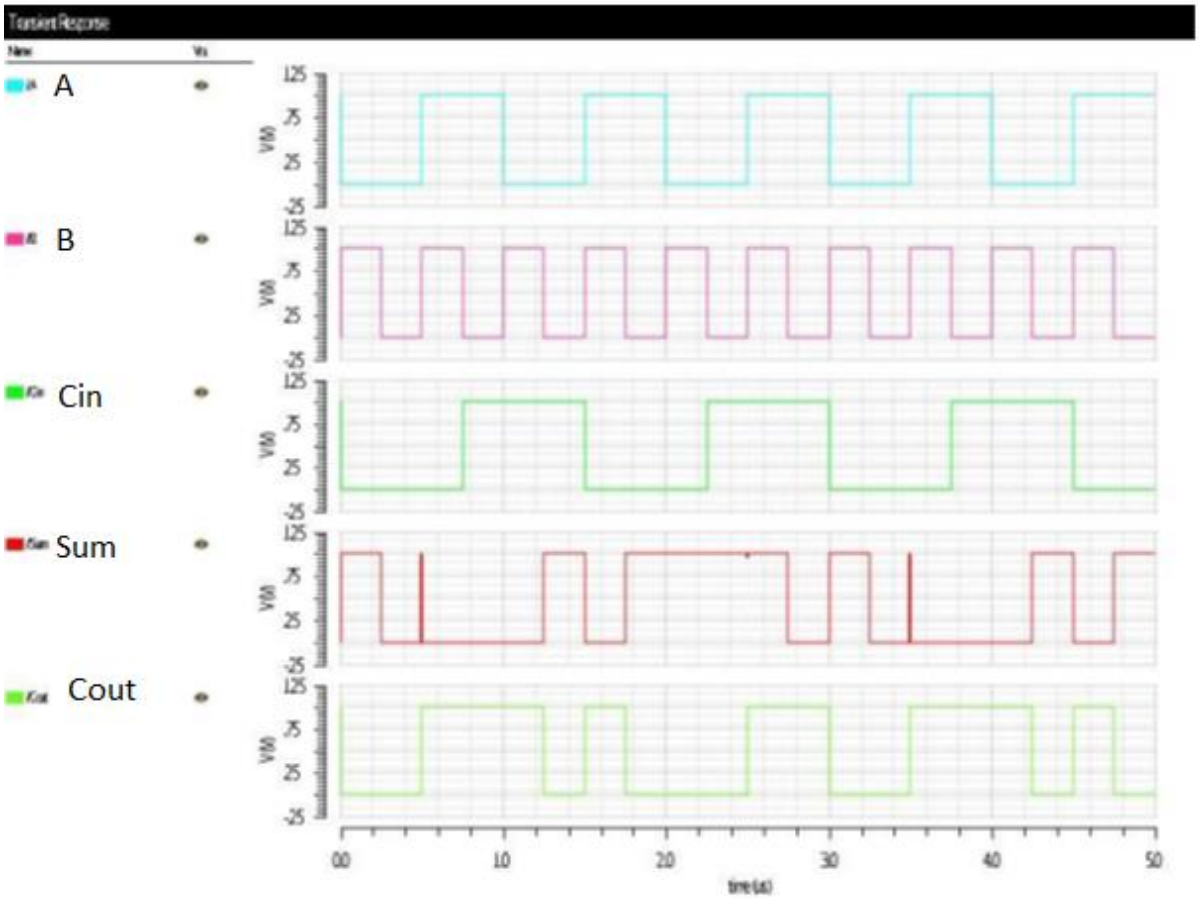

Fig-3.5 Transient response of C-CMOS full adder

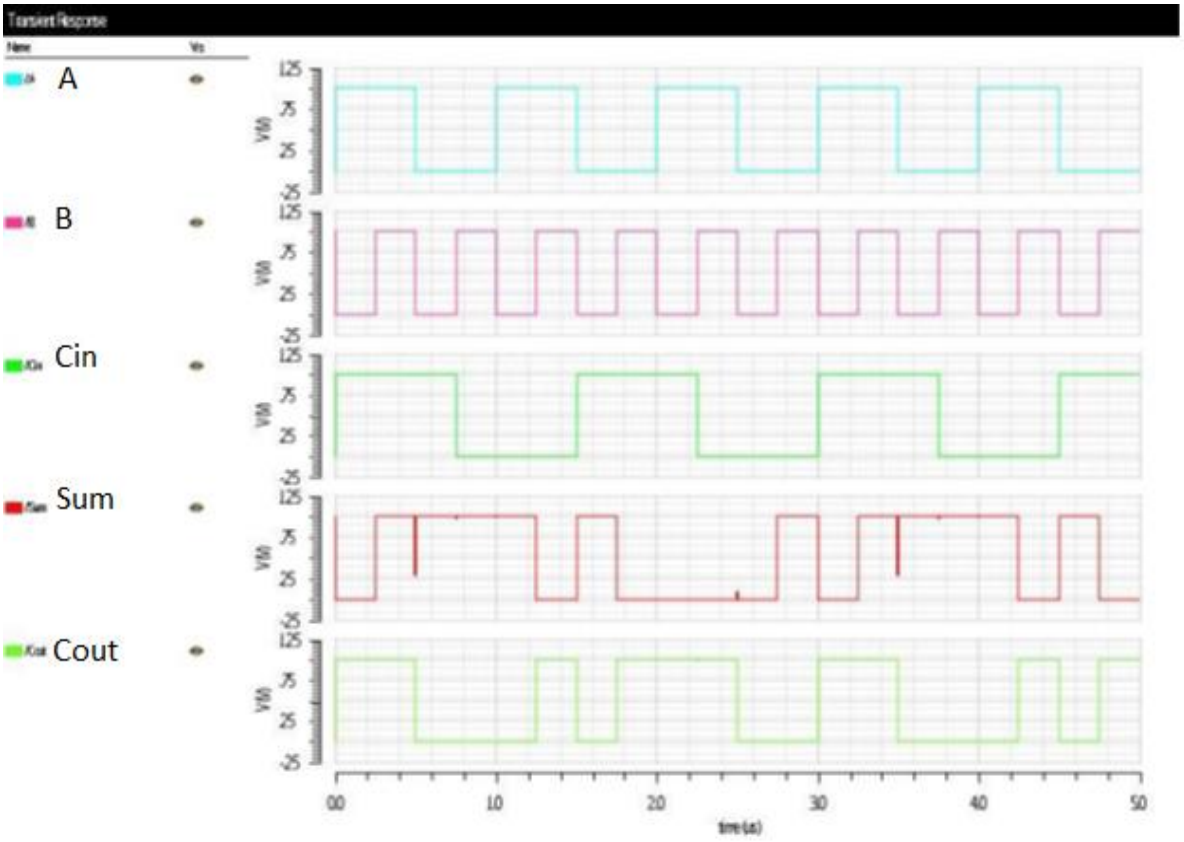

Fig-3.6 Transient response of CPL full adder

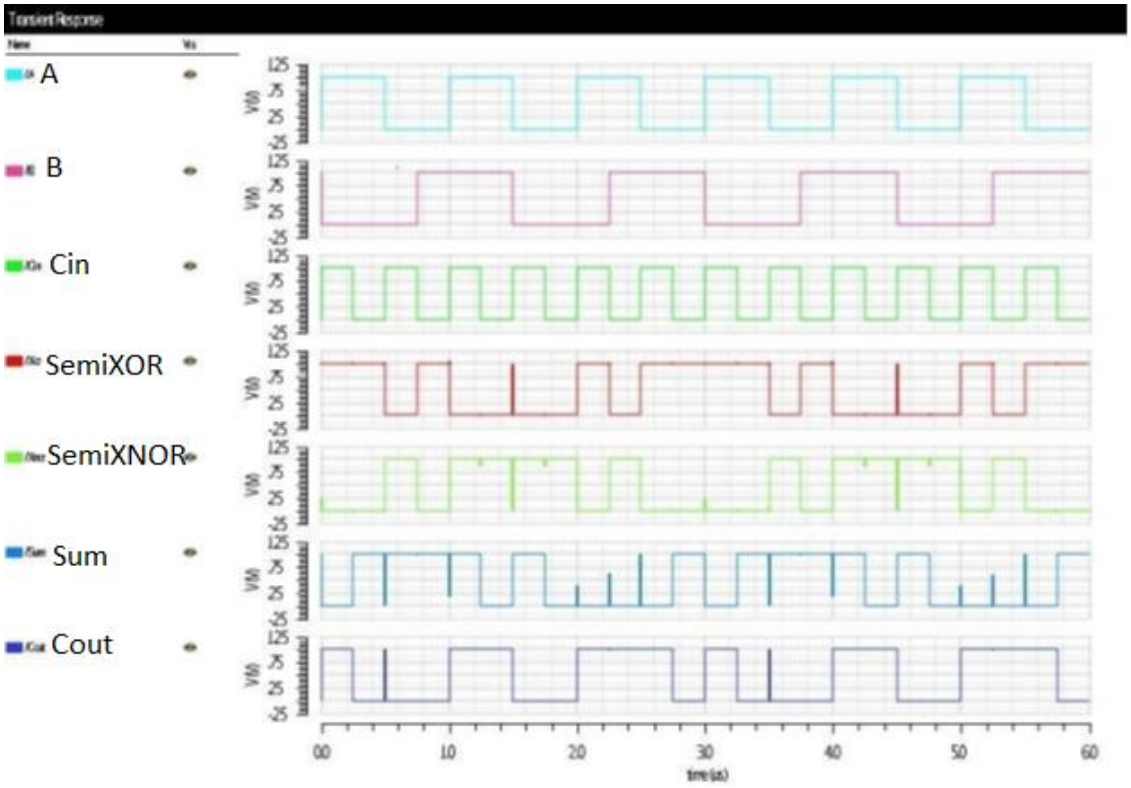

Fig-3.7 Transient response of Hybrid CMOS full adder

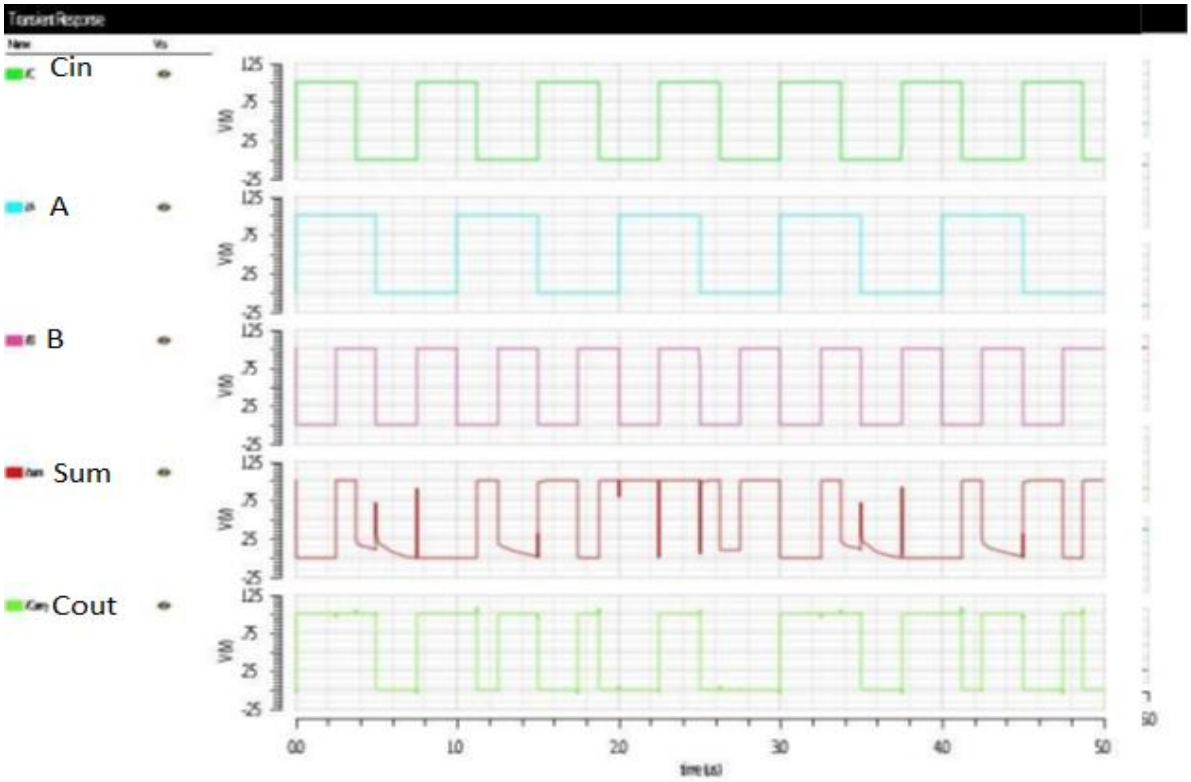

Fig-3.8 Transient response of ULP full adder

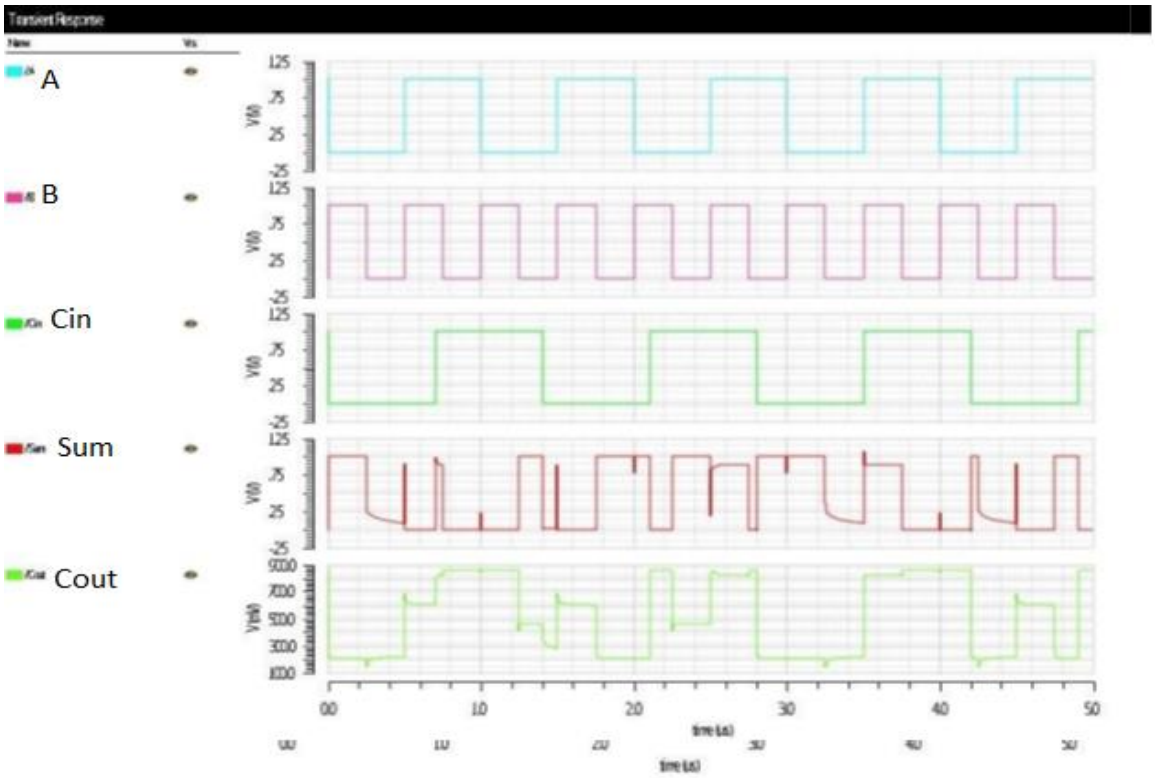

Fig-3.9 Transient response of new Hybrid full adder

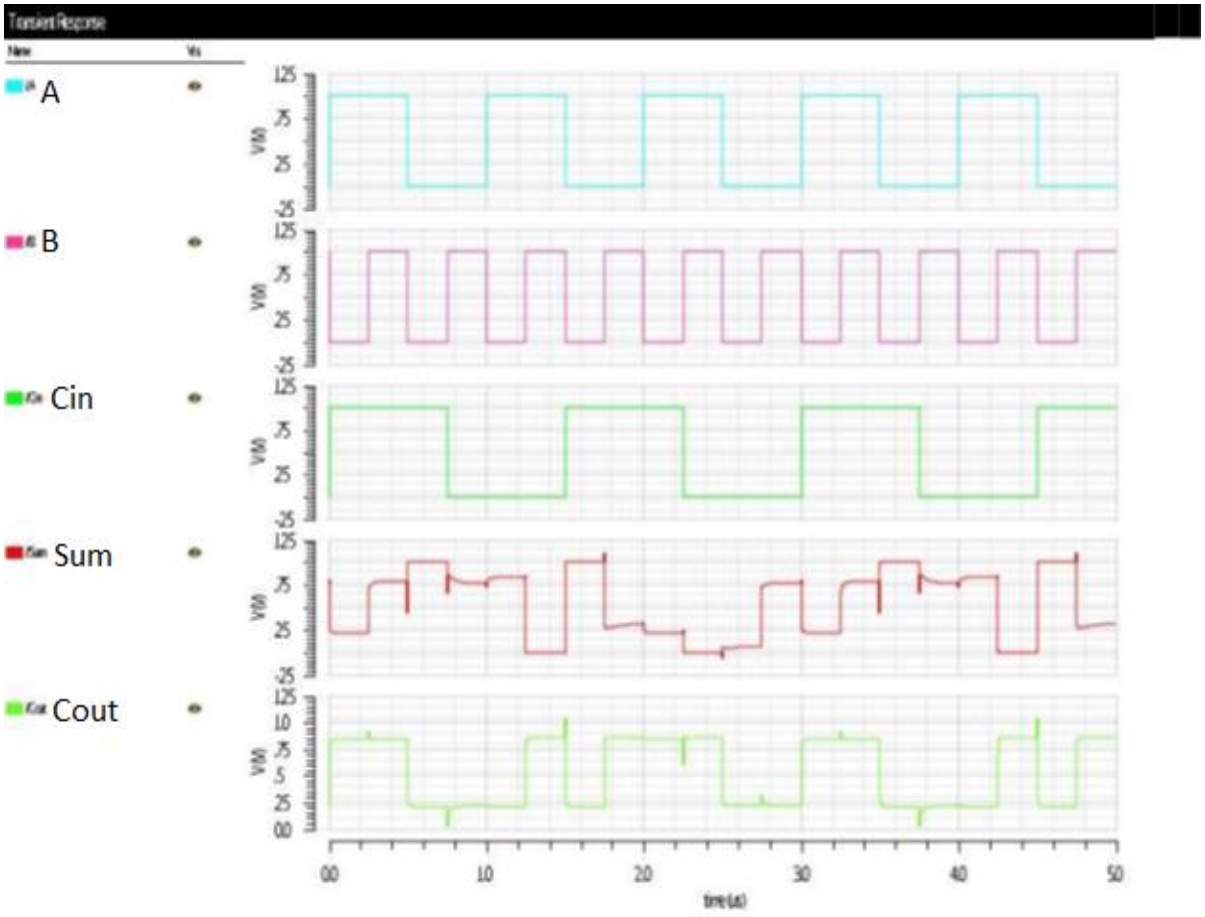

Fig-3.10 Transient response of GDI-MUX full adder

3.3) Comparison of power delay product of 28T,16T,14T and 10T full adders

All the 1-bit full adders have been simulated at 180nm technology under the voltage VDD=1.8V tabulated in below Table

FULL ADDER	VOLTAGE (V_{dd})	AVARAGE POWER (W)	PROPAGATION DELAY (S)	POWER DELAY PRODUCT (J)
28T	1.8	11.66E-06	12.35E-12	14.40E-17
16T	1.8	10.78E-06	9.379E-12	10.11E-17
14T	1.8	9.797E-06	11.35E-12	11.11E-17
10T	1.8	9.664E-06	10.07E-12	9.727E-17

3.4) Bar Graphs

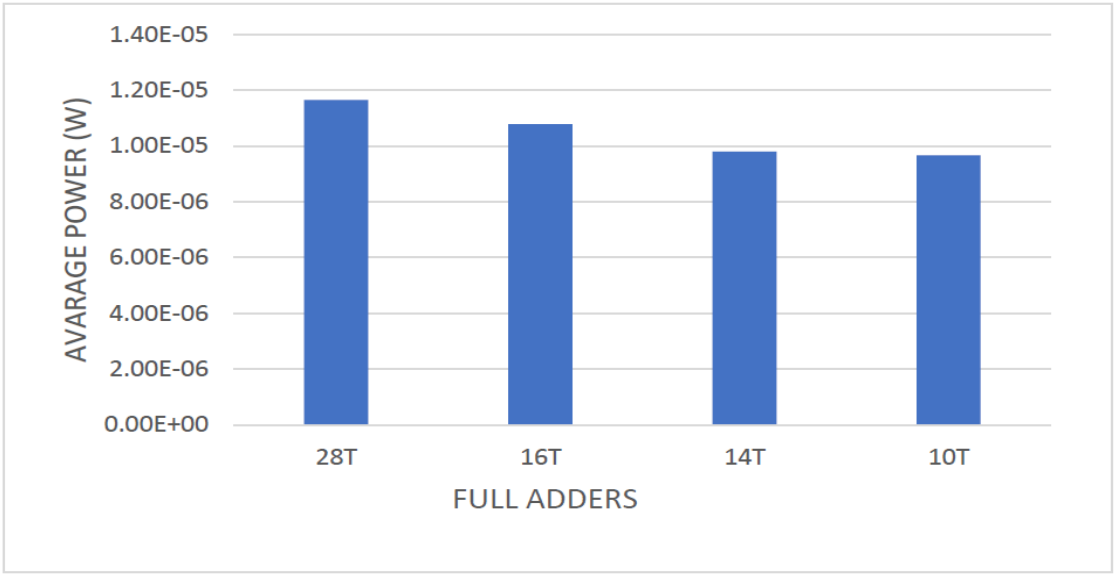

Fig-3.11 Full Adders vs Average Power

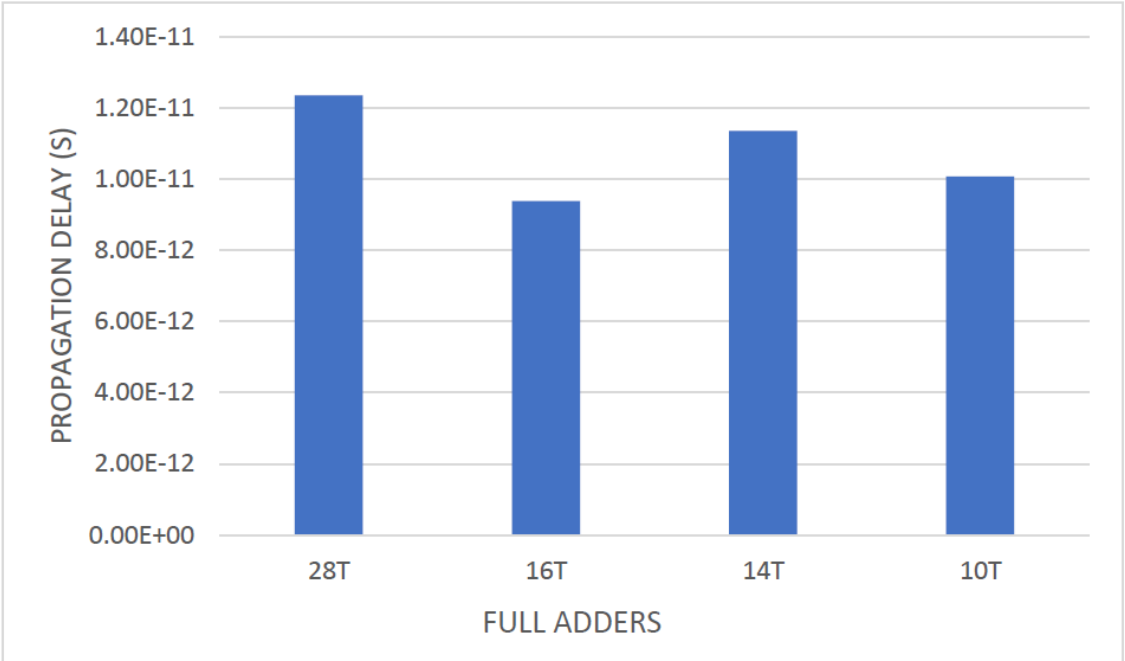

Fig-3.12 Full Adder vs Propagation Delay

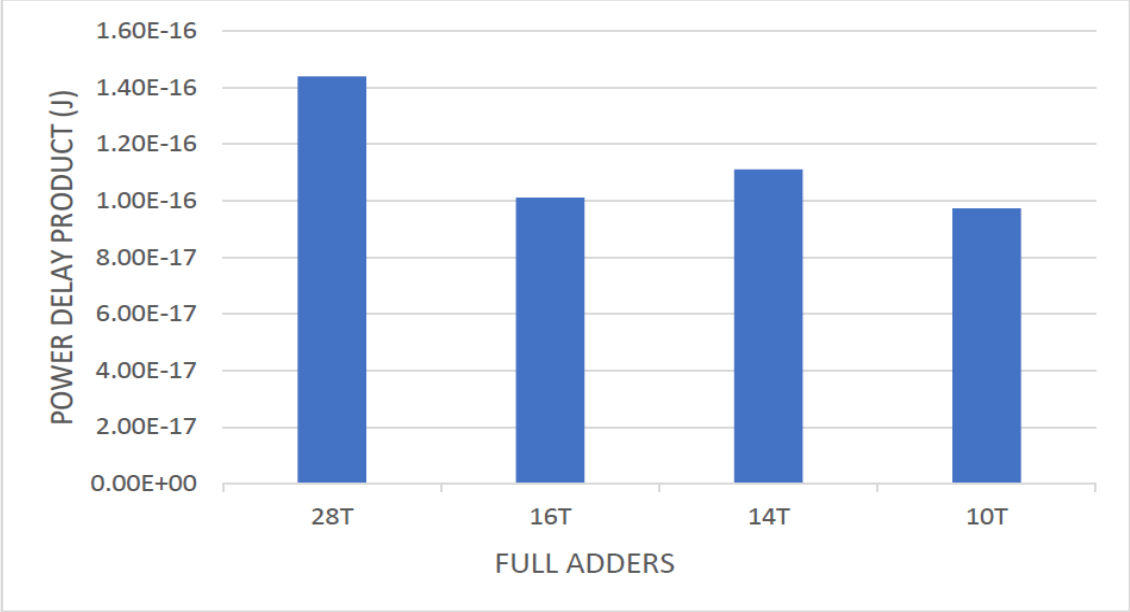

Fig-3.13 Full Adder vs Power Delay Product

3.5) Power dissipations outputs for supply voltages varying for 0.9 to 1.2V in 90nm

Supply Voltage (V)	Power dissipation in (µw)					
	C-MOS	CPL	Hybrid CMOS	ULPFA	Hybrid-2	GDI-MUX
0.9	0.05387	0.2120	0.1249	0.2762	1.915	0.04892
1	0.07602	0.2948	0.1620	0.3057	2.038	0.07984
1.1	0.1273	0.4447	0.2578	0.3744	2.454	0.2331
1.2	0.6655	1.391	1.237	1.198	4.088	0.8299

3.6) Power dissipation Graph

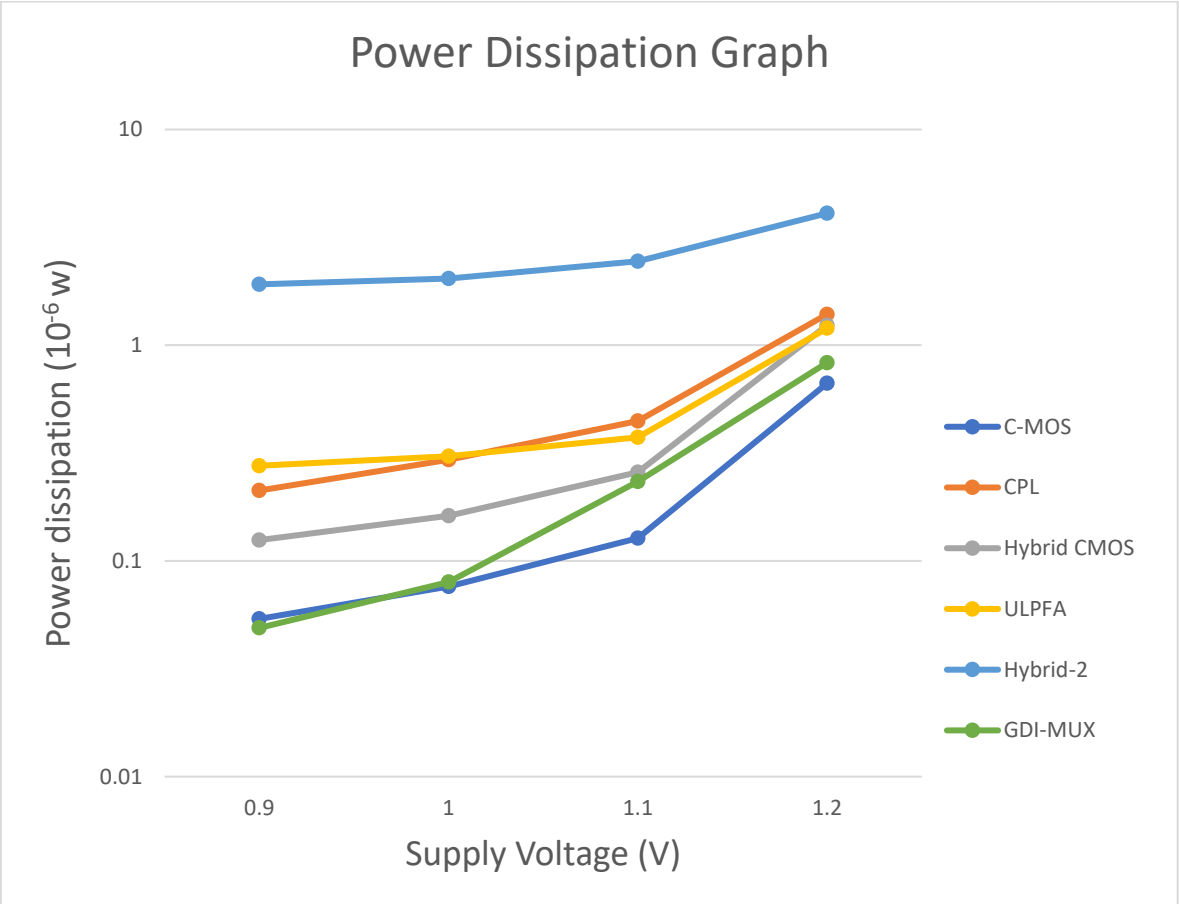

Fig-3.14 Supply voltage vs Power Dissipation

3.7) Delay outputs for supply voltages varying for 0.9 to 1.2V in 90nm

Supply Voltage (V)	Delay in (ps)					
	CMOS	CPL	Hybrid CMOS	ULPFA	Hybrid-2	GDI-MUX
0.9	124.5	132	104.8	110	100.45	102.65
1	119.5	107.7	104.1	104.2	97.45	99.4
1.1	107.9	86.9	99.9	100.1	97.15	99.05
1.2	108.9	85.1	96.8	97.45	99.3	102.45

3.8) Delay Graph

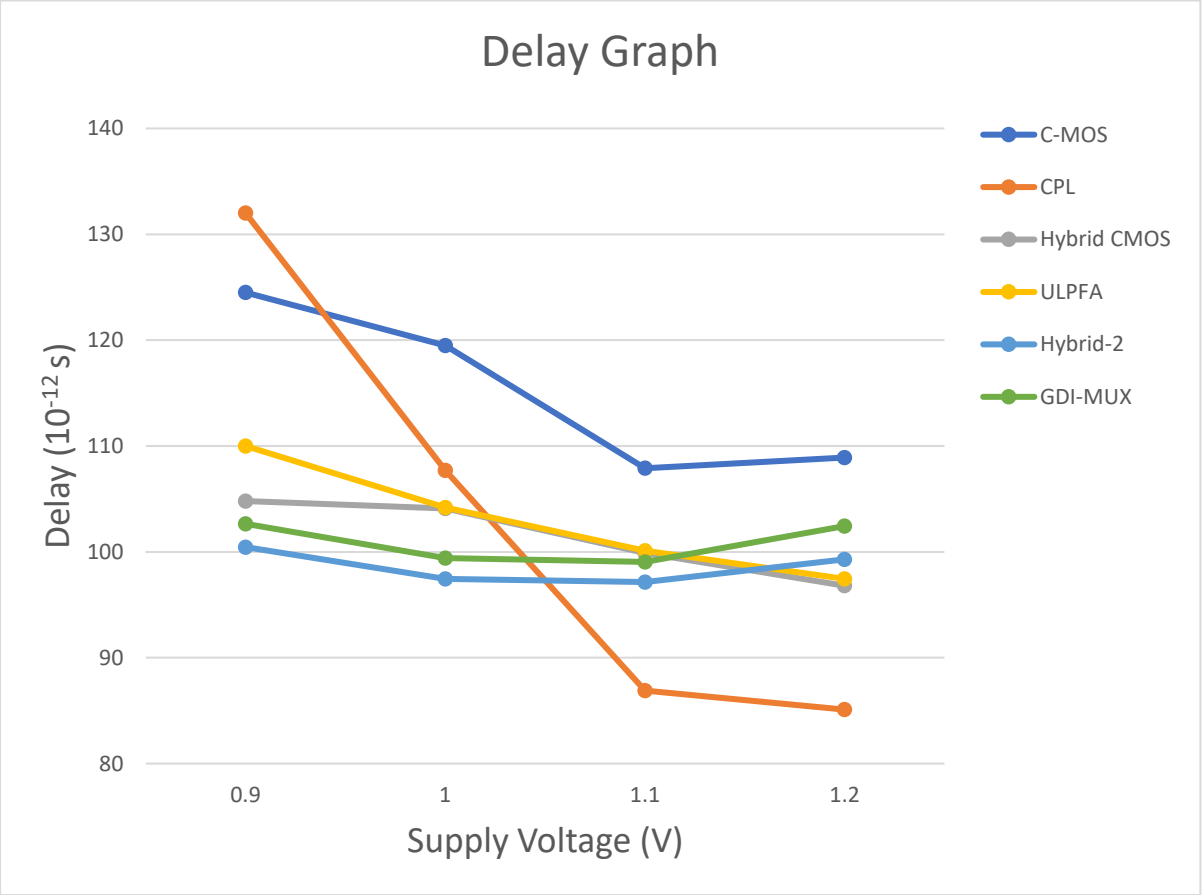

Fig-3.15 Supply voltage vs Delay

3.9) Power Delay product outputs for supply voltages varying for 0.9 to 1.2V in 90nm

Supply Voltage (V)	Power delay product in (µw-ps)					
	C-MOS	CPL	Hybrid CMOS	ULPFA	Hybrid-2	GDI-MUX
0.9	6.706815	27.984	13.08952	30.382	119.36175	5.021638
1	9.08439	31.74996	16.8642	31.85394	198.6031	7.936096
1.1	13.7567	38.6444	25.75422	37.47744	238.4061	23.088555
1.2	72.47295	118.3741	119.7416	116.7451	405.9384	85.023255

3.10) Power Delay Product Graph

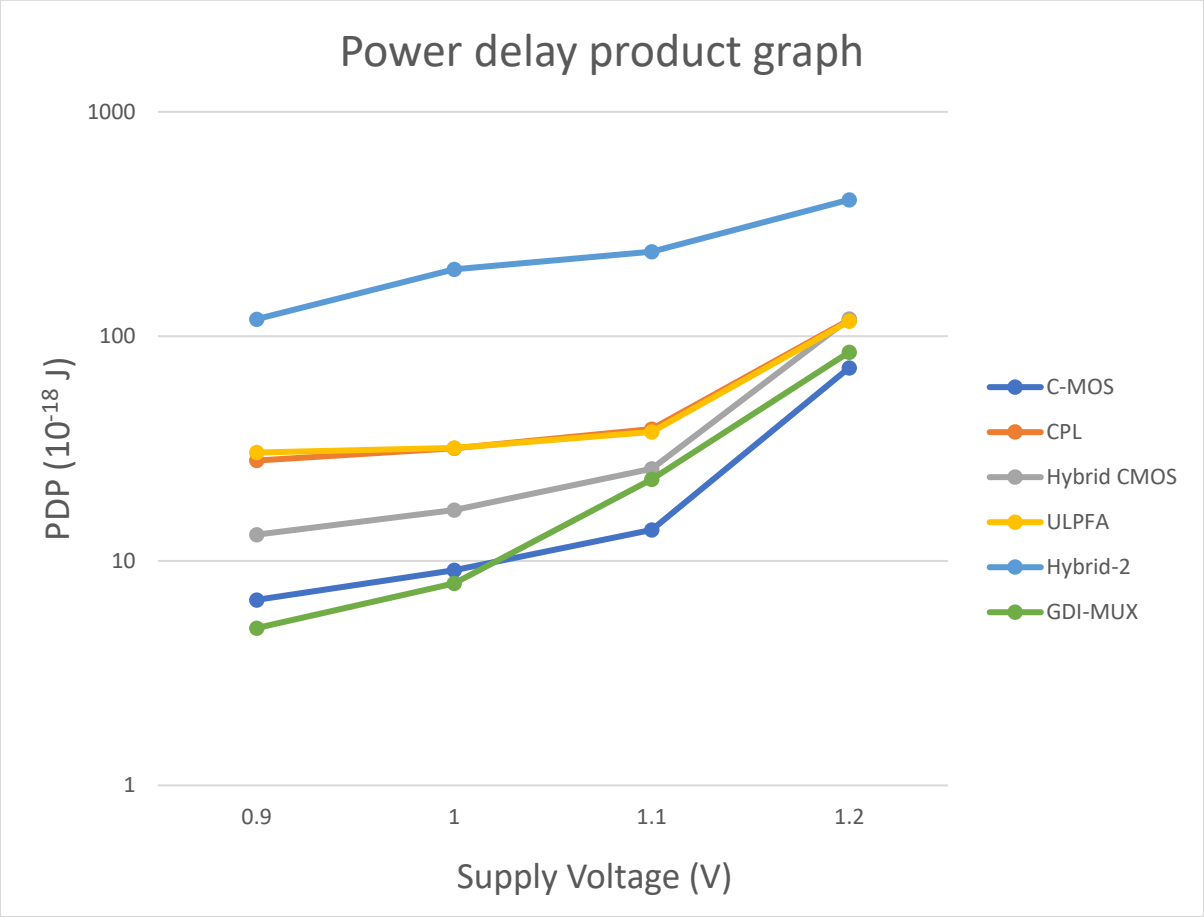

Fig-3.16 Supply Voltage vs PDP

Chapter 4

Conclusion

4.1 Overview

In this chapter we have introduced the final concluding remarks on our whole project work.

4.2 Observations and conclusions

From Table 1; 28T full adder has more power and delay and PDP compared to 16T, 14T, 10T full adders, because a greater number of transistors results in high input loads, more power consumption. In 16T full adder the XOR-XNOR module has been modified to reduce delay and power consumption. Lower power and delay have been obtained at the expense of 2 additional transistors. 14T full adder has simultaneous XOR and XNOR signals. Feedback transistors provide rail-to-rail outputs in XOR-XNOR module. However, they prompt high delay than 16T full adder. SERF use energy recovery technique to decrease the power consumption. Energy recovery logics reuse charge. Therefore, it consumes less energy than the other full adders. There are some problems in this circuit, SUM is generated from two cascaded XNOR gates which lead to long delay, compared to 16T full adder it has more delay. Various types of full adders with different logic styles have been implemented. These C-CMOS, CPL, Hybrid CMOS, ULPFA full adders are compared with new hybrid full adder and GDI-MUX full adder. The new hybrid full adder and GDI-MUX full adder consist of a smaller number of transistors. Smaller number of transistors results in less switching activity and area. A broad comparison of all the designs shows the gradual improvement in power dissipation, delay and Power delay product (PDP). The considerable reduction in power by minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP. Complementary MOS logic in 90nm technology node, complementary pass transistor full adder involving pass transistor logic, the hybrid CMOS logic full adder, ultra-low power full adder using Ultra low power diode and XOR and XNOR gates, hybrid full adder using semi XOR and XNOR logic and Gate Diffusion Input-multiplexer full adder are explored. Power delay product (PDP) is analyzed for these transistors at various supply voltages starting from 0.9 volt to 1.2 volt. Hybrid full adder using semi XOR and XNOR logic has the highest power delay product because of high power dissipation. The complementary pass transistor and ultralow power full adder logic styles has more or less the same power delay product profile for the entire range of supply voltages. The complementary MOS logic full adder and gate diffusion input multiplexer full adder has the overall least power delay product profile. For supply voltages from 0.9 volt to 1 volt we can go for gate diffusion input multiplexer logic full adder and for supply voltages from 1 volt to 1.2 volt we can go for conventional complementary MOS logic.

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REFERENCE FOR SIMULATORS

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https://community.cadence.com/cadence_blogs_8/b/cic/posts/virtuosity-creating-and-previewing-stimuli?CMP=CIC_VirtuosoBlog_AdTxt_GooSe_0501&gclid=Cj0KCQjwla7nBRDxARIsADll0kAT75knxFgxfS_a1pHInaJYVP_bUhR-DhmwDfGstfxjeC8M8WkecoUaAtwWEALw_wcB

Appendices

The codes for the simulations of 16T,14T,10T in TSPICE tools are given below

For 16T :-

```
MNMOS_1 N_21 A N_3 N_1 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=300 $y=300 $w=400 $h=600 $m
MNMOS_2 N_3 B Gnd N_2 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $ $x=-
100 $y=-400 $w=400 $h=600
MNMOS_3 N_19 B A N_4 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $ $x=-
600 $y=-2700 $w=600 $h=400 $r=90
MNMOS_4 B A N_19 N_5 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=800 $y=-2700 $w=600 $h=400 $r=90
MNMOS_5 Cin N_19 N_17 N_6 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=2100 $y=800 $w=600 $h=400 $r=270
MNMOS_6 N_19 Cin SUM N_7 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=2700 $y=200 $w=600 $h=400 $r=270
MNMOS_7 Cin N_21 Cout N_8 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=3200 $y=-2000 $w=600 $h=400 $r=270
MNMOS_8 A N_19 Cout N_9 NMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=3200 $y=-3200 $w=600 $h=400 $r=270
MPMOS_1 B A N_21 N_10 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $ $x=-
600 $y=1000 $w=600 $h=400 $r=90
MPMOS_2 N_21 B A N_11 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=400 $y=1000 $w=600 $h=400 $r=90
MPMOS_3 N_14 A Vdd N_12 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=300 $y=-1200 $w=400 $h=600 $m
MPMOS_4 N_19 B N_14 N_13 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=-100 $y=-1900 $w=400 $h=600
MPMOS_5 Cin N_21 N_17 N_15 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=2100 $y=1400 $w=600 $h=400 $r=90
MPMOS_6 N_21 Cin N_17 N_16 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=2700 $y=-400 $w=600 $h=400 $r=90
MPMOS_7 Cin N_19 Cout N_18 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=3200 $y=-1400 $w=600 $h=400 $r=90
MPMOS_8 A N_21 Cout N_20 PMOS W=1.62u L=180n AS=1.458p PS=5.04u AD=1.458p PD=5.04u $
$x=3200 $y=-2600 $w=600 $h=400 $r=90
VVoltageSource_1 Vdd Gnd  DC 1 $ $x=-6700 $y=-300 $w=400 $h=600
VVoltageSource_2 A Gnd  BIT({1010101010} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-5500
$y=700 $w=400 $h=600
VVoltageSource_3 B Gnd  BIT({0011001100} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-4000
$y=700 $w=400 $h=600
VVoltageSource_4 cin Gnd  BIT({00010001000} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-
5500 $y=-700 $w=400 $h=600
.PRINT TRAN V(cout) $ $x=5250 $y=-2950 $w=1500 $h=300
```

```
.PRINT TRAN V(sum) $ $x=4950 $y=50 $w=1500 $h=300
.PRINT TRAN V(A)
.PRINT TRAN V(B)
.PRINT TRAN V(cin)
.measure tran tdelay_cout_to_sum trig v(cout) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_A_to_sum trig v(A) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_B_to_sum trig v(B) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_cin_to_sum trig v(cin) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_A_to_cout trig v(A) val=.5 fall=2 targ v(cout) val=.5 fall=2
.measure tran tdelay_B_to_cout trig v(B) val=.5 fall=2 targ v(cout) val=.5 fall=2
.measure tran tdelay_cin_to_cout trig v(cin) val=.5 fall=2 targ v(cout) val=.5 fall=2

.power VVoltageSource_1 10n 500n
.power VVoltageSource_2 10n 500n
.power VVoltageSource_3 10n 500n
.power VVoltageSource_4 10n 500n

********* Simulation Settings - Analysis Section *********
.tran 400n 10000n
********* Simulation Settings - Additional SPICE Commands *********
.end
```

For 14T :-

```
MM3 N_1 A N_7 0 nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-1700 $y=100
$w=400 $h=600 $r=180
MM4 N_1 B Gnd 0 nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-2100 $y=-500
$w=400 $h=600
MM6 N_7 N_7 Gnd 0 nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=1800 $y=100
$w=400 $h=600
MM8 cin N_7 sum 0 nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=3400 $y=900
$w=600 $h=400 $r=270
MM12 cin N_7 cout N_4 nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=3400 $y=-
2400 $w=600 $h=400 $r=270
MM14 A N_7 cout N_6 nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=3400 $y=-
3800 $w=600 $h=400 $r=270
MNMOS_1 N_7 cin sum 0 nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=3400 $y=0
$w=600 $h=400 $r=270
MM1 B A N_7 Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=-2400 $y=1100
$w=600 $h=400 $r=90
MM2 N_7 B A Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=-1400 $y=1100
$w=600 $h=400 $r=90
MM5 N_7 N_7 Vdd Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=1800 $y=700
$w=400 $h=600
MM7 cin N_7 sum Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=3400 $y=1600
```

```
$w=600 $h=400 $r=90
MM10 N_7 cin sum N_2 ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=3400 $y=-600
$w=600 $h=400 $r=90
MM11 cin N_7 cout N_3 ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=3400 $y=-1700
$w=600 $h=400 $r=90
MM13 A N_7 cout N_5 ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=3400 $y=-3100
$w=600 $h=400 $r=90
VVoltageSource_1 Vdd Gnd  DC 1 $ $x=-6700 $y=-300 $w=400 $h=600
VVoltageSource_2 A Gnd  BIT({0101010101} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-5500
$y=700 $w=400 $h=600
VVoltageSource_3 B Gnd  BIT({0011001100} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-4000
$y=700 $w=400 $h=600
VVoltageSource_4 cin Gnd  BIT({00010001000} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-
5500 $y=-700 $w=400 $h=600
.PRINT TRAN V(cout) $ $x=5250 $y=-2950 $w=1500 $h=300
.PRINT TRAN V(sum) $ $x=4950 $y=50 $w=1500 $h=300
.PRINT TRAN V(A)
.PRINT TRAN V(B)
.PRINT TRAN V(cin)
.measure tran tdelay_cout_to_sum trig v(cout) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_A_to_sum trig v(A) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_B_to_sum trig v(B) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_cin_to_sum trig v(cin) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_A_to_cout trig v(A) val=.5 fall=2 targ v(cout) val=.5 fall=2
.measure tran tdelay_B_to_cout trig v(B) val=.5 fall=2 targ v(cout) val=.5 fall=2
.measure tran tdelay_cin_to_cout trig v(cin) val=.5 fall=2 targ v(cout) val=.5 fall=2

.power VVoltageSource_1 10n 500n
.power VVoltageSource_2 10n 500n
.power VVoltageSource_3 10n 500n
.power VVoltageSource_4 10n 500n

********* Simulation Settings - Analysis Section *********
.tran 400n 10000n
********* Simulation Settings - Additional SPICE Commands *********
.end
```

For 10T :-

```
MM2 N_1 B Gnd Gnd nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-1000 $y=-200
$w=400 $h=600
MM4 N_2 A N_1 Gnd nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=800 $y=700
$w=400 $h=600
MM6 N_3 N_2 Gnd Gnd nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=2400 $y=-200
$w=400 $h=600
```

```
MM8 sum cin N_3 Gnd nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=4800 $y=1000 $w=400 $h=600
MM10 cout N_3 B Gnd nh W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=4800 $y=-1600 $w=400 $h=600
MM1 N_1 B Vdd Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=-1000 $y=700 $w=400 $h=600
MM3 N_2 A B Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=800 $y=1600 $w=400 $h=600
MM5 N_3 N_2 Vdd Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=2400 $y=700 $w=400 $h=600
MM7 sum cin N_2 Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=4800 $y=1900 $w=400 $h=600
MM9 cout N_3 cin Vdd ph W=5u L=250n AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=4800 $y=-500 $w=400 $h=600
VVoltageSource_1 Vdd Gnd  DC 1 $ $x=-5600 $y=0 $w=400 $h=600
VVoltageSource_2 A Gnd  BIT({0101010101} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-4400 $y=300 $w=400 $h=600
VVoltageSource_3 B Gnd  BIT({0011001100} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-3800 $y=300 $w=400 $h=600
VVoltageSource_4 cin Gnd  BIT({00010001000} ON=1 RT=100p FT=100p LT=100n HT=100n) $ $x=-3200 $y=300 $w=400 $h=600
.PRINT TRAN V(cout) $ $x=5750 $y=-1150 $w=1500 $h=300
.PRINT TRAN V(sum) $ $x=5750 $y=1250 $w=1500 $h=300
.PRINT TRAN V(A)
.PRINT TRAN V(B)
.PRINT TRAN V(cin)
.measure tran tdelay_cout_to_sum trig v(cout) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_A_to_sum trig v(A) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_B_to_sum trig v(B) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_cin_to_sum trig v(cin) val=.5 fall=2 targ v(sum) val=.5 fall=2
.measure tran tdelay_A_to_cout trig v(A) val=.5 fall=2 targ v(cout) val=.5 fall=2
.measure tran tdelay_B_to_cout trig v(B) val=.5 fall=2 targ v(cout) val=.5 fall=2
.measure tran tdelay_cin_to_cout trig v(cin) val=.5 fall=2 targ v(cout) val=.5 fall=2

.power VVoltageSource_1 10n 500n
.power VVoltageSource_2 10n 500n
.power VVoltageSource_3 10n 500n
.power VVoltageSource_4 10n 500n

********* Simulation Settings - Analysis Section *********
.tran 1n 800n
********* Simulation Settings - Additional SPICE Commands *********
.end
```