Soham Mondal

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Education

Jadavpur University Kolkata, India

Bachelor of Engineering in Electronics and Telecommunications; GPA : 8.13/10.0 *2015 – 2019*

- Bachelor Thesis: Comparative analysis of low power full adders – Under Dr.Chandrima Mondal | Certificate
- Transcripts

South Point High School Kolkata, India

W.B.C.H.S.E; 85% and W.B.S.E; 90.28% *2014 – 2015*

- Transcripts

Experience

Senior SoC Design Verification Engineer July 2019 – Present

Samsung Semiconductor India R&D *Bangalore, India*

- Team (Storage SoC DV) - Design and Verification of Controller Host IP comprising Host subsystem + Flash controller + NAND with unit firmware
- Protocols - On-Chip (NOC/NIC) AXI3, AXI4, AHB Lite, Host UFS 3.1 (UTP-12Gbps, 2Lane), UFS 4.0, Unipro, MPHY, Peripherals I2C, SPI, UART, SMBUS
- End to End NOC/NIC coverage driven verification of AMBA slaves for connectivity checks, scoreboard creation, monitor development, report generation
- Strong knowledge of Cadence VIP and integration
- Developed Python and shell based tool for automated error-free verification and testbench creation for NOC/NIC slave verification for Enterprise NVME1.4 SSD. Reduced the Time-to-First-Test by almost 100%
- Makefile, Shell Scripting, TCL and Python Automation
- Development of Comprehensive testplan and UVM compliant VIP development
- Micro-architecture and State Machine Based custom controller RTL design
- Metric Driven Verification, Constraint Random Stimulus, Coverage, SV-assertions, Formality tool, equivalence check
- Knowledge of pipelining of design, Static Timing Analysis
- Simulators- cadence xcelium, synopsys vcs, mentor questasim | Waveform debugger- simvision, verdi | Fpga- xilinx SDx, vivado, ISE | Synthesis- synopsys dc, yosys | Revision control- git, svn | Agile- atlassian jira, Xray

Hardware Intern May. 2018 – July 2018

Samsung Semiconductor India R&D *Bangalore, India*

- Team (DRAM h/w) - Understand MBIST, MBISR architectures applicable for DDR4/5 and share knowledge sessions to improve proprietary MBIST architecture with new features
- Creation of driver/adapter IP to facilitate forward compatibility of DDR3 MBIST to DDR4/5 command sets and functionally verify the same with directed verilog testbench
- Port & validate the setup in xilinx virtex ultrascale vcu-108 board for proof-of-concept
- Received Pre-placement offer on basis of work Offer

Projects

Meta-Data based simulation Automation to overcome Verification Challenges of SoC Interconnect Bus Matrix | *Python, Shell, Make, TCL* 2019

- Tool to auto-generate SV-UVM & Cadence AMBA VIP integrated NOC/NIC testbench, complete test-scenarios with almost all forms of transactions supported between master and slaves, DUT-VIP connections, compilation & simulation scripts and report matrix indicating non-responding slaves, from IPXACT DUT information
- Facilitated huge reduction of verification efforts and overall time-to-first-test & time-to-market for product delivery and meeting verification goal quickly. Setup has been extensively used by Samsung DS Korea for fast error free end-2-end NOC/NIC verification of enterprise SSD SoC
- Won 3rd prize in Open Solutions Virtual Conference, Samsung R&D Global (memory) in smart work category for whitepaper presentation ppt. Cert

Academic Projects

Application specific Controller for computationally extensive synapse | *System-verilog, Verilog, Git* Dec 2019 – Present

- Hardware Modelling of Custom controller with custom multicycle floating point ISA and special function to simulate biologically extensive synapse and irregularities in synaptic circuits or pathways
- Hand drawn customized michro-architecture for high performance, low-power and cycle optimised operation
- State-machine based generic sub-controller design which can be generalised for other complex designs
- Concepts like simple handshake, state-machine, polling has been applied
- Research work is under supervision of Amitava Mukherjee, CSE Adamas University, Arnab Raha, Intel Edge.AI, USA and Janet L.Paluh, SUNY PolyTech, USA Git

High speed economical synaptic hardware design | *System-verilog, Verilog, Python, C++, Shell, Git* 2019

- Hardware design of Synaptic AI accelerator by taking realtime accurate intra-neuronal parameters in floating point single & double precision and recently developed number system Posit 32 bit with 4 bit exponent size
- Comparative study of them in terms of accuracy, precision and sensitivity handling and economic footprint. The designs are pipelined to meet 1 Ghz frequency in 45nm ASIC with extensively optimised area and power Git

Brain cancer image detection in Rpi3b+ | *Python, Shell, Git* Dec 2019 – Present

- Classification of brain cancer images using ML inference model which is greatly optimised for running in Rpi3b+ or resource constrained similar edge devices Git

Undergraduate Projects

Text search engine (a prototype) | *Java, Maven, Git* | Git
A comparative analysis of public key cryptography | *Matlab* | Git | Paper presentation Jadavpur University 2nd Prize
Marks prediction | *Python, Flask, Heroku* | Git
Dominant color for image segmentation | *Python, Flask, Heroku* | Git
Image Captioning | *Python, Flask, Heroku* | Git
Gui using Tkinter | *Python* | Git-1 Git-2
Medical imaging & digital topology | *C++, Make* | Git
Arduino board projects | *C++, Arduino, Esp8266* | Vid-1 Cert-1 | Vid-2 Cert-2

Other Experience

Network Management *@Nettech pvt. ltd.* (2016, India) | Trained in Network Management & Security Cert
Marketing Management *@IIM Lucknow* (2016, Remote-India) | Marketing Management Internship Under Dr. Sameer Mathur Project
Student Partner *@Internshala* (2016, Remote-India) | Cert
Equity Research *@Money Roller* (2017, Remote-India) | Research about happenings in global financial area Offer
Marketing Analyst *@Qrius* (2018, Remote-India) | Cert
Marketing Expansion Strategy *@Mentored Research* (2017, Remote-India) | Cert
Network management *@ONGC ltd.* (2018, India) | Cert
Student mentor *@Jadavpur University Science Club* (2015-19, India)
Member *@Jadavpur University IET* (2015-19, India)

Achievements

- **3rd prize in smart work category, whitepaper presentation** *@Open Solutions Virtual Conference, Samsung R&D Global(memory)* - More than 2600 selected Samsung developers/staffs all around the world as contestants | $500 + Samsung T7 SSD | Cert
- **Employee of the Month** *@SSIR,Bangalore* - Slave NOC/NIC automated error free verification of enterprise SSD in minimal time with custom designed tool. Multiple bugs filed in DUT by the setup and efforts are appreciated by DS-Korea VP Yoo.
- **2nd prize in the event papier** *@(Convolution) conducted by JU Electrical Engg. department sponsored by IET & IEEE Signal Processing Society* | ₹ 3000 | Cert
- **Qualifier** *@NTSE,MHRD*
- **1st prize in mathematics twice** *@South Point High School,Kolkata*

Technical Skills

Languages: Verilog, System Verilog, Python, C/C++, Shell, TCL, Make, Java, HTML/Js/CSS, LaTeX
Verification methodologies & Software frameworks: UVM, Heroku, Flask
Developer Tools: Git, Bitbucket Docker, Google Cloud Platform, VS Code, Visual Studio, DVT Eclipse IDE
Protocols: AMBA, UFS, PCIe, NVMe I2C, SPI, UART, SMBUS | **Analog design simulation**: cadence virtuoso, tanner
Simulators: cadence xcelium, synopsys vcs, mentor questasim | **Waveform debugger**: simvision, verdi | **Fpga**: xilinx SDx, vivado, ISE |
Synthesis: synopsys dc, yosys | **Revision control**: git, svn | **Agile**: atlassian jira, Xray