SOHAM MONDAL

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EXPERIENCE

Senior Engineer (Exp - 2yrs) June 2019 – Present

Samsung Semiconductor India R&D *Bangalore, India*

- (Memory Controller Group) SoC design and verification using SV,UVM for NVMe SSD controllers
- Completely owned End-to-End coverage driven verification of AMBA slaves of NOC/NIC
- Integrated Cadence UVCs and configured them as needed
- **Developed python based tool in collaboration with Samsung HQ team for automated error-free verification & automatic testbench creation with all necessary DUT-VIP connections and components ready for NOC/NIC slave verification for an enterprise SSD SoC with large number of slaves. Reduced the Time-to-First-Test & Time-to-Market by almost 100% and facilitated meeting of verification goal quickly | Setup has been extensively used by Samsung DS Korea and appreciated by Memory VP Samsung | Won 3rd prize in Samsung Global One Solution Virtual Conference in work smart category for whitepaper presentation Cert**
- Revamped flagship UFS SoC testbench setup, managed testplan, testcases creation for Unipro, functional coverage and took part in testbench integration
- Took complete ownership of peripherals I2C & UART UVC development and complete verification of the same
- Hands-on in understanding design specification & development of comprehensive testplan & UVM compliant UVC development & DV automation

Associate Engineer (Exp - 3months) May. 2018 – July 2018

Samsung Semiconductor India R&D *Bangalore, India*

- (DRAM h/w) - Researched to improve proprietary MBIST & architecture with new features | Developed (microarchitecture+RTL) glue logic IP to facilitate forward compatibility of MBIST commands from DDR3 to DDR4 in fpga for proof of concept
- Received Pre-placement offer on basis of work Offer

TECHNICAL SKILLS & CERTIFICATES

Languages: Verilog, System Verilog, Python, Shell, C, C++, Make, TCL, LaTeX, Html/Css/js

Verification methodologies: UVM

Dev Tools: VS Code, Vim, DVT Eclipse IDE

Protocols: AXI3&4, AHB, Unipro, UFS, Mphy, ToggleNAND, I2C, SPI, UART, DDR | **Concepts**: High Performance computer architecture, ARM ISA | **Simulators**: cadence xcelium, mentor questasim | **Waveform debug**: simvision, verdi **Fpga**: Vivado | **Synthesis**: synopsys dc | **VCS**: git, svn | **Agile**: Atlassian jira, Xray | **Certificates**: Cert1 Badge1 Badge2

EDUCATION

Jadavpur University Kolkata, India

Bachelor of Engineering in Electronics and Telecommunications; GPA : 8.13/10 | *Transcripts* *2015 – 2019*

- Bachelor Thesis: Comparative analysis of low power full adders – Under Dr. Chandrima Mondal | Certificate

South Point High School Kolkata, India

W.B.C.H.S.E; 85% and W.B.S.E; 90.28% | *Transcripts* *2014 – 2015*

PUBLICATIONS

PreSyNC: Hardware realization of the Presynaptic Region of a Biologically Extensive Neuronal Circuitry | VLSID-2021(IEEE) | Cert | Code

- Low area & power computationally extensive synaptic data-flow, floating point & posit based accelerator, deep pipelined, clocking 1GhZ in 45nm ASIC

SyNC: A neural net revealing impacts of synaptopathy mechanisms on glutamatergic neurons in autism | Under review, Frontiers

ACHIEVEMENTS

- **3rd prize in smart work category, whitepaper presentation**@*One Solutions Virtual Conference, Samsung R&D Global(memory)* - More than 2600 selected Samsung developers/staffs all around the world as contestants | $500 + Samsung T7 SSD | Cert
- **Employee of the Month(Aug-2020)**@*SSIR,Bangalore* - Slave NOC/NIC automated error free verification of enterprise SSD in minimal time with custom designed tool. Multiple bugs filed in DUT by the setup and efforts are appreciated by DS-Korea memory VP | Cert
- **2nd prize in the event papier**@*(Convolution) conducted by JU sponsored by IET & IEEE Signal Processing Society* | ₹ 3000 | Cert
- **Qualifier**@*National Talent Search Examination,MHRD*

Academic Projects

- **Application specific coprocessor for computationally extensive synapse** Custom ISA, multicycle, floating point, state optimized, ultra-low power and area real time synaptic coprocessor Code (ongoing)[**System-verilog, Verilog, Git**]
  RaspberryPi3b+ & ASIC based brain tumor image classification hardware Inference models highly optimized by novel techniques which can translate to a Rpi3b+ or a novel CNN/DNN ASIC hardware Code(ongoing)[**Tensorflow, Python, Shell, HLS, Git**]

Undergrad Projects

Text search engine (a prototype) | *Java, Maven, Git* | Git
A comparative analysis of public key cryptography | *Matlab* | Git | Paper presentation Jadavpur University 2nd Prize
Marks prediction | *Python, Flask, Heroku* | Git
Dominant color for image segmentation | *Python, Flask, Heroku* | Git
Image Captioning | *Python, Flask, Heroku* | Git
Gui using Tkinter | *Python* | Git-1 Git-2
Medical imaging & digital topology | *C++, Make* | Git
Arduino board projects | *C++, Arduino, Esp8266* | Vid-1 Cert-1 | Vid-2 Cert-2

Other Experience & Extra-curriculars

Network Management@*Nettech pvt. ltd.* (2016, India) | Trained in Network Management & Security Cert
Marketing Management@*IIM Lucknow* (2016, Remote-India) | Marketing Management Internship Under Dr. Sameer Mathur Project
Student Partner@*Internshala* (2016, Remote-India) | Cert
Equity Research@*Money Roller* (2017, Remote-India) | Research about happenings in global financial area Offer
Marketing Analyst@*Qrius* (2018, Remote-India) | Cert
Marketing Expansion Strategy@*Mentored Research* (2017, Remote-India) | Cert
Network management@*ONGC ltd.* (2018, India) | Cert
Student mentor@*Jadavpur University Science Club* (2015-19, India)
Member@*Jadavpur University IET* (2015-19, India)