Soham Mondal

sohammondal39@gmail.com | 8335805583

EDUCATION

JADAVPUR UNIVERSITY
B.E IN Electronics & Telecomm. Engg.

Grad. Dec 2019 | Kolkata, India
CGPA: 8.13/10(First Class)

-Results

SOUTH POINT HIGH SCHOOL
Grad. May 2015 | Kolkata, India

-Higher Secondary(W.B.C.H.S.E)-85%
-Madhyamik(Secondary)
(W.B.S.E)-90.28%

-Results

LINKS

LinkedIn: soham-mondal
Website: soham-mondal

SKILLS & LANGUAGES

•Verilog•Digital Design•OS•Python
•System Verilog•UVM•Bash•Cshell
•GNUMake•CMake•FPGA•ASIC•TcL
•C•C++•Java•EDA•HTML•RaspberryPI

•English,Bengali,Hindi(Standard proficiency & writing skills)

OBJECTIVE

Technology &
Management enthusiast.
Seeking to learn & deliver
value through challenging opportunities.

COURSES

-Digital Topology & Geometry in medical imaging:Theory and Application,GIAN-MHRD

CERTIFICATIONS

Network Management & Security@Nettech Pvt.Ltd
ID-NLP/16/01S/33

MINOR PROJECTS

1)Marks-prediction-dummy-app-heroku-deployment-Link
2)Dominant-Color-for-Image-Segmentation-Link
3)Image Captioning Generating Captions for images using CNN & LSTM on Flickr8K dataset-Link

EXPERIENCE

FULL-TIME

SAMSUNG SEMICONDUCTOR INDIA R&D,BANGALORE(SSIR)
July 2019 - Present (Senior Engineer)

- Team - Storage SoC DV (Controller Host IP/ Memory Solutions)
- Protocols - On-chip-interconnect AMBA AXI3, AXI4, AHBLite
  Host UFS 3.1(UTP12Gbps,2Lane), UFS 4.0, Unipro, MPHY
  Simple peripherals-I2C,SPI (connected to serial flash), UART,SMBUS
- Skills - Automated verification tool development and testbench creation with python with Cadence VIP integrated, python 2.x,python 3.x, modules like pandas,numpy basic text processing/parsing, file manipulation, gui development, end-to-end(e2e) interconnect (NOC,NIC) verification and connectivity checks, scoreboard and monitor creation, knowledge of bus protocols, Cadence VIPs of AMBA AXI3, AXI4,AHB5Lite,I2C,SMBUS,UART,SPI,IWB,scripting languages csh ,bash, tcl/tk, thorough knowledge of gnuMake, verilog, sv, uvm, c++, c, verification of multimillion gates(~60Mn) with unit/c firmware for ARM Cores (M&R series)
  Moderate knowledge of SV-assertions.
  Moderate backend knowledge of STA, pipelining etc.,
- Tools - Cadence Xcelium, Cadence Simvision, Synposys Verdi, Xilinx Vivado, Ultrascale-board, Artix-7 board, Questasim, Modelsim etc.,-Offer

SAMSUNG SEMICONDUCTOR INDIA R&D,BANGALORE
• May 2018 – July 2018 (Student Intern)

- Team - DRAM design
- Responsibilties - Understand MBIST, MBISR architectures applicable for DDR4/5 and take part in knowledge sharing sessions to improve existing Samsung MBIST architecture with new features. Creation of driver/adapter module to facilitate forward compatibility of Samsung DDR3 MBIST to DDR4/5 command sets and functionally verify the same with directed verilog testbench,port & validate the setup in Xilinx Virtex Ultrascale vcu108 fpga board for proof-of-concept.Got a pre-placement offer on basis of work.-Offer letter

NETTECH Pvt.Ltd., Network Management Course | Trainee
Jul 2016

- Trained in computer networks,file management in linux.
  -Certificate

IIM Lucknow
Marketing Management Intern | PROJECT LINK Dec 2016 – Jan 2017

Under Assistant
Prof. Sameer Mathur

Internshala
Internshala Student Partner 6.0 | Offer | Certificate
Aug 2016 – Feb 2017

The Money Roller Equity Research Project Intern | Jun-July 2017

- Researched about the happenings in the global financial area.
  -Offer | -1st term report

4)Classification of brain tumor cells images from MRI machine after applying compressive sampling to reduce data size and training them offline with custom NN and using the inference model in Rpi3b+ to make an exhaustive low power system to detect brain cancer category and put them in medical inventory pipeline to aid doctors. This interdisciplinary research is ongoing under supervision of Dr.Amitava Mukherjee,Present HOD CSE Adamas University,Arnab Raha ,Intel AI/ Movidius, USA and Janet L.Paluh,SUNY PolyTech,USA.

VOLUNTEERING

Student Mentor - JU Science Club

SOCIETIES

IET (Uk) JU Chapter

MINOR EXPERIENCES

1)ONGC Ltd., Trainee Jan 2018 – Feb 2018

• Training in network management system of ONGC zonal office.

- Certificate

2)QRIUS Marketing analyst Jan 2018 – Feb 2018

• -Certificate

2)Mentored Research India Marketing Expansion Strategy Intern | Jan 2017- March 2017

• Marketing and business development efforts.

-Certificate

PRIZES

• 2020 Employee of the Month(SSIR)- For taking complete ownership of slave ELAN(NVME1.4) SSD (~60Mn G.C)E2E(NOC/NIC) completely automated error free verification in minimal time. Multiple bugs filed in DUT and efforts are appreciated by DSKorea VP Yoo. Mentor and tight-coworker Junghwan Ryu(DSKorea)

MAJOR PROJECTS

Neuron Modelling with Post Synaptic Feedback

Hardware Modelling of Neuron Accelerator by taking intraneuronal stochastic parameters consisting of several polynomial approximations and large matrix multiplications in Floating Point IEEE-754 32 bit & 64 bit format and recently developed Posit<32,4> format and making a comparitive study of them in terms of accuracy,precision and sensitivity handling and hardware cost.The designs are pipelined to meet 1.5Ghz frequency in 45nm ASIC platform with low area and cost.This interdisciplinary research is ongoing under supervision of Dr.Amitava Mukherjee,Present HOD CSE Adamas University,Arnab Raha ,Intel AI/ Movidius, USA and Janet L.Paluh,SUNY PolyTech,USA.

Meta-Data based simulation Automation to overcome Verification Challenges of SoC Interconnect Bus Matrix

Python based tool to generate SV/UVM & Cadence AMBA VIP integrated bus-matrix interconnect testbench ,complete test-scenarios with variable transactions exchanged between master and slaves,DUT-VIP connections, compilation & simulation scripts and finally report matrix indicating non-responding slaves all from IPXACT meta-data information.This enables huge reduction of verification efforts and overall time to market for product delivery and meeting verification goal quickly. Setup is extensively used by Samsung DS Korea for fast error free E2E/ interconnect verification of any in-house memory SoC. Link

ACADEMIC PROJECT(Final Year) Under Dr. Chandrima Mondal

Comparative analysis of low power full adders

-Thesis-Certificate Cadence Virtuoso tool , Tanner

Text Search Engine(prototype) Java,Maven

PROJECT LINK

The aim of this project is to build a prototype of a search engine which will work on millions of wikipedia pages(which are in XML format) and retrieves the top 10 relevant wikipedia documents that match the input query.

Automated Street Lighting system using IoT.

LINK Arduino,ESP8266

CERTIFICATE

Wifi Controlled Robot

LINK

CERTIFICATE

A Comparative analysis of public key cryptography

LINK MATLAB

Medical Imaging & Digital Topology

LINK Qt

PRIZES

2020 Won 3rd prize in Work Smart Category by Solution P&D , Memory Business - DSKorea Samsung (OSVC), for whitepaper presentation. One Solution Virtual Conference award is the highest honor that can be bestowed on a developer in Solution Product & Development. More than 2600 staff within solution P&D participated in OSVC forum from global R&D centers across the world.- $500 cash prize+Samsung T5 SSD -Link

2018 Won 2nd prize in the event PAPIER conducted by JU Electrical Engg., IETdepartment Techfest (Convolution) Rs.3000 cash prize. -Prize

2011 Selected for NTSE examination(MHRD)

2010 First prize in mathematics in South Point School

2005 First prize in mathematics in South Point School