# SOHAM MONDAL

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#### **EXPERIENCE**

## Senior SoC Design Verification Engineer

(Exp - 2yrs) June 2019 - Present

Samsung Semiconductor India R&D

Bangalore, India

- · Team (Storage SoC DV) Responsibilities-Design and metric driven verification of SoC memory subsystem with unit firmware
- Completely owned End-to-End coverage driven verification of AMBA slaves of NOC/NIC
- · Integrated Cadence UVCs and configured them as needed
- Developed python and shell based tool in collaboration with Samsung HQ team for automated error-free verification & automatic
  testbench creation with all necessary DUT-VIP connections and components ready for NOC/NIC slave verification for an enterprise
  SSD SoC with large number of slaves. Reduced the Time-to-First-Test & Time-to-Market by almost 100% and facilitated meeting of
  verification goal quickly | Setup has been extensively used by Samsung DS Korea and appreciated by Memory VP Samsung | Won 3rd
  prize in Samsung Global One Solution Virtual Conference in work smart category for whitepaper presentation ppt. Cert
- · Revamped flagship UFS SoC testbench setup, developed testplan for Unipro and took part in testbench integration
- Hands-on in understanding design specification & development of comprehensive testplan & UVM compliant UVC development
- · Hands-on in development of constraint random verification environment, coverage, SV-assertions
- Hands-on in micro-architecture planning and development of state machine ASIP design, | RISC-V, pipelining, STA, graphics architecture

#### **Hardware Intern**

(Exp - 2months) May. 2018 - July 2018

Samsung Semiconductor India R&D

Bangalore, India

- Team (DRAM h/w) Researched to improve proprietary MBIST & MBISR architecture with new features | Developed (microarchitecture+RTL) adapter glue logic IP to facilitate forward compatibility from DDR3/DDR4 in ultrascale vcu-108 fpga for proof of concept
- · Received Pre-placement offer on basis of work Offer

#### TECHNICAL SKILLS & CERTIFICATES

Languages: Verilog, System Verilog, Chisel, Python, Shell, C, C++, Make, TCL, Java, OpenGL LATEX, Html/Css/js

Verification methodologies & Software libraries & frameworks: UVM | Heroku, Flask, Docker, Tensorflow

Dev Tools: VS Code, Docker, Google colab, Vim, DVT Eclipse IDE

Protocols: AXI3&4, AHB, Unipro, UFS, Mphy, ToggleNAND, I2C, SPI, UART, DDR | Concepts: HPC, ASM/FSM, Advanced memory hierarchy | Simulators: cadence xcelium, mentor questasim, synopsys vcs, | Waveform debug: simvision, verdi Fpga: xilinx vivado, HLS | Synthesis: synopsys dc, yosys | VCS: git, svn | Agile: Atlassian jira, Xray | Analog design simulation: virtuoso, tanner | Certificates: Cert1 Badge1 Badge2

#### **EDUCATION**

Jadavpur University Kolkata, India

Bachelor of Engineering in Electronics and Telecommunications; GPA : 8.13/10  $\mid$  Transcripts

2015 - 2019

• Bachelor Thesis: Comparative analysis of low power full adders – Under Dr. Chandrima Mondal | Certificate

South Point High School Kolkata, India

W.B.C.H.S.E; 85% and W.B.S.E; 90.28% | Transcripts

2014 - 2015

### **PUBLICATIONS**

#### PreSyNC: Hardware realization of the Presynaptic Region of a Biologically Extensive Neuronal Circuitry | VLSID-2021 | Code

• Low area & power computationally extensive synaptic data-flow, floating point & posit based accelerator, deep pipelined, clocking 1GhZ in 45nm ASIC | Selected among top five papers

SyNC: A neural net revealing impacts of synaptopathy mechanisms on glutamatergic neurons in autism | Under review, Frontiers

#### ACADEMIC PROJECTS

Application specific coprocessor for computationally extensive synapse | System-verilog, Verilog, Git

• Custom ISA, multicycle, floating point, state optimized, ultra-low power and area real time synaptic coprocessor Code (ongoing)

RaspberryPi3b+ & Fpga based brain tumor image classification setup | Tensorflow, Python, Shell, HLS, Git

• Inference models highly optimized by novel techniques which can translate to a Rpi3b+ or a novel CNN accelerator solution Code (ongoing)

## **ACHIEVEMENTS**

- Among top 5 papers@VLSID\_2021 | Conference
- 3rd prize in smart work category, whitepaper presentation@ One Solutions Virtual Conference, Samsung R&D Global(memory) More than 2600 selected Samsung developers/staffs all around the world as contestants | \$500 + Samsung T7 SSD | Cert
- Employee of the Month(Aug-2020)@SSIR, Bangalore Slave NOC/NIC automated error free verification of enterprise SSD in minimal time with custom designed tool. Multiple bugs filed in DUT by the setup and efforts are appreciated by DS-Korea memory VP
- 2nd prize in the event papier@(Convolution) conducted by JU sponsored by IET & IEEE Signal Processing Society | ₹ 3000 | Cert
- Qualifier@National Talent Search Examination,MHRD

# UNDERGRAD PROJECTS

Text search engine (a prototype) | Java, Maven, Git | Git

A comparative analysis of public key cryptography | Matlab | Git | Paper presentation Jadavpur University 2nd Prize

Marks prediction | Python, Flask, Heroku | Git

Dominant color for image segmentation | Python, Flask, Heroku | Git

Image Captioning | Python, Flask, Heroku | Git

Gui using Tkinter | Python | Git-1 Git-2

Medical imaging & digital topology | C++, Make | Git

Arduino board projects | C++, Arduino, Esp8266 | Vid-1 Cert-1 | Vid-2 Cert-2

#### OTHER EXPERIENCE & EXTRA-CURRICULARS

Network Management @ Nettech pvt. ltd. (2016, India) | Trained in Network Management & Security Cert

Marketing Management @IIM Lucknow (2016, Remote-India) | Marketing Management Internship Under Dr. Sameer Mathur Project

Student Partner@Internshala (2016, Remote-India) | Cert

Equity Research@Money Roller (2017, Remote-India) | Research about happenings in global financial area Offer

Marketing Analyst@ Qrius (2018, Remote-India) | Cert

Marketing Expansion Strategy@Mentored Research (2017, Remote-India) | Cert

Network management@ONGC ltd. (2018, India) | Cert

Student mentor@Jadavpur University Science Club (2015-19, India)

Member@Jadavpur University IET (2015-19, India)