

SOHAM MONDAL

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EXPERIENCE

Senior SoC Design Verification Engineer

June 2019 – Present

Samsung Semiconductor India R&D

Bangalore, India

- Team (Storage SoC DV) Responsibilities-Design and metric driven verification of Controller Host SoC comprising Host subsystem + Flash controller + NAND with unit firmware based on ARM cortex R7 & M7 controllers
- Knowledge in End-to-End coverage driven verification of AMBA slaves of NOC/NIC | monitor & scoreboard creation
- Strong knowledge of Cadence UVCs and integration
- Developed Python and shell based tool in collaboration with cross-cultural HQ team for automated error-free verification & automatic testbench creation for NOC/NIC slave verification for Enterprise NVME1.4 SSD with large number of slaves. Reduced the Time-to-First-Test by almost 100% | Won prize in Samsung Global OSVC conference for whitepaper presentation
- Played significant role in verification of Samsung flagship mobile UFS SoC | testplan development | testbench integration
- Knowledge in Python automation, Makefile, Shell Scripting, TCL
- Hands-on in micro-architecture and state machine based custom controller IP design
- Knowledge of pipelining techniques, STA
- Hands-on in understanding design specification & development of comprehensive testplan & UVM compliant UVC development
- Hands-on in constraint random stimulus, coverage, SV-assertions, formality tool & equivalence check
- Knowledge on protocols like On-Chip (NOC/NIC) AXI3, AXI4, AHB Lite | Host UFS 3.1, UFS 4.0 | Unipro, MPHY, PCIe(low) | Peripherals I2C, SPI, UART, SMBUS | Memory DDR, V-Nand

Hardware Intern

May. 2018 – July 2018

Samsung Semiconductor India R&D

Bangalore, India

- Team (DRAM h/w) - Understood MBIST, MBISR architectures applicable for DDR4/5 and share knowledge sessions to improve proprietary MBIST architecture with new features
- Created driver/adaptor IP to facilitate forward compatibility of DDR3 MBIST to DDR4/5 command sets and functionally verified the same with directed verilog testbench
- Ported & validated the setup in xilinx virtex ultrascale vcu-108 board for proof-of-concept
- Received Pre-placement offer on basis of work [Offer](#)

EDUCATION

Jadavpur University

Kolkata, India

Bachelor of Engineering in Electronics and Telecommunications; GPA : 8.13/10.0

2015 – 2019

- [Bachelor Thesis](#): Comparative analysis of low power full adders – Under Dr.Chandrima Mondal | [Certificate](#)
- [Transcripts](#)

South Point High School

Kolkata, India

W.B.C.H.S.E; 85% and W.B.S.E; 90.28%

2014 – 2015

- [Transcripts](#)

PROJECTS

Meta-Data based simulation Automation to overcome Verification Challenges of SoC Interconnect Bus Matrix

| *Python, Shell, Make, TCL*

2019

- Tool to auto-generate SV-UVM & Cadence AMBA VIP integrated NOC/NIC testbench, complete test-scenarios with almost all forms of transactions supported between master and slaves, DUT-VIP connections, compilation & simulation scripts and report matrix indicating non-responding slaves, from IPXACT DUT information
- Facilitated huge reduction of verification efforts and overall time-to-first-test & time-to-market for product delivery and meeting verification goal quickly. Setup has been extensively used by Samsung DS Korea for fast error free end-2-end NOC/NIC verification of enterprise SSD SoC
- Won 3rd prize in Open Solutions Virtual Conference, Samsung R&D Global (memory) in smart work category for whitepaper presentation [ppt](#). [Cert](#)

ACADEMIC PROJECTS

Application specific controller for computationally extensive synapse | *System-verilog, Verilog, Git*

Dec 2019 – Present

- Hardware design of custom bare-metal controller with custom multicycle floating point ISA and special function to simulate biologically extensive synapse and irregularities in synaptic circuits or pathways
- Custom made micro-architecture for low-area, low-power, reliable, and cycle optimised operation
- State-machine based generic sub-controller design which can be generalised for other complex designs
- Concepts like simple handshake, state-machine, polling has been applied
- Research work is under supervision of Amitava Mukherjee, CSE Adamas University, Arnab Raha, Intel Edge.AI, USA and Janet L.Paluh, SUNY PolyTech, USA [Git](#)

High speed ASIC design for biologically extensive synapse | *System-verilog, Verilog, Python, C++, Shell, Git*

2019

- Hardware design of synaptic accelerator by taking realistic, computationally extensive intra-neuronal parameters in floating point single & double precision & recently developed Posit unum number system (32 bit word with 4 bit exponent size)
- Comparative study in terms of accuracy, precision, sensitivity handling and silicon footprint. The designs are deep pipelined and meets 1 Ghz frequency in 45nm ASIC with extensively optimised area and power [Git](#)

Brain cancer image detection in RaspberryPi3b+ | *Tensorflow, Python, Shell, Git*

Dec 2019 – Present

- Classification of brain cancer images using ML inference model which is greatly optimised for running in Rpi3b+ or resource constrained similar edge devices [Git](#)

UNDERGRADUATE PROJECTS

Text search engine (a prototype) | *Java, Maven, Git* | [Git](#)

A comparative analysis of public key cryptography | *Matlab* | [Git](#) | Paper presentation Jadavpur University 2nd [Prize](#)

Marks prediction | *Python, Flask, Heroku* | [Git](#)

Dominant color for image segmentation | *Python, Flask, Heroku* | [Git](#)

Image Captioning | *Python, Flask, Heroku* | [Git](#)

Gui using Tkinter | *Python* | [Git-1](#) [Git-2](#)

Medical imaging & digital topology | *C++, Make* | [Git](#)

Arduino board projects | *C++, Arduino, Esp8266* | [Vid-1 Cert-1](#) | [Vid-2 Cert-2](#)

ACHIEVEMENTS

- **3rd prize in smart work category, whitepaper presentation**@Open Solutions Virtual Conference, Samsung R&D Global(memory) - More than 2600 selected Samsung developers/staffs all around the world as contestants | \$500 + Samsung T7 SSD | [Cert](#)
- **Employee of the Month(Aug-2020)**@SSIR,Bangalore - Slave NOC/NIC automated error free verification of enterprise SSD in minimal time with custom designed tool. Multiple bugs filed in DUT by the setup and efforts are appreciated by DS-Korea VP Yoo.
- **2nd prize in the event papier**@(Convolution) conducted by JU Electrical Engg. department sponsored by IET & IEEE Signal Processing Society | ₹ 3000 | [Cert](#)
- **Qualifier**@National Talent Search Examination,MHRD
- **1st prize in mathematics twice**@South Point High School,Kolkata

OTHER EXPERIENCE

Network Management@Nettech pvt. ltd. (2016, India) | Trained in Network Management & Security [Cert](#)

Marketing Management@IIM Lucknow (2016, Remote-India) | Marketing Management Internship Under Dr. Sameer Mathur [Project](#)

Student Partner@Internshala (2016, Remote-India) | [Cert](#)

Equity Research@Money Roller (2017, Remote-India) | [Research](#) about happenings in global financial area [Offer](#)

Marketing Analyst@Qrius (2018, Remote-India) | [Cert](#)

Marketing Expansion Strategy@Mentored Research (2017, Remote-India) | [Cert](#)

Network management@ONGC Ltd. (2018, India) | [Cert](#)

Student mentor@Jadavpur University Science Club (2015-19, India)

Member@Jadavpur University IET (2015-19, India)

TECHNICAL SKILLS

Languages: Verilog, System Verilog, Python, Shell, C, C++, Make, TCL, Java, \LaTeX , Html/Css/js

Verification methodologies & Software frameworks: UVM | Heroku, Flask

Dev Tools: VS Code, Docker, Google colab, Vim, DVT Eclipse IDE

Protocols: AMBA, DDR, UFS, I2C, SPI, UART, SMBUS | **Simulators:** cadence xcelium, mentor questasim, synopsys vcs, | **Waveform debug:** simvision, verdi

Fpga: xilinx vivado, HLS | **Synthesis:** synopsys dc, yosys | **VCS:** git, svn | **Agile:** Atlassian jira, Xray | **Analog design simulation:** cadence virtuoso, tanner