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Date: 21/4/22

COA CASE STUDY

Aim: Study of Flip-flop

LO: 6

LO STATEMENT: Design interfacing of peripheral devices with 8086 microprocessor.

Software and Hardware Requirements: TASM Software

Theory:

Flip flop is a sequential circuit which generally samples its inputs and changes its outputs only at particular instants of time and not continuously.

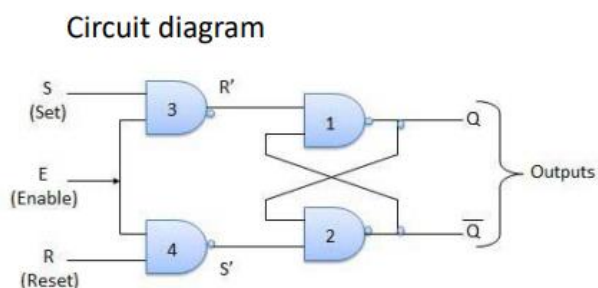
A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs.

There are basically four different types of flip flops and these are:

1. Set-Reset (SR) flip-flop or Latch.
2. JK flip-flop.
3. D (Data or Delay) flip-flop.
4. T (Toggle) flip-flop.

S-R Flip Flop :

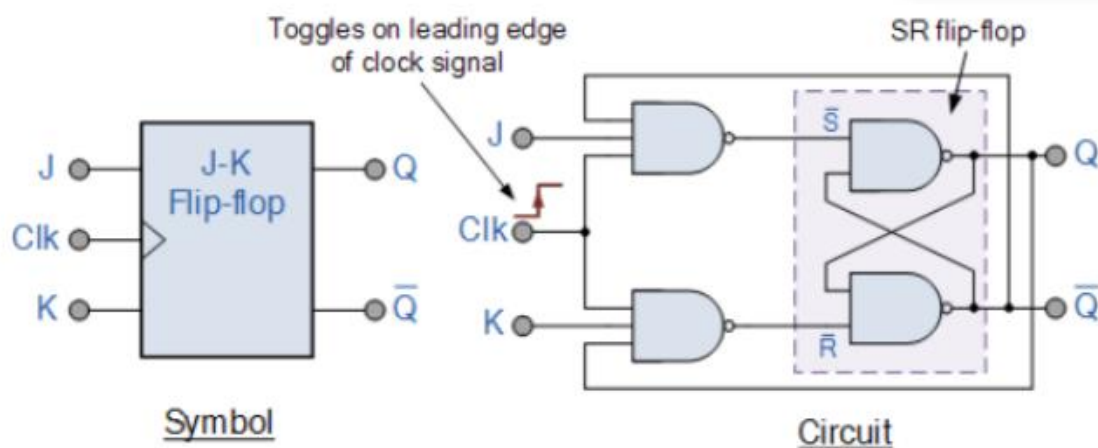
It is basically S-R latch using NAND gates with an additional enable input. For this circuit, output will take place if and only if the enable input (E) is made active. In short this circuit will operate as an S-R latch if $E = 1$ but there is no change in the output if $E = 0$.



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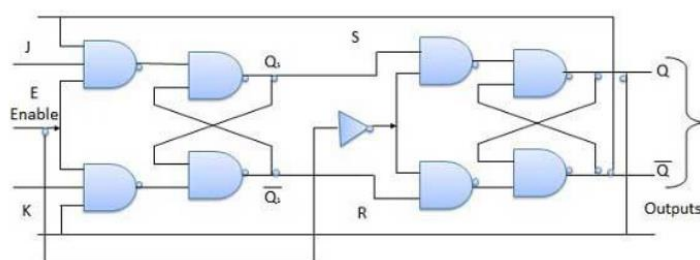
JK Flip-flop :

The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”



Master Slave JK Flip Flop :

Master slave JK FF is a cascade of two S-R FF with feedback from the output of second to input of first. Master is a positive level triggered. But due to the presence of the inverter in the clock line, the slave will respond to the negative level. Hence when the clock = 1 (positive level) the master is active and the slave is inactive. Whereas when clock = 0 (low level) the slave is active and master is inactive.

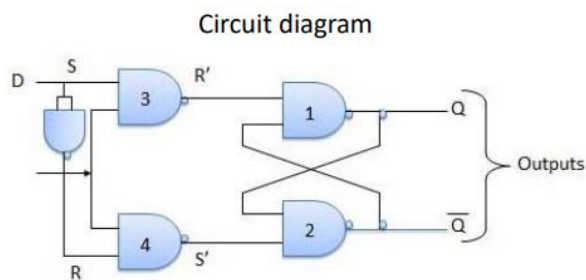


Inputs			Outputs		Comments
E	J	K	Q_{n+1}	\bar{Q}_{n+1}	
1	0	0	Q_n	\bar{Q}_n	No change
1	0	1	0	1	Rset
1	1	0	1	0	Set
1	1	1	\bar{Q}_n	Q_n	Toggle

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Delay Flip Flop / D Flip Flop :

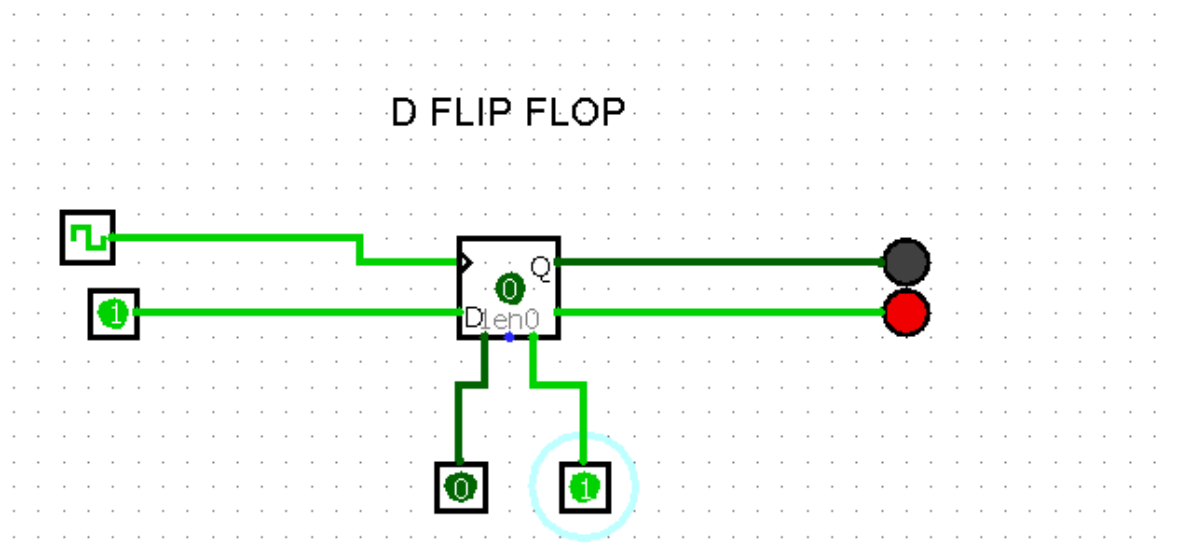
Delay Flip Flop or D Flip Flop is the simple gated S-R latch with a NAND inverter connected between S and R inputs. It has only one input. • The input data is appearing at the output after some time. Due to this data delay between i/p and o/p, it is called delay flip flop. • S and R will be the complements of each other due to NAND inverter. Hence $S = R = 0$ or $S = R = 1$, these input condition will never appear. This problem is avoided by $SR = 00$ and $SR = 11$ conditions.



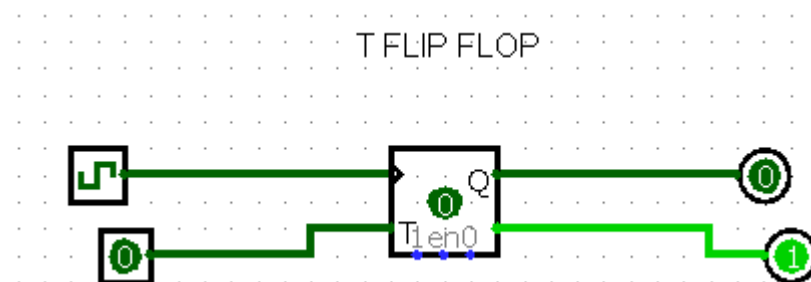
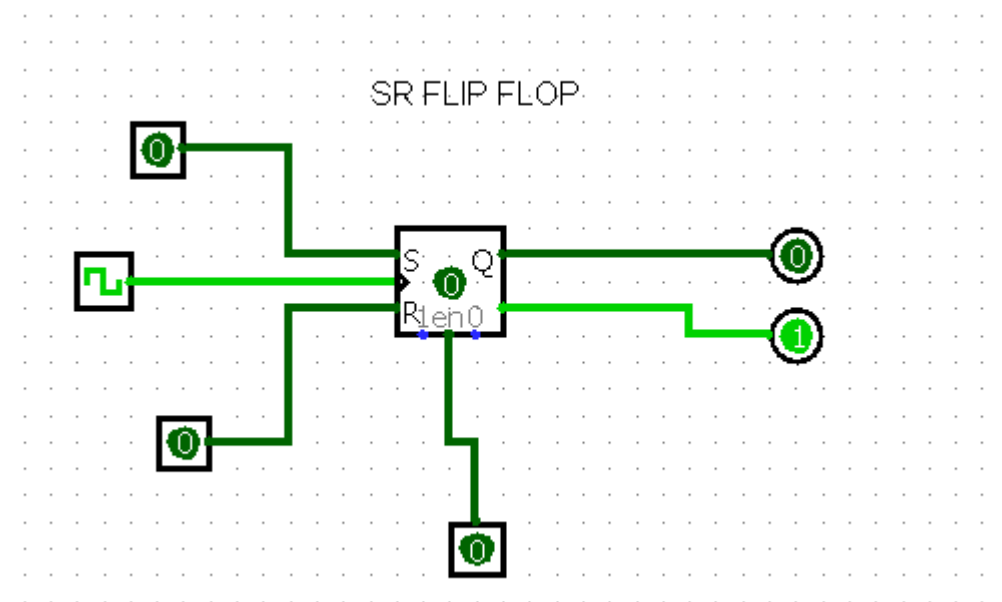
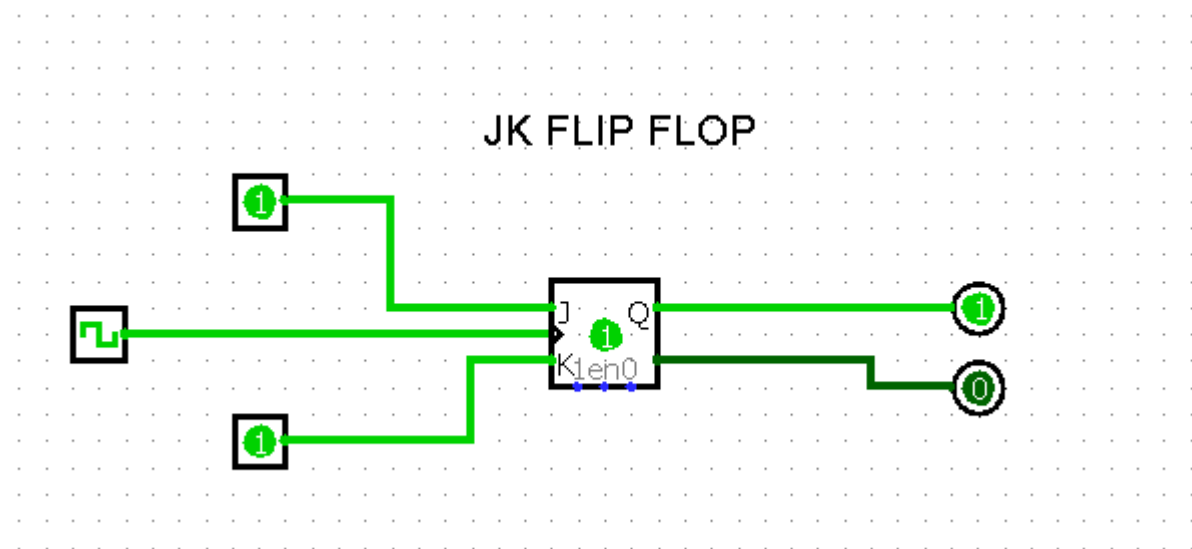
Truth Table

Inputs		Outputs		Comments
E	D	Q_{n+1}	\overline{Q}_{n+1}	
1	0	0	1	Rset
1	1	1	0	Set

Logism Outputs:



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Conclusion: From this study we have learned about the different types of flip flops and also how to design them in Logism software.