VLSI Project Report

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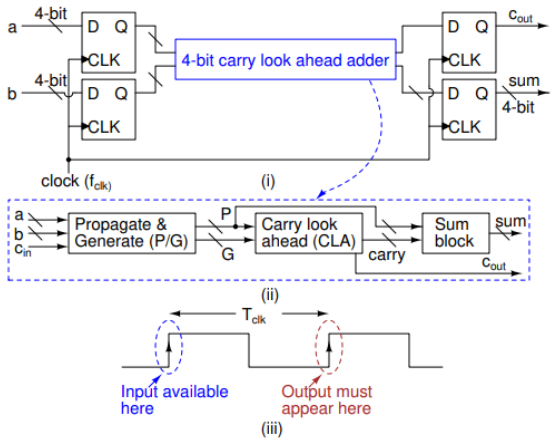
I. Introduction

A 4-bit Carry Look-Ahead (CLA) Adder computes the sum of two 4-bit numbers and outputs a 4-bit sum with a 5th carry bit. Unlike a Ripple Carry Adder, which calculates carries sequentially, the CLA Adder determines all carries simultaneously, minimizing propagation delay.



CLA Block Diagram

II. Proposed Structure for CLA

We need to create Three Blocks that are Carry(c_i), Propagate(p_i) and Generate(g_i)

p_i and g_i are given by

$p_i = a_i \oplus b_i$
$g_i = a_i * b_i$

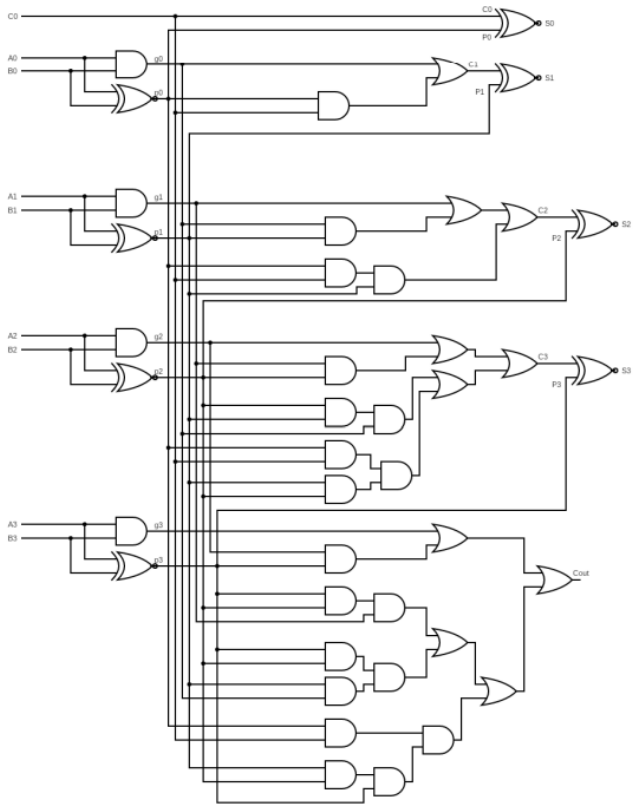
Then we use Propagate and Generate to calculate Carry
$c_{i+1} = p_i * c_i + g_i$

Finally we get all the carries as-
$c_1 = (p_0*c_0) + g_0$
$c_2 = (p_1*p_0*c_0) + (p_1*g_0) + g_1$
$c_3 = (p_2*p_1*p_0*c_0) + (p_2*p_1*g_0) + (p_2*g_1) + g_2$
$c_4 = (p_3*p_2*p_1*p_0*c) + (p_3*p_2*p_1*g0) + (p_3*p_2*g_1) + (p_3*g_2) + g_3$

And the final Sum can be calculated as

$S_i = p_i \oplus c_i$

Now we represent the above circuit as Combination of 2-i/p AND,OR and XOR Gates

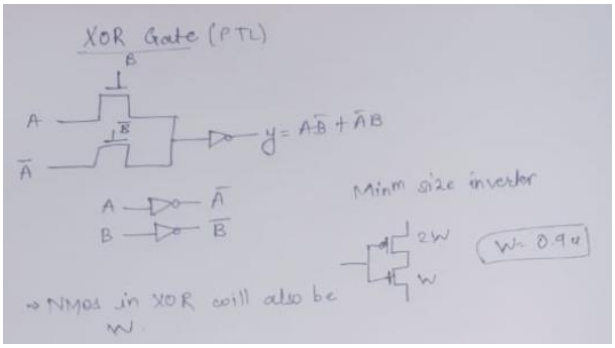


CLA Circuit Diagram

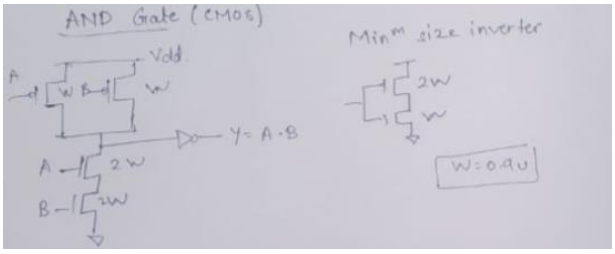
III. Topology and Sizing

A. CLA Combinational Circuit

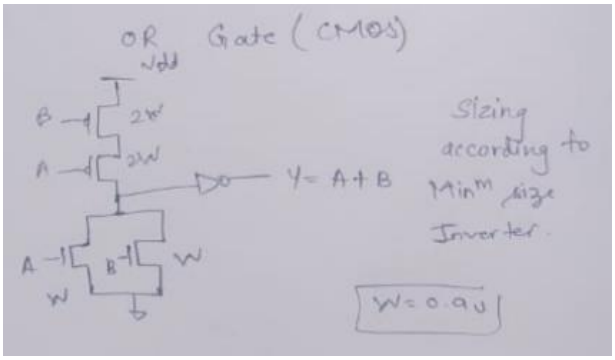
We need 2-input AND, OR and XOR gates for designing the proposed Circuit. AND, OR gates and Inverters are made using CMOS Style and XOR is made using PTL Logic style.



XOR Gate



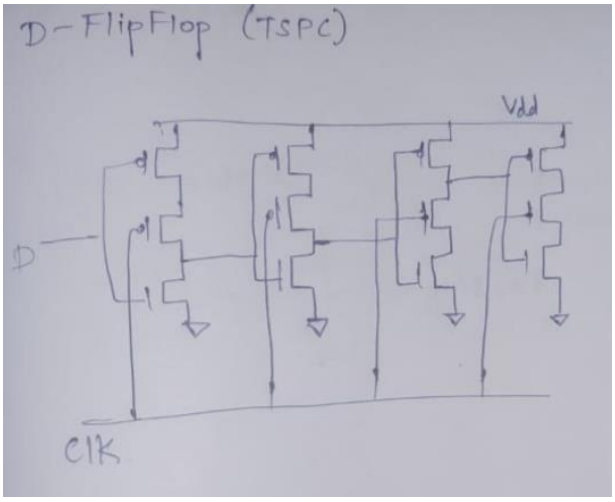
AND Gate



OR Gate

B. D-FlipFlop

We use a TSPC D-flipflop working on Positive Edge. PMOS Width = 40W and NMOS Width = 20W

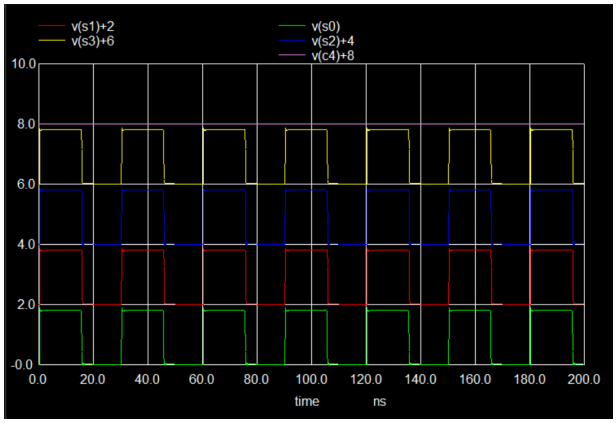


TSPC D-FlipFlop

IV. Pre-Layout Simulations in NGSPICE

A. CLA Combinational Circuit

For eg,we take inputs as 1001 and 0110 and we get output as 01111,hence we verify the working of CLA Circuit in NgSpice.

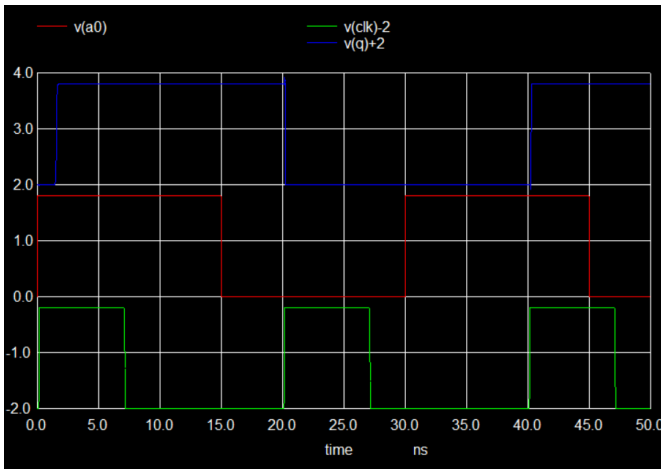


Now to calculate Propagation Delay we give all Inputs as 1 .i.e a=1111,b=1111 , including Cin. So, we get the Delays as Below

```
tpd_carry          =  1.670580e-10 targ=  2.170580e-10 trig=  5.000000e-11
tpd_s3             =  2.674000e-10 targ=  3.174000e-10 trig=  5.000000e-11
tpd_s2             =  2.668316e-10 targ=  3.168316e-10 trig=  5.000000e-11
tpd_s1             =  3.089448e-10 targ=  3.589448e-10 trig=  5.000000e-11
tpd_s0             =  5.456553e-11 targ=  1.045655e-10 trig=  5.000000e-11
```

We have T_{pd}(max)=0.3089 ns and T_{pd}(min)=54.55 ps.

B. D-FlipFlop



Finding T_{PCQ} of the FlipFlop

```
tpcq_min          =  1.153144e-10 targ=  2.316531e-08 trig=  2.305000e-08
tpcq_max          =  1.579699e-10 targ=  3.207970e-09 trig=  3.050000e-09
```

V. Timing Analysis

A.D-Flipflop

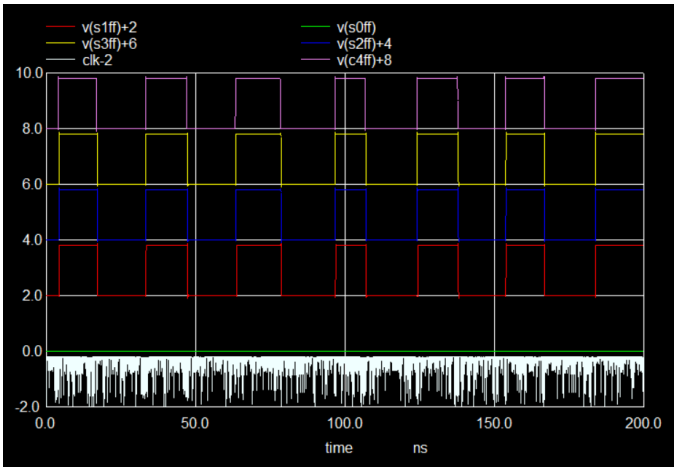
As we have used a TSPC topology while Designing the Flipflop as there is no ~clk involved T_{HOLD} of our Flipflop is zero.

By Hit and Trial we observe that if clock comes before 0.111ns we don't get an output, hence T_{SETUP}=0.111ns.

B.Finding Maximum Clock Frequency

$T_{CLK}(min) = T_{SETUP}+T_{PD}(max)+T_{PCQ}(max)$
$= 0.111+ 0.3089 + 0.1579$ ns
$= 0.5778$ ns

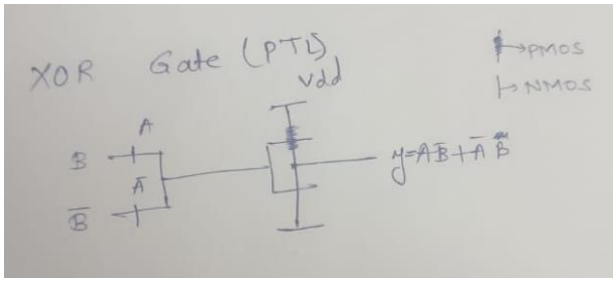
$F_{CLK}(max) = 1/ T_{CLK}(min) = 1.73$ GHz



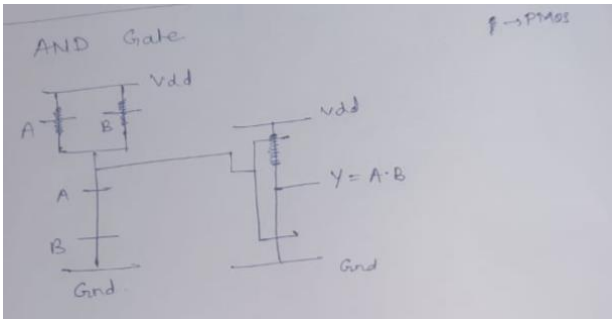
Output at T_{CLK}=0.6ns

We get Reliable Results at T_{CLK}=0.6ns which is quite close to our theoretical Calculations.

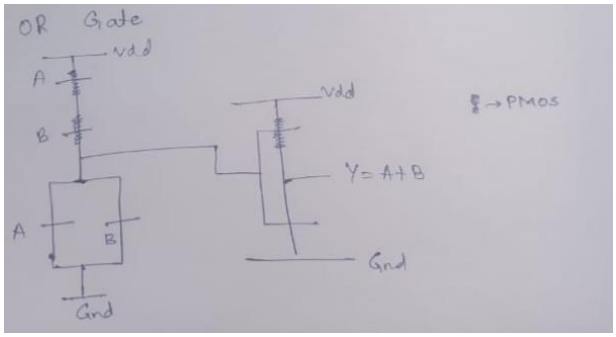
VI. Stick Diagrams for Unique Components



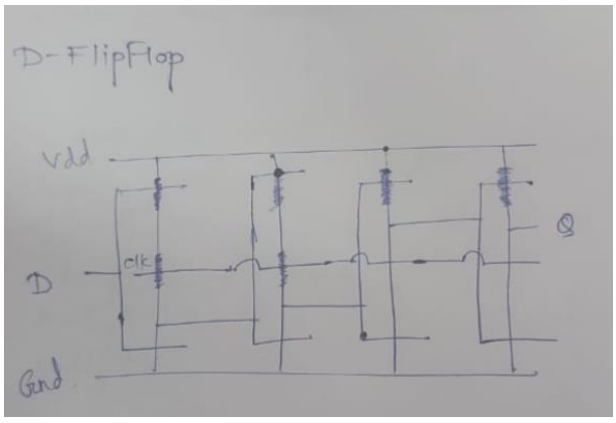
XOR Gate



AND Gate



OR Gate

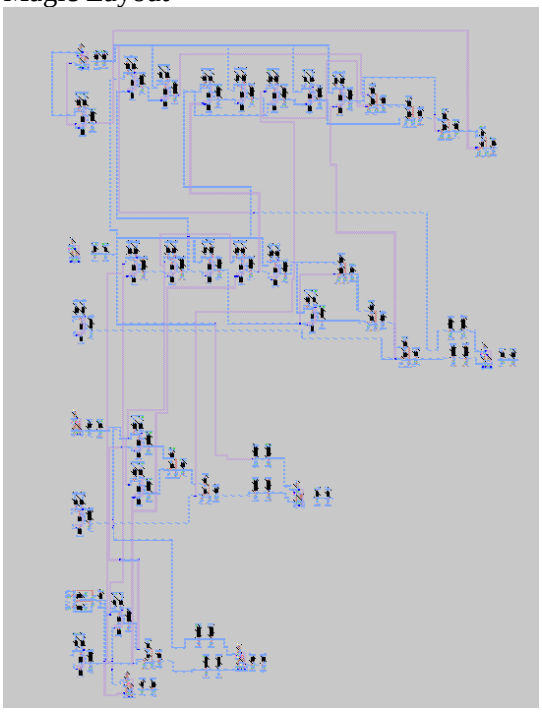


D FlipFlop

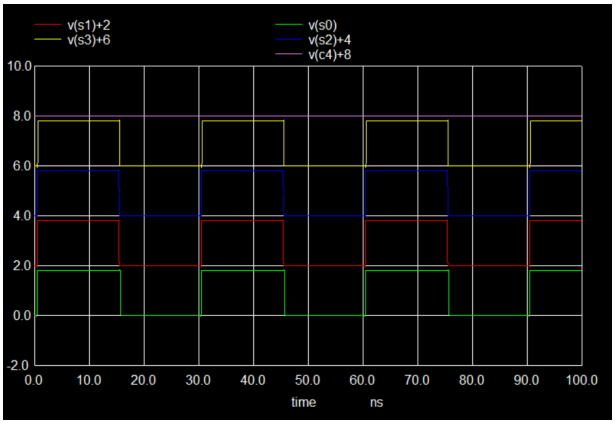
VII. POST LAYOUT SIMULATIONS

A. *CLA Combinational Circuit*

Magic Layout-



First,we test the same input that we used Pre-Layout i.e 1001 and 0110



CLA output for a=1001 and b=0110

Our CLA is working fine Post-Layout.

Lets Take more case as 0111,0111 and 1111,1111 we can verify the output is 01110 and 11110.Hence, our CLA is functioning Properly.

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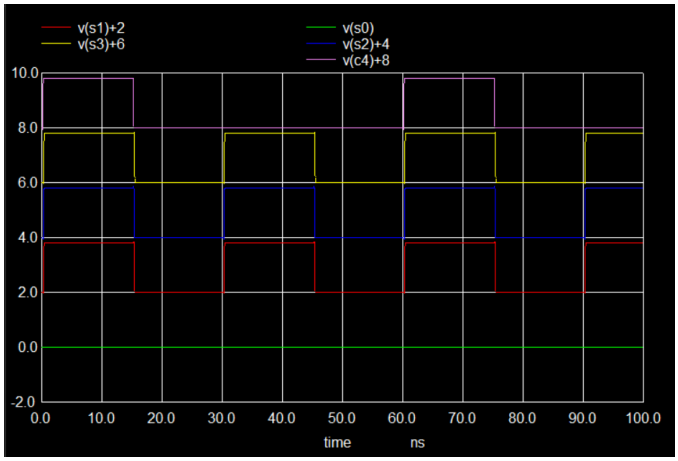


CLA output for a=1111/0111 and b=1111/0111

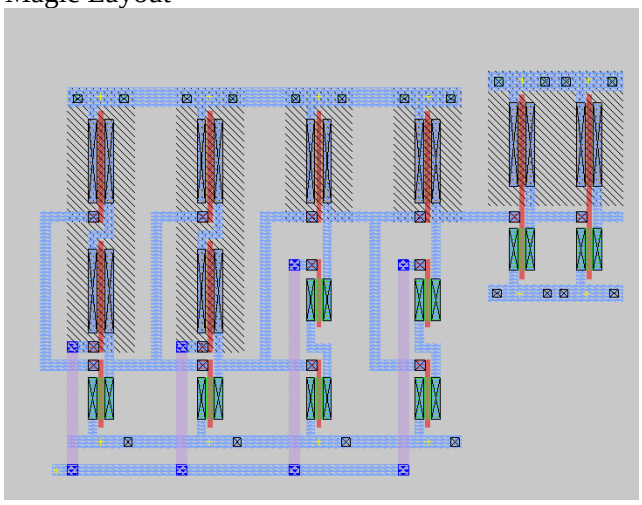
Now to calculate Propogation Delay we give all Inputs as 1 .i.e a=1111,b=1111 , including Cin. So,we get the Delays as Below

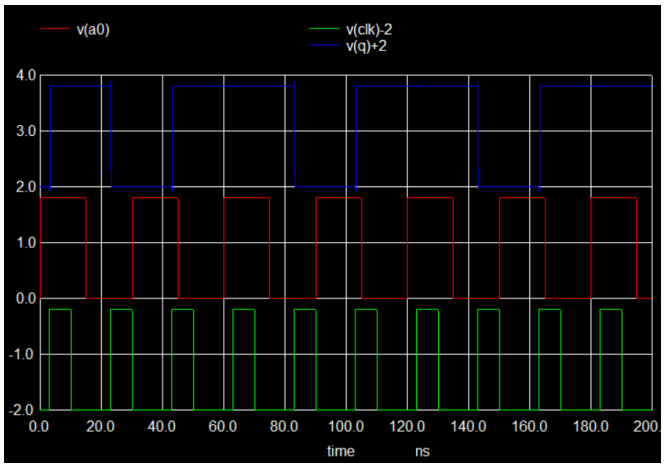
```
No. of Data Rows : 10016
  Measurements for Transient Analysis
tpd_carry           =  1.548711e-10 targ=  1.598711e-10 trig=  5.000000e-12
tpd_s3              =  4.306739e-10 targ=  4.356739e-10 trig=  5.000000e-12
tpd_s2              =  3.868852e-10 targ=  3.918852e-10 trig=  5.000000e-12
tpd_s1              =  4.080594e-10 targ=  4.130594e-10 trig=  5.000000e-12
tpd_s0              =  1.077756e-10 targ=  1.127756e-10 trig=  5.000000e-12
```

We have T_{pd}(max)=0.430 ns and T_{pd}(min)=0.154 ns

B. *D-FlipFlop*

Magic Layout-






```
tpcq_min            =  1.196361e-10 targ=  6.023564e-08 trig=  6.011600e-08
tpcq_max            =  1.691219e-10 targ=  4.028512e-08 trig=  4.011600e-08
```

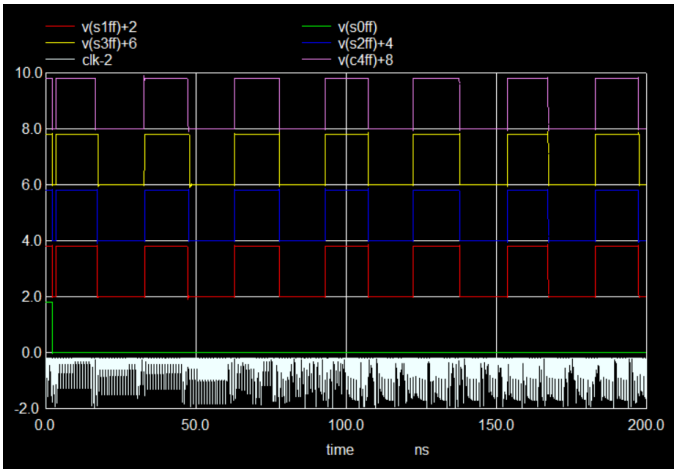
As we have used a TSPC topology while Designing the Flipflop as there is no ~clk involved T_{HOLD} of our Flipflop is zero.

By Hit and Trial we observe that if clock comes before 0.111ns we don't get an output, hence T_{SETUP}=0.117ns.

Finding Maximum Clock Frequency

$T_{CLK}(min) = T_{SETUP}+T_{PD}(max)+T_{PCQ}(max)$
$= 0.117+ 0.430 + 0.1691$ ns
$= 0.7161$ ns

$F_{CLK}(max) = 1/ T_{CLK}(min) = 1.39$ GHz

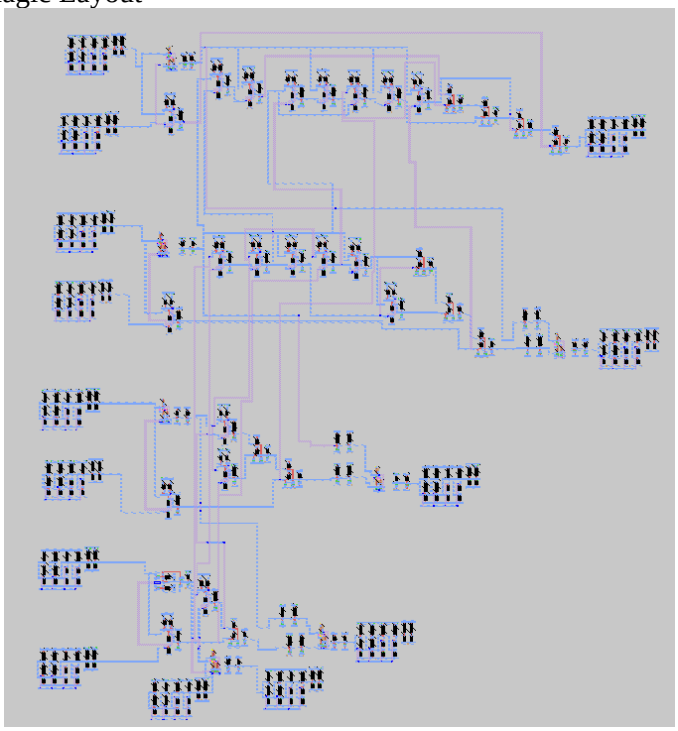


Output at T_{CLK}=0.9ns

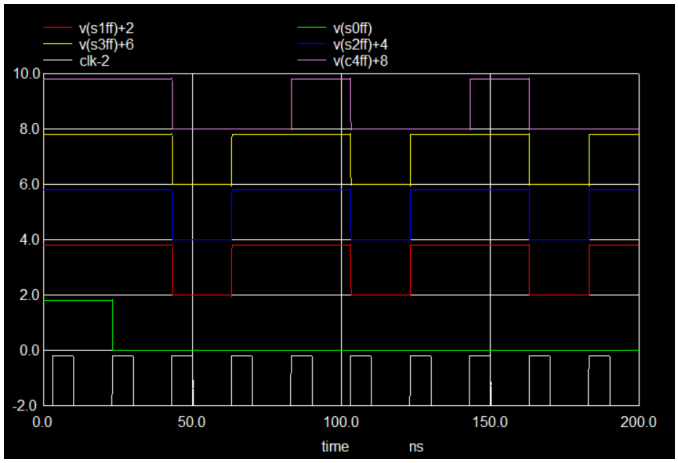
We find for the inputs a=1111 and b=1111 we find Reliable Outputs for T_{CLK}=0.9 ns.

C. *Final Circuit*

Magic Layout-



Let's Take test case as 0111,0111 and 1111,1111 we can verify the output is 01110 and 11110.Hence, our CLA is functioning Properly



Output for a=0111/1111 and b=0111/1111

Horizontal Pitch=256.32 um
Vertical Pitch=283.68 um

VIII. PRE AND POST LAYOUT COMPARISONS

	Pre Layout	Post Layout
T_{PD}(max)	0.3089 ns	0.430 ns
T_{PD}(min)	0.054 ns	0.154 ns

	Pre Layout	Post Layout
T_{PCQ}(max)	0.157 ns	0.169 ns
T_{PCQ}(min)	0.115 ns	0.119 ns

	Pre Layout	Post Layout
F_{CLK}(max) theoretical	1.73 GHz	1.39 GHz
F_{CLK}(max) observed	1.66 GHz	1.11 GHz

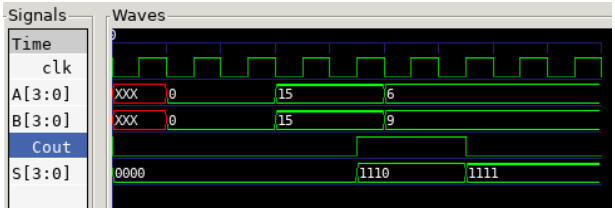
IX. VERILOG SIMULATIONS

We test the Verilog Circuit with inputs a=1111,b=1111 and a=0110,b=1001

```
Reset = 0 | A = 1111 | B = 1111 | Cout = 0 | S = 0000
Reset = 0 | A = 1111 | B = 1111 | Cout = 1 | S = 1110
Reset = 0 | A = 0110 | B = 1001 | Cout = 1 | S = 1110
Reset = 0 | A = 0110 | B = 1001 | Cout = 0 | S = 1111
```

Verilog Output

Now plotting the Waveform of these Outputs



GTKWave Output

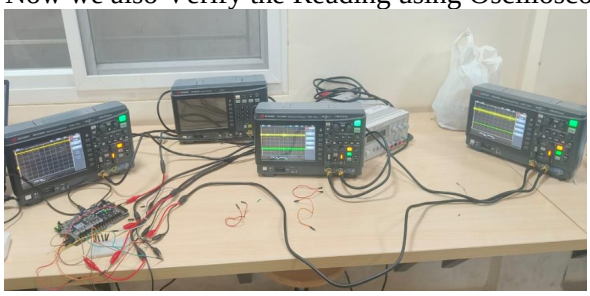
We can Observe that after input comes, we get output on next +ve clock edge. 15+15=11110 and 6+9=01111

X. FPGA SIMULATION

We give input as 7 and 10 in FPGA

FPGA Output

We can see the output 10001(17).
Now we also Verify the Reading using Oscilloscope.

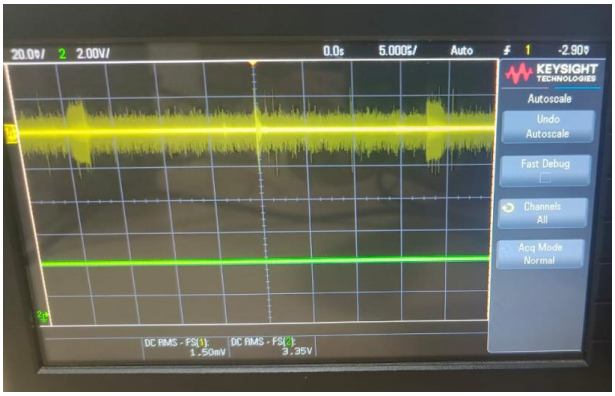


Oscilloscope Outputs

Oscilloscope Readings:
Output>3.2V is considered high i.e 1

Cout=1

S3=0 and S2=0



S1=0 and S0=1

The output is 10001.

ACKNOWLEDGMENT

I would like to express my gratitude to **Prof. Abhishek Srivastava** and VLSI-D TAs for their invaluable guidance and mentorship throughout the course and this project.

REFERENCES

[1] Digital Logic and Computer Design by Morris Mano
[2] Verilog HDL - Samir Palnitkar
[3] Various IEEE Papers