1. 16 kB per wireOut, and 512kB if all 32 registers are used.
2. 20 kB per wireIn, 640kB if all 32 registers are used. Retrieved from table below:

Measured Performance (CPS = Calls Per Second)

API Call	USB 3.0 (CPS)	USB 2.0 (CPS)	PCIe (CPS)
UpdateWireIns	5,000+	1,000+	4,000+
UpdateWireOuts	4,000+	800+	3,000+
ActivateTriggerIn	8,000+	2,000+	66,000+
UpdateTriggerOuts	4,000+	800+	3,000+

3. Here is the table from lab 2 project summary.

Resource	Utilization	Available	Utilization %
LUT	1059	47200	2.24
LUTRAM	32	19000	0.17
FF	1113	94400	1.18
BRAM	2	105	1.90
IO	55	285	19.30
BUFG	4	32	12.50
MMCM	1	6	16.67

   The biggest difference is in the number of LUT and FF (1059 vs 30, 1113 vs 33, respectively). We also used LUTRAM, BRAM, MMCM, in lab 2 which was not used in the first lab.
4. 4294967295 is the max value a 32 bit register can hold. The sum should not exceed this value. We tried this, and if the sum does exceed the value then the result overflows to a smaller value.