

Quadrature Down-converter for Wireless Communications

by

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Abstract

Future generation of wireless systems will feature high data rates and be implemented in low voltage CMOS technologies. Direct conversion receivers (DCRs) will be used in such systems which will require low voltage RF front-ends with adequate linearity. The down-converter in a DCR is a critical block in determining linearity. In addition to detailed DCR modeling in MATLAB, this thesis, completed in 2005, deals with the design and characterization of a 1V, 8GHz quadrature down-converter. It consists of two mixers and a quadrature generator implemented in a $0.18\mu\text{m}$ CMOS technology.

The mixer architecture proposed in this work uses a new trans-conductor. It simultaneously satisfies the low voltage and high linearity requirements. It also relaxes the inherent trade-off between gain and linearity governing CMOS active mixers. The implemented mixer occupies an area of $320 \times 400 \mu\text{m}^2$ and exhibits a power conversion gain of +6.5dB, a P-1dB of -5.5dBm, an IIP3 of +3.5dBm, an IIP2 of better than +48dBm, a noise figure of 11.5dB, an LO to RF isolation of 60dB at 8GHz and consumes 6.9mW of power from a 1V supply.

The proposed quadrature generator circuit features a new architecture which embeds the quadrature generation scheme into the LO-buffer using active inductors. The circuit offers easy

tune-ability for process, supply and temperature variations by relaxing the coupling between amplitude and phase tuning of the outputs. The implemented circuit occupies an area of $150 \times 90\mu\text{m}^2$ and exhibits an amplitude and quadrature phase accuracy of 1 dB and 1.5° respectively over a bandwidth of 100 MHz with a power consumption of 12mW from a 1V supply including the LO-buffer.

The quadrature down-converter features an image rejection ratio of better than 40 dB and satisfies the potential target specifications of future mobile phones, extracted in this work.

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Table of Contents

	Page
CHAPTER 1 Introduction	1
1.1 Receiver Architecture	3
1.2 Mixer Architectures	8
1.2.1 Active Mixers vs. Passive Mixers.....	8
1.2.2 Mixer Performance Metrics	10
1.2.3 Previous Work on CMOS Active Mixers	14
1.3 Quadrature Generators	18
1.3.1 Quadrature Generator Performance Parameters	19
1.3.2 Previous Work on Quadrature Generators.....	19
1.4 Objectives and Outline of the Thesis	26
CHAPTER 2 Down-converter System Level Simulation	33
2.1 Introduction.....	33
2.2 OFDM Communication System	33
2.3 DCR Behavioural Modeling	36
2.4 Simulation Results	37
2.5 Summary	42
CHAPTER 3 CMOS Down-conversion Mixer	45
3.1 Introduction.....	45
3.2 Current Commutating Mixers	45
3.2.1 Trans-conductor	47
3.2.2 Mixing Stage	47

	Page
3.2.3 Trans-resistance Stage	48
3.3 CCM Linearization Techniques.....	48
3.3.1 Source Degeneration (SDE).....	49
3.3.2 Dynamic Matching (DMA).....	49
3.3.3 Cross-coupled Trans-conductors (CCT).....	50
3.3.4 Trans-conductor using a CMOS Pair (CMP).....	51
3.3.5 Class AB Trans-conductor (ABT)	52
3.3.6 Summary	53
3.4 Low-Voltage, High Linearity Mixer Design Issues.....	54
3.4.1 Effect of the trans-resistance Stage on the Linearity of CCM	54
3.4.2 Effect of the Mixing Stage on the Linearity of the CCM	54
3.4.3 Effect of the Trans-conductor on the linearity of the CCM.....	55
3.5 Proposed Mixer and Design Methodology	57
3.5.1 Background	57
3.5.2 Novel Mixer Architecture	58
3.6 Layout	64
3.6.1 High Frequency Layout Considerations	65
3.6.2 Layout Considerations for Best Linearity Performance	65
3.6.3 Mixer Layout	66
3.7 Post Layout Simulation.....	68
3.8 Summary	72
CHAPTER 4 CMOS Quadrature Generator	75
4.1 Introduction.....	75
4.2 Conventional Quadrature Generator	75
4.3 Novel Quadrature Generator Architecture.....	78
4.4 Design and Analysis of the Proposed Quadrature Generator	80
4.5 Layout of the Quadrature Generator	86
4.6 Post Layout Simulations	87
4.7 Summary	91

	Page
CHAPTER 5 Implementation and Experimental Results	93
5.1 Introduction.....	93
5.2 Mixer Implementation and Characterization	93
5.3 Quadrature Generator Implementation and Characterization	104
5.4 Quadrature Down-converter Implementation and Characterization.....	111
5.5 Summary	114
CHAPTER 6 Conclusion.....	123
APPENDIX A Design Ported to TSMC CMOS 65nm Technology	127
A.1 Introduction.....	127
A.2 Summary	130

List of Tables

	Page
Table 1.1: Mobile Phone Generations	2
Table 1.2: Tentative Target Specifications for a Mixer and Quadrature Generator Potentially Suitable for Future Mobile Phone Receivers	7
Table 1.3: A Comparison Between Generic Types of CMOS Mixers	9
Table 1.4: State of the Art Implementation of Various Mixer Architectures	18
Table 1.5: State of the Art Quadrature Generators	26
Table 2.1: Specifications of the OFDM System under Consideration	35
Table 2.2: Assumed LNA Characteristics	36
Table 2.3: Tentative Specifications of the Mixer and Quadrature Generator.....	42
Table 3.1: Target Specifications and Post Layout Simulations	70
Table 3.2: Effect of Process Variations on the Performance of the Mixer	71
Table 3.3: Effect of Temperature Variation on the Performance of the Mixer...	71
Table 4.1: Comparison between Target Specification and Post Layout Simulation for the Quadrature Generator	90
Table 4.2: Effect of Process Variation on the Performance of the Quadrature Generator.	90
Table 4.3: Effect of Temperature Variation on the Performance of the Proposed Quadrature Generator	91
Table 5.1: Comparison of the Low Voltage Mixer of this Work with Other Low Voltage Mixers using Different Architectures (up to 2005)	100
Table 5.2: Comparison of the Low Voltage Mixer of this Work with Other Low Voltage Mixers using Different Architectures (2005 to 2011)	101
Table 5.3: Comparing the Linearity Characteristics of the Proposed Mixer and the Conventional CCM [7,52]	102

	Page
Table 5.4: Comparison of the Proposed Quadrature Generator to Previous Work up to 2004	109
.....
Table 5.5: Comparison of the Proposed Quadrature Generator to Previous Work up to 2011	110
.....
Table 5.6: I/Q Amplitude and Quadrature Phase Error Obtained from the IRR Method and the Time Domain Characterization.....	113
Table 5.7: Quadrature Down-converter (QD) compared to other DCRs targeting similar applications.....	113
Table A.1: Down-converter comparison.....	128
Table A.2: Quadrature Down-converter port to 65nm technology	129

List of Figures

	Page
Fig. 1.1: Effect of nonlinear RF front-end on the spectrum of the received signal	2
Fig. 1.2: Typical architecture of a direct conversion receiver (DCR)	4
Fig. 1.3: The LO to RF leakage due to poor LO-RF port isolation	5
Fig. 1.4: The effect of AC-coupling on WCDMA and OFDM communication systems....	5
Fig. 1.5: Current commutating mixer. (a) Block diagram. (b) Typical CMOS implementation	14
Fig. 1.6: Harmonic mixer	15
Fig. 1.7: Dual gate mixer. (a) Block diagram. (b) Typical CMOS implementation.....	16
Fig. 1.8: Back gate mixer. (a) Block diagram. (b) Typical CMOS implementation	17
Fig. 1.9: RC-CR filter used as quadrature generator. (a) Circuit diagram. (b) Phase of the transfer function of the two outputs. (c) Magnitude of the transfer function of the two outputs	20
Fig. 1.10: Single stage polyphase filter used as quadrature generator	21
Fig. 1.11: Haven's technique for generating quadrature signals	22
Fig. 1.12: Frequency division technique	23
Fig. 1.13: Ring oscillator quadrature generator	24
Fig. 1.14: I-Q signal generator architecture using CON	25
Fig. 1.15: Quadrature LC-oscillator	25
Fig. 2.1: Typical OFDM communication system.	34
Fig. 2.2: Typical direct conversion receiver block diagram.	34
Fig. 2.3: OFDM modulator and demodulator block diagram.	35
Fig. 2.4: SNR vs. phase noise of the mixer LO CLK.	38
Fig. 2.5: Mixer LO phase noise mask meeting BER spec of 10^{-3}	38
Fig. 2.6: Receiver BER versus quadrature phase error.....	39

	Page
Fig. 2.7: System-level SNR in terms of mixer linearity	40
Fig. 2.8: Overall system noise figure in terms of mixer noise figure	41
Fig. 3.1: Current commutating mixer (CCM). (a) Block diagram of the CCM. (b) Conventional MOS implementation of the CCM	46
Fig. 3.2: Various conventional possibilities to implement the trans-conductance stage of a CCM. (a)-(c) Common gate implementations. (d)-(f) Common source implementations	47
Fig. 3.3: Cross-coupled differential pairs as mixing stage	48
Fig. 3.4: Conventional CCM using source degeneration for linearizing the mixer	49
Fig. 3.5: Linearized CCM using dynamic matching	50
Fig. 3.6: Linearized CCM using cross-coupled transconductors	51
Fig. 3.7: Linearized CCM using the CMOS pair	52
Fig. 3.8: Linearized CCM using a class AB transconductor	53
Fig. 3.9: Conventional transconductor in CCM. (a) Circuit diagram. (b) Actual and ideal I_V transfer characteristics. (c) Actual and ideal transconductance	55
Fig. 3.10: The original form of the bias-offset technique applied to a CMOS differential pair transconductor [16]	58
Fig. 3.11: The proposed transconductor for the CCM. (a) The bias-offset technique for M1 and M2 (M3 and M4) using a floating voltage source. (b) The complete circuit diagram of the new differential transconductor using the bias-offset technique	59
Fig. 3.12: Normalized G_m as a function of V_{inp}	61
Fig. 3.13: V_{offset} as a function of the ratio of the aspect ratio, α , of the transistors building the floating voltage source	61
Fig. 3.14: Transconductance of the RF transconductor, G_m , for three different values of the offset voltage. The flat transconductance ($V_{offset}=750\text{mV}$) was obtained for $(W/L)_1=32\mu\text{m}/0.18\mu\text{m}$, $(W/L)_2=20\mu\text{m}/0.18\mu\text{m}$, $(W/L)_5=30\mu\text{m}/0.25\mu\text{m}$, $(W/L)_6=16\mu\text{m}/0.18\mu\text{m}$	63
Fig. 3.15: Schematic of the Proposed Mixer. (M1, M3 : 32/0.18; M2, M4 : 20/0.18; M5, M7: 30/0.25; M6, M8 : 16/0.18; M9, M10, M11, M12 : 8/0.18; all dimensions are in microns. $L=0.5\text{ nH}$; $C1=1\text{pF}$, $C2=8\text{pF}$, $C3=0.8\text{ pF}$, $C4=2\text{pF}$, $R=500\Omega$)	64

	Page
Fig. 3.16: Layout consideration to achieve best linearity performance	66
Fig. 3.17: Layout of the proposed mixer	67
Fig. 3.18: Layout of the integrated spiral inductor designed using the ADS software.....	67
Fig. 3.19: (a) Spiral integrated inductor. (b) Lumped model at 8 GHz for post layout simulation	68
Fig. 3.20: Two-tone simulation revealing an IIP3 of +2 dBm	69
Fig. 3.21: Power transfer characteristics of the mixer illustrating a simulated P-1dB of -10 dBm and a PCG of +12 dB	69
Fig. 4.1: Quadrature generation components embedded in the LO buffer	76
Fig. 4.2: Block diagram of the quadrature generator under consideration	78
Fig. 4.3: Differential active inductor implementation based on the G_m -C architecture.....	79
Fig. 4.4: Common-mode stabilizer circuit	80
Fig. 4.5: Small signal model of the MOST in the active region of operation	80
Fig. 4.6: Circuit of the quadrature generator. (M_1 to M_8 : 10/0.18; M_{21} , M_{22} , M_{24} and M_{25} : 9/0.18; M_{13} , M_{14} , M_{19} and M_{20} : 12/0.18; M_9 to M_{12} : 5/0.18; M_{15} to M_{18} : 12/0.18; M_{23} and M_{26} are zero threshold voltage devices : 6/0.5; all dimensions are in μm . $V_{dd}=1\text{V}$, $V_B=750\text{mV}$, $V_{B1}=150\text{mV}$, $V_{B2}=0$, $V_C=850\text{mV}$	81
Fig. 4.7: Equivalent common mode half circuit of the quadrature generator	84
Fig. 4.8: Post-layout simulation characteristics of the quadrature generator. (a) The magnitude and phase of the transfer function of the four outputs. (b) The time domain quadrature outputs.....	88
Fig. 4.9: Simulation results of the quadrature generator over the bandwidth of interest. (a) The phase of the transfer function of the outputs. (b) The amplitudes of the quadrature outputs.....	89
Fig. 5.1: Micrograph of the mixer.....	94
Fig. 5.2: Conversion gain and 1-dB compression point measurement setup	95
Fig. 5.3: Power transfer characteristics of the mixer illustrating a measured 1-dB compression point of -5.5dBm and a power conversion gain (PCG) of +6.5 dB	96
Fig. 5.4: Two-tone test measurement setup	96
Fig. 5.5: Two-tone test revealing a measured IIP3 of +3.5 dBm versus a simulated IIP3 of +2 dBm.....	97

	Page
Fig. 5.6: Noise figure measurement setup	98
Fig. 5.7: RF port to LO port isolation measurement setup	99
Fig. 5.8: CMOS mixers published in the literature [14-59]. Input referred third order intercept point versus noise.....	103
Fig. 5.9: Proposed CMOS mixer compared to state of the art published work [14-59]. The vertical axis represents linearity over power in decibels	104
Fig. 5.10: Micrograph of the quadrature generator	105
Fig. 5.11: Quadrature accuracy measurement setup	105
Fig. 5.12: Comparison between measurement and simulation results. (a) Quadrature phase. (b) Magnitude of the transfer function of the outputs	106
Fig. 5.13: The time domain measured output of the quadrature generator.....	107
Fig. 5.14: Phase noise measurement setup.....	107
Fig. 5.15: Measured phase noise of the quadrature generator	108
Fig. 5.16: Quadrature generator comparison to previous work [60-81]	110
Fig. 5.17: Micrograph of the fabricated quadrature downconverter	111
Fig. 5.18: Image rejection ratio measurement setup.....	112
Fig. 5.19: Image rejection ratio measurement results over a bandwidth of 100 MHz.....	112
Fig. A.1: CMOS technology threshold voltage and supply voltage scaling.....	128

List of Appendices

	Page
Appendix A: Design Ported to 65nm CMOS Technology	127

Glossary

- ABT: Class AB Trans-conductor
ADC: Analog to Digital Converter
ADS: Advanced Design System
AGC: Automatic Gain Control
BAW: Bulk Acoustic Wave
BER: Bit Error Ratio
BGM: Back Gate Mixer
BPF: Band-Pass Filter
CCM: Current Commutating Mixer
CCT: Cross-Coupled Trans-conductor
CDMA: Code Division Multiple Access
CLK: Clock
CMP: Complementary Metal Oxide Semiconductor Pair
CON: Cellular Oscillator Network
DCR: Direct Conversion Receiver
DGM: Dual Gate Mixer
DMA: Dynamic Matching
DSB: Double Side Band
DUT: Device Under Test
FD: Frequency Division
FDMA: Frequency Division Multiple Access
FFT: Fast Fourier Transform
HAM: Harmonic Mixer
HBT: Hetero-junction Bipolar Transistors
IF: Intermediate Frequency

IFFT: Inverse Fast Fourier Transform
I/Q: In-phase/Quadrature
IIP2: 2nd Order Input Referred Intercept Point
IIP3: 3rd Order Input Referred Intercept Point
IRR: Image Rejection Ratio
ISI: Inter-Symbol Interference
LCQ: LC Quadrature Oscillator
LNA: Low Noise Amplifier
LO: Local Oscillator
LPF: Low-Pass Filter
LPTV: Linear Periodic Time Varying
MMT: Manual Microwave Tuners
MOST: Metal Oxide Semiconductor Transistor
NF: Noise Figure
NL: Non-Linear
OFDM: Orthogonal Frequency Division Multiplexing
PCG: Power Conversion Gain
PPF: Poly-Phase Filter
QD: Quadrature Down-converter
QG: Quadrature Generator
RCF: RC-CR Filter
RF: Radio Frequency
RO: Ring Oscillator
SAA: Subtraction and Addition
SDE: Source Degeneration
SGS: Signal Ground Signal
SNR: Signal to Noise Ratio
SOLT: Short Open Load Through
SSB: Single Side Band
TDMA: Time Division Multiple Access

VCO: Voltage Controlled Oscillator

VGA: Variable Gain Amplifier

WCDMA: Wide-band Code Division Multiple Access

WLAN: Wireless Local Area Network

CHAPTER 1: Introduction

It is generally expected that the number of portable handsets will exceed the number of personal computers (PC) connected to the internet with the deployment of the next generation of mobile phones [1]. The first steps toward this have been taken at the system level to support advanced and wideband multimedia services, which makes low voltage, low power CMOS receivers supporting these systems highly desirable.

Table 1.1 compares some of the tentative specifications of the future mobile phone system (as reported in the literature) to its previous generations. The specifications listed in the table, directly affect the circuit level implementation of radio frequency (RF) receiver front-ends. The future generation of mobile phones is expected to use a data rate of 100 Mbps or more [2]. Depending on the modulation and multiple access scheme applied, this data rate may translate into a bandwidth of 50 MHz or more. This relatively wide bandwidth causes the issue of linearity to become one of the major concerns in the design of RF receiver front ends. Fig. 1.1 is a simple illustration of the way nonlinear RF front-end degrades the performance of the receiver through in-band intermodulation products. Increasing the bandwidth of the RF/IF front-end degrades the linearity characteristics of these circuitry due to increased intermodulation products hitting each desired channel. In addition to intermodulation products, the two horizontal shaded portions of the spectrum show the scaled convolution of the incoming spectrum, causing a widening of the spectrum due to second and third order non-linearities which in turn degrades the quality of the received signal.

Chapter 1 - Introduction

As mentioned in Table 1.1, orthogonal frequency-division multiplexing (OFDM) is a strong candidate for the multiplexing scheme used in future mobile systems [3-5].

Table 1.1 Mobile Phone Generations

Characteristics	1G	2G	3G	Future Mobile Systems*
Spectrum	900MHz	1800MHz	2GHz	2-8GHz
Multiplexing	Analog FDMA	TDMA	CDMA	OFDM
Targeted data rate	N/A	14.4kbits/sec	2Mbits/sec	>100Mbits/sec
Real data rate	2.4kbits/sec	9.6kbits/sec	384kbits/sec	**
Bandwidth	30 kHz	200 kHz	5-20 MHz	50-100 MHz
Modulation	FM	GMSK	QPSK	64QAM
Time frame	1980-1994	1995-2001	2002-2005	> 2010

* These are tentative system level specifications, obtained from the available literature.

** The data rate associated with these mobile systems varies for different conditions. For instance, vehicular data rate versus static data rate.

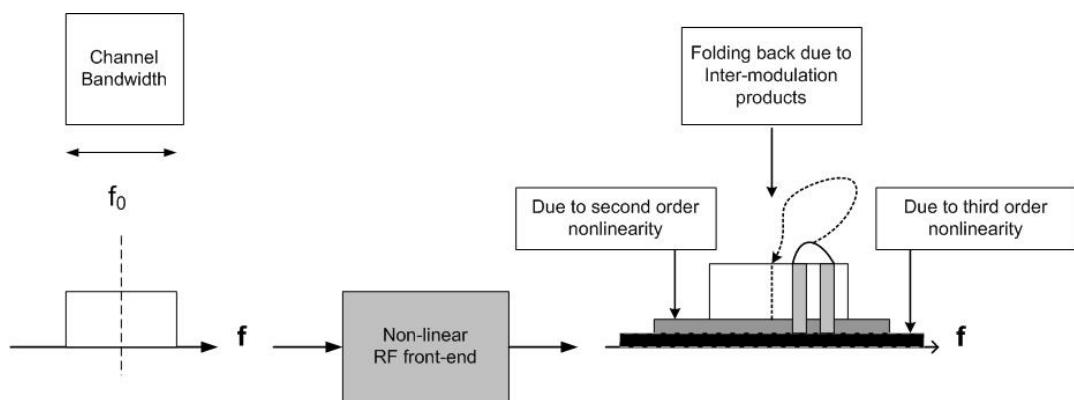


Fig.1.1 Effect of nonlinear RF front-end on the spectrum of the received signal.

Chapter 1 - Introduction

The analog and digital front end of a mobile phone is usually partitioned based on technology usage. This allows a flexible choice of technologies which typically results in the use of BiCMOS for RF and analog, mainly because of the superior RF performance of hetero-junction bipolar transistors (HBT) over metal oxide semiconductor transistors (MOST)[6], and CMOS for the digital signal processing due to the high level of achievable integration. If the whole receiver is to be implemented on a single chip, the partitioning of the chip is no longer based on the technology, but rather on the required functionality. This obviously requires the integration of the analog and digital signal processing sections on the same chip. Since the Digital section of the whole system uses CMOS, it is likely that the analog front end will also be implemented in CMOS [7]. In this work, a standard CMOS 0.18 μm technology is chosen to implement the RF circuitry under consideration using a 1V power supply¹. Such a low voltage supply allows for easy migration of the RF circuits, designed in this work, to more advanced CMOS technologies which will be used in the digital section of the chip to achieve superior functionality².

1.1 Receiver Architecture

Among various RF wireless receiver architectures reported in the literature [8-12], the direct conversion receiver (DCR), illustrated in Fig. 1.2, is considered as the most likely architecture to be used in the future generation of mobile phones³. The DCR offers a simple architecture which allows a low power, fully monolithic implementation of the RF front end [13]. That front-end consists of three main blocks, namely an RF filter to eliminate the undesired frequency content of the signal and to select the channel of interest, a low-noise amplifier (LNA), and a quadrature down-converter to demodulate the incoming angle-modulated data. The main issues involved in

¹ The nominal power supply for standard devices in a CMOS 0.18 μm technology is 1.8V.

² The proposed design in this work is ported to 65nm CMOS to prove the portability of the design to more advanced, lower supply voltage CMOS technologies. See Appendix A.

³ Currently, most mobile handsets use DCR. Base station receivers are also migrating to DCR to ease the design of down-converter and base-band circuitry.

Chapter 1 - Introduction

the design of a DCR include the DC-offset, even and odd order intermodulation terms, flicker noise and the gain and phase mismatches between the in-phase and quadrature paths [14,15]. These issues are briefly discussed in the following paragraphs.

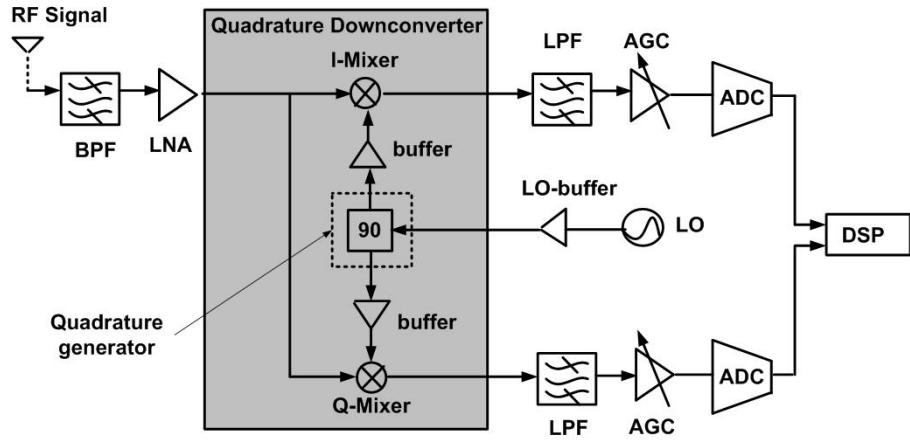


Fig.1.2 Typical architecture of a direct conversion receiver (DCR).

In addition to DC-offset present in integrated circuits due to device mismatches, the DC-offset becomes a more pronounced concern in DCRs because the LO signal applied to the mixer is at the same frequency as the RF carrier. The leakage of the LO signal to the RF port of the mixers, as shown in Fig. 1.3, results in an undesired self-down-conversion of the LO signal to DC. This leakage appears at the output of the RF front end in the form of a DC-offset and falls within the bandwidth of interest. In order to overcome this problem, a number of solutions have been reported in the literature [16,17]. Most of these approaches add to the area, power consumption and complexity of the design and may not be acceptable.

The simplest option which does not add to the complexity of the design, is to AC-couple the output of the mixer to the low-pass filter [14], within the DCR. The feasibility of this approach depends on the multiplexing scheme and the bandwidth of the received signal [17,18]. As mentioned previously, OFDM is a possibility for the multiplexing scheme of future mobile systems. The feasibility of AC-coupling for other types of multiple access schemes such as WCDMA has already been investigated in the literature. As illustrated in Fig. 1.4, applying AC-coupling to

Chapter 1 - Introduction

WCDMA, suppresses the DC-offset along with part of the desired spectrum. In the case of OFDM, if no data is assigned to the baseband subcarrier located at DC, as implemented in the OFDM IEEE 802.11a wireless local area network (WLAN) standard [19], AC-coupling does not affect the information bearing portion of the spectrum, as shown in Fig. 1.4. In this work, OFDM is assumed as the multiple access scheme, due to its obvious advantages over WCDMA in view of DCRs [4].

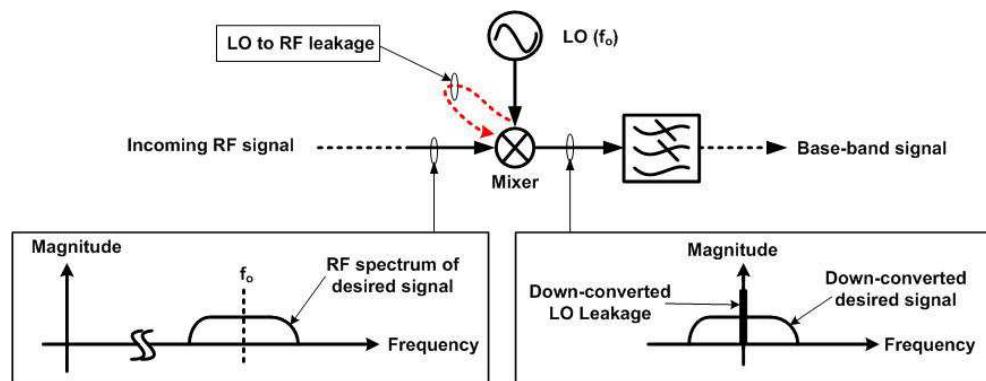


Fig.1.3 The LO to RF leakage due to poor LO to RF isolation.

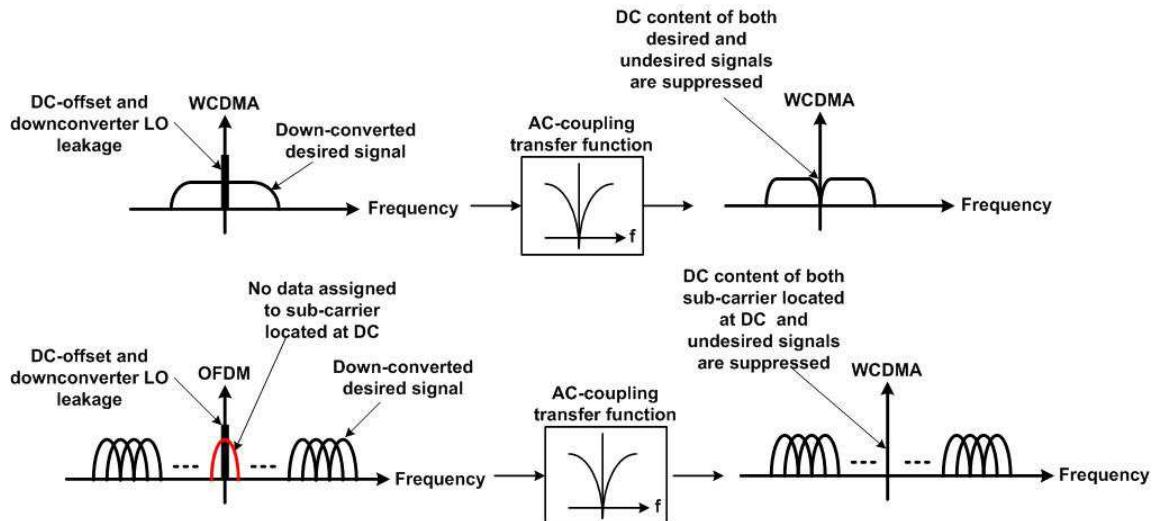


Fig.1.4 Implication of AC-coupled receivers on WCDMA and OFDM communication systems.

Chapter 1 - Introduction

In a direct conversion receiver, even order intermodulation terms resulting from out of band blockers fall in the bandwidth of the incoming signal after down conversion. For this reason, the second order nonlinearity of the down converter should be set such that it meets the requirement of the targeted application. Depending on frequency planning and amount of out-of-band rejection provided by the RF filter, the significance of even order intermodulation products varies. Bautista et al. [20], introduced a novel way of reducing second order intermodulation products by adding a considerable amount of circuit overhead to the core of the design.

The issue of flicker noise in DCRs arises from the fact that most of the noise power is concentrated in the same region of the spectrum as the desired signal. In the case considered in this work, simple AC-coupling can be used to mitigate this issue as described above.

The gain and phase mismatch between the in-phase and quadrature paths in a DCR degrades the quality of the received signal. The mismatch is partly attributed to the unbalance between the two mixers involved in the receive path and partly due to imperfections in the quadrature generator. These mismatches affect the image rejection ratio (IRR) defined as the down-converter's ability to reject signals at its image frequency. IRR is normally expressed as the ratio of the image signal to the desired signal in dB at the output of the down-converter.

The linearity characteristics of the RF front-end of a DCR are to a great extent determined by the linearity of the mixer. This is because the RF signal captured by the antenna reaches the mixers after one or possibly two steps of amplification by the one or two LNAs. This imposes stringent requirements on the dynamic range of the mixers which play an important role in determining the linearity of the RF front-end [21].

The goal of this thesis is to devise a new architecture and design methodology for low voltage, low power CMOS RF down conversion mixers, and quadrature generators with adequate linearity, amplitude matching and quadrature phase accuracy for direct conversion receivers operating

Chapter 1 - Introduction

at 8 GHz [2]. The quadrature down-converter (the combination of the mixer and the quadrature generator) is intended to satisfy the tentative target specifications listed in Table 1.2¹.

Table 1.2 Tentative Target Specifications for a Mixer and Quadrature Generator Potentially Suitable for Future Mobile Phone Receivers.

Circuit	Parameter	Value
Mixer	Supply Voltage**	1 V
	RF & LO frequency**	8 GHz
	Conversion Gain**	> 6 dB
	IIP2**	> 50 dB
	IIP3	> 3dB
	P-1dB	> -7dBm
	LO-RF Isolation**	> 50 dB
	Noise Figure	<13 dB
	Power Consumption and Area	Minimum
Quadrature generator	Supply Voltage**	1 V
	I/Q phase mismatch	<2°
	Power Consumption and Area	Minimum
	Phase noise at 1MHz offset	-110dBc/Hz
Quadrature Downconverter	Image Rejection Ratio (IRR)	> 40 dB

** These values are set as target to stay competitive with the state of the art design. The rest of the targets are obtained from system-level simulation in MATLAB. See Chapter 2 and the MATLAB codes available at: <http://www.vrg.utoronto.ca/~ngwt/Resources/MATLAB/DCR>.

¹The tentative target specifications of the design were generated through system level simulations using MATLAB, as discussed in Chapter 2.

1.2 Mixer Architectures

Mixers are used to translate the frequency of the incoming RF signal to the intermediate frequency (IF) of interest, which is zero in the case of a DCR. Frequency translation is typically performed by multiplying the incoming RF signal by the local oscillator (LO) signal in the time domain. The multiplication of the RF signal and the LO signal is typically done by exploiting the nonlinear (NL) characteristics of a circuit or by using the LO signal to convert a linear time invariant circuit to a linear periodically time variant (LPTV) one [22].

1.2.1 Active Mixers Vs. Passive Mixers

Mixers can be classified as active or passive depending on whether or not they provide power gain at the input radio frequency. They can use an unbalanced, single balanced or double balanced architecture. The typical properties of each of these generic mixers are listed in Table 1.3.

In a DCR, the only opportunity for amplifying the received RF signal is through the LNA and one step of down-conversion. Therefore, the RF front end gain is relatively low by comparison to most other types of receivers. This issue degrades the noise characteristics and hence the sensitivity of the receiver which is a measure of how well the receiver captures weak signals. Since active mixers typically result in better sensitivity, in this work they are preferred over passive ones despite the very good linearity performance of the latter.

Chapter 1 - Introduction

Table 1.3 A Comparison Between Generic Types of CMOS Mixers

	Passive			Active		
	Un-Balanced	Single Balanced	Double Balanced	Un-Balanced	Single Balanced	Double Balanced
Conversion gain	<1			>1, desirable for better noise performance and sensitivity		
Linearity	Excellent			Relatively poor, can be improved by circuit techniques		
Noise figure (NF)	Depending on the devices used as switches, can have relatively poor noise performance, due to the inherent conversion loss.			Relatively good, depending on the amount of conversion gain, and whether noise optimization is done on the transistors individually.		
Even order nonlinearity	Good	Good	Ideally None	Poor	good	Ideally None
Compression point	Relatively good			Relatively poor, due to the saturation effect of active devices		
Bandwidth	Relatively wide bandwidth. Limited by switch parasitic capacitance			Relatively narrow band		
Spurious tone(s)	LO, RF, relatively weak $n\omega_{LO}-m\omega_{RF}^*$ and $k\omega_{LO}-\omega_{RF}^{**}$	LO, RF and relatively weak $n\omega_{LO}-m\omega_{RF}$ and $k\omega_{LO}-\omega_{RF}$	relatively weak $n\omega_{LO}-m\omega_{RF}$ and $k\omega_{LO}-\omega_{RF}$	LO, RF and relatively strong $n\omega_{LO}-m\omega_{RF}$	LO, RF and relatively strong $n\omega_{LO}-m\omega_{RF}$	Relatively strong $n\omega_{LO}-m\omega_{RF}$
DC current	Zero			Significant		

* These spurs are caused by ' $m+n$ ' order non-linearities.

** $k=3,5,7,\dots$ in case of square LO signal.

Chapter 1 - Introduction

1.2.2 Mixer Performance Metrics

The critical performance metrics for a mixer employed in a DCR intended for relatively wide-band portable applications are: its third order and second order nonlinearities, RF-port to LO-port isolation, noise figure at baseband frequencies, LO-power required for driving the mixer LO port, conversion gain and 1-dB compression point. These metrics are discussed briefly in the following paragraphs.

A mixer can be described by the following nonlinear relation between the input signal x and the output signal y

$$y = F(x) \quad (1.1)$$

Assuming weakly nonlinear behaviour, using Taylor expansion of (1.1) and omitting the signal independent term for the sake of simplification (without loss of generality), y can be expressed as

$$y = b_1 x + b_2 x^2 + b_3 x^3 + \dots \quad (1.2)$$

Defining the input signal x as the sum of two cosines of equal amplitudes at angular frequencies ω_1 and ω_2 , given by

$$x = A \cos \omega_1 t + A \cos \omega_2 t \quad (1.3)$$

then y is given by

$$\begin{aligned} y = & b_1 A \cos \omega_1 t + b_1 A \cos \omega_2 t + b_2 \frac{1}{2} A^2 \cos(\omega_1 - \omega_2) t \\ & + b_3 \frac{3}{4} A^3 \cos(2\omega_1 - \omega_2) t + b_3 \frac{3}{4} A^3 \cos(2\omega_2 - \omega_1) t + \dots \end{aligned} \quad (1.4)$$

Chapter 1 - Introduction

Because of the third order nonlinearity x^3 , and second order nonlinearity x^2 terms, the output will contain undesired tones located at angular frequencies $2\omega_1-\omega_2$, $2\omega_2-\omega_1$ and $|\omega_1-\omega_2|$ respectively as shown in equation (1.4). These spurious tones are usually considered because they likely fall in the frequency band of interest (i.e. the signal band); and degrade the bit-error-rate (BER) of the received signal.

- Third Order Intercept Point

The third order input intercept point (IIP3) is a measure of the third order nonlinearity of the mixer and is defined as the magnitude of the input signal (x_{IIP3}) for which the third order intermodulation term at the output has the same magnitude as the first order term. X_{IIP3} is derived from (1.4) and is given by

$$x_{IIP3} = \sqrt{\frac{4b_1}{3b_3}} \quad (1.5)$$

- Second Order Intercept Point

The second order input intercept point (IIP2) is defined as the magnitude of the input signal (x_{IIP2}) for which the second order intermodulation term at the output has the same magnitude as the linear (first order) term. This definition results in

$$x_{IIP2} = 2 \frac{b_1}{b_2} \quad (1.6)$$

- Power Conversion Gain

The power conversion gain of a mixer is the ratio of the power delivered to the load at the IF when the power of all out of band components is excluded, over the available power of the source. The power conversion gain is usually expressed in Decibels (dB). Appropriate conver-

Chapter 1 - Introduction

sion gain of the mixer, helps to decrease the effect of the noise generated by subsequent stages, and hence improves the noise performance of the RF front end. Increasing the conversion gain too much, may impose stringent requirement on the dynamic range of the following stage.

- 1-dB Compression Point

In a weakly nonlinear system, the third order nonlinearity of mixers generates a term at the same frequency as the output first order term which contributes to the gain of the mixer. This phenomenon can be explained based on the following trigonometric identity given that $x=\cos\omega t$

$$x^3 = (\cos \omega t)^3 = \frac{1}{4} \cos 3\omega t + \frac{3}{4} \cos \omega t \quad (1.7)$$

As observed, the second term on the right-hand side of (1.7) affects the linear gain of the mixer. From (1.2) and (1.7) it can be seen that the effective gain of the mixer due to both the linear term and third order nonlinearity is given by

$$\text{Effective gain} = b_1 + \frac{3}{4}b_3A^2 \quad (1.8)$$

Depending on the sign of b_3 , the third order nonlinearity may result in either an increase or decrease of the mixer gain. In most practical cases, this phenomenon results in the reduction of the gain which results in the definition of the 1-dB compression point as the magnitude of the input signal for which the gain drops by 1 dB.

- Port-to-Port Isolation

The port-to-port isolation of the mixer is defined as the ratio (in dB) of the power level applied at one port of the mixer to the resulting power level at the same frequency at the other port. In the case of a direct conversion receiver, as illustrated in Fig. 1.3, poor RF port to LO port isolation results in a DC-offset which may saturate the stage following the mixer.

Chapter 1 - Introduction

- Noise

The mixer noise is a concern because it can mask a weak desired signal. It is characterized by the noise figure (NF) as a metric of the degradation of the signal to noise ratio (SNR) while the signal passes through the mixer, and is defined as

$$NF = \frac{\text{SNR at the input, in the input signal band}}{\text{SNR at the output, in the output signal band}} \quad (1.9)$$

If the signal band is very narrow, the conversion gain and noise power spectral density in the input and output signal bands are almost flat, in this case

$$NF = \frac{\left(\frac{S_i}{N_i}\right)}{\left(\frac{S_o}{N_o}\right)} = \frac{S_i}{S_o} \cdot \frac{N_o}{N_i} = \frac{1}{A} \cdot \frac{N_o}{N_i} = \frac{\text{Total output noise}}{\text{Output noise due to the input noise in the input frequency band}} \quad (1.10)$$

where S_i , S_o , N_i , N_o and A are the input signal power per unit bandwidth, output signal power per unit bandwidth, input noise power per unit bandwidth, output noise power per unit bandwidth and power gain of the mixer, respectively. In DCRs the image band is part of the input signal band and contributes to the denominator of (1.10); in this case, the NF is called double-sideband (DSB) as opposed to the single-sideband (SSB) NF in heterodyne receivers where the image band is not part of the input signal and therefore does not contribute to the denominator of (1.10).

The DSB NF is typically 3 dB lower than the SSB NF.

- LO Power

The amount of power applied to the LO port of the mixer is often a concern and must be minimized. This issue is of particular concern in low voltage designs.

Chapter 1 - Introduction

1.2.3 Previous Work on CMOS Active Mixers

CMOS active mixers reported to date, fall within one of the following categories: Current Commutating Mixers (CCM) [23], Harmonic Mixers (HAM) [24], Dual Gate Mixers (DGM) [25] and Back Gate Mixers (BGM)[26]. In what follows, the various CMOS active mixer architectures and associated design issues are briefly discussed.

- Current Commutating Mixers (CCM) [23]

The block diagram and a typical CMOS implementation of a current commutating mixer is illustrated in Fig. 1.5. It is a LPTV circuit and typically requires a trans-conductor at the input to convert the incoming voltage to current. As shown, the LO signal switches the RF current between the two output branches periodically at a frequency equal to the applied LO frequency, and performs the multiplication between the LO-signal and the RF-signal in this way. In this architecture, the trans-conductor is a critical block in determining the overall performance of the mixer.

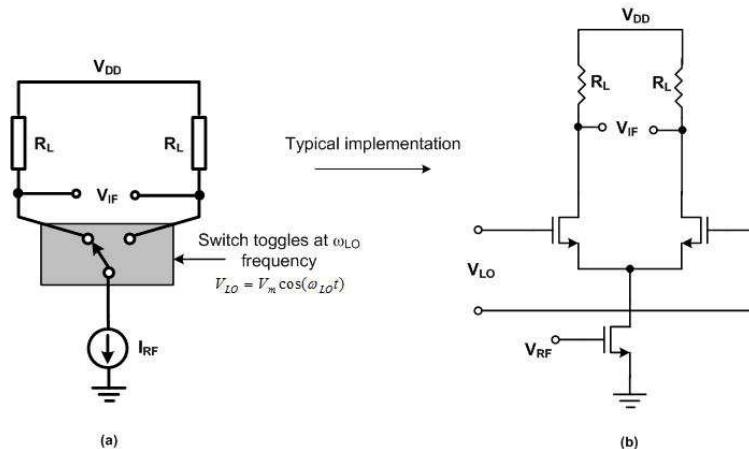


Fig.1.5 Current commutating mixer (CCM). (a) Block diagram. (b) Typical CMOS implementation.

Chapter 1 - Introduction

- Harmonic Mixers (HAM) [24]

The harmonic mixer is a variant of the CCM and therefore a LPTV circuit. It allows for the use of a local oscillator at a fraction of the LO frequency of a CCM. An example of an even harmonic mixer is illustrated in Fig. 1.6. The main drawback associated with this architecture is the dependence on a four-phase local oscillator with precise quadrature phase and 50% duty cycle which adds to the complexity and power consumption of the design.

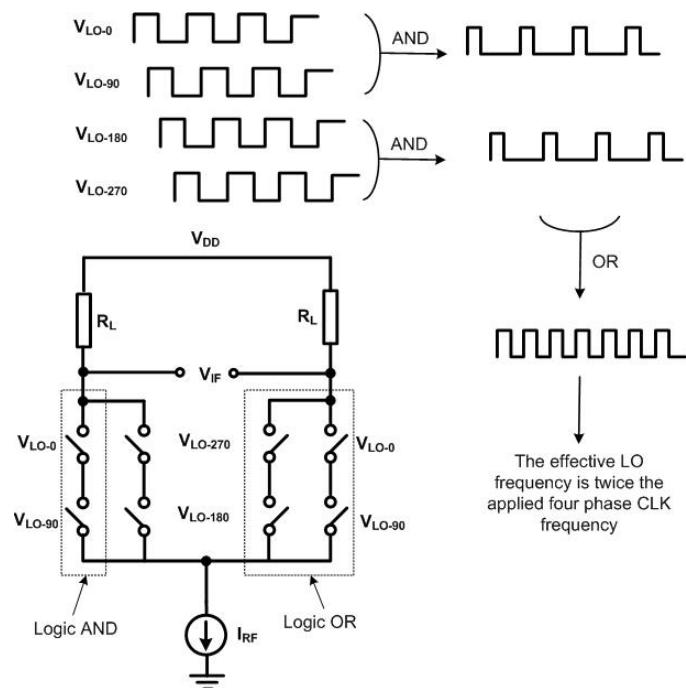


Fig.1.6 Harmonic mixer.

- Dual Gate Mixers (DGM) [25]

Dual gate transistors have been traditionally used as mixers in GaAs technology. They can also be implemented in CMOS technology. Fig. 1.7 illustrates the block diagram of a dual gate mixer showing its principle of operation. In this scheme, the local oscillator, modulates the transconductance of the RF transistor at a frequency equal to the LO frequency and hereby introduces the

Chapter 1 - Introduction

concept of periodically time variance. Therefore the dual-gate mixer is also a LPTV circuit. The circuit architecture of a DGM typically consists of at least two stacked transistors. Because of this feature the DGM is unsuitable for low-voltage applications.

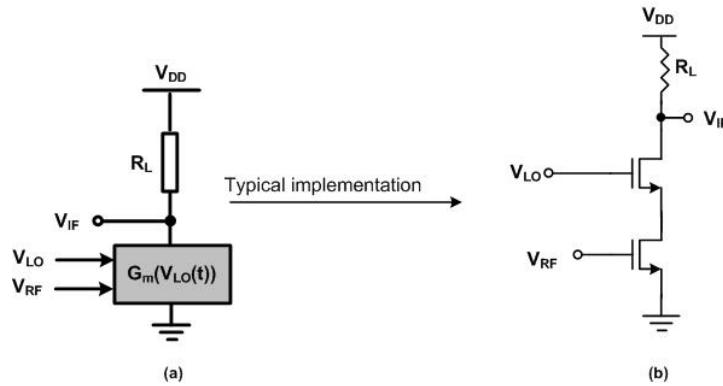


Fig.1.7 Dual gate mixer. (a) Block diagram. (b) Typical CMOS implementation.

- Back-Gate Mixer (BGM) [26]

Fig. 1.8 shows the principle of operation of a back gate mixer. In this architecture the LO signal varies the threshold voltage of the transistor at a frequency equal to the frequency of the LO, therefore the BGM is also a LPTV circuit. In this circuit, since the LO signal is applied to the bulk of the MOST, it may inject a considerable amount of noise to the substrate which is highly undesirable for GHz applications. Therefore, the application of this architecture is practically limited to twin-tub technologies or technologies where the deep N-well is an option. The isolation between the LO port and all the other ports of this type of mixer is poor because of the parasitic capacitance between the terminals of the MOST and its bulk.

Chapter 1 - Introduction

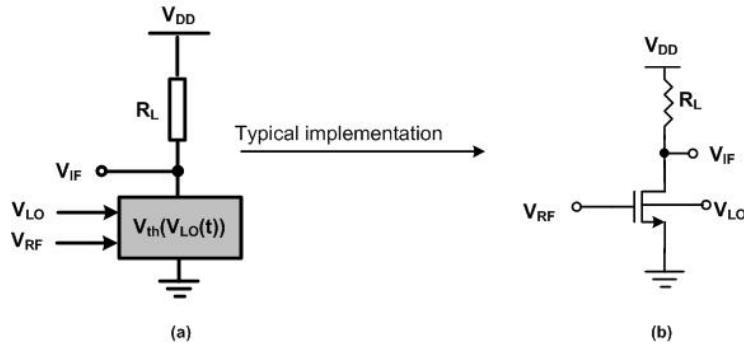


Fig.1.8 Back gate mixer. (a) Block diagram. (b) Typical CMOS implementation.

- Summary of Previous Mixer Work

The state of the art implementation of each of the above mentioned active mixer topologies in various CMOS technologies are summarized in Table 1.4. From the Table, and the previous brief discussion on the mixer architectures, it is evident that none of the previously reported architectures provides an efficient solution to meet the good linearity, low voltage operation and design simplicity requirements of the future generation of mobile phones.

Chapter 1 - Introduction

Table 1.4 State of the art mixer architectures.

Parameter	CCM		HAM		DGM		BGM	
	[36]	[23]	[37]	[24]	[38]	[25]	[39]	[26]
Technology (μm)	0.18	0.18	0.18	0.25	0.18	0.8	0.18	0.5
Supply Voltage (V)	1.8	1.8	1.8	3	1.8	3	1	1
Radio frequency (GHz)	2.4	2.42	1.575	2.012 2	24	1.9	5.8	6.912
LO frequency (GHz)	2.4	2.45	0.789	1.006	24	1.65	5.8	7
IIP2 (dBm)	---	---	---	+40	---	---	---	---
IIP3 (dBm)	---	-3.7	-1.1	-13.5	0	0	15.3	-2
P-1dB (dBm)	-2	-15.9	---	---	---	-10	6.5	-16
Gain (dB)	-1	+27	21	11.61	10	0	-0.8	+6
LO-RF isolation (dBm)	---	---	---	---	>54	>30	67	29
Noise figure (SSB, dB)	22	9.5	31.4	15	23	13.6	37	21
LO Power (dBm)	---	---	---	---	---	+5	---	0
Power Consumption (mW)	---		2.124	5.13	8.3	14.1	1	0.18
Chip Area (mm^2)	0.24	---	0.487	---	0.374	0.09	0.15	0.019

1.3 Quadrature Generators

The quadrature generator is an important part of a direct conversion receiver. It generates two sets of differential signals which are 90° apart to perform the in-phase and quadrature down-conversion.

Chapter 1 - Introduction

1.3.1 Quadrature Generator Performance Parameters

The most important performance metrics of quadrature generators are the amplitude matching, precise 90° phase shift between the in-phase (I) and quadrature phase (Q) of the output signal and the phase noise of the four-phase CLK.

Amplitude mismatch is typically characterized by the percentage mismatch between the I and the Q amplitudes described by equation (1.11)

$$\text{Amplitude mismatch (\%)} = \frac{| \text{I-output amplitude} - \text{Q-output amplitude} |}{\text{Nominal output amplitude}} \times 100 \quad (1.11)$$

The deviation from the quadrature phase is characterized in terms of degrees. Amplitude mismatch of the I/Q outputs or deviation of their phase difference from 90°, results in the degradation of the bit error rate of the received signal [27].

Ideally, the mixer LO CLK is expected to be a single tone signal. In practice the LO contains undesired frequency content around the desired tone. This phenomenon is described as phase noise. In a receiver, if a modulate RF signal is mixed with a clean LO source, a modulated IF signal is generated. If the LO source is also modulated (with phase noise), the noise components act as additional undesired LO's that are offset from the main carrier. Each of these undesired LO tones, translates the modulated RF signal to a new IF frequency with the same frequency offset which obviously degrades the performance of the receiver. Phase noise is measured in dBc/Hz (Decibels below carrier, per unit bandwidth).

1.3.2 Previous Work on Quadrature Generators

Previously reported quadrature generators fall within one of the following categories: RC-CR Filters (RCF)[28], Poly-phase Filters (PPF)[29,30], Subtraction and Addition (SAA)[31], Fre-

Chapter 1 - Introduction

quency Division (FD)[32], Ring Oscillators (RO)[33], Cellular Oscillator Networks (CON)[34], Active LC Quadrature oscillators (LCQ)[35]. Each of the above mentioned types of quadrature generator is discussed briefly in the following paragraphs.

- RC-CR Filters (RCF) [28]

The RC-CR filter is the simplest way of generating quadrature signals from a LO signal. Fig. 1.9(a) shows the circuit diagram of a RC-CR filter used as quadrature generator. As observed in Fig. 1.9(b), this circuit ideally provides 90° phase difference between its two outputs at all frequencies; but, as depicted in Fig. 1.9(c), the amplitudes of the two outputs are equal only at one frequency ($1/2\pi RC$) which limits its application to very narrowband ones.

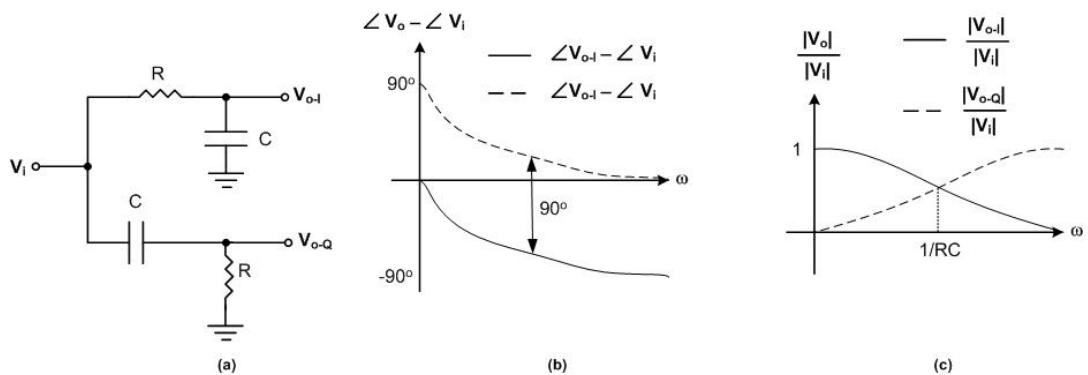


Fig.1.9 RC-CR filter used as quadrature generator. (a) Circuit diagram. (b) Phase of the transfer functions of the two outputs. (c) Magnitude of the transfer functions of the two outputs.

- Poly-phase Filters (PPF) [29,30]

A typical implementation of a single stage passive poly-phase filter, used as quadrature generator is shown in Fig. 1.10. This structure has the capability of generating a four-phase signal with 90° of phase difference between the four outputs at all frequencies. However, similar to the RCF

Chapter 1 - Introduction

case, the amplitudes of the four outputs are equal only at one frequency. To overcome this limitation, multiple stages of the basic structure, shown in Fig. 1.10, are cascaded, each tuned at a different frequency to evenly cover the bandwidth of interest such that the combination of the cascaded stages provides a flat gain over that frequency band. A multistage poly-phase filter achieves better gain and phase matching over process and temperature variations [29], compared to the single stage poly-phase filter, at the expense of higher form factor. The architecture also requires two sets of buffers operating at the LO frequency. One set located between the voltage controlled oscillator (VCO) and the quadrature generator at its input, and the other set located between the quadrature generator and the mixers at its output to provide isolation. This feature translates into high power consumption which is undesirable for mobile receiver circuits operating at GHz frequencies.

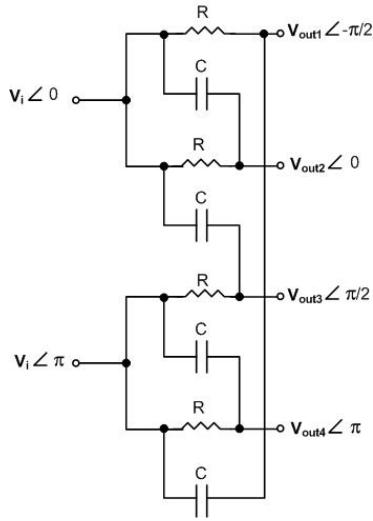


Fig.1.10 Single stage poly phase filter used as quadrature generator.

- Subtraction and Addition (SAA) [31]

The subtraction and addition method or Haven's technique is shown in Fig. 1.11. In this technique, the LO signal is first sent to delay cells to produce two signals approximately 90° out of

Chapter 1 - Introduction

phase. Two RF limiters are used to equalize the amplitudes of these signals. The next stage subtracts and adds these two signals to produce signals with 90° phase difference but different amplitudes. A second set of RF limiters is used to equalize the amplitudes which ideally result in quadrature outputs V_{o-I} and V_{o-Q} of equal amplitudes.

The main drawbacks associated with this technique are the requirement of four RF limiters which make the design less attractive for low power applications and the amplitude modulation to phase modulation (AM-to-PM) conversion in the second set of RF limiters which adds to the output phase error. Due to these serious design limitations, there has been no recent implementation of this architecture.

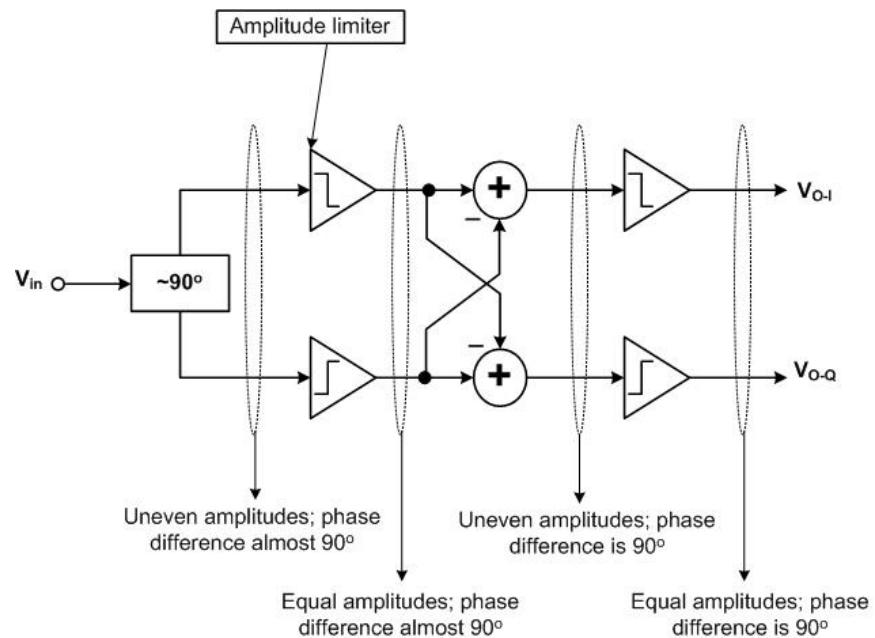


Fig.1.11 Haven's technique for generating quadrature signals.

- Frequency Division (FD) [32]

The frequency division approach is a popular method for generating quadrature signals. Fig. 1.12 illustrates the block diagram of the conventional way to implement a divide by two circuit which

Chapter 1 - Introduction

consists of a master-slave flip-flop to divide a signal with a frequency of 2ω (two times the desired LO frequency) by a factor of two. The main issue linked with this approach is that generating and dividing the signal at a frequency of 2ω may consume more power or simply be impossible due to technology limitation and cost, depending on the desired LO frequency. Another issue that adds to the design complexity of the LO generation circuitry, is the deviation of the input signal duty cycle from 50% which results in phase imbalance at the output.

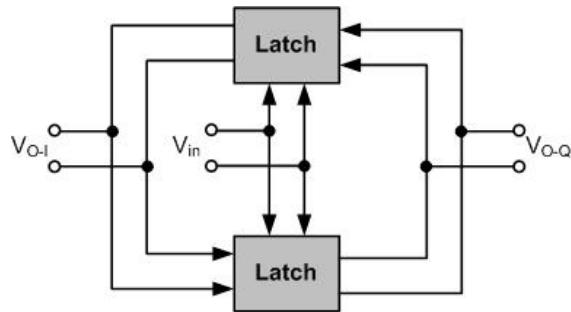


Fig.1.12 Frequency division technique.

- Ring Oscillators (RO) [33]

Ring oscillators typically used as quadrature generators consist of four identical differential delay cells as shown in Fig. 1.13. The delay across each cell is set to be equivalent to a phase shift of 90° in the signal. This architecture requires buffers at the output and three additional sets of dummy buffers at the output of the remaining three delay cells to maintain the symmetry of the design and equalize the delay through each delay cell, and is not suitable for low-power portable applications. This approach is known for its relatively poor phase noise performance which makes it unattractive for most wireless applications.

Chapter 1 - Introduction

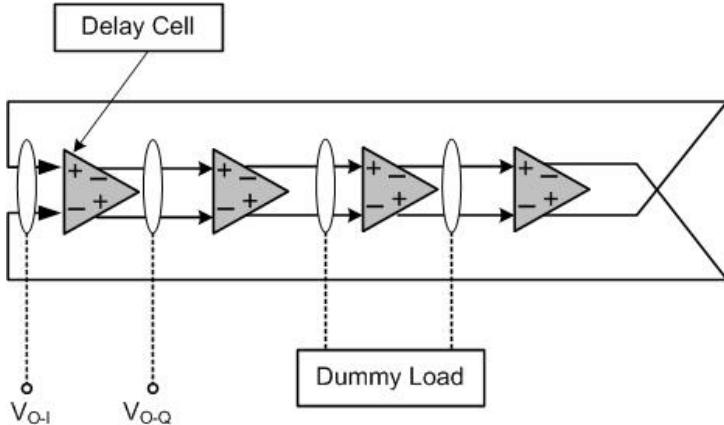


Fig.1.13 Ring oscillator quadrature generator.

- Cellular Oscillator Networks (CON) [34]

The simplest form of a cellular oscillator network used to generate quadrature signal is shown in Fig. 1.14. This approach is based on a simple form of the digital ring oscillator with an odd number of inverting amplifiers. It can be shown that if the inner loop (6-5-4) has larger driving force than the outer loops (1-6-5, 6-2-4, 5-4-3) this circuit will start to oscillate [34]. The required larger driving force for the inner loop is achieved by using larger transistors in the CMOS inverters participating in the loop. The phase shift on each inverter on the outer border and the inner loop will be 30° ($360^\circ/12$, where, 12 is the number of inverters on the outer border) and 120° ($360^\circ/3$, where 3 is the number of inverters forming the inner loop) respectively. Therefore any three consecutive inverters on the outer border will produce 90° of phase shift; an example of two signals with 90° phase shift, labeled V_{o-I} and V_{o-Q} , is illustrated in Fig. 1.14. Twelve sets of I and Q signals are generated by any three consecutive inverter on the outer border. This approach offers relatively accurate quadrature phase and amplitude matching at the expense of high power consumption due to the large number of inverters employed in the design. It also requires buffers at every node of the circuit to preserve the symmetry of the design which is crucial to match the delays at all the nodes in the circuit. Similar to RO, this approach presents relatively poor phase

Chapter 1 - Introduction

noise. Phase noise can be improved in CON at the expense of power consumption as in CMOS inverters.

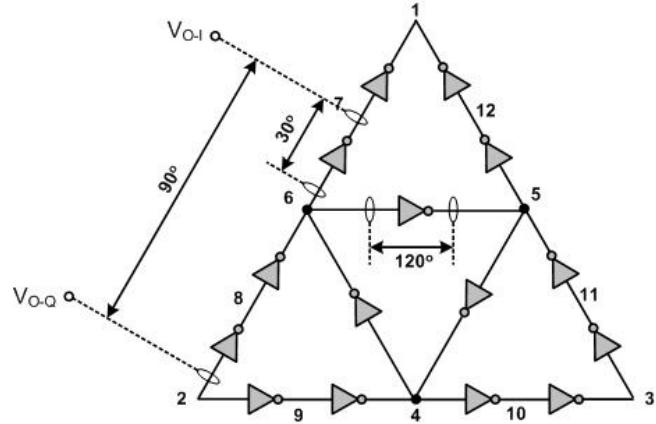


Fig.1.14 I/Q generation using CON.

- LC Quadrature Oscillators (LCQ) [35]

Fig. 1.15 shows the basic cell of a quadrature LC-oscillator. It consists of two identical LC-oscillators coupled for quadrature outputs. This architecture requires perfect matching and symmetry among oscillators A and B to achieve precise quadrature oscillation [35]. This architecture typically requires four inductors which consume a relatively big chip area, in addition the necessity for two identical LC-oscillators makes the design power hungry which is not favorable for portable applications.

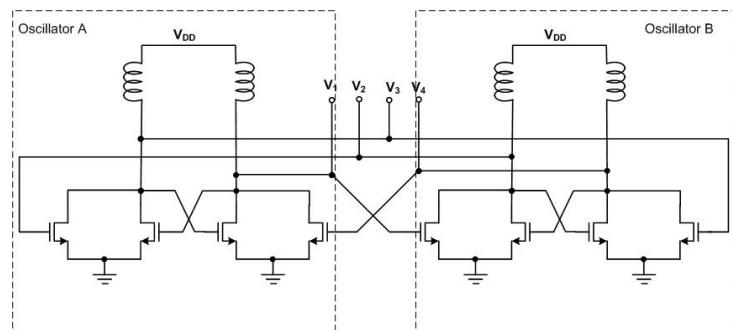


Fig.1.15 Quadrature LC VCO.

Chapter 1 - Introduction

- Summary of Previous Quadrature Generator Work

Table 1.5 summarizes the state of the art reported quadrature generators designs. According to the previous discussion on different types of quadrature generators and the state of the art works listed in Table 1.5, it is observable that none of these simultaneously satisfy all the requirements of future mobile phones in an efficient way.

Table 1.5 State of the Art Quadrature Generators

Parameter	RCF		PPF		FD		RO	CON*	LCQ	
	[28]	[40]	[30]	[41]	[32]	[42]	[33]	[34]	[35]	[43]
Technology (µm)	0.35	0.065	0.18	0.18	0.18	0.09	0.18	0.5	0.18	0.13
Supply Voltage (v)	---	1.2	---	1.8	1.8	0.09	1.8	3	1.8	1
Frequency (GHz)	2	2	2	10	2	7	3.5	4.66	2.5	2.1
Amplitude Mis-match (%)	7.5	12	< 2.8	2.9	< 9	---	---	0	< 5	2
Phase Mismatch (°)	4.5	5	< 2	1.5	< 2.5	7	< 3.2	< 1	< 1.2	2
Power Consumption (mW)	0	15	---	---	---	15.6	16.2	---	7.2	0.6
Chip Area (mm²)	---	---	---	---	---	---	---	---	0.55	---

* Only simulation results were reported.

** Using BAW resonator which is installed inside package.

1.4 Objectives and Outline of the Thesis

As pointed out previously, the RF front-end's linearity at low voltage supplies is one of the main design challenges for future generation of mobile phone receivers. Furthermore, the linearity of the mixer has considerable influence on the overall linearity of the RF front-end of the receiver. The goal of this thesis is to devise a new architecture and design methodology for the implemen-

Chapter 1 - Introduction

tation of CMOS RF quadrature down-converters, operating at 8GHz, which simultaneously satisfy the low voltage and linearity requirements. The quadrature down-converter is intended to meet the tentative target specifications obtained using MATLAB, listed in Table 1.2, and is to be implemented in CMOS technology. A $0.18\text{ }\mu\text{m}$ CMOS technology was chosen for the implementation, since it is a well-established process which satisfies both the performance and the low cost requirements envisaged.

Chapter 2 deals with the system level simulation of a direct conversion receiver in MATLAB considering a wireless channel and an OFDM system. The effect of the quadrature down-converter's non-idealities on the performance of the OFDM system under consideration is studied in terms of the bit-error-rate (BER) of the received signal, and a set of tentative specifications for the mixer and the quadrature generator is extracted to meet a target un-coded BER of 10^{-3} .

In Chapter 3, the design, simulation and analysis of a new current commutating CMOS mixer is presented [44, 45]. The main factors affecting the linearity of CMOS current commutating mixers are discussed and a novel architecture, based on the bias-offset-technique is proposed to simultaneously satisfy the high linearity, low voltage and design simplicity requirements of the future generation of mobile phones. A design methodology for the new architecture is also presented.

The design methodology of a new quadrature generator based on a simple analytical model is presented in Chapter 4 [46]. The design uses active inductors embodied in the LO-buffer and features relatively low power consumption by omitting the buffers located between the quadrature generator and the mixers. The coupling between amplitude tuning and quadrature phase tuning is relaxed, allowing for relatively easy tuning and good quadrature phase and amplitude matching.

Chapter 1 - Introduction

Chapter 5 presents the implementation and experimental results of the quadrature generator and the mixer [47], building the quadrature down-converter. Conclusions and guidelines for future work are presented in Chapter 6.

In order to show the applicability of the proposed circuitry and associated design methodologies to more advanced CMOS technologies, the circuitry are ported to TSMC 65nm technology, the results of which is included in Appendix A.

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CHAPTER 2: Down-converter System Level Simulations

2.1 Introduction

The relatively wide bandwidth targeted by future generation of mobile phones translates into demanding system and circuit level requirements. In this chapter, system level simulations are carried out; using MATLAB on a direct conversion receiver (DCR) to understand the effect of quadrature down-converter impairments on the performance of the whole receive chain, including the baseband circuitry. A set of tentative specifications are also extracted for the mixer and the quadrature generator, assuming OFDM as the multiple access scheme.

2.2 OFDM Communication System

Fig. 2.1 shows a typical OFDM communication system. The data and OFDM modulation/demodulations are performed in the digital part of the transceiver. The analog portion of the system consists of the transmitter, the wireless channel and the receiver. The channel is modeled as a Rayleigh fading channel¹. The receiver was intended to satisfy a target un-coded BER of 10^{-3} [1].

¹ See MATLAB codes located at: <http://www.vrg.utoronto.ca/~ngwt/Resources/MATLAB/DCR>.

Chapter 2- Downconverter System Level Simulations

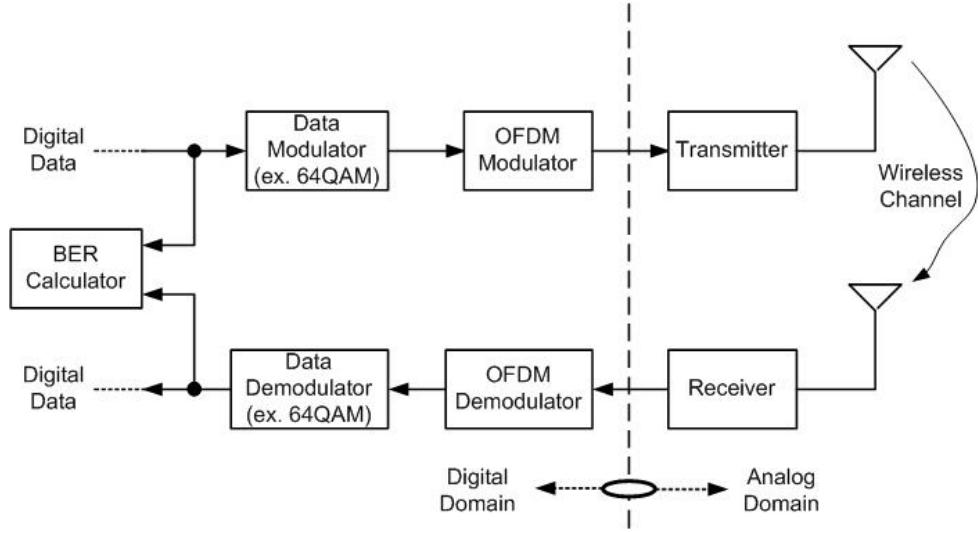


Fig.2.1 Typical OFDM Communication system.

A typical receiver block is shown in Fig. 2.2 in detail. This scheme was used in modeling the receiver. The receiver consists of two RF low-noise-amplifiers (LNA), two RF band-select filters, single-ended to differential converter balun, attenuator, down-conversion mixer, baseband low-pass filter, baseband variable-gain-amplifier (VGA), anti-alias filter and analog to digital converter.

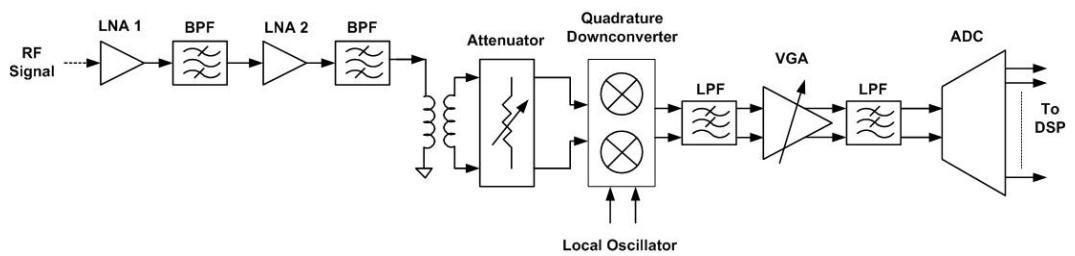


Fig.2.2 Typical direct conversion receiver block diagram [2].

The OFDM modulator/demodulator was modeled as shown in Fig. 2.3. As observed in the figure, the modulator first converts the data from a serial stream to parallel sets. The parallel data is then modulated to the orthogonal carrier frequencies. The inverse-fast-Fourier-transform (IFFT) converts the parallel data into time domain waveforms. Finally, these waveforms are combined to create a single time domain signal for transmission. In the demodulator, the

Chapter 2- Downconverter System Level Simulations

received data is first converted to parallel data streams. The FFT block converts the parallel data into frequency domain data; at this point the data is available in modulated form on the orthogonal carriers. A final demodulation step recovers the data. The parallel to serial converter then converts the parallel data to a serial stream to recover the original signal. Table 2.1 summarizes the parameters used for MATLAB simulation of the OFDM system under consideration based on the system configuration in Fig. 2.3. The cyclic extension parameter, listed in the Table, refers to the redundancy added to the symbols to reduce or eliminate inter-symbol interference due to delay spread in the wireless channel.

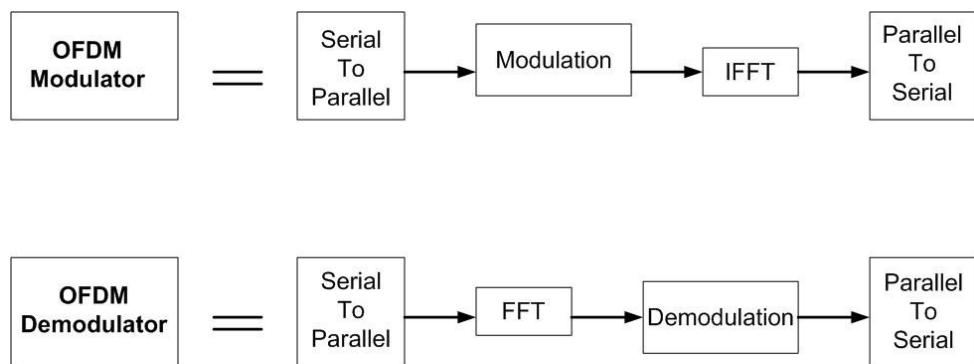


Fig.2.3 OFDM modulator and demodulator block diagram [2].

Table.2.1 Specifications of the OFDM System Under Consideration

	Value
Number of Subcarriers	1024
IFFT/FFT Size	1024
Subcarrier Spacing	25 KHz
Cyclic Extension Duration	15% of a Symbol
Subcarrier Modulation	64QAM

Chapter 2- Downconverter System Level Simulations

2.3 DCR Behavioral Modeling

The receiver illustrated in Fig. 2.2 was modeled in Matlab. The LNA, RF BPF, RF Attenuator, VGA and ADC characteristics assumed in the model are tabulated in Table 2.2. These values are taken from actual components. Assuming all blocks behave in a weakly nonlinear manner, all nonlinearities are modeled by polynomials. Non-idealities such as mixer noise, quadrature phase imbalance of the quadrature generator and phase noise of the oscillator signal applied to the mixer, were also considered to extract a tentative set of specifications for the quadrature down-converter assuming an un-coded BER of 10^{-3} ¹.

Table 2.2 Assumed Receive Path Block Characteristics

	Gain (dB)	OIP3 (dBm)	NF (dB)	SNDR (dBFS)	Phase Accuracy (Degrees)
LNA	15	24	2	---	---
RF BPF	-2	---	-2	---	---
RF Attenuator	-10 → 0	30	---	---	2
VGA	0 → 20	15.8*	8	---	2
ADC	N/A	40	---	67	---

* This number represents the OIV3 in dBV.

The amplitude mismatch at the output of the mixers in terms of percentage of mismatch between the in-phase and quadrature amplitudes (A) is modeled as $(b_1 \cdot A)/100$, where b_1 is the linear conversion gain of the mixer.

¹ All Matlab codes, along with top-level test benches used to model the receiver shown in Fig.2.2 are located at the following URL: <http://www.vrg.utoronto.ca/~ngwt/Resources/MATLAB/DCR>

Chapter 2- Downconverter System Level Simulations

The noise characteristics of the LNA and the mixers are modeled by noise sources added to the input of the LNA and the mixers to model their input-referred noise. The local oscillator is modeled as a sine wave source at frequency f_{LO} and the phase noise of the oscillator is modeled by additional sources, at the frequencies of $f_{LO} + \Delta f$, where Δf represents the offset frequencies to build the intended phase noise mask. The quadrature phase imbalance between the in-phase and quadrature branches of the receiver is also modeled. Notch filters at DC are included in the model to consider the effect of the AC-coupling used at the output of the mixers. AC-coupling [4-6] is used at the output of the mixers to eliminate the DC content of the signal. As discussed in Chapter 1, in the case of OFDM, AC-coupling is practical and does not affect the performance of the system, by leaving the subcarriers located at DC and close to DC empty¹.

2.4 Simulation Results

In this section, the effect of the quadrature down-converter non-idealities, on the performance of the receiver shown in Fig.2.2 are studied in terms of the un-coded BER of the received signal. Initially, each one of the quadrature down-converter non-idealities were considered one at a time, to understand the effect of each non-ideality on the overall performance individually. This study helps resolve the trade-offs between opposing non-idealities such as noise and linearity in the actual circuit design. Next, all the non-idealities were considered simultaneously and their corresponding metrics were adjusted to satisfy the target un-coded BER of 10^{-3} . For the data modulation scheme considered in this work (64QAM), un-coded $BER=10^{-3}$ translates to $SNR=23dB$ at receiver's output (ADC output). The resulting values were set as the tentative target specifications for the quadrature down-converter under consideration.

Fig. 2.4 shows a plot of the SNR of the received signal versus the deviation from the target phase noise specification. The number zero on the horizontal axis represents mixer LO phase noise of -

¹In this work, four subcarriers located at DC and near DC are filled with 0s.

Chapter 2- Downconverter System Level Simulations

105dBc/Hz at 1MHz offset, which means the phase noise is varied from -115dBc/Hz to -95dBc/Hz at 1 MHz offset.

Based on Fig.2.4, the phase noise performance of the quadrature generation circuitry should be better than -105dBc/Hz at 1MHz offset to guaranty SNR better than 23dB. The LO phase noise mask corresponding to the zero on the horizontal axis of Fig.2.4 is illustrated in Fig.2.5.

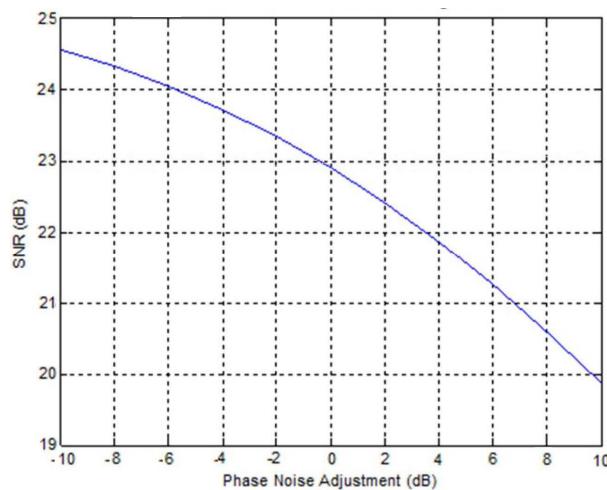


Fig.2.4 SNR versus phase noise of the mixer LO CLK.

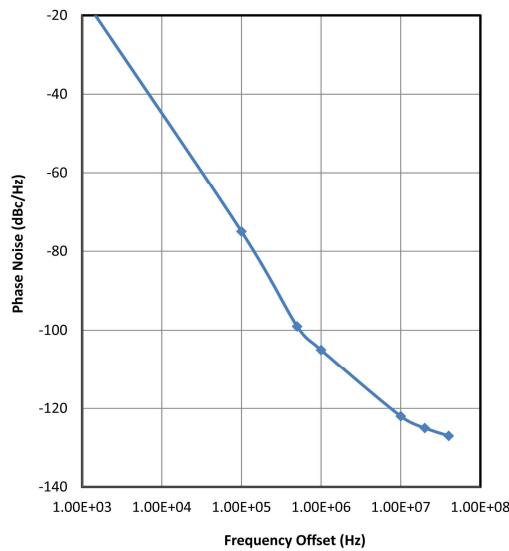


Fig.2.5 Mixer LO phase-noise mask meeting BER spec of 10^{-3} .

Chapter 2- Downconverter System Level Simulations

The effect of the I/Q phase imbalance in a DCR on the performance of the OFDM system is shown in Fig. 2.6. The quadrature phase imbalance is defined as the deviation from 90° in the phases of the I with respect to the Q channel. Assuming quadrature phase error being the only non-ideality in the receive chain, the maximum tolerable quadrature phase error is 4 degrees in the system under consideration in order to maintain BER better than 10^{-3} . As observed from the plot, quadrature phase error below 2 degrees does not cause any bit error in the received signal. A similar simulation assuming 16QAM data modulation (instead of 64QAM assumed for this work), suggests the DCR is insensitive to phase error below 3° . This observation reinforces the fact that communication system level specifications directly affect circuit level requirements.

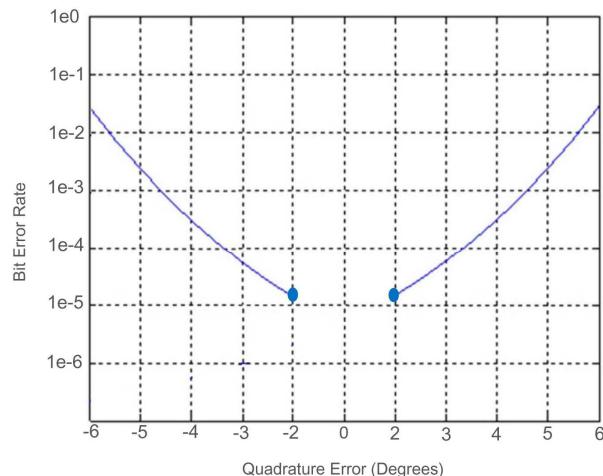


Fig.2.6 Receiver BER versus quadrature phase error.

Quadrature phase error spec also depends on IRR requirement. Typical IRR requirement for DCRs is 40dB [3] which translates into quadrature phase accuracy of better than 2° .

The nonlinearity of the mixer also affects the performance of the OFDM system by introducing inter-symbol interference (ISI) and intermodulation distortion components in the band of interest of the received signal. Fig. 2.7 illustrates the SNR performance of the DCR versus mixer IIP3.

Chapter 2- Downconverter System Level Simulations

As observed from the figure, Mixer's IIP3 should be better than +3dBm to meet the target 23dB system SNR.

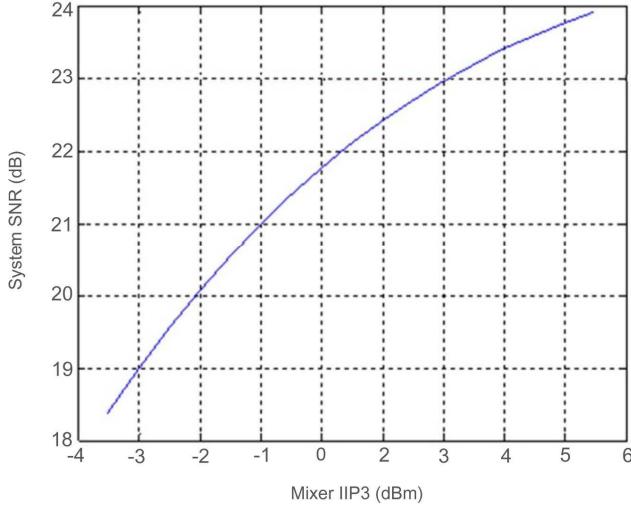


Fig.2.7 System-level SNR in terms of mixer linearity.

The maximum allowed noise contribution by the receiver is characterized with its Noise Figure (NF). The required NF of wireless receivers are extracted from their target sensitivity, defined as the minimum detectable signal at the receiver's input. In this work the noise floor at the receiver antenna is calculated as -174dBm/Hz¹, and the target minimum detectable signal is set to -97dBm². Given the fact that minimum required SNR to successfully demodulate 64QAM data at the output of the receiver is 23dB, the maximum allowed NF for the complete front-end is calculated to be 4.78dB³ with sub-carrier bandwidth of 16.28KHz.

¹ This number represents the thermal noise floor of the antenna assuming 50Ω antenna impedance at 300°K.

² The LTE standard which is the closest industry-defined standard to this work, assumes -106.8dBm sensitivity for 1.4MHz bandwidth and -101.5dBm for 20MHz bandwidth. In a given wireless standard, sensitivity scales with target bandwidth to maintain constant SNR. In this work, -97dBm sensitivity is assumed for bandwidth above 50MHz.

³ $NF_{RX} = RX_{SENS} - [-174 + 10LOG(BW)] - SNR$ where NF_{RX} , RX_{SENS} , BW and SNR represent the complete receiver's noise figure, the desired receiver's sensitivity, sub-carrier bandwidth and required SNR at receiver's output, respectively.

Chapter 2- Downconverter System Level Simulations

The maximum allowed NF calculated above includes the loss associated with the antenna system. Assuming a typical antenna system loss of 1.5dB, results in a complete receiver NF requirement of 3.2dB. The NF target for this work is set to 3dB.

Fig.2.8 illustrates the effect of mixer NF on the overall receiver NF. This plot depends strongly on the noise and gain characteristics of all blocks preceding the mixer. This plot is generated assuming the rest of the receiver components performance is as listed in Table 2.2, it assumes VGA and mixer gain of 6dB each.

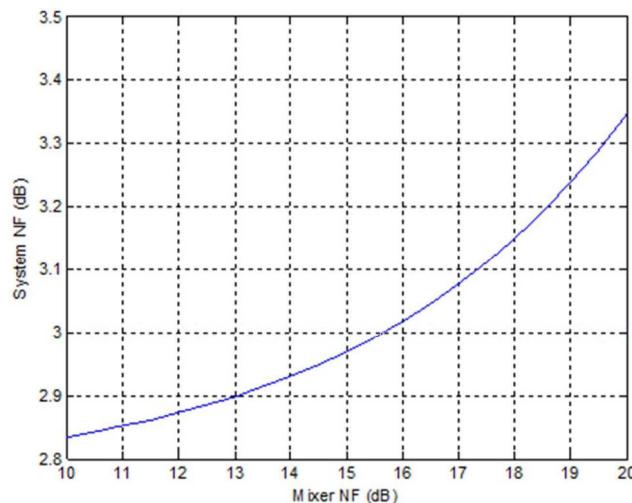


Fig.2.8 Overall system noise figure in terms of mixer noise figure.

As observed from Fig.2.8, the mixer NF should be below 16dB over the band of interest to guaranty an overall receiver NF better than 3dB.

In order to extract a set of quadrature down-converter target specification for the communication system described in this chapter, All the quadrature down-converter non-idealities were applied simultaneously in the MATLAB model¹. the quadrature down-converter performance metrics were interactively varied to guaranty an SNR above 23dB or equivalently un-coded BER of 10^{-3}

¹ MATLAB model is located at: <http://www.vrg.utoronto.ca/~ngwt/Resources/MATLAB/DCR>.

Chapter 2- Downconverter System Level Simulations

at the receiver's output. The resulting values are listed in Table 2.3. These values were set as tentative target specifications for the quadrature down-converter designed in this work. The numbers listed in Table 2.3 are applicable when all non-idealities are simultaneously applied to the model, as would be the case in practice.

Table 2.3 Tentative Specifications for the Mixer and Quadrature Generator

Circuit	Parameter	Value
Mixer	IIP2*	> 50 dBm
	IIP3	> 3 dBm
	Noise Figure	<13 dB
Quadrature Generator	Phase noise @ 1MHz offset	<-110dBc/Hz
	I/Q phase mismatch	<2°
Quadrature Downconverter	Image Rejection Ratio (IRR)	>40 dB

* In a DCR, the IIP2 spec is mainly determined by the out of band linearity requirements, which in terms depends on the detailed system specification and amount of available out of band filtering. The target of 50dBm is arbitrary chosen to remain competitive to the state of the art in the literature.

2.5 Summary

All blocks in a direct conversion OFDM receiver (DCR) were modeled at the behavioral level in MATLAB. The wireless channel was modeled as a Rayleigh fading channel. The effect of all non-idealities associated with the quadrature down-converter in a DCR on the performance of the OFDM system were individually examined in terms of the un-coded bit-error-rate (BER) of the received signal, or equivalently SNR at the output of the receiver. Tentative specifications for the quadrature down-converter building blocks were extracted. This was done while all non-idealities were simultaneously applied to the receiver.

Chapter 2- Downconverter System Level Simulations

These specifications were considered while applying the new low-voltage, low power design technique proposed in this work to an 8GHz quadrature down-converter.

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CHAPTER 3: CMOS Down-conversion Mixer

3.1 Introduction

The design, layout and post layout simulation of an 8 GHz down-conversion mixer are discussed in this chapter. Linearization techniques for current commutating mixers are briefly mentioned and the circuit of the proposed mixer and its evolution from the bias offset technique, originally applied to differential pair CMOS trans-conductors, are discussed. The mixer's design methodology and characteristics are also presented.

3.2 Current Commutating Mixers

The current commutating mixer (CCM) is the most widely used CMOS mixer [1] because it offers advantages such as relatively high conversion gain and high port-to-port isolation. CCMs which are based on the multiplication of two signals, exhibit superior performance compared to other CMOS mixers as discussed in Chapter 1. Furthermore, the principle of operation of the CCM is technology independent¹ which makes it easier to migrate from one technology to another.

The block diagram and a conventional CMOS implementation of the current commutating mixer are illustrated in Fig. 3.1. As observed from Fig. 3.1(a), the CCM consists of a trans-conductor to

¹Regardless of the technology used: CMOS, BICMOS or Bipolar (and its variants), the conventional CCM consists of a trans-conductor followed by switching pairs to perform the frequency translation.

Chapter 3 - CMOS Downconversion Mixer

convert the incoming voltage to current, followed by a mixing stage to perform the frequency translation, and finally a trans-impedance stage to convert the resulting down-converted current back to voltage. Fig. 3.1(b) shows a conventional implementation of the CCM using MOSTs. In what follows, the three main blocks involved in a CCM are briefly discussed.

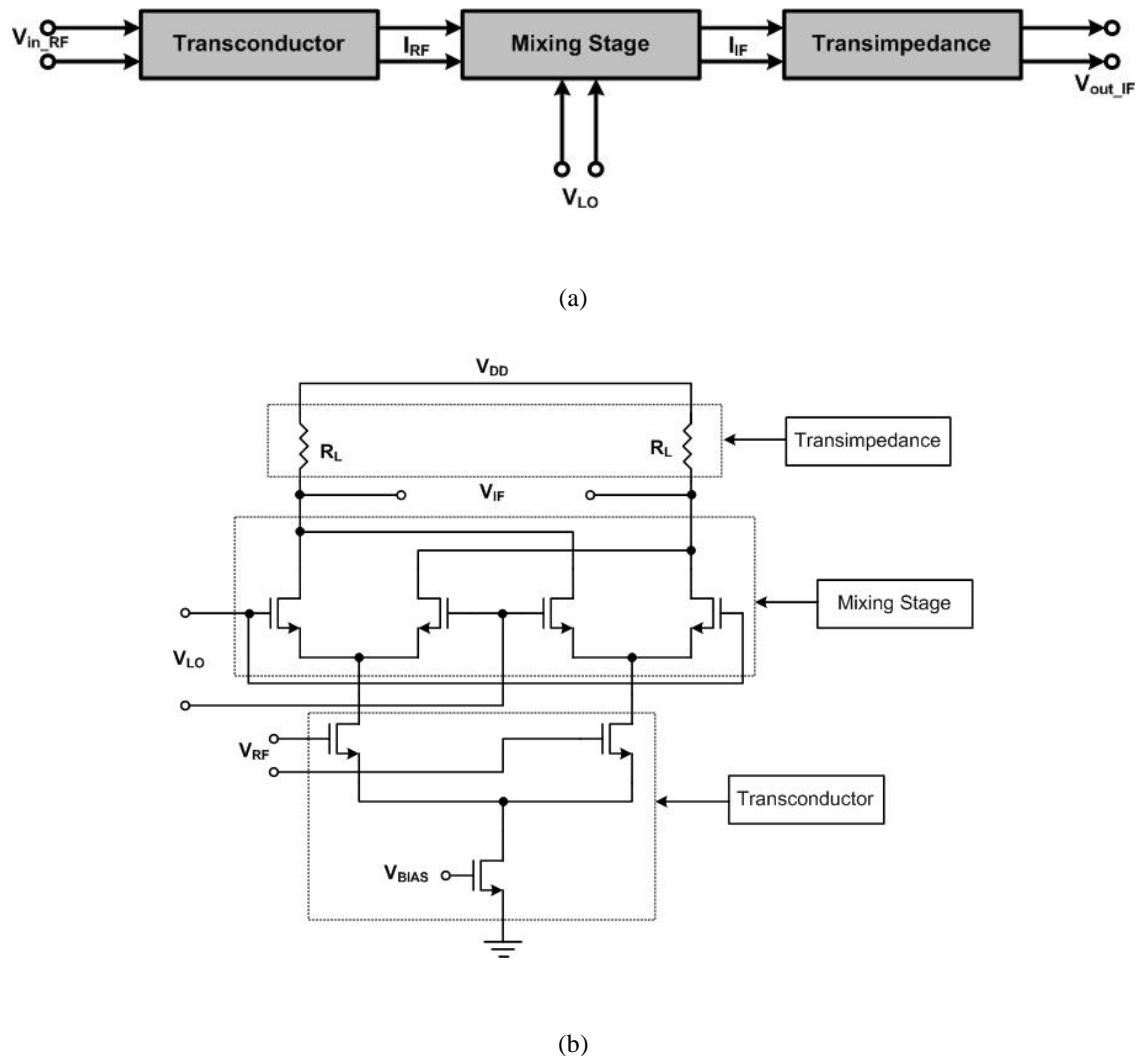


Fig.3.1 Current commutating mixer (CCM). (a) Block diagram of the CCM. (b) Conventional circuit diagram of the CCM.

Chapter 3 - CMOS Downconversion Mixer

3.5.1 Trans-conductor

The trans-conductance stage of a CCM can be implemented using either common-gate or common-source stages [2,3]. Both single ended and differential implementations are possible. Various options for differential implementations of these configurations are illustrated in Fig. 3.2. Figs. 3.2(a)-(c) illustrate the common-gate implementations and Figs. 3.2(d)-(f) illustrate the common-source implementations. Some trans-conductors use a combination of Fig. 3.2 (d) and (e) configurations.

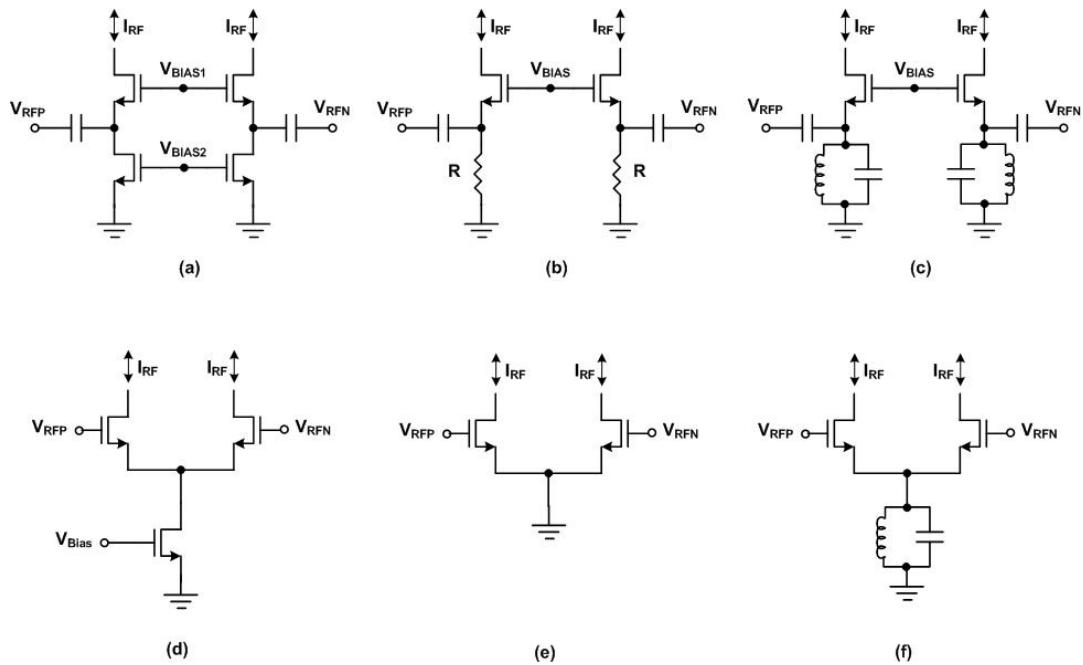


Fig.3.2 Various conventional possibilities to implement trans-conductors. (a)-(c) Common gate implementations. (d)-(f) Common source implementations.

3.5.2 Mixing Stage

The mixing stage of a CCM performs the frequency translation, and typically consists of cross-coupled differential pairs as shown in Fig. 3.3. The bias of the transistors in the mixing stage and the amplitude of the local oscillator signal, denoted as V_{in-LO} are typically chosen such that the transistors act as close as possible to ideal switches. The closer to ideal switching, the better the

Chapter 3 - CMOS Downconversion Mixer

performance of the complete CCM in terms of conversion gain and noise figure is. The maximum theoretical conversion gain for an ideal mixing stage as shown in Fig.3.3 is $\pi/4$.

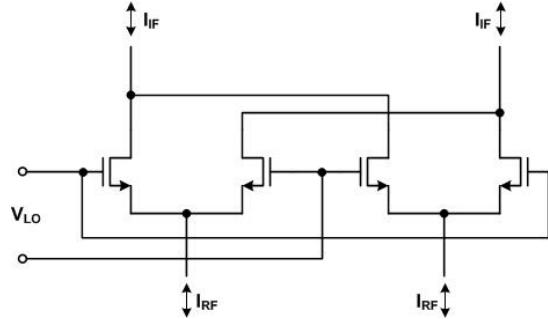


Fig.3.3 Cross-coupled differential pairs as mixing stage.

3.5.3 Trans-impedance Stage

The trans-resistance stage converts the down-converted current at IF back to voltage. It may be implemented using resistors or active loads, or a combination of the two to provide adjustability to the load resistance and achieve offset or device mismatch cancellation [4].

As mentioned in Chapter 1, achieving good linearity at low supply voltages is one of the main challenges in the design of future generations CMOS RF receiver front-ends. In the next section, the linearization techniques previously applied to the CCM are briefly discussed.

3.3 CCM Linearization Techniques

Linearization techniques previously proposed to improve the linearity characteristics of CCMs include: source degeneration (SDE) [5], dynamic matching (DMA) [6], cross coupled transconductors (CCT) [7], a CMOS pair (CMP) [8] and class A-B transconductors (ABT) [9]. These approaches are briefly discussed in the next few paragraphs.

3.3.1 Source Degeneration (SDE)

Fig. 3.4 shows the circuit diagram of a CCM with source degeneration [5]. Both resistive and inductive source degeneration is possible. Typically, resistive degeneration is more suitable for wideband applications at the expense of voltage headroom loss, while inductive degeneration works only for narrow band applications due to its frequency selectivity.

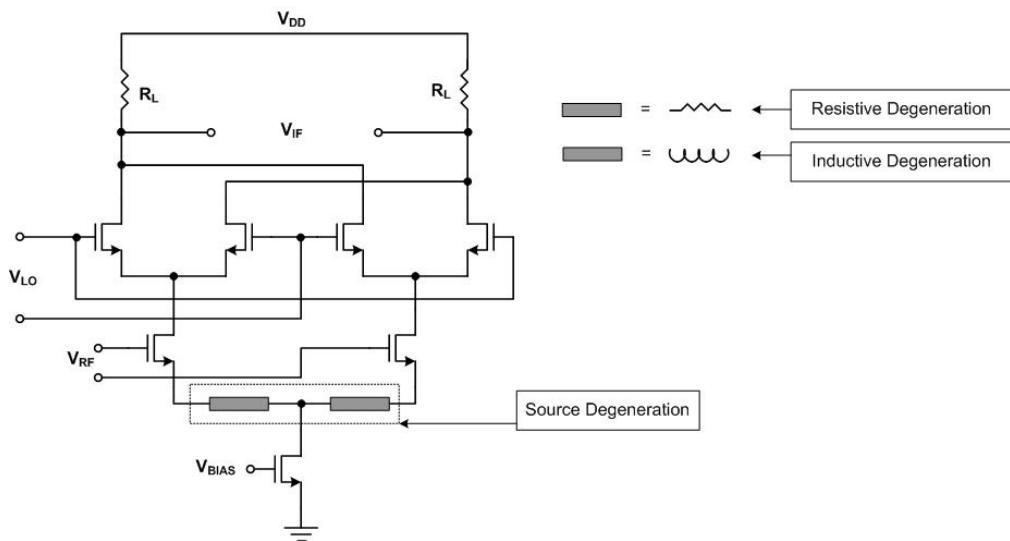


Fig.3.4 Conventional CCM using source degeneration for linearizing the mixer.

The source degeneration resistor or inductor acts as a series-series feedback which reduces the trans-conductance gain of the circuit while improving its linearity. This technique is popular for bipolar transistors [10]. However it is not as efficient in the case of MOST differential pairs because the trans-conductance of a MOST is typically lower than its bipolar counterpart.

3.3.2 Dynamic Matching (DMA)

Dynamic matching involves enhancing the balance of a fully differential mixer through decreasing both component and device mismatches [6]. It basically moves the second order

Chapter 3 - CMOS Downconversion Mixer

intermodulation products and flicker noise created by the mixer, to frequency bands outside the down-converted bandwidth of interest. A CMOS implementation of this technique is shown in Fig. 3.5. Differential clocks operating at higher frequencies than the channel bandwidth of interest are necessary [6].

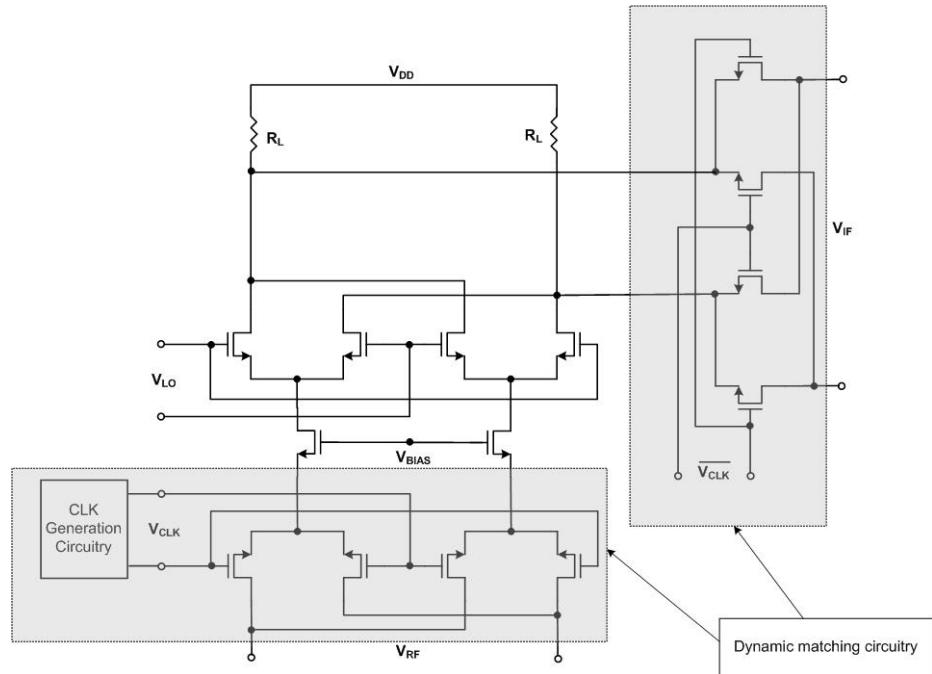


Fig.3.5 Linearized CCM using dynamic matching technique.

3.3.3 Cross-Coupled Trans-conductor (CCT)

In this approach, the differential pair trans-conductance of the conventional CCM is replaced by two cross-coupled differential pairs as illustrated in Fig. 3.6 [7]. The objective is to have the nonlinearities of the two differential pairs cancel out. The power consumption of this technique can be close to twice the power consumption of the conventional CCM, depending on the relative size of the two cross-coupled differential pairs.

Chapter 3 - CMOS Downconversion Mixer

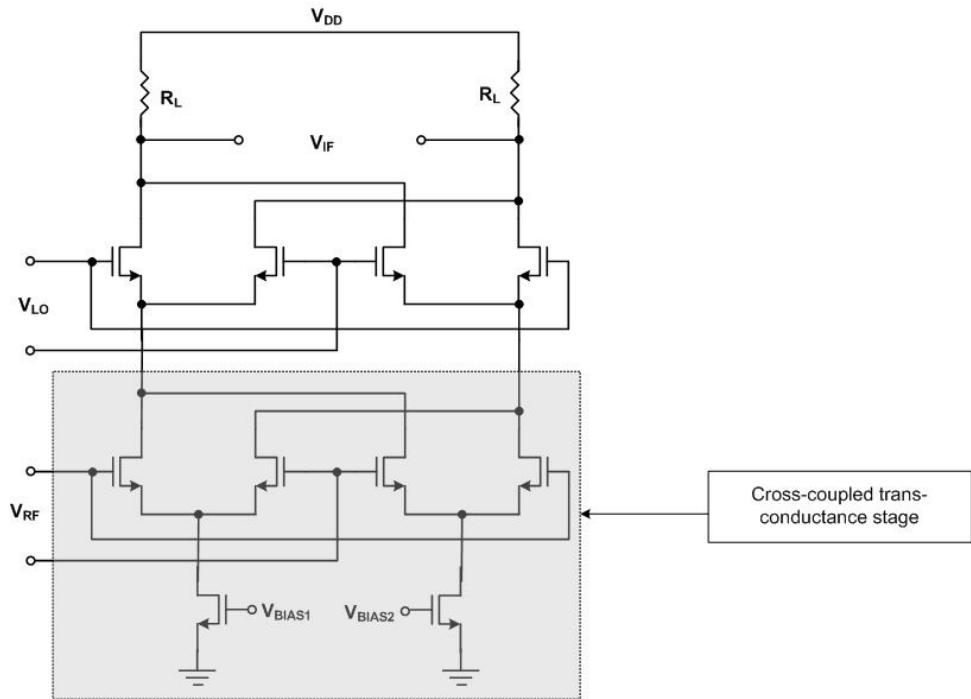


Fig.3.6 Linearized CCM using cross-coupled trans-conductors.

3.3.4 Trans-conductor Using a CMOS Pair (CMP)

In this approach, the linearity of the CCM is improved by merging the trans-conductance stage and the mixing stage in the form of a CMOS pair [12], as depicted in Fig. 3.7 [8]. This technique works only if the MOST obeys the well-known quadratic behaviour in the saturation region of operation. However, in modern deep submicron CMOS technologies, where the I-V transfer characteristics of the MOS transistors are no longer quadratic, the effectiveness of this technique is reduced. Furthermore, the CMOS pair is equivalent to a single transistor with a threshold voltage equal to the sum of the absolutes of the threshold voltages of the N-channel and P-channel transistors. This results in an equivalent threshold voltage roughly twice that of a single transistor making the approach impractical for low-voltage designs.

Chapter 3 - CMOS Downconversion Mixer

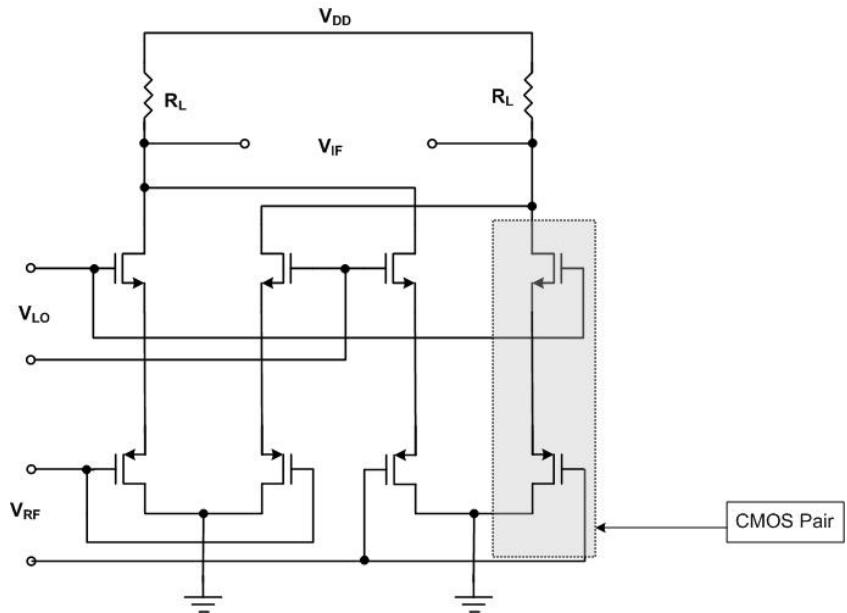


Fig.3.7 Linearized CCM using CMOS pair.

3.3.5 Class A-B Trans-conductor (ABT)

In this CCM linearization approach, the nonlinear class-A trans-conductor of the conventional CCM is replaced by a class AB trans-conductor stage [9]. This design provides 1.4 times the input signal range of a simple differential pair (class A) trans-conductor, and results in more linear trans-conductance range with respect to the input signal. The circuit diagram of a CCM using the class AB trans-conductor is shown in Fig. 3.8. The technique improves the linearity of the trans-conductance stage at the expense of increasing the power consumption and degrading the noise figure characteristics of the design.

Chapter 3 - CMOS Downconversion Mixer

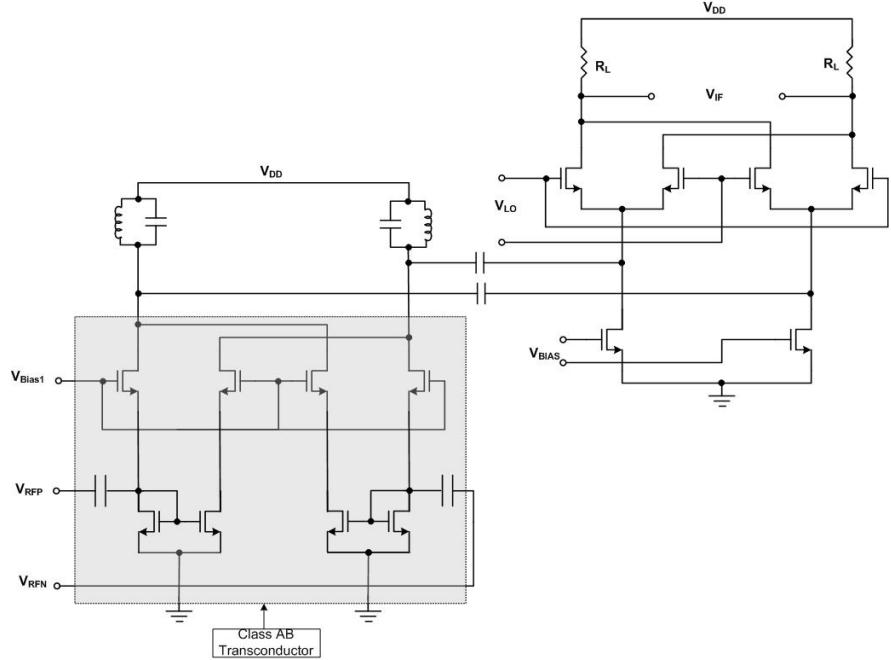


Fig.3.8 Linearized CCM using class AB trans-conductor.

3.3.6 Summary

Previous CCM linearization techniques do not provide an optimum solution to meet the low voltage and good linearity requirements of future generation of mobile phones. The SDE approach is not as efficient to linearize MOS trans-conductors compared to their bipolar counterpart. A typical implementation of this technique at low-GHz range uses 15nH of inductive degeneration which is not reasonable in terms of chip area [5]. The DMA technique adds to the complexity because of the requirement of clock generation circuitry and associated buffers [6]. The CCT increases the power consumption at higher frequencies [7] and the CMP is not suitable for low voltage applications [8]. At GHz frequencies, the ABT shows a relatively high noise figure due to the large number of transistors used in its trans-conductance stage [9]. In this work a low-power solution is proposed for the linearity/low-supply problem which is described in details in the next section.

3.4 Low-Voltage, High-Linearity Mixer Design Issues

In this section, the linearity characteristics of the main blocks involved in the CCM are discussed.

3.4.1 Effect of the Trans-impedance Stage on the Linearity of CCM

As mentioned previously, the trans-impedance stage of a CCM may be implemented using resistors or transistors. Trans-impedance blocks implemented using resistors are typically expected to be more linear than those implemented using transistors since resistors ideally¹ have a linear behaviour. In the case of integrated resistors, depending on their type and the frequency of operation they may exhibit nonlinear behaviour which is mainly attributed to the nonlinear parasitic capacitances associated with the integrated resistors. At low frequencies², the effect of the parasitic capacitances on the linearity characteristics of the integrated resistors is negligible.

3.4.2 Effect of the Mixing Stage on the Linearity of CCM

The effect of the mixing stage of a CCM shown in Fig. 3.4 on linearity has been previously investigated in the literature [15]. It depends to a great extent on the frequency of operation. At low frequencies where the parasitic capacitances associated with the transistors are negligible, the nonlinearity of the switching pairs is low and increases at higher frequencies where the parasitic capacitances and their nonlinear behaviour come into play. Although the nonlinearity of the mixing stage becomes more pronounced at higher frequencies, the trans-conductor stage is

¹ Due to the voltage coefficient present in integrated resistors (IR) caused by the end effects, IRs may show nonlinear behaviour. This behaviour depends mainly on resistors aspect ratio and width. This should be considered while choosing the aspect ratio and width of the resistor. In TSMC 0.18 μm CMOS width > 1 μm and aspect ratio > 2 should be chosen to ensure perfect linearity of resistors.

² Baseband frequency in a direct conversion receiver (DCR).

Chapter 3 - CMOS Downconversion Mixer

still the dominant source of nonlinearity in a conventional CCM compared to the mixing stage [15].

3.4.3 Effect of the Trans-conductor on the Linearity of CCM

In a conventional CCM, with a trans-conductor implemented using a simple differential pair, as illustrated in Fig. 3.9(a), The differential pair has a nonlinear voltage to current transfer characteristics resulting in a non-constant trans-conductance (G_m) as shown in Figs. 3.9(b) and (c) respectively, which degrades the linearity of the CCM.

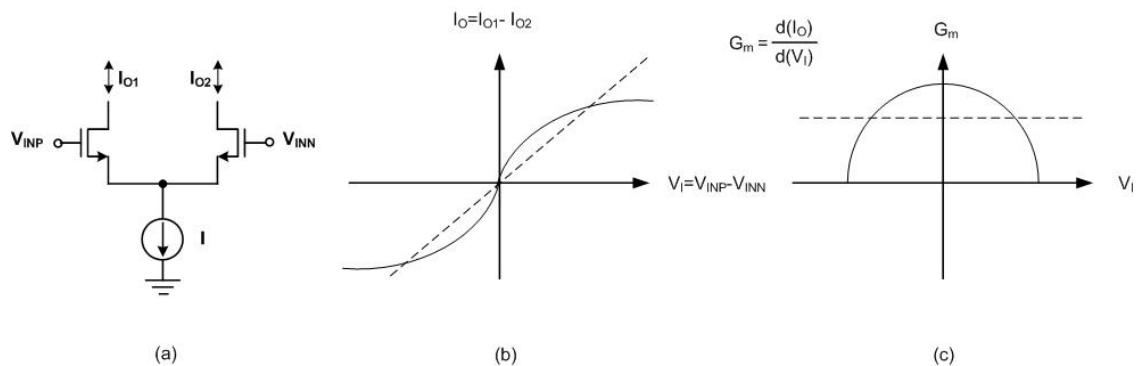


Fig.3.9 Conventional trans-conductor in CCM. (a) Circuit diagram. (b) Actual and ideal I-V transfer curves. (c) Actual and ideal trans-conductance.

In older generations of CMOS technology in which the MOSTs feature a quadratic behaviour in the active region of operation, the relationship between the output differential current $I_o = I_{o1} - I_{o2}$ and the input differential voltage V_i in Fig. 3.9(a) is given by the following nonlinear relationship

$$I_{o2} - I_{o1} = \beta \cdot V_i \cdot \sqrt{\frac{2I}{\beta} - V_i^2} \quad (3.1)$$

where

$$\beta = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \quad (3.2)$$

Chapter 3 - CMOS Downconversion Mixer

where μ_n is the bulk mobility of the MOS transistor, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and the length of the MOS transistor; V_{th} is the threshold voltage of the MOS transistor and I is the value of the tail current source. Removing the tail current source (grounding the sources of the differential pair transistors), linearizes the transfer characteristic which is now given by

$$I_{o2} - I_{o1} = \beta \cdot V_{th} \cdot V_i \quad (3.3)$$

In deep submicron advanced technologies, the I-V characteristics of the transistor in the saturation region is no longer quadratic [13,14]; and the transfer characteristics of the differential pair trans-conductor without the tail current source becomes nonlinear and given by

$$I_{o1} - I_{o2} = \frac{\beta V_i}{2} \left[\frac{\theta \left(\frac{V_i^2}{4} + V_{th}^2 \right) + V_{th}(k - \theta V_{th})}{(k - \theta V_{th})^2 - \frac{\theta^2 V_i^2}{4}} \right] \quad (3.4)$$

Where

$$k = 1 + \xi \frac{V_{ds, sat}}{L} \quad (3.5)$$

where ξ is the mobility degradation factor due to the vertical electric field in the channel of the device, θ is the mobility degradation factor due to the horizontal electric field in the channel and $V_{ds, sat}$ is the saturation voltage of the transistor.

From the above discussion, it is apparent that to improve the performance of the conventional CCM in terms of linearity, it is necessary to improve the characteristics of the trans-conductor stage, particularly at low supply voltages.

3.5 Proposed Mixer and Design Methodology

3.5.1 Background

A trans-conductor which improves the linearity of differential pair CMOS trans-conductors was proposed by Wang and Guggenbuhl [16] and is shown in Fig. 3.10. It features a bias-offset technique which involves applying an offset to the biasing voltages of the transistors acting as trans-conductors (M_1 , M_2 , M_3 and M_4) in order to generate a constant trans-conductance. The offset bias is applied through transistors M_5 , M_6 , M_7 and M_8 . These transistors are equally sized. Since the DC current flowing through M_5 and M_6 (M_7 and M_8) are equal, the DC voltage V_{offset} applied to the gate-source junction of M_6 (M_8) is copied to the gate-source of M_5 (M_7) and the desired offset between the gate bias voltages of M_1 and M_3 (M_2 and M_4) is hereby created. The technique, however, is not suitable at low voltages and for low power and high frequency applications. For proper operation of the circuit, it is necessary for the ac signal at the gates of M_1 and M_3 (M_2 and M_4) to be identical which may not necessarily be the case at high frequencies. At low supply voltages, the linearity of the circuit degrades due to the large number of stacked transistors. In addition, due to the large number of parallel paths, the architecture is not suitable for low power designs. Furthermore, all the trans-conductor transistors are subject to different threshold voltage modulation effects due to the unequal source and bulk voltages which introduce nonlinearities.

Chapter 3 - CMOS Downconversion Mixer

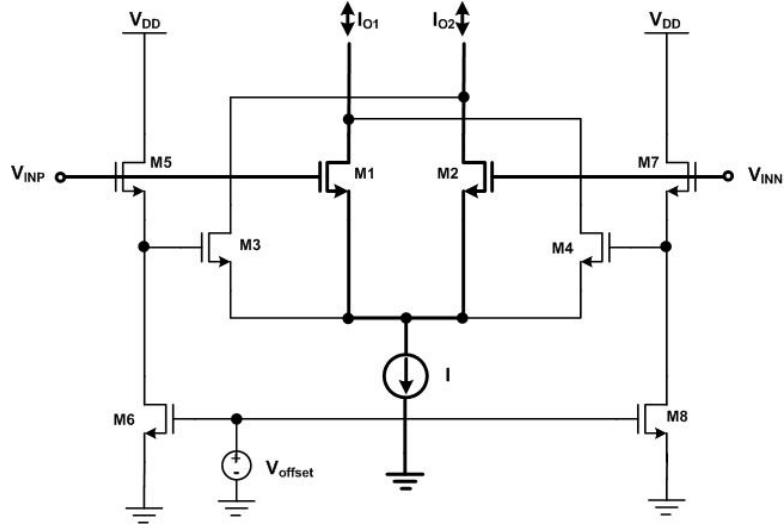


Fig.3.10 The original form of the bias offset technique applied to a conventional NMOS differential pair (highlighted in bold lines) [16].

3.5.2 Novel Mixer Architecture

In this work, a new version of the bias offset technique is used in the trans-conductor design to relax the trade-off between the power conversion gain and linearity while preserving the trans-conductance gain of the circuit and operating at low supply voltages.

Fig.3.11(a) illustrates the novel trans-conductor architecture [17,18]. The offset voltage V_{offset} provides a controlled bias between the gates of M₁ and M₂ (M₃ and M₄). In order to decrease the power consumption of the circuit, current reuse [19,20] is employed in the design through the N and P-channel common source transistors M₁ and M₂ (M₃ and M₄). This technique allows doubling the trans-conductance gain for the same power consumption.

Chapter 3 - CMOS Downconversion Mixer

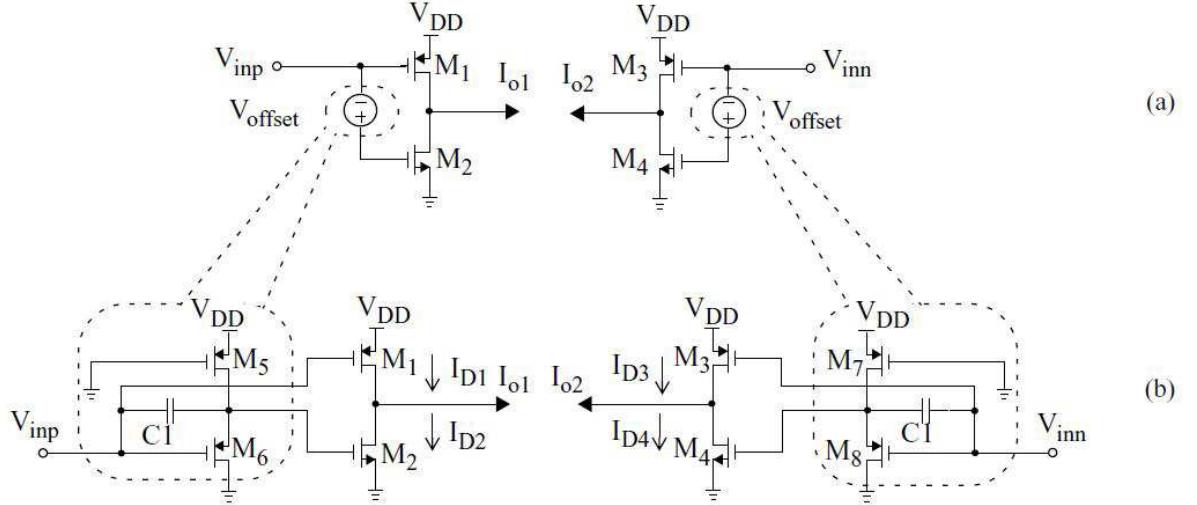


Fig.3.11 The proposed trans-conductor. (a) The bias-offset-technique applied to M₁ and M₂ (M₃ and M₄). (b) The circuit diagram of the proposed bias-offset technique.

In order to gain analytical insight into the linearization technique, the trans-conductance of the circuit shown in Fig. 3.11(a) was derived using the following I_D-V_{GS} transfer characteristics for the MOS transistors [21]

$$I_D = \frac{\mu_0 C_{ox}}{2 \left[1 + \theta(V_{GS} - V_{th}) + \xi \frac{V_{DS, sat}}{L} \right]} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2 \quad (3.6)$$

where μ_0 is the low field bulk mobility of the carriers and V_{GS} is the gate to source voltage of the device. This equation preserves the required simplicity for hand calculations while taking into account short channel effects which impact the linearity of the trans-conductance of the device. The trans-conductance g_m of a MOS transistor calculated from equation (3.6) is

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot \frac{V_{GS} - V_{th}}{1 + 2 \left(\theta + \frac{\xi}{L} \right) \cdot (V_{GS} - V_{th})} \quad (3.7)$$

The trans-conductance G_m of the half circuit consisting of M₁, M₂ and the floating voltage source V_{offset} in Fig. 3.11(a) is given by

Chapter 3 - CMOS Downconversion Mixer

$$G_m = \frac{\partial I_{O1}}{\partial V_{inp}} = \frac{\partial(I_{D1} - I_{D2})}{\partial V_{inp}} = \frac{\partial I_{D1}}{\partial V_{inp}} - \frac{\partial I_{D2}}{\partial V_{inp}} \quad (3.8)$$

where V_{inp} is the voltage applied to the input of the trans-conductor half circuit, as illustrated in Fig. 3.11.

Since $V_{SG1}=V_{DD}-V_{inp}$ and $V_{GS2}=V_{inp}+V_{offset}$, for a fixed V_{DD} and V_{offset} , ∂V_{inp} is given by

$$\partial V_{inp} = -\partial V_{SG1} = \partial V_{GS2} \quad (3.9)$$

From equations (3.8) and (3.9), G_m can be expressed in terms of the trans-conductances g_{m1} and g_{m2} of transistors M_1 and M_2 as

$$G_m = -(g_{m1} + g_{m2}) \quad (3.10)$$

From equations (3.7) and (3.10), G_m can be obtained in terms of V_{offset} , V_{inp} and the aspect ratio of transistors M_1 and M_2 as

$$G_m = -C_{ox}\mu_{on} \cdot \left(\frac{W}{L}\right)_2 \cdot \frac{V_{inp} + V_{offset} - V_{thn}}{1 + 2\left(\theta_n + \frac{\xi_n}{L_2}\right)(V_{inp} + V_{offset} - V_{thn})}$$

$$-C_{ox}\mu_{op} \cdot \left(\frac{W}{L}\right)_1 \cdot \frac{V_{dd} - V_{inp} - |V_{thp}|}{1 + 2\left(\theta_p + \frac{\xi_p}{L_1}\right)(V_{dd} - V_{inp} - |V_{thp}|)} \quad (3.11)$$

To achieve a maximally flat (maximally constant) G_m as a function of V_{inp} at peak G_m , which eventually results in a maximally linear trans-conductor, the second and third order derivatives of G_m with respect to V_{inp} are set to zero at peak G_m by choosing a proper value for V_{offset} and $(W/L)_2/(W/L)_1$. For typical values of the technology parameters, Fig. 3.12 is a normalized plot of G_m without applying the flattening technique (plot with diamond markers), and with its second and third order derivatives set to zero (plot with square markers).

Chapter 3 - CMOS Downconversion Mixer

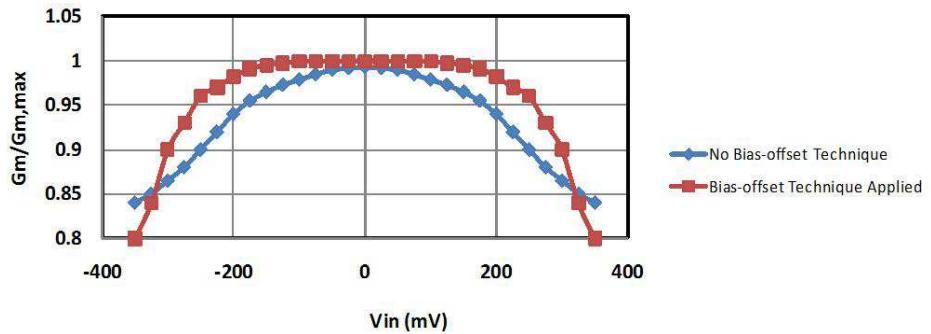


Fig.3.12 Normalized G_m as a function of V_{inp} .

The voltage V_{offset} is realized by transistors M_5 and M_6 (M_7 and M_8). It is described as a function of the aspect ratios of M_5 and M_6 (M_7 and M_8) by the following equation

$$V_{\text{offset}} = \frac{\alpha}{\alpha + 1} |V_{\text{thp}}| + \sqrt{\left(\frac{\alpha}{\alpha + 1} |V_{\text{thp}}|\right)^2 - \frac{\alpha |V_{\text{thp}}|^2 - V_{\text{dd}}^2}{\alpha + 1}} \quad (3.12)$$

where

$$\alpha = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} \quad (3.13)$$

Fig.3.13 shows a plot of V_{offset} versus α for the typical threshold voltage ($V_{\text{thp}} = -0.45\text{V}$) of the technology under consideration. V_{dd} is set to 1V.

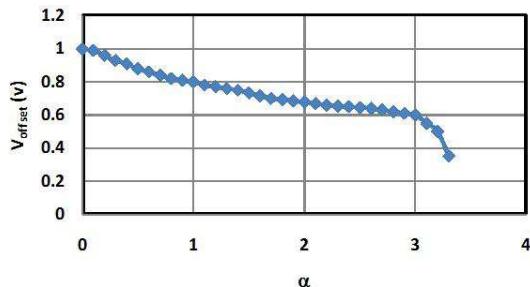


Fig.3.13 V_{offset} as a function of the ratio of the aspect ratio, α , of the transistors building the following voltage source.

Chapter 3 - CMOS Downconversion Mixer

The low-voltage capability of the trans-conductor shown in Fig.3.11(b) is achieved by offsetting the gate bias voltage of M_1 and M_2 (M_3 and M_4) to provide simultaneously high input voltage range for both M_1 and M_2 (M_3 and M_4) at a supply voltage of 1V. The design ensures simultaneous operation of M_1 , M_2 , M_3 and M_4 in the active region over a relatively large range of the input signal levels. This feature along with the fully symmetric characteristics of the design is key to the good linearity behaviour of the design in terms of second-order nonlinearity. Capacitor C_1 in Fig. 3.11(b) provides a feed forward path for the RF signal and improves the high frequency performance of the floating voltage source. By introducing C_1 , the RF signal appearing at the gates of M_1 and M_2 (M_3 and M_4) will be identical as required for the proper operation of the circuit. This form of the bias offset technique is applicable at any RF frequency as long as the transistor is capable of providing a reasonable trans-conductance. In order to further improve the linearity of the trans-conductor, threshold voltage modulation is eliminated by shorting the source-bulk junctions of all the transistors used in the stage. The Deep-N-Well (DNW) non-linear capacitor is choked by adding a $10k\Omega$ resistor in DNW ties to the power supply (soft tied DNW).

Fig. 3.14 illustrates the simulated trans-conductance G_m of the half circuit shown in Fig.3.11(b) and consisting of M_1 , M_2 , M_5 and M_6 for three different values of V_{offset} and for $(W/L)_1=32\mu m/0.18\mu m$ and $(W/L)_2=20\mu m/0.18\mu m$. As observed, a value of $V_{offset}=750mV$ results in a constant trans-conductance over a relatively wide range of the input differential voltage (-280mV to 280mV), which in turn translates into good linearity performance of the mixer.

Chapter 3 - CMOS Downconversion Mixer

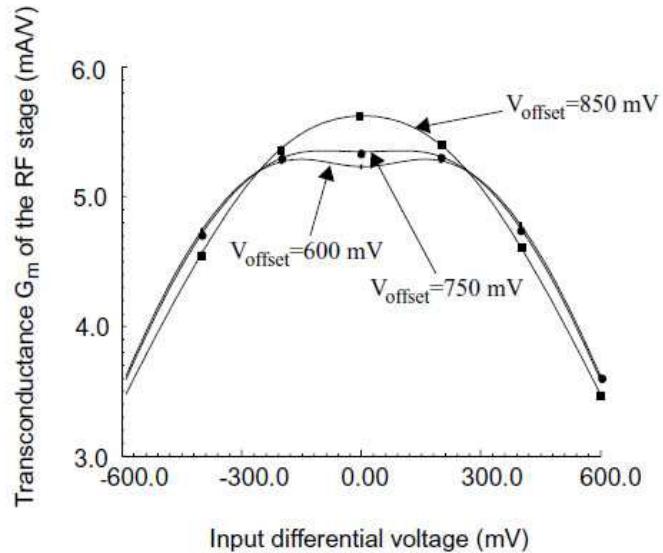


Fig.3.14 Trans-conductance G_m of the trans-conductor, for three different values of offset voltage. The flat trans-conductance ($V_{offset}=750\text{mV}$) was obtained for $(W/L)_1=32\mu\text{m}/0.18\mu\text{m}$, $(W/L)_2=20\mu\text{m}/0.18\mu\text{m}$, $(W/L)_5=30\mu\text{m}/0.25\mu\text{m}$, $(W/L)_6=16\mu\text{m}/0.18\mu\text{m}$.

The final schematic of the mixer under consideration is illustrated in Fig. 3.15 and the values of all the components are given in the caption. As illustrated, the RF trans-conductor is ac-coupled to a mixing stage made of cross-coupled differential pairs which is terminated in a low pass load to eliminate any undesirable high frequency content in the output signal. Active loads are avoided at the output of the mixer to minimize flicker noise and improve the NF at baseband frequencies. The cross coupled mixing stage is biased through LC resonators (set at 8 GHz) instead of the conventional current sources to enable low-voltage operation [22] and optimize the performance of the mixing stage at 8GHz.

Chapter 3 - CMOS Downconversion Mixer

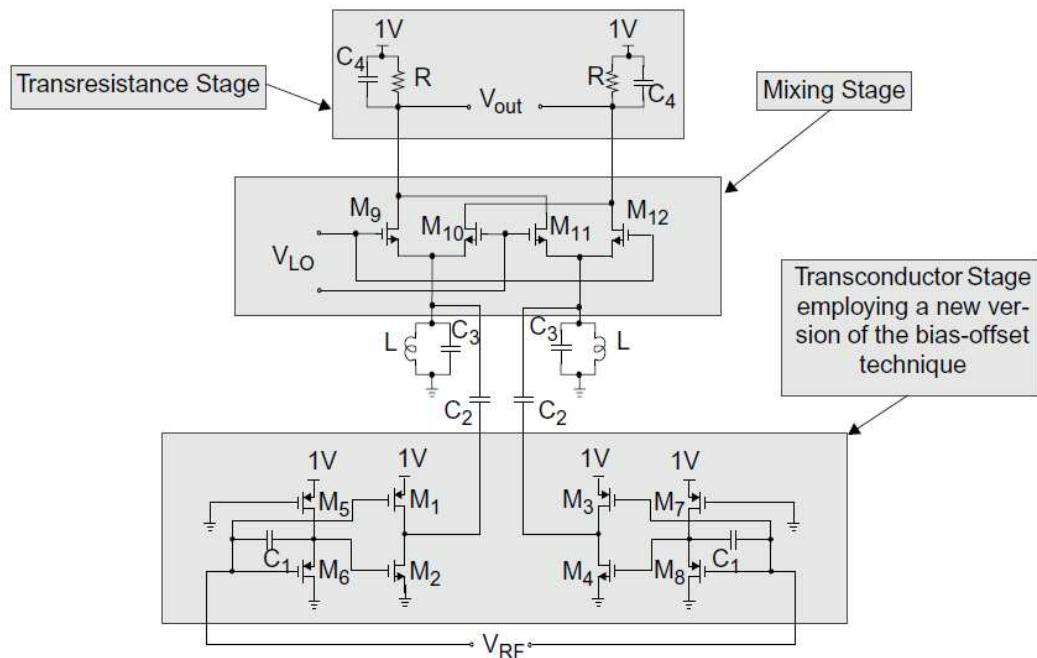


Fig.3.15 Schematic of the proposed mixer. ($M_1, M_3 : 32/0.18$; $M_2, M_4 : 20/0.18$; $M_5, M_7 : 30/0.25$; $M_6, M_8 : 16/0.18$; $M_9, M_{10}, M_{11}, M_{12} : 8/0.18$; all dimensions are in microns. $L=0.5\text{ nH}$; $C_1=1\text{ pF}$, $C_2=8\text{ pF}$, $C_3=0.8\text{ pF}$, $C_4=2\text{ pF}$. $R=500$). The DC level of the RF input is 0V and the DC value of the LO input is 0.55V.

3.6 Layout

In the case of RF circuits, the performance of the implemented design is to a great extent dependent on the way the circuit is laid out. This is mainly due to the fact that the parasitic coupling between interconnects and devices and/or the substrate is relatively high. In addition, RF circuits are more sensitive to parasitic resistance, inductance and capacitances associated with the interconnects. These undesired couplings and parasitics affect the performance of the circuit. In deep sub-micron CMOS technologies second order layout effects such as Length of Diffusion (LOD) and Well-Proximity-Effect (WPE) intensifies the importance of layout in the final circuit performance.

3.6.1 High Frequency Layout Considerations

In this work, the substrate is covered with the lowest layer of metal as a ground plane where possible, to shield it from the noise coming from the high frequency interconnects and pads.

All transistor gates are connected at both ends to reduce gate resistance. Guard rings are placed around the transistors to reduce the equivalent substrate resistance and to lower noise injection to the substrate. Dummy diffusions and fingers are placed where applicable to achieve predictable and matched device performance. Also, a large number of contacts and vias are used to decrease interconnect resistance. The finger width in the transistor layout is chosen such that the transistor's noise and speed performance are optimized (in this case, a finger width of $2.5\mu\text{m}$ results in optimal performance for noise).

To improve the RF-port to LO-port isolation, the separation between the RF and the LO sections of the mixer is maximized in addition to placing all transistors individually in DNWs isolated from the substrate to minimize coupling between the two ports. The mixing cross-coupled transistors are placed in one DNW as a group to minimize parasitic capacitance.

3.6.2 Layout Considerations for Best Linearity Performance

The second order nonlinearities in a CMOS differential design can be affected by any asymmetry or systematic mismatch in the differential paths. Therefore, it is important for the layout to be fully symmetric to maximize the differential signal paths matching. The symmetry of the layout also helps in rejecting the common noise picked up by the circuit from other devices located on the same chip.

Undesired threshold voltage modulation due to the body effect is one of the factors affecting the linearity characteristics of MOS transistors. It can be eliminated by shorting the source and the

Chapter 3 - CMOS Downconversion Mixer

bulk of the transistors and surrounding each transistor with sufficient bulk contacts shorted to the source. In doing so, the DNW where the device resides is soft-tied to VDD to minimize the non-linear effect of the DNW parasitic diode. Fig. 3.16 illustrates the layout considerations used to eliminate the threshold voltage modulation assisted nonlinearity for N-channel MOS transistors. A similar approach may be used to eliminate the body effect of the P-channel MOS transistor.

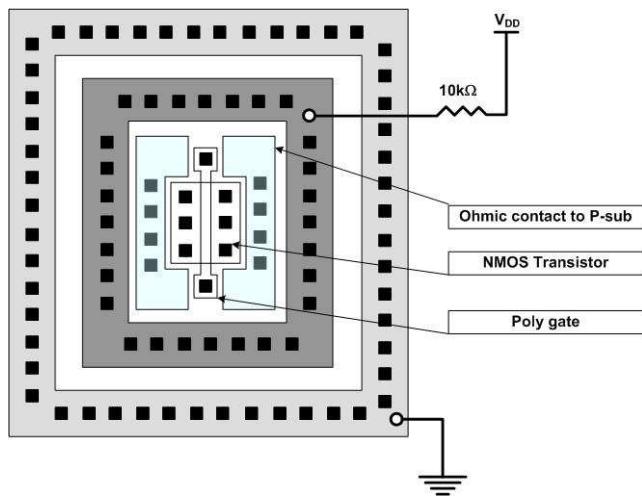


Fig.3.16 Layout consideration to achieve best linearity performance.

3.6.3 Mixer Layout

The mixer was designed in a standard $0.18 \mu\text{m}$ CMOS technology with six layer of metallization. The layout of the mixer is illustrated in Fig. 3.17. The core area of the design is $320 \times 400 \mu\text{m}^2$. The test chip area including the pads is $1080 \times 710 \mu\text{m}^2$. Decoupling capacitors (100 pF) were used on-chip at V_{DD} . All capacitors are implemented using metal-insulator-metal (MIM) integrated capacitors. The resistors are implemented using un-silicided poly-silicon resistors sitting on a deep-NWELL soft tied to VDD.

Chapter 3 - CMOS Downconversion Mixer

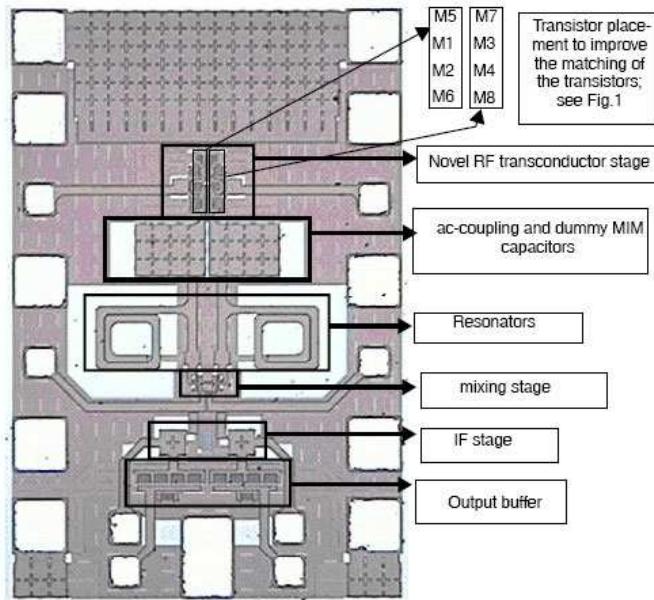


Fig.3.17 The proposed mixer layout.

The inductors were implemented as spirals using the sixth metal layer. They were designed using Agilent Technologies Advanced Design System (ADS) software package [23]. The layout of a typical 0.5nH inductor is shown in Fig. 3.18. The dimensions of the inductor are displayed in the diagram.

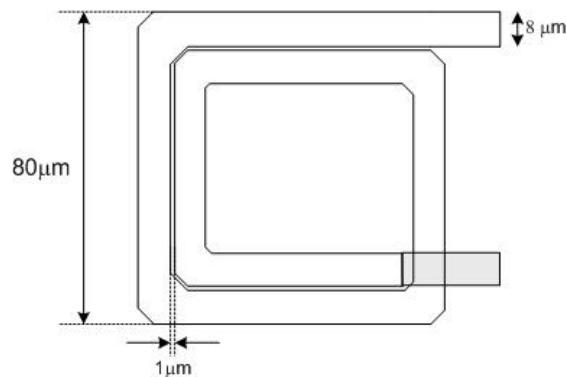


Fig.3.18 0.5nH integrated inductor aspect ratio.

For post layout simulations, the inductors were replaced by a lumped model at 8 GHz, obtained using ADS and shown in Fig. 3.19.

Chapter 3 - CMOS Downconversion Mixer

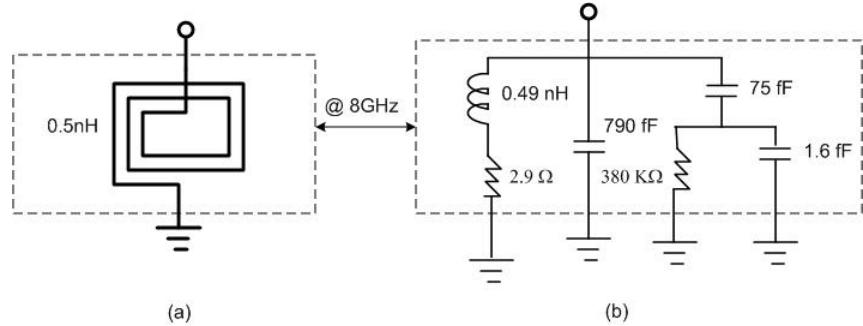


Fig.3.19 Integrated inductor lumped model used for post layout simulation.

3.7 Post-Layout Simulations

The simulations of the mixer were carried out using the Spectre simulator [24]. Fig. 3.20 illustrates the two-tone test post-layout simulation results at 8001MHz and 8003MHz. The intercept of the linear extrapolation of the first and third order terms indicates an IIP3 of +3 dBm. The IIP2 of the mixer was simulated and found to be better than +52 dBm using Monte-Carlo simulation. The linearity characterization was carried out using time domain simulations and taking the Discrete Fourier transform (DFT) of the output waveform to find the power of the linear and intermodulation tones present in the output spectrum.

Fig. 3.21 shows a plot of the power transfer characteristics of the mixer. From the plot, it is apparent that the mixer exhibits a 1-dB compression point of -8 dBm and a power conversion gain (PCG) of +10 dB.

Chapter 3 - CMOS Downconversion Mixer

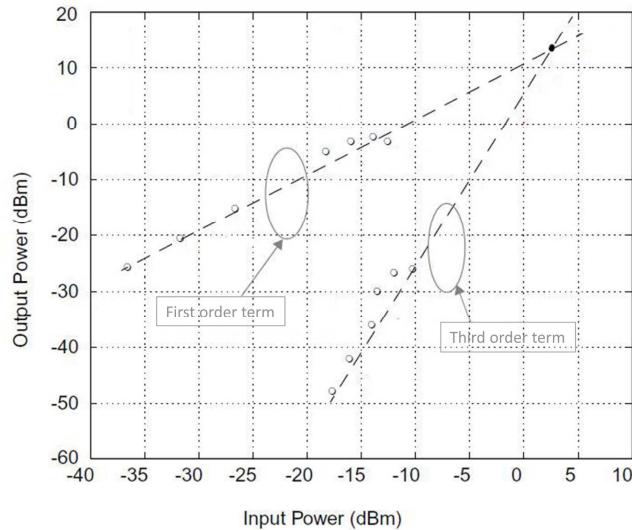


Fig.3.20 Two-tone simulation.

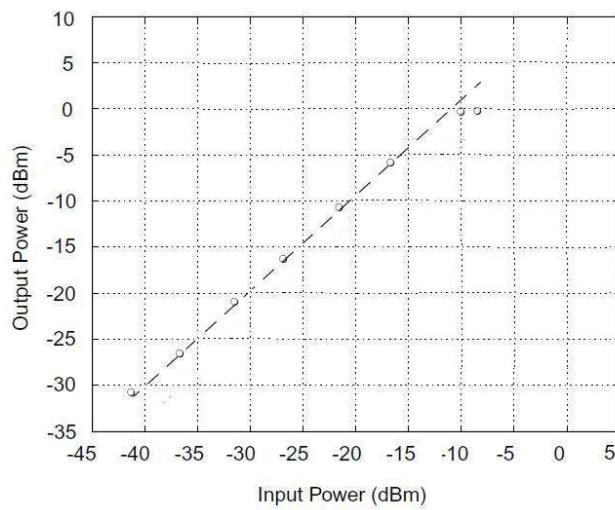


Fig.3.21 Power transfer characteristics of the mixer.

The noise figure simulation for the mixer reveals a minimum noise figure of 10dB.

Chapter 3 - CMOS Downconversion Mixer

Table 3.1 compares the post layout simulation results to the target specifications listed in Chapter 1. As observed, the proposed mixer meets the low-voltage and linearity requirements of future generations of mobile phones. Specifically, the design relaxes the trade-off between power conversion gain and linearity of CCMs which allows for simultaneously improving the gain and linearity of the mixer. The design offers considerable advantages over the conventional CCM [5] in terms of gain and linearity and in addition operates at 1 V supply which is not possible in the conventional case.

Table 3.1 Target Specifications and Post Layout Simulations

	Target specifications	Simulation Results; Typical Process Parameters, 25°C
Technology (mm)	0.18	0.18
Supply Voltage (v)	1	1
Frequency (GHz)	8	8
Noise Figure (dB)	<13	10
IIP3(dBm)	> 3	+3
IIP2 (dBm)	> 50	+52
P-1dB (dBm)	> -7	-8
Conversion Gain (dB)	> 6	+ 10
Power Consumption (mW)	Minimum	6.2

Table 3.2 shows the effect of process variation on the performance of the proposed mixer architecture. The speed worst case and power worst case listed in the Table include power supply variations of +10% and -10% respectively. The Table confirms the robustness of the design to process and supply voltage variations.

Chapter 3 - CMOS Downconversion Mixer

Table 3.2 Effect of Process Variations on the Performance of the Mixer

	Typical Process Parameters	Slow Corner Parameters	Fast Corner Parameters
Gain	10 dB	7 dB	12 dB
IIP3	+3 dBm	+4 dBm	+2.5dBm
IIP2	+52dBm	+58dBm	+51dBm
P-1dB	-8 dBm	-9.5 dBm	-7.5 dBm
Power Consumption	6.2 mW	6 mW	6.9 mW

The characteristics of the proposed mixer, were simulated, for standard process parameters, over a temperature range of -25°C to 125°C. Table 3.3 summarizes the performance of the circuit at -25°C, 27°C and 125°C. The change in the behaviour of the proposed design as a function of temperature is mainly due to threshold voltage dependence of MOSTs on temperature [9,26].

Table 3.3 Effect of Temperature Variation on the Performance of the Mixer

	-25°C	27°C	125°C
Gain (dB)	8	10	6
IIP3 (dBm)	+3.1	+3	+2
IIP2 (dBm)	+51	+52	+49
P-1dB (dBm)	-8	-8	-8.4
Power consumption (mW)	6.1	6.2	6.5

3.8 Summary

The current commutating mixer (CCM) and the three main blocks involved in the architecture of CCM were discussed. The various linearization techniques previously applied to the CCM were presented and the limitations of each of those techniques were considered. A novel CCM architecture using a bias offset technique was proposed. This architecture relaxes the inherent trade-off between power conversion gain and linearity that governs all type of active mixers. The post-layout simulation results indicate that the proposed design satisfies the linearity, low voltage and design simplicity requirements of future generations of mobile phones.

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Chapter 3 - CMOS Downconversion Mixer

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CHAPTER 4: CMOS Quadrature Generator

4.1 Introduction

This chapter deals with the design and analysis of the 8 GHz quadrature generator. The design embodies the quadrature generation scheme into the LO-buffer using active inductors. The layout and post layout simulations of the proposed design are presented.

4.2 Conventional Quadrature Generators

Signals with equal amplitudes and quadrature phases are widely used in a variety of applications including direct conversion receivers to demodulate the incoming angle-modulated data. Previously reported quadrature generators and their pros and cons were discussed in Chapter 1. As mentioned in that chapter, the necessity for buffering stages between the local oscillator and the quadrature generator as well as between the quadrature generator and the mixers in previously reported quadrature generators, increases the power consumption. To decrease the power consumption, these buffers should be eliminated.

The concept of integrating the quadrature generating scheme into the LO-buffer was previously introduced by Steyaert and Roovers [1] using bipolar technology. A CMOS implementation of the design is illustrated in Fig. 4.1.

Chapter 4 - CMOS Quadrature Generator

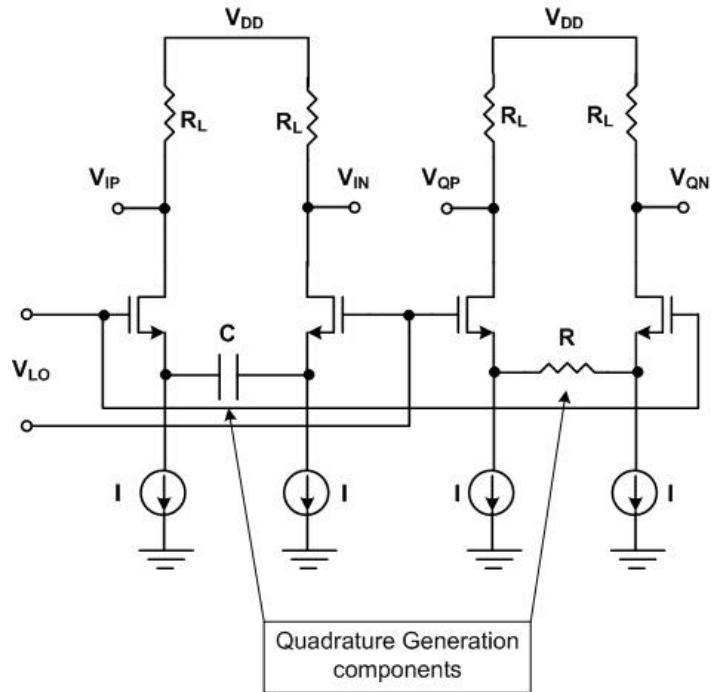


Fig 4.1 Quadrature generation components imbedded in the LO buffer [1].

In this circuit, the differential input voltages denoted as V_{LOn} and V_{LOp} in the figure are transformed to current by the capacitive and resistive degenerated differential pairs, resulting in i_I and i_Q given by

$$i_I = (V_{LOp} - V_{LOn}) \cdot sC \quad (4.1)$$

$$i_Q = \frac{V_{LOp} - V_{LOn}}{R} \quad (4.2)$$

As observed from equations (4.1) and (4.2), i_I and i_Q exhibit a phase difference of 90° . The resistive loads R_L transform the currents i_I and i_Q to voltages while preserving the 90° phase shift resulting in the four quadrature phase outputs, V_{Ip} , V_{In} , V_{Qp} and V_{Qn} defined as

Chapter 4 - CMOS Quadrature Generator

$$V_{Ip} = -R_L(V_{Lop} - V_{Lon}) \cdot sC \quad (4.3)$$

$$V_{In} = R_L(V_{Lop} - V_{Lon}) \cdot sC \quad (4.4)$$

$$V_{Qp} = -R_L \frac{(V_{Lop} - V_{Lon})}{R} \quad (4.5)$$

$$V_{Qn} = R_L \frac{(V_{Lop} - V_{Lon})}{R} \quad (4.6)$$

The magnitudes of the four outputs in equations (4.3) to (4.6) are equal only at one frequency. This frequency is obtained by equating the magnitudes of the four outputs which results in

$$\left| R_L(V_{Lop} - V_{Lon}) \cdot sC \right| = \left| R_L \frac{(V_{Lop} - V_{Lon})}{R} \right| \quad (4.7)$$

and implies that $|s| = |j\omega| = \omega = 1/RC$. This technique provides a 90° phase difference between the outputs of the capacitive and resistive degenerated sections of the circuit only if the quality factor of the capacitor is infinite.

Although the design achieves relatively low power consumption by eliminating the buffers located between the quadrature generator and the mixers, in a CMOS implementation, it tends to cause instability due to the negative real part at the gate of the input transistors (M_1 and M_2) generated by the capacitance used for capacitive degeneration (capacitor C in Fig. 4.1) [2].

The focus of this chapter is to present a design scheme that eliminates the buffer between the quadrature generator and the mixers, and integrates the quadrature generation circuitry into the local-oscillator buffer.

4.3 Novel Quadrature Generator Architecture

The block diagram of the proposed design is illustrated in Fig.4.2 [3]. It consists of a LO-buffer, a differential active inductor and two common-mode stabilizers. In this architecture, there is no need for isolating the quadrature generator from the mixers by using additional buffers, since the capacitive loading of the mixers on the quadrature generator can be used in the active inductor design. The LO-buffer consists of common source n-channel transistors loaded by p-channel transistors. The differential active inductor is illustrated in Fig.4.3 and is based on the conventional G_m -C structure. The value of the inductance in this architecture is given by [4]

$$L = \frac{C_t}{g_{mi} \cdot g'_{mi}} \quad (4.8)$$

where g_{mi} and g'_{mi} are the trans-conductances of M_7 (M_8) and M_5 (M_6) respectively and C_t is the total differential parasitic capacitance at the input of the trans-conductor blocks. The capacitive loading of the mixers on the quadrature generator shown in Fig. 4.2 contribute to the capacitance C_t .

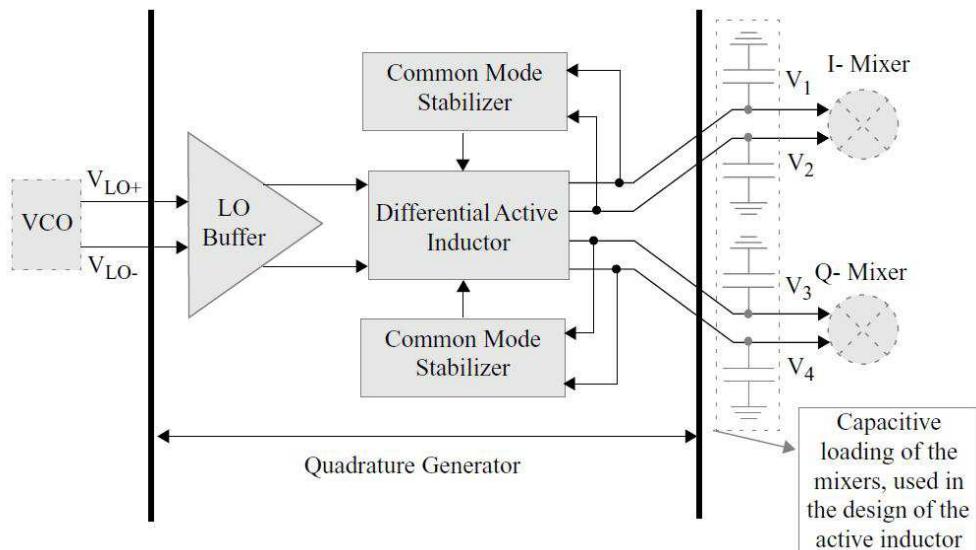


Fig 4.2 Block diagram of the quadrature generator under consideration.

Chapter 4 - CMOS Quadrature Generator

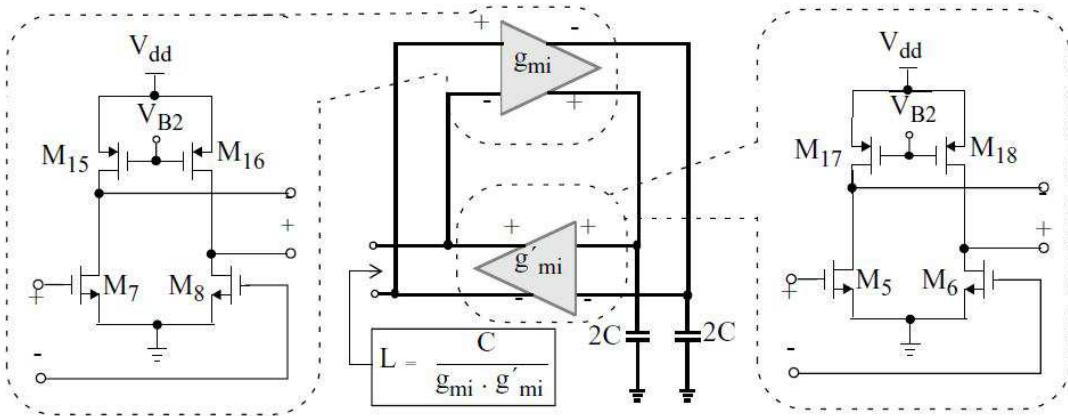


Fig 4.3 Differential active inductor implementation based on the G_m -C architecture.

The common mode stabilizer is illustrated in Fig. 4.4 [5]. In the differential mode of operation of this circuit, replacing transistors M_{21} and M_{22} with the small signal model shown in Fig. 4.5 and replacing transistor M_{23} with an equivalent resistor in the triode region of operation, the common-mode stabilizer appears as impedance Z_o with a real part given by

$$\text{Re}\{Z_o\} \approx \frac{g_{ms}}{B^2 + g_{ms}^2} \parallel r_{os} \quad (4.9)$$

where g_{ms} is the trans-conductance of M_{21} or M_{22} , B is the total susceptance at the outputs of the common-mode stabilizer and r_{os} is the output resistance of M_{23} in the triode region which can be controlled by V_C . As observed, the value of the real part of the impedance is negative and controlled by r_{os} provided that

$$|r_{os}| > \left| \frac{g_{ms}}{B^2 + g_{ms}^2} \right| \quad (4.10)$$

Chapter 4 - CMOS Quadrature Generator

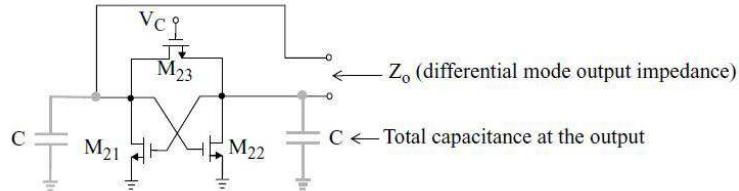


Fig 4.4 Common mode stabilizer circuit.

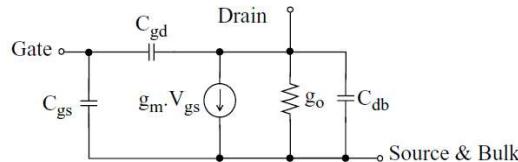


Fig 4.5 Small signal model of the MOS transistor in the active region of operation.

4.4 Design and Analysis of the Proposed Quadrature Generator

The complete circuit of the proposed quadrature generator is shown in Fig.4.6. Transistors M_1 , M_2 , M_{13} and M_{14} form the LO-buffer and M_3 , M_4 , M_{19} and M_{20} are dummy transistors identical to M_1 , M_2 , M_{13} and M_{14} , added to the circuit to preserve the symmetry of the circuit, which is crucial for proper quadrature operation. The capacitors C_{aux} implemented by the gate to source and gate to drain capacitances of the n-channel transistors M_9 , M_{10} , M_{11} and M_{12} , are included in the design to relax the coupling between the amplitude and phase tuning of the quadrature generator by cancelling out the gate to drain capacitances of transistors M_1 , M_2 (M_3 , M_4). This is done by setting the aspect ratio (W/L) of M_9 to M_{12} to be half of that of M_1 to M_4 such that the sum of the gate to drain and the gate to source capacitances of M_9 to M_{12} equals the gate to drain capacitance of M_1 to M_4 . To obtain analytical insight into the quadrature signal generation of the circuit, the outputs of the circuit of Fig.4.6 are derived in terms of the differential local oscillator voltage (V_{LO}). This is done by replacing transistors M_1 , M_2 and M_5 to M_8 by the small signal model illustrated in Fig.4.5 and replacing transistors M_3 , M_4 and M_{13} to M_{20} by parallel RC circuits, representing the output resistance and the sum of the drain to bulk and drain to gate capacitances of each transistor. In the differential mode of operation, the common-mode

Chapter 4 - CMOS Quadrature Generator

stabilizers are replaced by a negative resistance which is designed to cancel out the equivalent conductance at nodes A, B, C and D in Fig.4.6, which is necessary for the quadrature phase matching of the outputs. The output capacitance of the common-mode stabilizer is merged in the equivalent capacitances at nodes A, B, C and D. The resulting equations specifying voltages V_1 to V_4 are listed below:

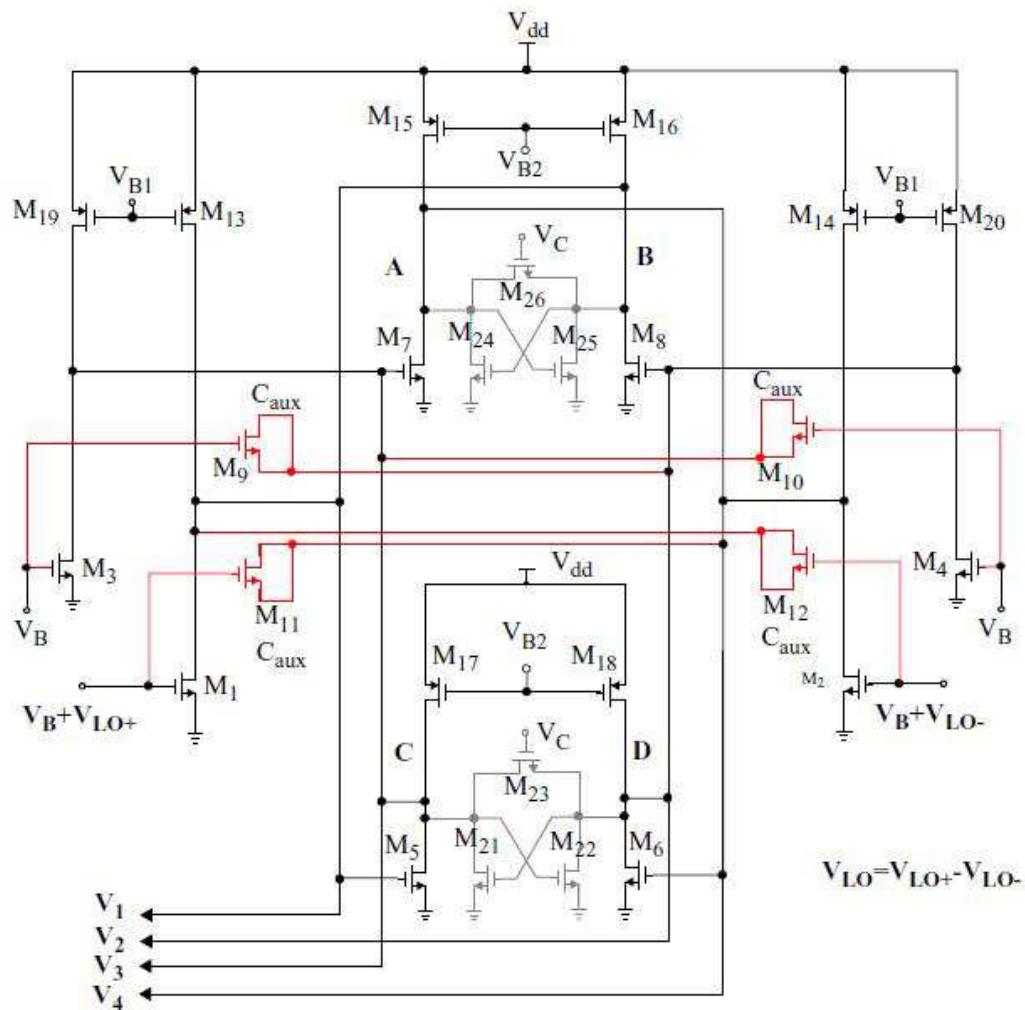


Fig 4.6 Circuit of the quadrature generator. (M_1 to M_8 : 10/0.18; M_{21} , M_{22} , M_{24} and M_{25} : 9/0.18; M_{13} , M_{14} , M_{19} and M_{20} : 12/0.18; M_9 to M_{12} : 5/0.18; M_{15} to M_{18} : 12/0.18; M_{23} and M_{26} are zero threshold voltage devices: 6/0.5; all dimensions are in μm . $V_{dd}=1\text{V}$, $V_B=750\text{mV}$, $V_{B1}=150\text{mV}$, $V_{B2}=0$, $V_C=850\text{mV}$)

Chapter 4 - CMOS Quadrature Generator

$$V_1 = H(s)[g_{mb} + s(C_{aux} - C_{gdb})][g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})]V_{LO} \quad (4.11)$$

$$V_2 = H(s)[g_{mb} + s(C_{aux} - C_{gdb})]g_{mi}V_{LO} \quad (4.12)$$

$$V_3 = -H(s)[g_{mb} + s(C_{aux} - C_{gdb})]g_{mi}V_{LO} \quad (4.13)$$

$$V_4 = -H(s)[g_{mb} + s(C_{aux} - C_{gdb})][g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})]V_{LO} \quad (4.14)$$

where

$$H(s) = \frac{(g_{mi} - 2sC_{gdi})^2 - [g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})]^2}{a(s) - b(s)} \quad (4.15)$$

and

$$a(s) = \left[(g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux}))^2 + 2C_{gdi}(g_{mi} - sC_{gdi}) \right]^2 \quad (4.16)$$

$$b(s) = \left[s^2 C_{gdi}^2 + (g_{mi} - sC_{gdi})^2 \right]^2 \quad (4.17)$$

where C_{gdb} is the gate to drain capacitance of the n-channel transistors in the LO-buffer, C_{gdi} represents the gate to drain capacitor of the n-channel transistors forming the active inductor, C_{eq} is the equivalent capacitance at nodes A, B, C and D, g_{mb} is the transconductance of the n-channel transistors in the LO-buffer, g_{mi} is the transconductance of the n-channel transistors in the active inductor and g_{oeq} is the equivalent conductance at nodes A, B, C and D.

As observed from equations (4.11) to (4.14), by eliminating the equivalent conductance at nodes A, B, C and D in Fig.4.6 (i.e. $g_{oeq}=0$), using the negative output conductance of the common-

Chapter 4 - CMOS Quadrature Generator

mode stabilizer circuit in its differential mode of operation, the voltages V_1 and V_4 have a 90° phase shift relative to V_2 and V_3 respectively. This phase shift is represented by the term $s(2C_{gdi}+C_{gdb}+C_{eq}+C_{aux})$ in the analytical expressions for V_1 and V_4 . V_c can also be used to apply an optional automatic phase tuning signal to this circuit to compensate for process and temperature variations of the output phase [6]. From equations (4.11) to (4.14) it is clear that once the quadrature phase matching is achieved ($g_{oeq}=0$), the amplitudes of V_1 to V_4 can be made equal at a desired frequency, provided that

$$g_{mi} = \omega \cdot (2C_{gdi} + C_{gdb} + C_{eq} + C_{aux}) \quad (4.18)$$

The value of g_{mi} is adjusted by setting the DC currents of M_5 to M_8 using the p-channel transistor M_{15} to M_{18} in Fig. 4.6 to satisfy equation (4.18).

By choosing $C_{aux}=C_{gdb}$, the multiplicand $[g_{mb} + s(C_{aux}-C_{gdb})]$ in equations (4.11) to (4.14), reduces to g_{mb} , and therefore the magnitudes of V_1 , V_2 , V_3 and V_4 can be adjusted independently of their phases by varying g_{mb} . The trans-conductance g_{mb} is controlled by the bias current flowing through M_1 and M_2 using the p-channel transistors M_{13} and M_{14} and V_{B1} . An optional automatic amplitude control signal V_{B1} can be applied to the gates of M_{13} and M_{14} to compensate for process and temperature variations of the output amplitudes [5].

The common-mode equivalent half-circuit of the quadrature generator illustrated in Fig. 4.6 is shown in Fig. 4.7. The auxiliary capacitors are not included in this Figure. In the common mode of operation, they are absorbed in the gate-drain capacitances of the n-channel transistors in the LO-buffer. In order to explain how the common mode stabilizer stabilizes the proposed circuit, the common mode transfer function of the circuit is extracted for two different cases: one excluding the common mode stabilizer transistors (M_{21} and M_{24}) and one including them. These two cases are discussed in details below.

Chapter 4 - CMOS Quadrature Generator

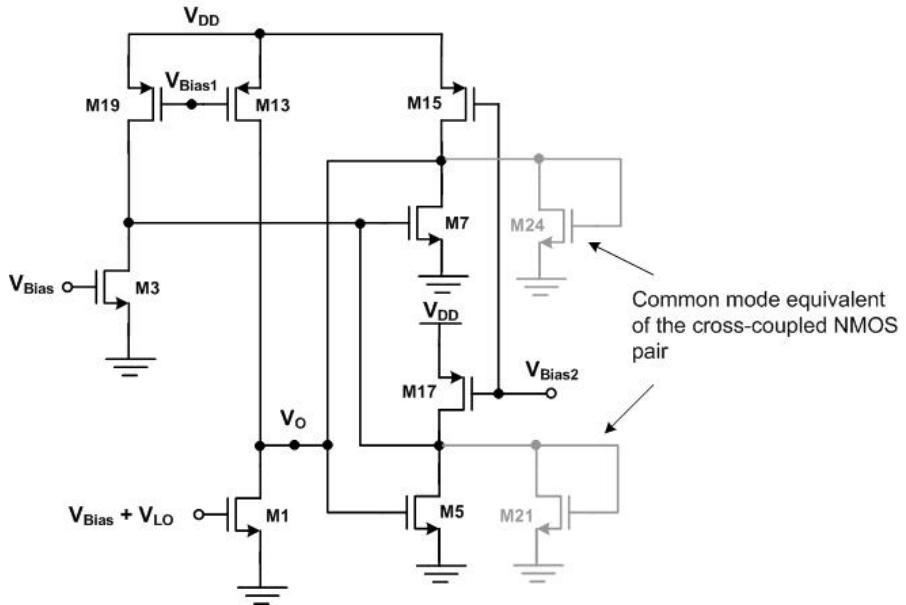


Fig 4.7 Equivalent common mode half circuit of the proposed quadrature generator.

The common mode transfer function of the quadrature generator without the common mode stabilizer transistors M_{21} and M_{24} is obtained from the common mode equivalent circuit illustrated in Fig. 4.7, by replacing transistors M_1 , M_5 , M_7 with their small signal model, and replacing the rest of the transistors with their parasitic resistances and capacitances and is given by

$$\frac{V_o}{V_{LO}} = \frac{(g_{m1} - sC_{gd1})(g_2 + s(C_2 + C_3))}{qs^2 + rs + g_1g_2 - g_{m5}g_{m7}} \quad (4.19)$$

Where

$$q = C_3(C_1 + C_2 + C_{gd1}) + C_2(C_1 + C_{gd1}) \quad (4.20)$$

$$r = g_1(C_2 + C_3) + g_2(C_1 + C_2 + C_{gd1}) + C_2(g_{m5} + g_{m7}) \quad (4.21)$$

$$C_1 = C_{o7} + C_{o13} + C_{o15} + C_{o1} + C_{gs5} \quad (4.22)$$

Chapter 4 - CMOS Quadrature Generator

$$C_2 = C_{gd7} + C_{gd5} \quad (4.23)$$

$$C_2 = C_{gd7} + C_{gd5} \quad (4.24)$$

$$C_3 = C_{o3} + C_{o5} + C_{o17} + C_{o19} + C_{gs7} \quad (4.25)$$

$$g_1 = g_{o1} + g_{o7} + g_{o13} + g_{o15} \quad (4.26)$$

$$g_2 = g_{o3} + g_{o5} + g_{o17} + g_{o19} \quad (4.27)$$

and C_{o1} , C_{o3} , C_{o5} , C_{o7} , C_{o13} , C_{o15} , C_{o17} and C_{o19} are the total capacitance seen at the drain of M_1 , M_3 , M_5 , M_7 , M_{13} , M_{15} , M_{17} and M_{19} respectively; g_{o1} , g_{o3} , g_{o5} , g_{o7} , g_{o13} , g_{o15} , g_{o17} and g_{o19} are the output conductance of M_1 , M_3 , M_5 , M_7 , M_{13} , M_{15} , M_{17} and M_{19} respectively and C_{gd1} , C_{gd5} and C_{gd7} are the gate-drain capacitances of M_1 , M_5 and M_7 respectively.

The denominator of the common mode transfer function in equation (4.19) is a second order polynomial where q and r have positive values. The term $(g_1g_2 - g_{m5}g_{m7})$ is negative since the trans-conductances g_{m3} and g_{m5} typically have a greater value than the output conductances g_1 and g_2 of MOS transistors in the active region of operation. The signs of the three coefficients q , r and $(g_1g_2 - g_{m5}g_{m7})$ in the denominator of equation (4.19) imply that, in the common mode of operation, the circuit has two poles, one located in the left half plane and the other located in the right half plane. The common mode pole located on the right half plane results in the common mode instability of the circuit. To solve this problem, the common mode stabilizer depicted in Fig. 4.4 is added to the design.

The common mode transfer function of the quadrature generator including the common mode stabilizer is given by

$$\frac{V_o}{V_{LO}} = \frac{(g_{m1} - sC_{gd1})(g_2 + g_{ms} + s(C_2 + C_3))}{qs^2 + r's + (g_1 + g_{ms})(g_2 + g_{ms}) - g_{m3}g_{m5}} \quad (4.28)$$

Chapter 4 - CMOS Quadrature Generator

Where

$$r' = (g_1 + g_{ms})(C_2 + C_3) + (g_2 + g_{ms})(C_1 + C_2 + C_{gd1}) + C_2(g_{m3} + g_{m5}) \quad (4.29)$$

By properly choosing the trans-conductance of transistors M_{21} and M_{24} (i.e. g_{ms}) the term $[(g_1+g_{ms})(g_2+g_{ms})-g_{m3}g_{m5}]$ will be positive and therefore all three coefficients in the denominator of equation (4.28) (q , r' and $[(g_1+g_{ms})(g_2+g_{ms})-g_{m3}g_{m5}]$) are positive which means both roots of the second order polynomial in the denominator of equation (4.28) are in the left half plane guarantying the common mode stability of the circuit.

In summary, the common mode stabilizer of Fig. 4.4 is designed such that in the differential mode of operation the equivalent resistance of transistor M_{23} is used to adjust the quadrature phase of the four outputs. In the common mode of operation, the trans-conductance of transistors M_{21} and M_{22} (i.e. g_{ms}) moves the common mode poles of the quadrature generator to the left half plane and thereby stabilizes the common mode behaviour of the circuit.

4.5 Layout of the Quadrature Generator

The core area of the quadrature generator layout is $150 \times 90 \mu\text{m}^2$. The total area of the test chip including the testing pads and decoupling capacitors is $1100 \times 700 \mu\text{m}^2$. Decoupling capacitors were used to bypass the supply and control voltage nodes to ground and hereby eliminate high frequency noise picked up by the DC lines and interconnects. All n-channel transistors are placed in deep n-wells to minimize the crosstalk between them thought the substrate. Accordingly, p-channel transistors are located in separate n-wells. The finger widths of the transistors were chosen to be $2.5 \mu\text{m}$ for optimum speed and noise performance. Perfect layout symmetry is crucial for good circuit performance.

4.6 Post Layout Simulations

The post layout simulations were done using the Spectre RF simulator [7] embedded in the Cadence circuit design software. The characteristics of the circuit were extracted using time domain simulations. Frequency domain simulations were also carried out to examine the amount of matching between frequency domain and time domain simulation results. Both time domain and frequency domain simulations are in agreement with equations (4.10) to (4.13) characterizing the outputs V_1 to V_4 of the quadrature generator shown in Fig. 4.5.

Fig.4.8(a) illustrates the post layout simulated magnitude and phase behaviour of the four outputs of the quadrature generator of Fig.4.6 in the frequency domain. The peaking in the magnitudes of the outputs in the frequency response indicates the inductive behaviour of the circuit. The circuit is designed such that it has a simulated gain of 0 dB to prevent the attenuation of the local oscillator signal. The circuit exhibits a phase difference of 90° between the outputs and equal amplitudes for the four quadrature outputs at 8 GHz¹, as shown in Fig. 4.8(b).

¹This frequency was chosen as the tentative carrier frequency for the future generation of mobile phones[8].

Chapter 4 - CMOS Quadrature Generator

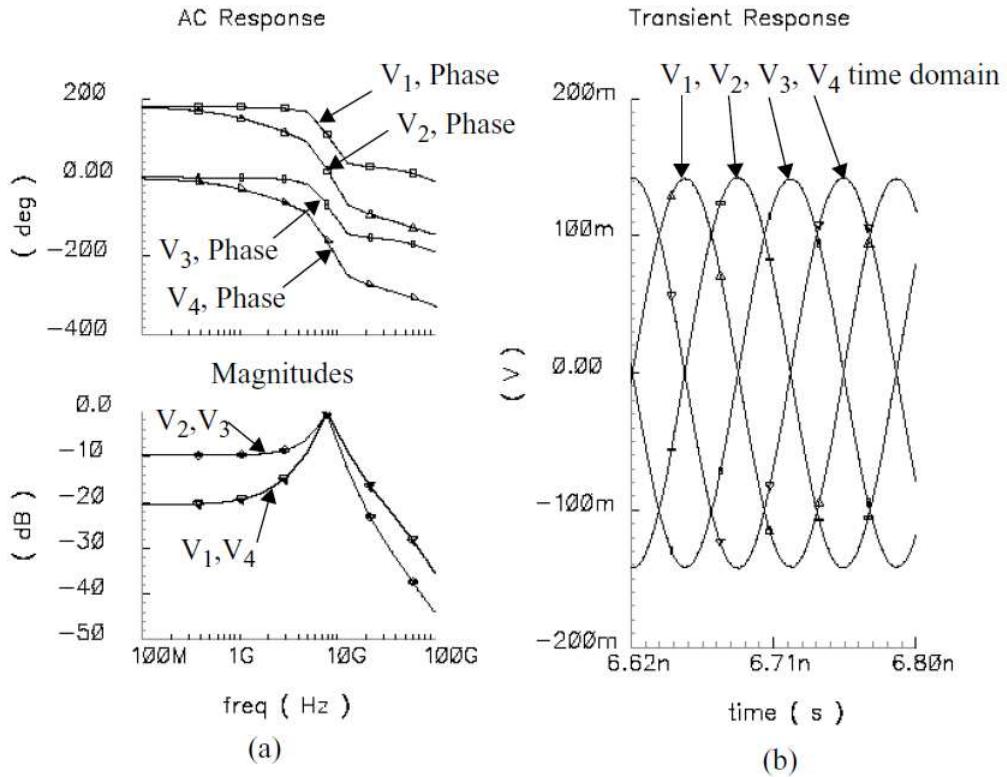


Fig 4.8 Post layout simulation characteristics of the quadrature generator. (a) The magnitude and phase of the transfer function of the four outputs. (b) The time domain quadrature outputs.

Fig. 4.9 shows the simulated quadrature phase and amplitude matching of the design for a peak-to-peak differential local oscillator input of 300 mV over a bandwidth of 100 MHz [9]. The circuit illustrates a quadrature phase and amplitude matching of less than 1° and 0.4 dB respectively for the typical device parameters over the bandwidth of interest. The output quadrature phase and amplitude mismatch for the process corners were observed to be less than 6° and 1.5 dB respectively without applying any tuning.

Chapter 4 - CMOS Quadrature Generator

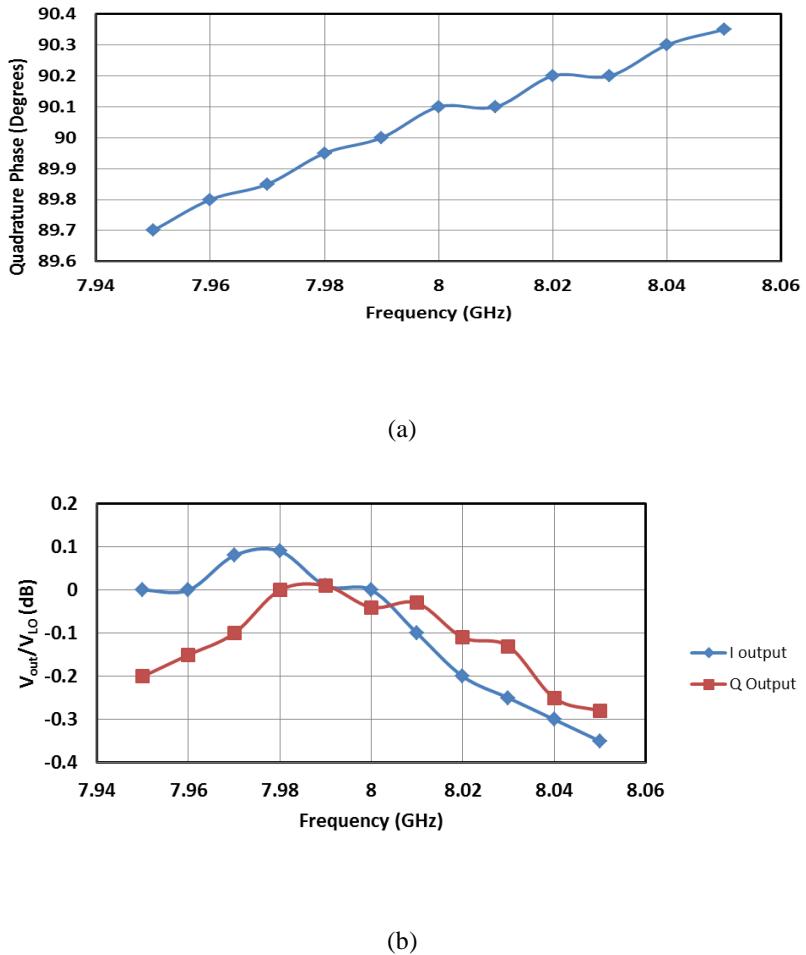


Fig 4.9 Simulation results of the quadrature generator. (a) Quadrature phase error. (b) Amplitude mismatch.

The variation in the control voltage required to compensate for process and supply voltage variations under worst case process corners and a power supply voltage variation of +10% and -10%, is less than 200mV. This control voltage can be generated by automatic amplitude and phase tuning circuitry previously reported in the literature [6].

Table 4.1 compares the post layout simulation results of the quadrature generator to the target specifications as listed in Table 1.2 in Chapter 1. As observed from the Table, the post layout simulation results meet the target specifications of the quadrature generator under consideration.

Chapter 4 - CMOS Quadrature Generator

Table 4.1 Comparison between Target Specification and Post Layout Simulation for the Quadrature Generator

	Target specifications	Simulation results
Technology (CMOS)	0.18 μm	0.18 μm
Supply Voltage	1V	1V
Frequency	8 GHz	8 GHz
I/Q phase mismatch	<2°	<1°*
Power consumption	Minimum	12 mW**

* Over a bandwidth of 100 MHz around 8 GHz after tuning

** Including the LO-buffer

Table 4.2 summarizes the effect of process variations on the performance of the quadrature generator. The associated required change in the tuning voltage necessary to compensate for the process-induced phase imbalance is also listed in the Table.

Table 4.2 Effect of Process Variation on the Performance of the Quadrature Generator

	No tuning	With tuning
Amplitude mismatch*	1.5dB	0.4dB
Quadrature phase mismatch*	6°***	<1°
Tuning voltage variance	245mV**	200 mV

* Over a bandwidth of 100 MHz around 8 GHz

** This value of tuning is required to bring the performance within 1° of quadrature imbalance

*** This is the un-tuned value. After tuning the imbalance is below 1°

Chapter 4 - CMOS Quadrature Generator

The performance of the proposed quadrature generator was also simulated, using standard technology parameters, over a temperature range of -25°C to 125°C. Table 4.3 summarizes the simulation results for three operating temperatures of -25°C, 27°C and 125°C. The control voltages are set for proper operation of the quadrature generator at 27°C. As mentioned previously, the easy tunability of the circuit allows compensating for phase and amplitude mismatches. The circuit specifications at other temperatures can be brought within the values reported at 27°C, by applying a control voltage of less than 225 mV. Such a voltage can be generated by previously reported automatic tuning circuitry [6].

Table 4.3 Effect of Temperature Variation on the Performance of the Quadrature Generator

	-25°C	27°C	125°C
Amplitude mismatch*	0.5dB*	0.4dB*	0.6dB
Quadrature phase mismatch*	< 1.6°*	< 1°*	< 3°*
Power consumption (mW)	11 **	12 **	13.6 **

* Over a bandwidth of 100 MHz around 8 GHz

** Including the LO-buffer

4.7 Summary

A novel quadrature generator architecture using active inductors was presented in this Chapter. The design eliminates the need for buffers between the quadrature generator and the mixers and thereby decreases the power consumption of the circuit. It relaxes the coupling between quadrature phase and amplitude tuning which facilitates the phase and amplitude tuning of the design to compensate for process and supply voltage variations. The post layout simulation results confirm the tunability of the design and show that the quadrature generator satisfies the quadrature accuracy and low voltage operation requirements of future generation of mobile phones.

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CHAPTER 5: Implementations and Experimental Results

5.1 Introduction

This Chapter deals with the experimental implementation and characterization of the mixer, the quadrature generator and the quadrature down-converter discussed in Chapters 2, 3 and 4. The circuits are implemented using a standard CMOS 0.18 μm technology¹.

5.2 Mixer Implementation and Characterization

Fig. 5.1 illustrates the micrograph of the implemented mixer using 0.18 μm CMOS technology. The layout of the mixer was discussed in Chapter 3, section 3.6. The core area of the mixer is $320 \times 400 \mu\text{m}^2$. The area of the complete test chip including the testing pads is $710 \times 1080 \mu\text{m}^2$ [82,83].

¹MOSTs are sensitive to electrostatic discharge (ESD). To avoid gate oxide breakdown, ESD protection circuitry must be used at the input pads of the circuit. In the design kit under consideration, the behaviour of ESD protection circuits is not modeled at radio frequencies, and protection circuits were not used to allow for more accurate characterization of the building blocks under consideration.

Chapter 5 - Implementations and Experimental Results

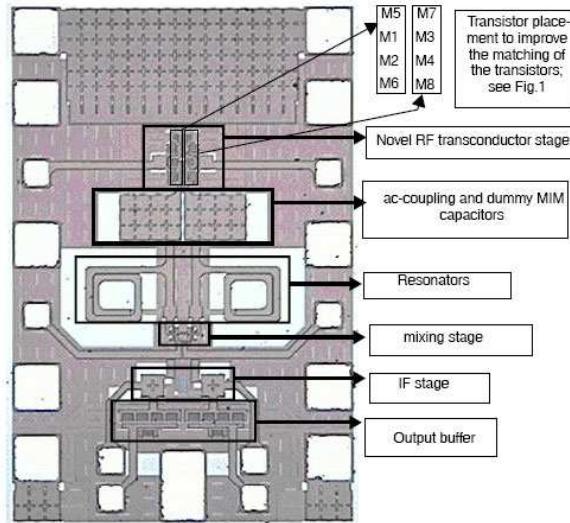


Fig. 5.1 Micrograph of the fabricated mixer.

All measurements were carried out using on-chip probing. All probes were from GGB Industries and featured a Signal-Ground-Signal (SGS) configuration. Measurements were conducted on five different die samples to verify the repeatability of the results. All reported values are the average of the five measured results¹.

The setup used to measure the conversion gain and 1-dB compression point characteristics of the mixer is illustrated in Fig. 5.2. It consists of: two signal generators (HP83712B and HP83650B) used with two Narda 4346 180° hybrid to provide differential signals from the single ended signal generator, four manual microwave tuners from Focus Microwaves (MMT 1808) used to externally match the RF and LO ports of the mixer to 50Ω for correct measurements, four Picosecond 5575A Bias-Tees to apply biasing to the mixer through HP E3631A DC power supplies, a Mini-Circuit ZSCJ-2-1,2 180° 2-way combiner, used at the output of the mixer to convert the differential output of the mixer to single ended and apply it to a HP8563E spectrum analyzer. The output of the mixer was internally matched to 50Ω .

¹ All available dies were from the same split with similar performances. The measurement variation associated with each performance metric for all five die samples are reported in the corresponding section.

Chapter 5 - Implementations and Experimental Results

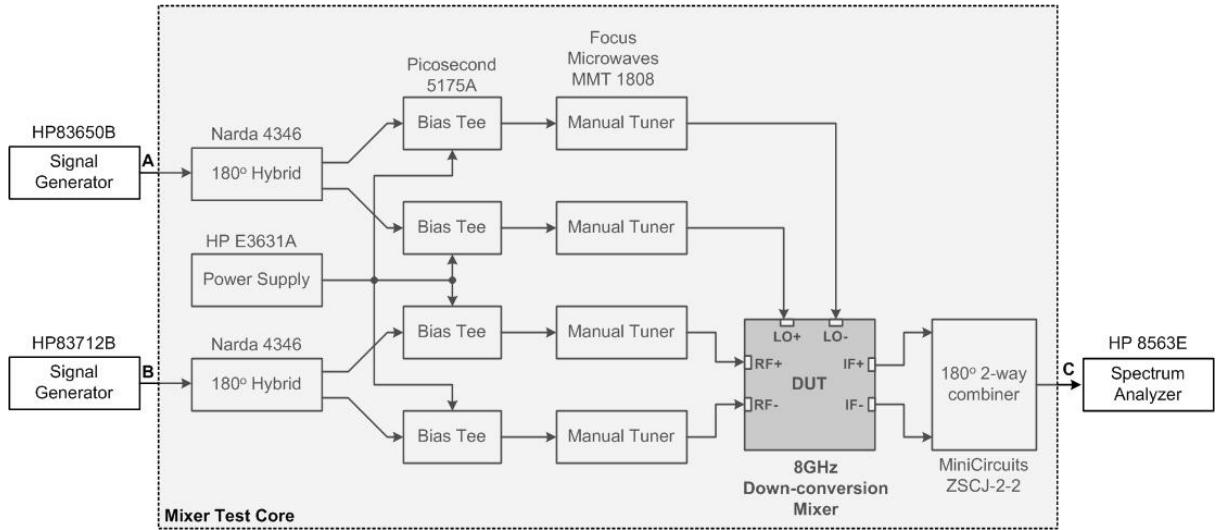


Fig. 5.2 Mixer conversion gain and 1-dB compression point measurement setup.

Fig.5.3 illustrates a plot of the experimental and simulated power transfer characteristics of the mixer. The experimental results reveal a 1-dB compression point of -5.5 dBm and a power conversion gain (PCG) of +6.5 dB while operating from a supply voltage of 1V. By comparison, the simulated power conversion gain and the 1-dB compression point are +10 dB and -8 dBm respectively. The discrepancy between experimental and simulated results is partly due to inaccuracies in the inductor and on-chip Metal-Insulator-Metal (MIM) capacitor, and partly due to the parasitic resistances at the RF signal path which are not extracted by the design kit used. The former effect is captured in simulation by correcting the resonance value based on measurement results; and the latter is simulated by annotating parasitic resistances to the mixer circuit. The residual discrepancy between measurement and simulation can be attributed to device modeling inaccuracies at the operating frequency.

Five loose dies were measured. Gain and compression point variation among five dies were 0.15dB and 0.17dB respectively.

Chapter 5 - Implementations and Experimental Results

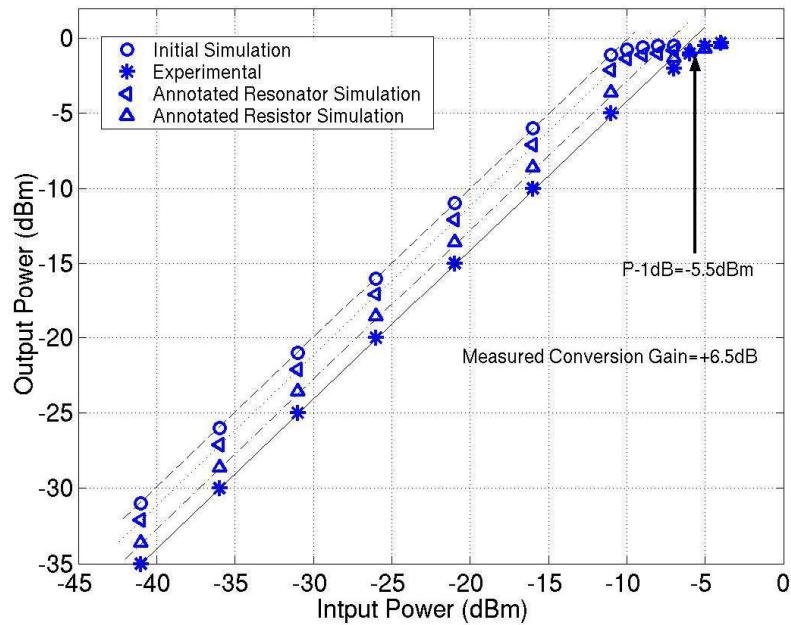


Fig. 5.3 Experimental and simulated conversion gain of the mixer.

The two-tone test setup shown in Fig. 5.4 was used to measure the IIP3 and IIP2 of the mixer. The two RF tones located at 8001 MHz and 8003 MHz applied to the RF port of the mixer were combined using a Mini-Circuits ZB4PD1-8.4, 4-way RF combiner (see Fig. 5.2 for the mixer test core). The two unused inputs of the combiner were terminated to 50Ω broadband loads as shown in the figure.

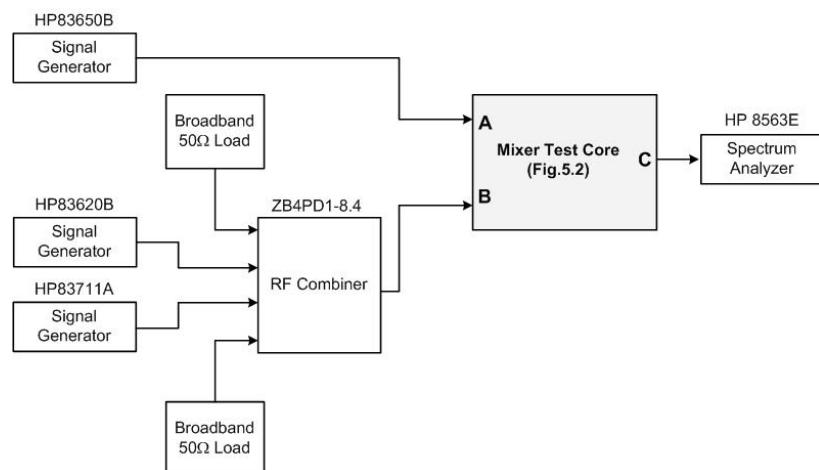


Fig. 5.4 Mixer two-tone test measurement setup.

Chapter 5 - Implementations and Experimental Results

Fig. 5.5 illustrates the two-tone experimental results. The intercept of the linear extrapolation of the first and third order terms indicates an IIP3 of +3.5 dBm. The IIP2 of the mixer was found to be better than +48 dBm. Due to the relatively high noise floor of the measurement setup, particularly the spectrum analyzer, and the fact that the magnitude of the second order nonlinearity was small and comparable to the noise floor for most values of the input signal power below the 1-dB compression point of the mixer, it was only possible to conclude that the IIP2 of the mixer is better than +48 dBm. The corresponding simulated results for IIP3 and IIP2 were +3 dBm and +52 dBm respectively. The higher experimental linearity observed is to be expected due to the lower experimental gain discussed with reference to Fig. 5.2. Decreasing the gain in a CCM, typically results in higher linearity. The measured IIP3 variation among all five samples was 0.1dB.

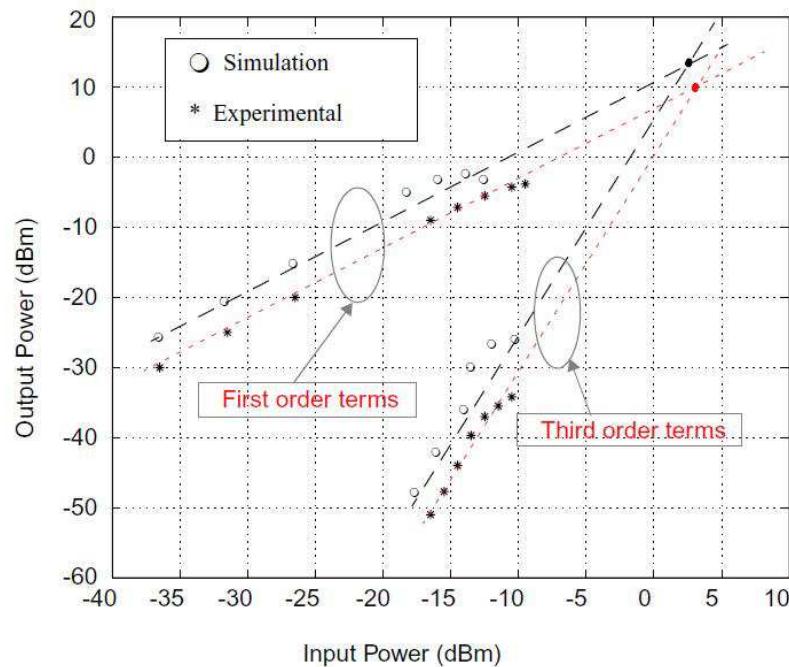


Fig. 5.5 Two tone test plot of the mixer.

Chapter 5 - Implementations and Experimental Results

The test setup for characterizing the noise figure (NF) of the mixer is shown in Fig. 5.6. Manual microwave tuners (MMT 1808) from Focus Microwaves were used to externally match the RF port of the mixer to 50Ω as required by definition, for correct measurements (see Fig. 5.2 for the mixer test core). An HP8970B noise figure meter along with a NC346B noise source were used to characterize the amount of noise degradation caused by the mixer under test. In the calibration phase, the DUT was replaced by a thru connection, available on the calibration substrate of the probes, to eliminate the parasitic effects of the measurement setup including the insertion loss and the noise of the components.

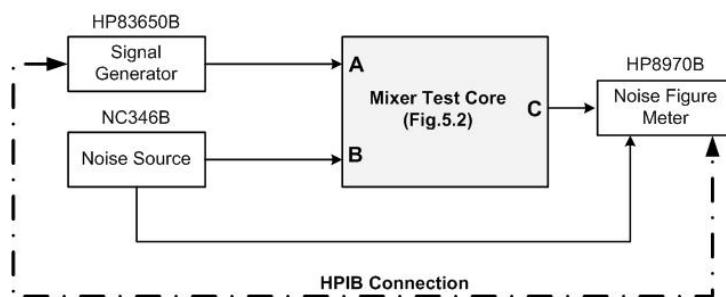


Fig. 5.6 Mixer noise figure measurement setup.

The noise figure of the mixer was measured in the baseband frequency range of 10MHz to 200MHz¹. The minimum noise figure at base band was 11.5dB. The noise figure variation among all five samples is 0.35dB.

The isolation between the LO-port and the RF-port (LO to RF isolation) of the mixer at 8 GHz was measured using the frequency domain method (S-parameter). The test setup is illustrated in Fig. 5.7. For proper measurements, a full 2-port SOLT² calibration was performed to bring the reference plane of the S-parameter measurements to the tip of the RF probes, and eliminate the

¹The lower end frequency of measurable NF was 10 MHz on the HP8970B noise figure meter.

²SOLT stands for Short-Open-Load-Thru.

Chapter 5 - Implementations and Experimental Results

parasitic effect of all the components between the network analyzer and the DUT (see Fig. 5.2 for the mixer test core).

The mixer exhibits an RF to LO isolation of better than 60 dB¹ at 8 GHz. This result was achieved by maximizing the separation of the RF and the LO sections of the mixer to minimize the substrate assisted coupling between the two ports and by placing the transistors of the mixing stage individually in deep N-wells isolated from the substrate.

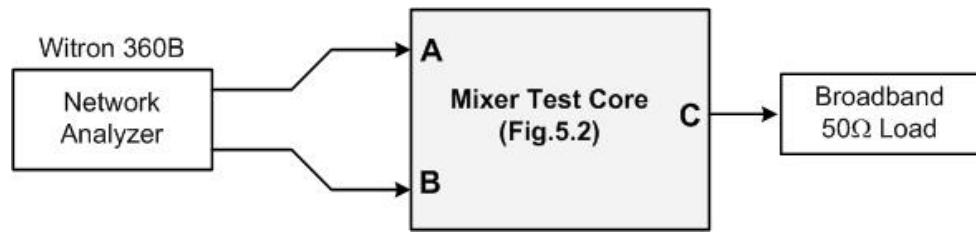


Fig. 5.7 Mixer RF port to LO port isolation measurement setup.

The mixer design proposed in this work was completed and published in 2004. Tables 5.1 and 5.2 compare the present design to other low voltage mixers reported in the CMOS technology up to 2005 and to date, respectively. As observed from the Tables, the architecture implemented in this work relaxes the trade-off between power conversion gain and linearity which governs all conventional CMOS active mixers while operating at low supply voltages. The power-gain/linearity characteristics of the proposed design are superior to that of other low voltage designs reported in the literature. This is a valuable feature, particularly in low voltage DCR implementations.

¹ Isolation measurement conducted on all five loose dies reveal RF to LO isolation better than 60dB.

Chapter 5 - Implementations and Experimental Results

Table 5.1 Comparison of the Low Voltage Mixer of this Work with Other Low Voltage Mixers using Different Architectures (up to 2005).

No. of Reference	[2] 2004	[3] 2004	[4] 2003	[5] 2004	[6] 2004	[83] This Work 2004
Architecture	Back-Gate Mixer	Transformer Based Mixer	Transformer Based Mixer	Folded Switching Mixer	Switched Transconductor	Bias-Offset Transconductor
Technology (μm)	0.09	0.13	0.13	0.18	0.18	0.18
Supply Voltage (V)	1.2	0.6	1	1	1	1
Frequency (GHz)	4	2.5	2	2.4	6	8
Noise Figure (SSB, dB)	20.4	14.8	14.5	13.9	25	11
IIP3 (dBm)	-2.1	-2.8	0	-3	+3	+3.5
IIP2 (dBm)	---	---	---	---	---	>+48
P-1dB (dBm)	-13.3	-9.2	-10	---	---	-5.5
Conversion Gain (dB)	3.2	5.4	5.5	11.9	7.4	+6.5 (Power)
Power Consumption (mW)	1.8	1.6	40	3.2	1	6.9
Area (μm^2)	490 x 470	1000 x 1000	630 x 800	160 x 200	75 x 65	320 x 400

Chapter 5 - Implementations and Experimental Results

Table 5.2 Comparison of the Low Voltage Mixer of this Work with Other Low Voltage Mixers using Different Architectures (2005 to 2011)

No. of Reference	[29] 2007	[42] 2008	[36] 2008	[38] 2008	[58] 2011	[83] This Work
Architecture	Back-Gate Mixer	Back-Gate Mixer	Transformer Based Mixer	Capacitor Coupled Mixer	Cascode Bulk Injection	Bias-Offset Transconductor
Technology (μm)	0.18	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	0.8	1	0.8	1	0.7	1
Frequency (GHz)	2.4	5.8	5.8	2	6	8
Noise Figure (SSB, dB)	15	37	14.8	18	15.2	11
IIP3 (dBm)	-5.7	15.3	3	11	0	+3.5
IIP2 (dBm)	---	---	19	---	---	>+48
P-1dB (dBm)	---	6.5	-3	2.2	---	-5.5
Conversion Gain (dB)	5.7	-0.8	-1.6	8.1	6	+6.5 (Power)
Power Consumption (mW)	0.77	1	10	4.1	0.28	6.9
Area (μm^2)	180 x 200	300 x 500	1780 x 1390	900 x 900	150 x 236	320 x 400

Table 5.3 shows the linearity improvement achieved in this work compared to the conventional CCM implemented in a standard 0.18 μm CMOS technology [7,52]. The first column in the Table lists the characteristics of a conventional CCM (Fig.3.1(b)) optimized for linearity. The second column shows the performance of a CCM with inductive degeneration (Fig. 3.4). The

Chapter 5 - Implementations and Experimental Results

third column shows the CCM mixer optimized for linearity using resistive degeneration. The proposed design characteristics are listed in the third column. Note that the present mixer uses a power supply of 1 V, while the conventional CCMs use a power supply of 1.8V. The effectiveness of the proposed technique is evident since it achieves better linearity at lower supply voltages compared to [7], The design using resistive degeneration achieves good linearity at the expense of conversion gain and noise.

Table 5.3 Comparing the Linearity Characteristics of the Proposed Mixer and the Conventional CCM [7,52]

	[7]-without inductive source degeneration	[7]-with 15nH of inductive source degeneration	[52] CCM with resistive source degeneration	[83] This work 0.18μm	This work 65nm*
Technology (μm)	0.18	0.18	0.18	0.18	0.065
Supply Voltage (V)	1.8V	1.8	1.8	1	0.9
Frequency (GHz)	2.45	2.45	5.8	8	8
Noise Figure (dB)	8.2	12.5	22	11.5	13
IIP3 (dBm)	-12	-3.7	---	+3.5	3.2
IIP2 (dBm)	---	---	---	>+48	---
P-1dB (dBm)	-21	-15.9	-2	-5.5	-5.7
Power Conversion Gain (dB)	+12	+2	-1	+6.5	5
Power Consumption (mW)	---	---	---	6.9	6.2

* Simulation Results

Fig.5.8 summarizes the CMOS mixers published in the literature in various CMOS technologies. The data points are arranged in terms of input-referred third order intercept point versus $10\log(F-1)$, where F represents the noise factor of the circuit. The expression $10\log(F-1)$ indicates the amount in Decibels by which the input referred noise of the mixer sits above the

Chapter 5 - Implementations and Experimental Results

thermal noise floor. Fig.5.8 does not include the power consumption associated with the circuit. It provides a clear view of the noise/linearity performance. The mixer design proposed in this work is represented by the cross-shaped marker. The closer the marker is to the top left corner of the plot, the better the noise/linearity performance of the mixer is. By scaling the linearity of the circuit (IIP3) with its power consumption, in Fig.5.9, it is observed that the proposed design stands at a fairly competitive spot in the plot, which highlights the low-power characteristics of the proposed design. The plots in Figs 5.8 and 5.9 show that the proposed low-voltage, low power linearity improvement technique is an effective technique [14-59]. The dashed line in Fig.5.9 highlights the noise linearity tradeoff governing RF circuitry. Designs situated on the dashed line trade linearity for noise or vice versa while samples closer to the top left corner of the diagram, incorporate novelty to relax noise-linearity trade-off. The vertical cross represents this work in 65nm CMOS. It is worth noting that by migrating to more advanced CMOS technologies (i.e. 45nm or 28nm,...) the performance of the proposed mixer is expected to be limited to the leftmost dashed line in Figure 5.9; Depending on noise/linearity tradeoff decision, the mixer's performance is expected to move along that line.

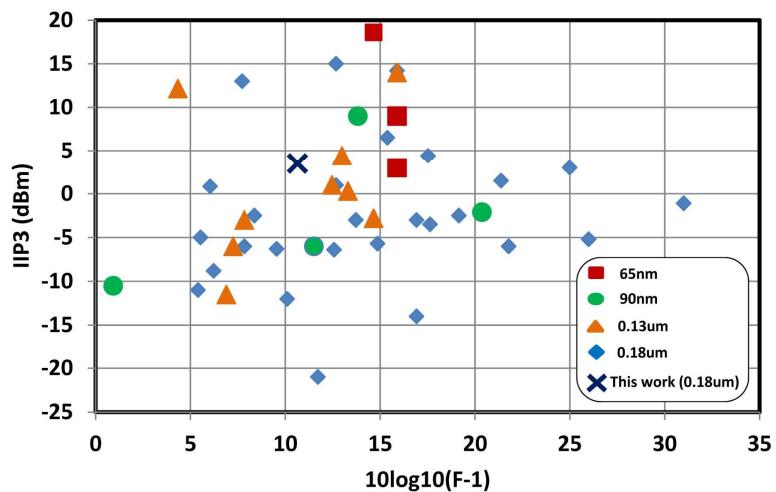


Fig. 5.8 CMOS mixers published in the literature [14-59]. Input referred third order intercept point versus noise.

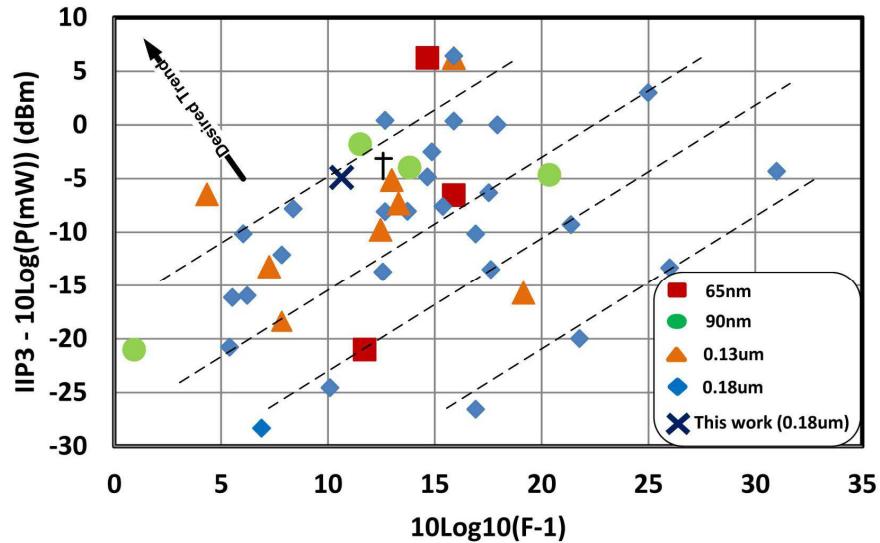


Fig. 5.9 Proposed CMOS mixer compared to state of the art published work [14-59]. The vertical axis represents linearity over power in decibels.

5.3 Quadrature Generator Implementation and Characterization

Fig. 5.10 shows the micrograph of the quadrature generator [84]. The core dimensions of the design are $150 \times 90 \mu\text{m}^2$. The dimensions of the complete test chip, including the testing pads are $1100 \times 700 \mu\text{m}^2$. The layout of the quadrature generator was discussed in Chapter 4, section 4.5.

Measurements were carried on five separate dies to examine both the repeatability of the results and the variances in quadrature phase and amplitude of the outputs under similar biasing and control voltage conditions. All reported values are the average of the values obtained from five measured chips.

Chapter 5 - Implementations and Experimental Results

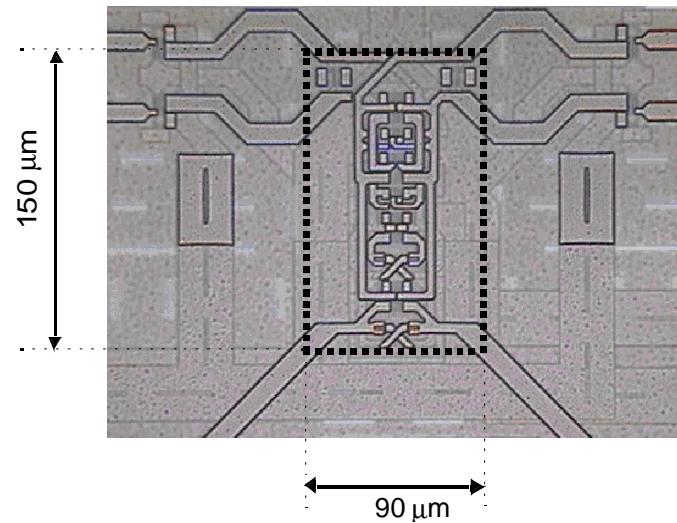


Fig. 5.10 Micrograph of the fabricated quadrature generator in $0.18\mu\text{m}$ CMOS.

The setup used to measure the quadrature phase and amplitude accuracy at the output of the quadrature generator is illustrated in Fig. 5.11. A Tektronix TDS8000 oscilloscope was used to characterize the output waveform of the quadrature generator in the time domain.

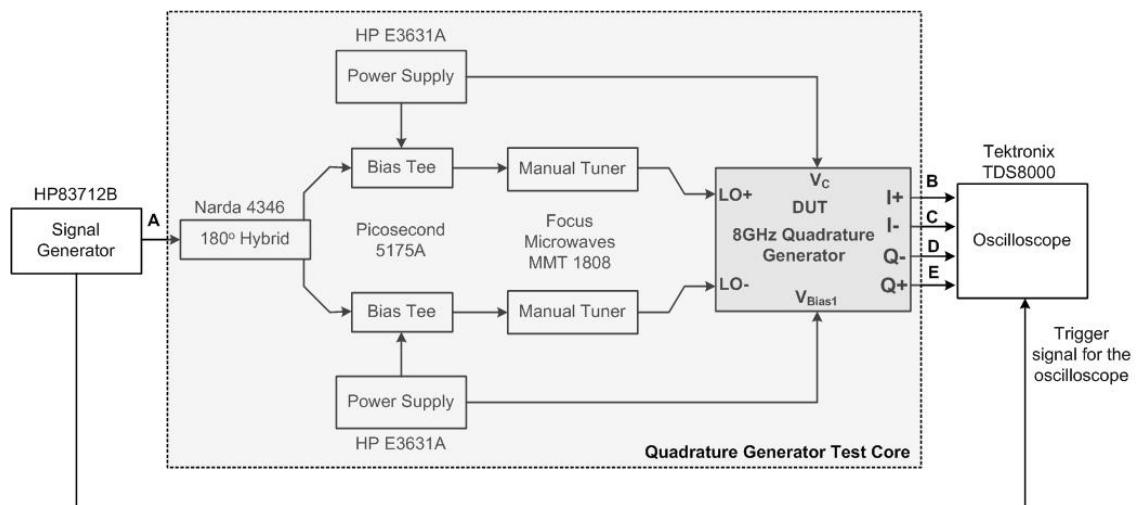


Fig. 5.11 Quadrature Generator measurement setup.

Fig. 5.12 is a plot of the measured quadrature phase and amplitude matching of the design. Post layout simulation results are also shown for the purpose of comparison. The slight discrepancy

Chapter 5 - Implementations and Experimental Results

between the measured and simulated results is mainly attributed to the uncertainty in measurements due to the built-in jitter of the equipment and the phase and amplitude error introduced by the interconnections. The circuit demonstrates a quadrature phase and amplitude matching of better than 1.5° and 1 dB over the bandwidth of interest. The fine tuning of the quadrature generator performance for all the measured samples requires applying a variation of less than 150 mV in V_C (4° of variance in the output quadrature phase) and less than 80 mV in V_{B1} (1 dB of variance in amplitude) to achieve the experimental values reported in Fig. 5.12. These control voltage variations can be generated by automatic amplitude and phase tuning circuitry previously reported in the literature [8]. Given the tenability of the design, all five measured dies were tuned to the same performance levels with less than 10mV and 5mV variance in V_C and V_{B1} respectively.

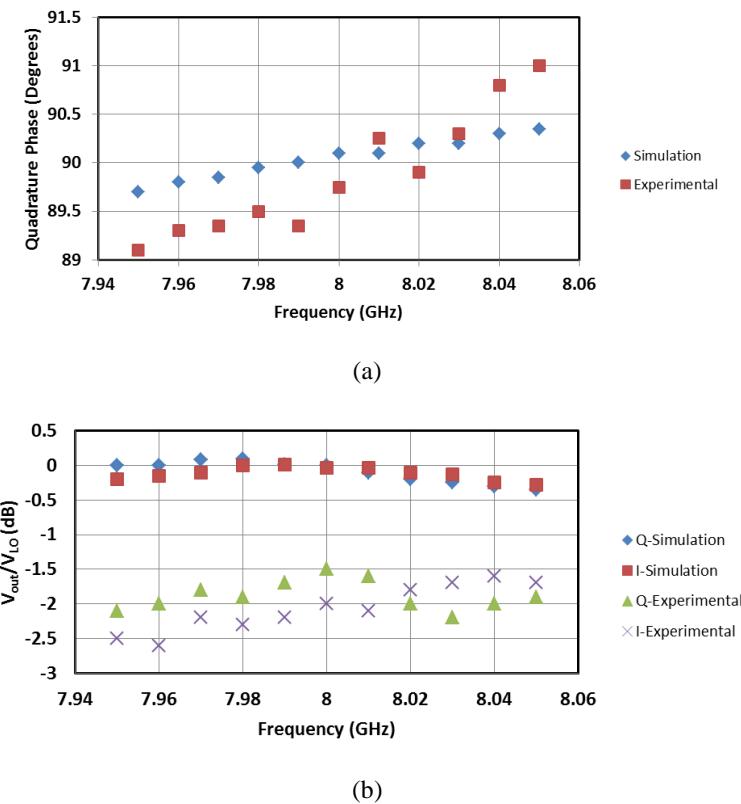


Fig. 5.12 Measured and simulated results for quadrature phase and amplitude accuracy of the quadrature generator. (a) Quadrature phase accuracy. (b) Quadrature amplitude.

Chapter 5 - Implementations and Experimental Results

Fig. 5.13 illustrates the measured time domain representation of the outputs of the quadrature generator without applying averaging on the results. The gain of the fabricated quadrature generator at 8 GHz is almost 2 dB lower than the simulated value. This discrepancy is due to the parasitic resistances which are not extracted by the design kit used in this work.

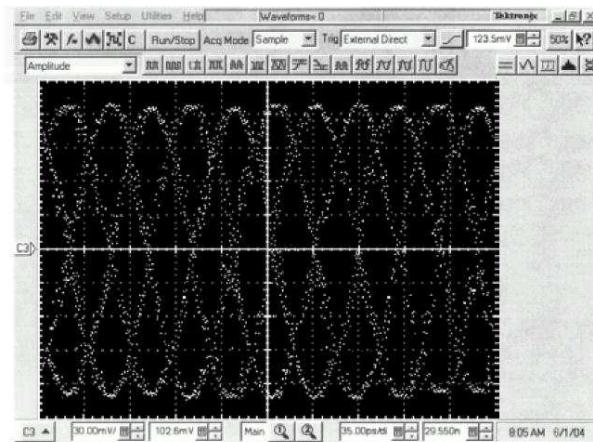


Fig. 5.13 Time domain output of the quadrature generator measured at 8GHz.

The phase noise was measured with and without the device under test using the test setup illustrated in Fig. 5.14, and the result is illustrated in Fig. 5.15. The signal generator phase noise is low. The measurement setup includes an HP8560A spectrum analyzer equipped with a 85671 phase noise utility from Agilent Technologies. The plots in Fig. 5.15, reveals that the phase noise at the output of the quadrature generator is -108 dBc/Hz at 1 MHz offset frequency.

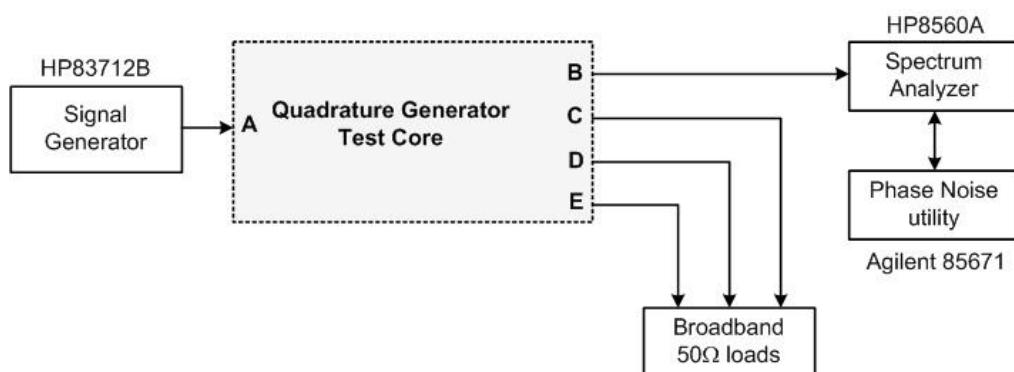


Fig. 5.14 Quadrature generator phase-noise measurement setup.

Chapter 5 - Implementations and Experimental Results

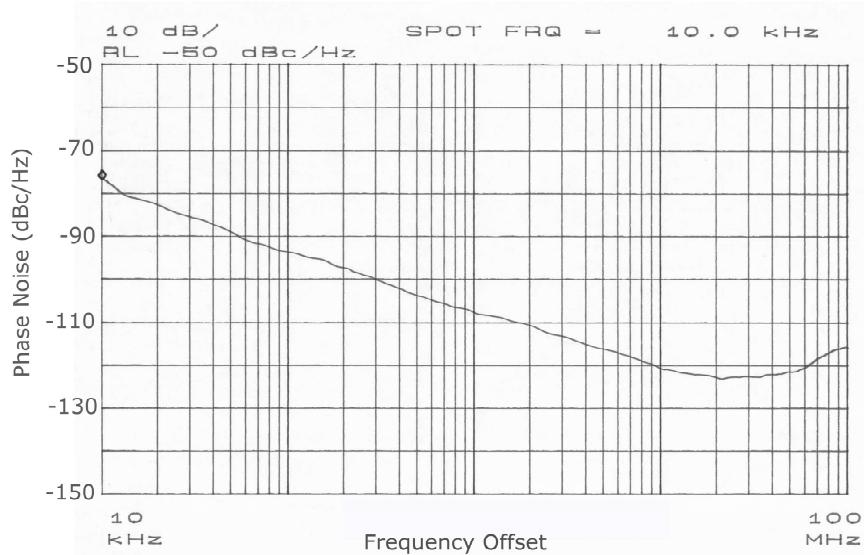


Fig. 5.15 Measured phase noise of the quadrature generator.

The experimental performance of the proposed design is compared to four previous designs reported prior to 2005 [8-11] and more recent designs in Table 5.4 and Table 5.5 respectively. Each design uses a different architecture to generate quadrature signals, as listed in the Table. By comparison, the design proposed in this work, reduces the power consumption by omitting the buffers between the quadrature generator and the mixers. It also relaxes the coupling between amplitude and phase tuning which facilitates the use of automatic amplitude and phase tuning circuitry. The design also features a very small form factor since it does not include passive devices.

Fig.5.16 summarizes previously published quadrature generator work [60-81]. The vertical axis shows the phase noise at 1MHz offset and the horizontal axis represents the quadrature phase error. The closer the design is to the lower left corner, the better the design is. The quadrature generator designed in this work is represented by the cross shaped marker.

Chapter 5 - Implementations and Experimental Results

The two rectangle shaped points are quadrature VCOs based on bulk acoustic wave (BAW) technology. This circuit is capable of achieving excellent phase noise performance at the expense of increased cost due to the placement of the BAW resonator inside the package. The diamond point at the top left corner represents an LC quadrature oscillator equipped with phase tuning capability. The added phase tuning circuitry considerably degraded the phase noise performance of the design.

Table 5.4 Comparison of the Proposed Quadrature Generator to Previous Work up to 2004.

No. of Reference	[8] 2002	[9] 2002	[10] 2003	[11] 2004	[84] This Work 2005
Architecture	One Stage Poly-Phase Filter	Quadrature LC Oscillator	Ring Oscillator	Four Stage Poly-Phase Filter	Active Inductors
Technology	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.18μm	BICMOS 0.4μm	CMOS 0.18μm
Supply Voltage	1.8 V	1.8 V	1.8 V	2.5 V	1 V
Frequency	5 GHz	2.5 GHz	3.5 GHz	5.8 GHz	8 GHz
Phase Mismatch	2°	<1.2°	< 3.2°	5°	1.5°
Amplitude Mismatch	---	<5%	---	---	<1 dB
Area	0.12 mm ²	0.55 mm ²	---	0.183 mm ²	0.009 mm ²
Power Consumption	2.7 mW*	7.2 mW*	16.2 mW*	50 mW	12 mW**

* This number does not include the power consumption of the buffers used in the design

** Including the LO buffer

Chapter 5 - Implementations and Experimental Results

Table 5.5 Comparison of the Proposed Quadrature Generator to Previous Work up to 2011.

No. of Reference	[80] 2010	[73] 2008	[67] 2009	This Work 2011	[84] This Work 2005
Architecture	QVCO	Divider	Poly-Phase Filter	Active Inductors	Active Inductors
Technology	CMOS 65 nm	CMOS 0.18μm	CMOS 0.18μm	CMOS 65 nm	CMOS 0.18μm
Supply Voltage	1.0 V	1.8 V	1.8 V	1.0 V	1 V
Frequency	4.5 GHz	1.57 GHz	10 GHz	15 GHz*	8 GHz
Phase Mismatch	2°	6°	< 0.15°	2.1°*	1.5°
Amplitude Mismatch	---	12%	0.2dB	0.8dB*	<1 dB
Area	0.28 mm ²	---	---	---	0.009 mm ²
Power Consumption	43 mW	3.06 mW	---	9 mW	12 mW

* Based on simulation

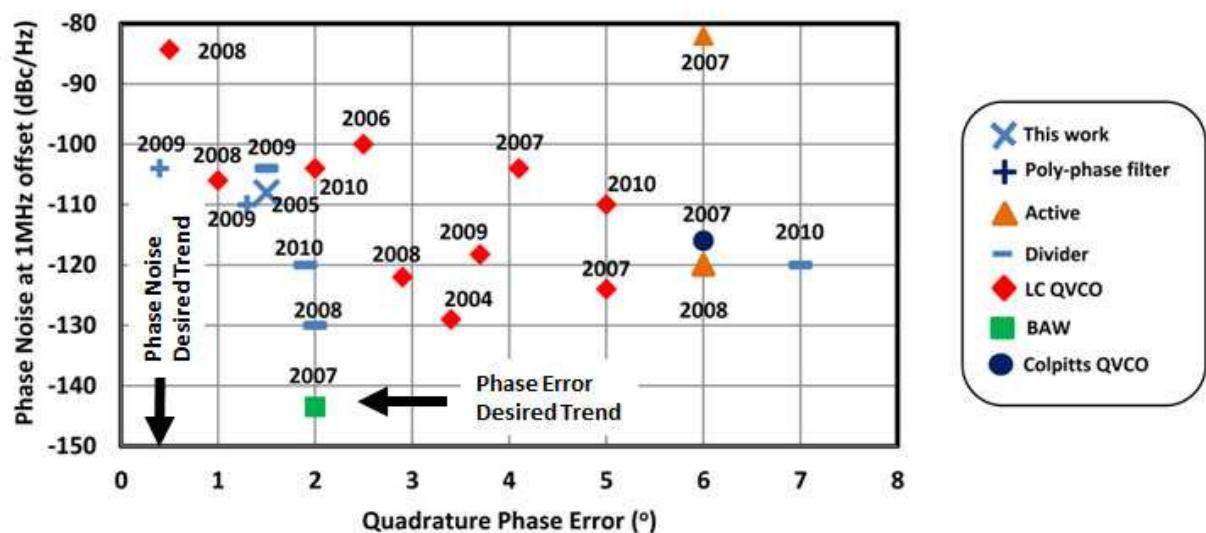


Fig. 5.16 Quadrature generator comparison to previous work [60-81].

5.4 Quadrature Down-converter Implementation and Characterization

Fig. 5.17 shows the micrograph of the complete quadrature down-converter including two mixers and a quadrature down-converter tested in sections 5.2 and 5.3 respectively. The dimensions of the chip including the testing pads are $1000 \times 1360 \mu\text{m}^2$ [85].

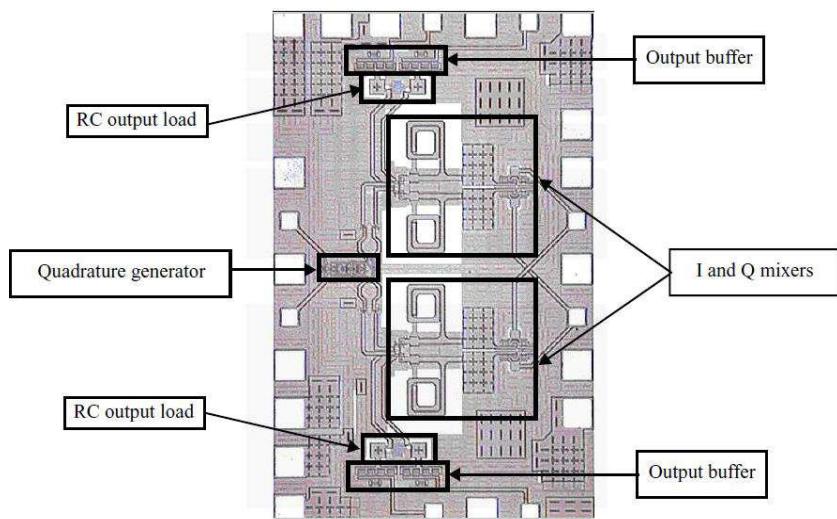


Fig. 5.17 Micrograph of the fabricated quadrature down-converter.

The quadrature down-converter circuit of Fig. 5.17 was used to measure the image rejection ratio (IRR) of the circuit. The approach suggested in reference [12] was used in this measurement and the test setup is illustrated in Fig. 5.18. Two -25dBm RF signals, equally spaced around the 8 GHz LO signal were applied at the RF inputs. The two RF signals were varied from 7.95 GHz and 8.05 GHz to 7.999 GHz and 8.001 GHz to cover the bandwidth of interest of 100 MHz.

The measured IRR over a bandwidth of 100 MHz is illustrated in Fig. 5.19. The quadrature phase and amplitude accuracy of the quadrature generator can be inferred from the measured IRR by referring to the plots in reference [13], as mentioned in Chapter 2. It is observed that the

Chapter 5 - Implementations and Experimental Results

measured IRR shown in Fig. 5.19 corresponds to a quadrature phase mismatch of better than 2° over the RF bandwidth of interest.

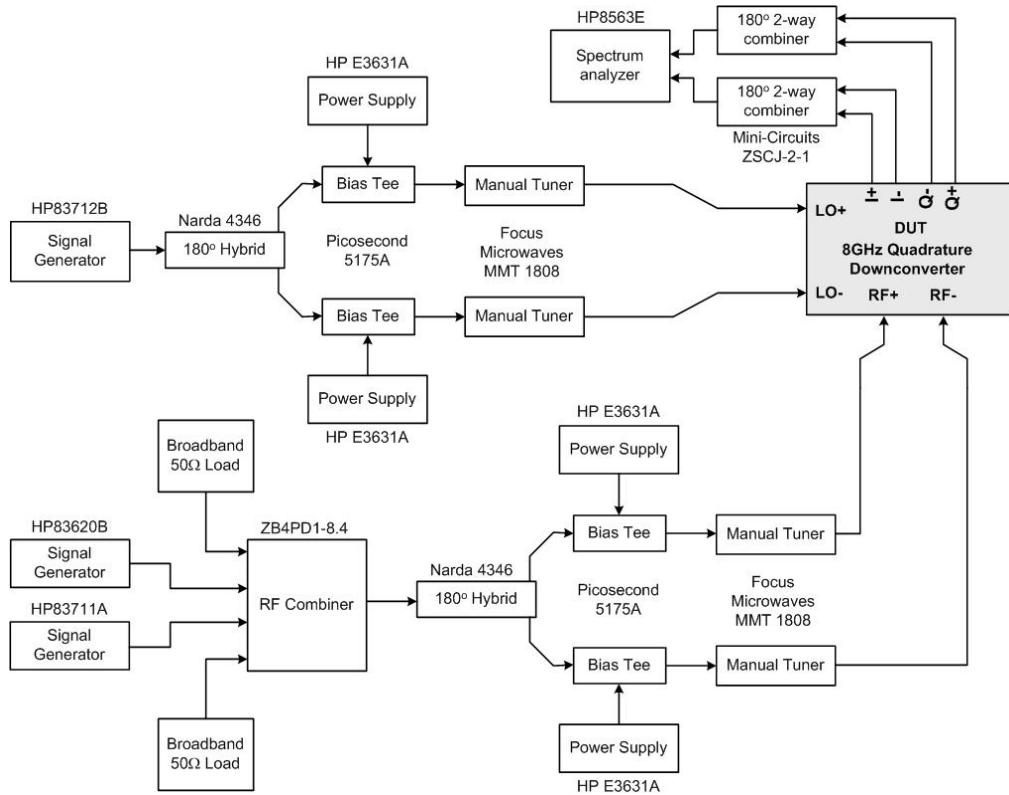


Fig. 5.18 Image-rejection ratio measurement setup.

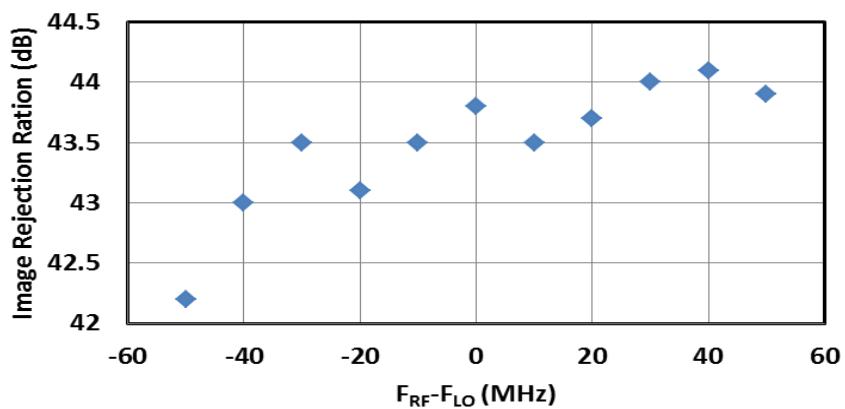


Fig. 5.19 Image rejection ration measurement results over 100MHz IF bandwidth.

Chapter 5 - Implementations and Experimental Results

Table 5.6 summarizes the quadrature phase and amplitude accuracy obtained from both time domain measurements on the quadrature generator alone and IRR measurements on the quadrature down-converter. The results from time domain measurements are listed for an LO frequency of 8 GHz. The amplitude and quadrature phase error extracted from the IRR method are obtained for fixed LO frequency at 8 GHz and varying the RF signal over a bandwidth of 100 MHz around the carrier frequency of 8 GHz. The Proposed QD is compared to DCRs targeting similar applications in table 5.7.

Table 5.6 I/Q Amplitude and Quadrature Phase Error Obtained from the IRR Method and the Time Domain Characterization

	Amplitude Error	Quadrature Phase Error]
IRR Method	---	< 2°
Time Domain Method	1.5dB**	1.5°

Table 5.7 Quadrature Down-converter (QD) compared to other DCRs targeting similar applications.

Architecture	DCR [86] 2010	DCR [87] 2010	This Work [85] 2006
Technology	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply Voltage	1.2V	1.8V	1.0V
Frequency	5.8GHz	6GHz	8GHz
IRR	37dB	40dB	40dB
Gain	+48dB*	---	+6dB
Area	6.24mm ² *	2.1mm ² *	1.36mm ²
Power	52mW*	75mW*	25.8mW

* Based on simulation

**The power, area and gain numbers include LNA and baseband filters

5.5 Summary

The implementation and characterization of an 8 GHz CMOS mixer with improved linearity under low supply voltage, and a quadrature generator with easy tunability suited for direct conversion receivers were discussed in this Chapter. They are implemented in TSMC's CMOS 0.18 μ m technology. The experimental results were in reasonable agreement with the simulated data and the analytical expressions describing the behaviour of both circuits in Chapters 3 and 4. The mixer architecture relaxes the inherent trade-off between power conversion gain and linearity. The quadrature generator circuit relaxes the coupling between the amplitude and quadrature phase tuning which makes it easier to apply automatic tuning circuitry to the design to compensate for temperature and process variations. It also decreases the power consumption by omitting the buffers located between the quadrature generator and the mixers. The mixer and the quadrature generator meet the potential target specifications of the future generation of mobile phones in terms of low supply voltage and good linearity requirements.

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CHAPTER 6: Conclusions

The simultaneous demand for high data rates in future generations of mobile communication systems and higher portability, along with the use of low supply voltages, has increased the demand for single chip, low voltage CMOS receiver RF front ends with adequate linearity to satisfy the requirements of future, relatively wideband systems. The simultaneous satisfaction of low voltage operation and relatively high linearity requirements is one of the most challenging parts of the RF receiver design.

The direct conversion receiver (DCR), is most suitable for monolithic implementation due to its simplicity and lack of off-chip components. In a DCR, the down-converter plays an important role in the overall linearity of the RF front-end.

In this thesis, the design, analysis and implementation of a low voltage quadrature down-converter consisting of a mixer and a quadrature generator, satisfying the tentative specifications for future mobile phones, are presented. Four chips were successfully fabricated in TSMC 0.18 μ m CMOS technology, to verify the performance of the proposed circuitry through measurements.

The tentative specifications for the mixer and the quadrature generator were obtained using MATLAB assuming a DCR in a Rayleigh fading channel. OFDM was assumed as the multiple access scheme and an un-coded bit-error rate of 10^{-3} , or equivalently SNR=23dB at receiver's output was considered.

Chapter 6 - Conclusions

The proposed mixer falls in the current commutating mixer topology and uses a new bias-offset technique to allow good linearity at reduced operating voltages. It relaxes the inherent trade-off between power conversion gain and linearity which governs CMOS active mixers. The experimental circuit uses a 1V power supply, operates at 8 GHz and occupies an area of $320 \times 400 \mu\text{m}^2$. It features a power conversion gain of +6.5 dB and a 1-dB compression point of -5.5 dBm. It has an IIP3 of +3.5 dBm, an IIP2 of better than +48 dBm, a noise figure of 11.5 dB and an RF port to LO port isolation of better than 60 dB. The mixer consumes 6.9 mW of power.

In the proposed quadrature generator, the quadrature generation circuitry is integrated into the LO-buffer using active inductors. The design eliminates the requirement for additional high frequency buffers between the quadrature generator and the mixers and thus improves the power consumption of the quadrature down-converter. One of the salient features of the quadrature generator is the relaxed coupling between quadrature phase and amplitude tuning of the circuit outputs which facilitates the application of automatic quadrature tuning to the design. The experimental quadrature generator uses a 1V power supply, operates at 8 GHz and occupies an area of $150 \times 90 \mu\text{m}^2$. It features a worst case quadrature phase imbalance of 1.5° and amplitude mismatch of 1dB after tuning and consumes 12mW of power including the LO-buffer.

The quadrature down-converter, consisting of the above mentioned mixer and quadrature generator, exhibits an image rejection ratio of better than 40 dB in the band of interest and meets the specifications of future generation of mobile communication systems and is particularly suitable for low voltage implementations.

The major contributions of this work include (verified through successful fabrication of four chips in TSMC 0.18 μm CMOS technology):

Chapter 6 - Conclusions

- detailed modeling of a complete direct conversion receiver including the base-band analog to digital converter in MATLAB. The model is used to understand the effect of quadrature down-converter circuit characteristics on system level performance,
- the development of a new low voltage mixer circuit topology using a new bias-offset-technique with improved linearity and its associated design methodology [1,2],
- the development of a new, easily tunable quadrature generator circuit topology with improved power consumption and its corresponding design methodology [3], and
- the design, implementation and characterization of an 8 GHz quadrature down-converter, using the above mentioned mixer and quadrature generator [4].

Future work should focus on:

- taking advantage of the easy tunability of the proposed new quadrature generator to examine the feasibility of this new topology for reconfigurable quadrature generators for multi-standard receivers,
- implementing process monitors on chip, integrated with the proposed quadrature generator for automatic process-induced phase imbalance compensation,
- migrating the designs to lower voltages and higher frequencies by using more advanced CMOS technologies and the design methodologies proposed in this thesis, and
- adding GSM to the list of the standards modeled in MATLAB towards completing the model for multi-standard receiver system simulations.

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Appendix A: Design Ported to TSMC 65nm CMOS Technology

A.1 Introduction

To prove the portability of the proposed circuitry and the applicability of the associated design methodologies to more advanced CMOS technologies, the circuitry discussed in Chapters 3 and 4 are ported to TSMC 65nm CMOS Technology¹.

Fig. A.1 shows the typical supply voltage (VDD) and typical threshold voltage (V_{th}) scaling of the CMOS technology from 3 μ m down to 45nm node. This plot highlights the increased difficulty associated with designing high linearity circuits as the technology scales down. This is happening mainly due to the fact that CMOS transistors threshold voltage scales down at a much slower rate the supply voltage does, and eventually leaves the transistor with less voltage headroom.

The low-voltage, high linearity circuit technique proposed in this work, allows for the 0.18 μ m circuit to operate at 1V supply voltage which is 44% below its nominal value, while maintaining competitive linearity characteristics. This feature is the key behind easy portability of the proposed circuit topologies to more advanced, lower voltage CMOS technologies.

¹ The original design was implemented in 0.18 μ m CMOS technology.

APPENDIX A- Design Port to TSMC 65nm CMOS Technology

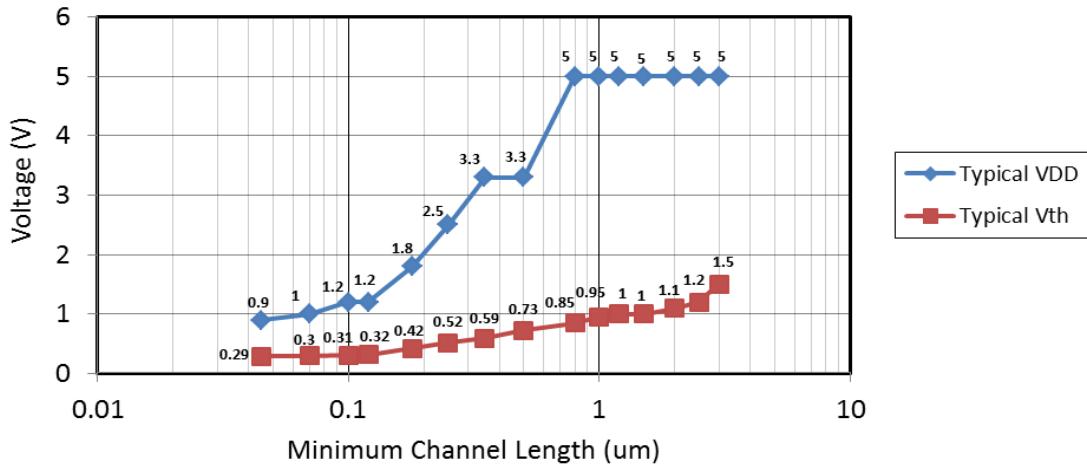


Fig. A.1 CMOS technology threshold voltage (Vth) and supply voltage (VDD) scaling.

The down-converter circuit was first ported to 65nm based on fixed current density scaling. The transconductor stage transistors current density was then decreased by 14% to achieve the same performance as the original design. This was done by increasing the transistor widths.

The performance of the down-converter redesigned in TSMC 65nm CMOS is tabulated and compared to the original design in TSMC 0.18 μm CMOS, in Table A.1.

Table A.1 Down-converter comparison

Technology	0.18 μm	65nm	65nm
RF Frequency	8 GHz	8GHz	8 GHz
Supply Voltage	1V	1V	0.9V
Power	6.9mW	6.9mW	6.2mW
LO Power	-3 dBm	-2dBm	-2dBm
IIP3	+3.5	+5	+3.1
Conversion Gain	+6.5	+5	+5
Noise Figure (SSB)	11dB	13dB	13dB
1-dB Compression	-5.5 dBm	-5dBm	-5.7dBm

APPENDIX A- Design Port to TSMC 65nm CMOS Technology

As expected, the proposed circuit maintains its linearity performance under low-supply voltage of 65nm technology.

The quadrature generator presented in Chapter 4 was also ported to 65nm CMOS. The same principle depicted in Fig.A.1 explains the easy portability of the proposed design to more advanced technologies. The design was ported to 65nm based on the same porting strategy as the downconverter circuit. Current density in all active inductor transistors was increased by 8%. The buffer transistors current density was decreased by 11% in the 65nm circuit compared to its 0.18 μ m counterpart.

Table A.2 summarizes the performance of the quadrature signal generator in 65nm technology compared to its 0.18 μ m counterpart.

Table A.2 Quadrature Down-converter port to 65nm technology

Technology	0.18 μ m	65nm
RF Frequency	8 GHz	15GHz
Supply Voltage	1V	0.9V
Power	12mW	10.5mW
Phase Error	1 Degree	2.1 Degrees
Amplitude Error	0.4dB	0.8dB
Area	0.009 mm ²	---

Due to the relatively higher transition frequency of the 65nm versus 0.18 μ m technology, the quadrature generator designed in 65nm is capable of providing accurate quadrature phase shift upto 15GHz².

² The 0.18 μ m implementation works only upto 8.2GHz.

APPENDIX A- Design Port to TSMC 65nm CMOS Technology

A.2 Summary

The proposed low-voltage, high linearity circuit design techniques proposed in Chapters 3 and 4 are not limited to 0.18 μ m CMOS technology. They are directly applicable to advanced nano-scale CMOS technologies. The quadrature generator is capable of proving accurate quadrature signals up to 15GHz, compared to 8.25GHz in 0.18mm. The increase of speed is attributed to the higher transition frequency of 65nm transistors compared to 0.18 μ m.