VLSI - Assignment 2

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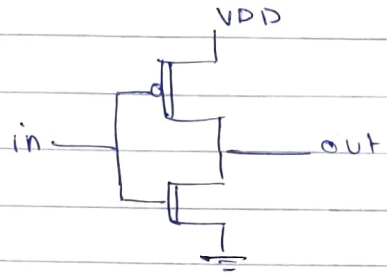
Q1.

(a) NOT



max delay = 5.08499×10^{-11} s.

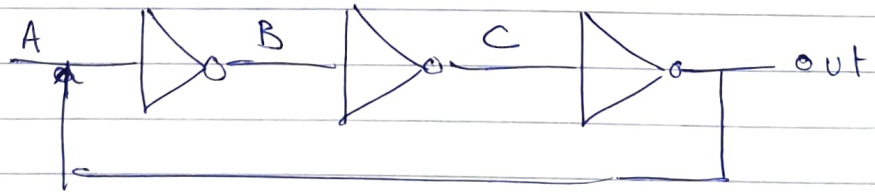
(b) 5-input - AND

(c) 4-input - OR

(d) 2-input - XOR

plots & delays attached in pictures after this page.

Q2. 3-Not-gate Ring Osc ↓



out is complement of A(t)

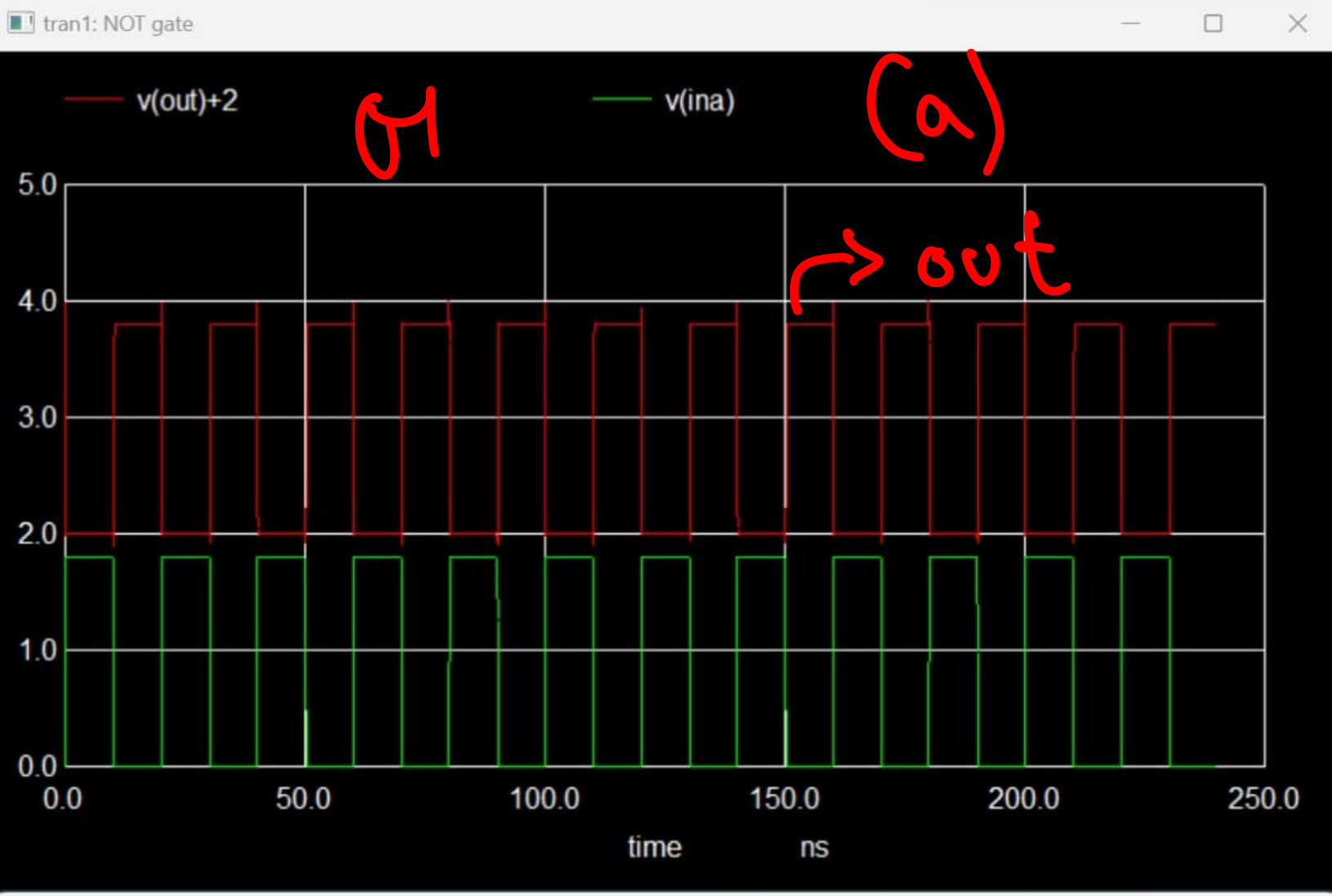
& $A(t+1) = out$

$B(t) = A'(t)$

& $C(t) = B'(t) = A(t)$.

& $out(t) = A'(t)$.

flow of bits.



ngspice 41

```
vdd#branch                      -7.20754e-12

No. of Data Rows : 385

  Measurements for Transient Analysis

trise                =   3.869565e-11 targ=  8.869565e-11 trig=  5.000000e-11
tfall                =   6.300415e-11 targ=  1.021300e-08 trig=  1.015000e-08
tpd                  =   5.08499e-11

ngspice 5 ->
```

NOT_mag.cir | -- ready -- | Stop | Quit

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
a                                            0
b                                            0
c                                            0
d                                            0
e                                            0
vdd                                        1.8
out                                  8.4831e-09
vdd#branch                          -1.78588e-11
ve#branch                                    0
vd#branch                                    0
vc#branch                                    0
vb#branch                                    0
va#branch                                    0

No. of Data Rows : 731

  Measurements for Transient Analysis

trisea          =  2.761446e-10 targ=  3.261446e-10 trig=  5.000000e-11
tfalla          =  1.739981e-10 targ=  1.032400e-08 trig=  1.015000e-08
tpd             =  2.25071e-10
triseb          =  2.761446e-10 targ=  3.261446e-10 trig=  5.000000e-11
tfallb          =  1.027400e-08 targ=  1.032400e-08 trig=  5.000000e-11
tpd             =  5.27507e-09
trisec          =  2.761446e-10 targ=  3.261446e-10 trig=  5.000000e-11
tfallc          =  1.027400e-08 targ=  1.032400e-08 trig=  5.000000e-11
tpd             =  5.27507e-09
trised          =  2.761446e-10 targ=  3.261446e-10 trig=  5.000000e-11
tfalld          =  1.027400e-08 targ=  1.032400e-08 trig=  5.000000e-11
tpd             =  5.27507e-09
trisee          =  2.761446e-10 targ=  3.261446e-10 trig=  5.000000e-11
tfalle          =  1.027400e-08 targ=  1.032400e-08 trig=  5.000000e-11
tpd             =  5.27507e-09

ngspice 5 ->
```

07 (b)

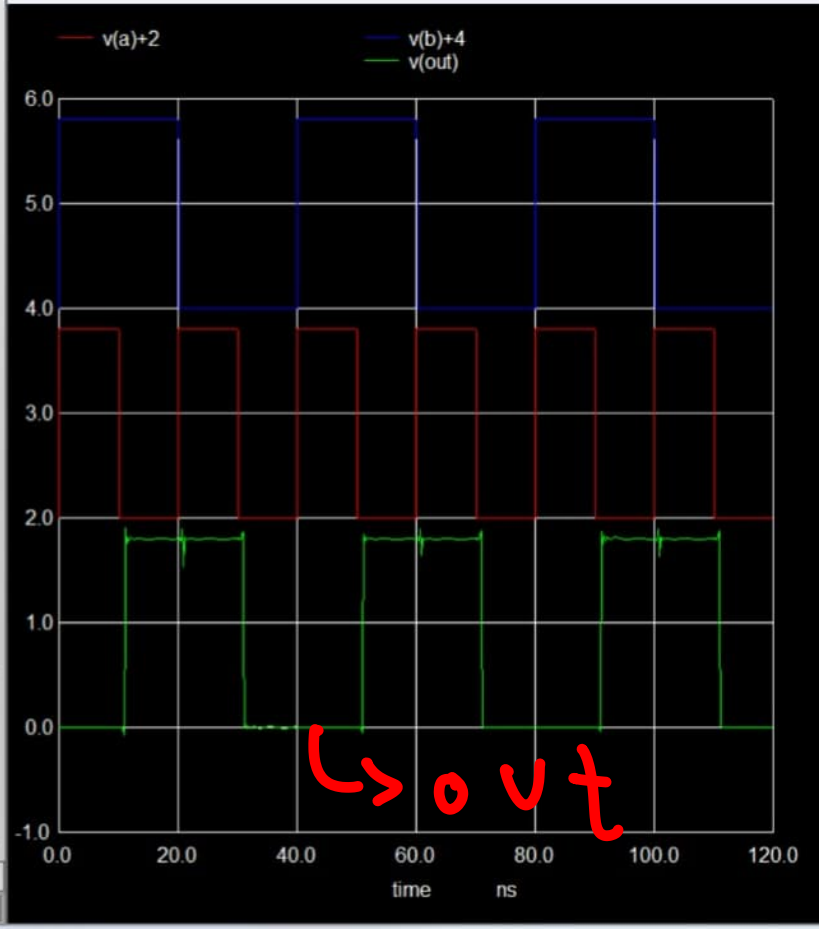
out

```
Circuit: * spice3 file created from 4_input.ext - technology: scmos

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


Checking parameters for BSIM 3.2 model cmosp
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.

Checking parameters for BSIM 3.2 model cmosn
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
a                                            0
b                                            0
c                                            0
d                                            0
vdd                                        1.8
out                                 1.49449e-08
vdd#branch                         -3.93867e-11
vd#branch                                    0
vc#branch                                    0
vb#branch                                    0
va#branch                                    0


No. of Data Rows : 370

  Measurements for Transient Analysis

trisea          =  9.220763e-11 targ=  1.422076e-10 trig=  5.000000e-11
tfalla          =  1.406528e-07 targ=  1.508028e-07 trig=  1.015000e-08
tpd             =  7.03725e-08
triseb          =  9.220763e-11 targ=  1.422076e-10 trig=  5.000000e-11
tfallb          =  1.507528e-07 targ=  1.508028e-07 trig=  5.000000e-11
tpd             =  7.54225e-08
trisec          =  9.220763e-11 targ=  1.422076e-10 trig=  5.000000e-11
tfallc          =  1.507528e-07 targ=  1.508028e-07 trig=  5.000000e-11
tpd             =  7.54225e-08
trised          =  9.220763e-11 targ=  1.422076e-10 trig=  5.000000e-11
tfalld          =  1.507528e-07 targ=  1.508028e-07 trig=  5.000000e-11
tpd             =  7.54225e-08

ngspice 6 ->
```

(c)

```
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Checking parameters for BSIM 3.2 model cmosn
Warning: Ps = 0 is less than W.

Checking parameters for BSIM 3.2 model cmosn
Warning: Ps = 0 is less than W.

Checking parameters for BSIM 3.2 model cmosn
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.

Checking parameters for BSIM 3.2 model cmosp
Warning: Pd = 0 is less than W.

Checking parameters for BSIM 3.2 model cmosp
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.

Checking parameters for BSIM 3.2 model cmosp
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
a                                            0
b                                            0
vdd                                        1.8
out                                 2.26166e-08
vdd#branch                         -9.93418e-11
vb#branch                                    0
va#branch                                    0


No. of Data Rows : 318

   Measurements for Transient Analysis

trisea               =  1.100765e-08 targ=  1.105765e-08 trig=  5.000000e-11
tfalla               =  3.097587e-08 targ=  3.102587e-08 trig=  5.000000e-11
tpd                  =  2.09918e-08
triseb               =  1.100765e-08 targ=  1.105765e-08 trig=  5.000000e-11
tfallb               =  3.097587e-08 targ=  3.102587e-08 trig=  5.000000e-11
tpd                  =  2.09918e-08

ngspice 8 ->
```

(d)



XOR_mag.cir -- ready -- Stop Quit

The plots for ngspice & magic simulaⁿ have been attached after this page.

~~No,~~ ~~the~~ Function of 1 NOT-gate osc. will be be same in terms of input/output

but the periodicity of oscillation increases in case of 3-NOT gate osc due to added delay of 3 NOT gates. It is 3 times (nearly) lesser in 1-NOT gate osc.

=> less oscillations for 3-inverter osc. than 1-inverter osc for same time frame.

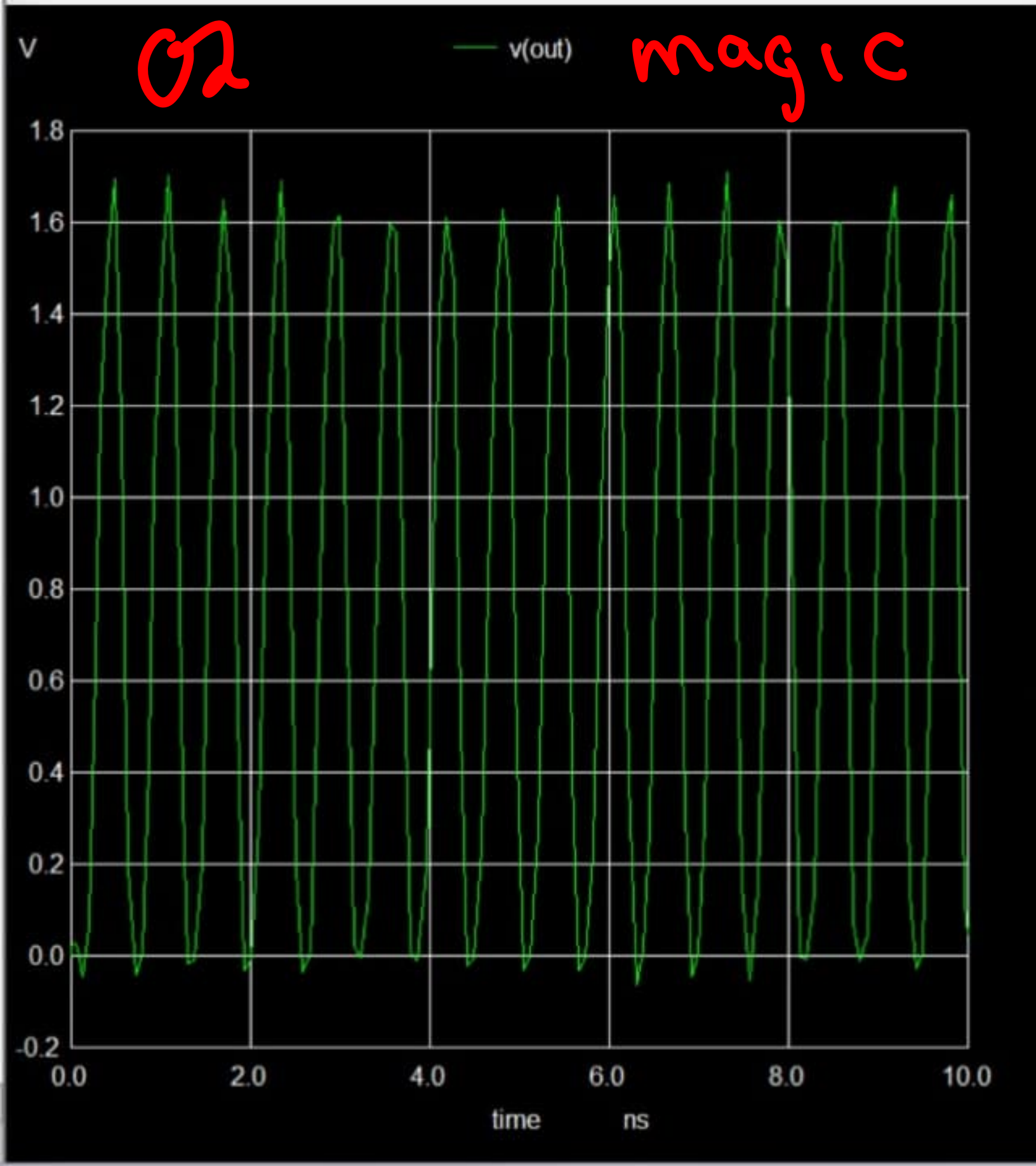
Q3. Truth table

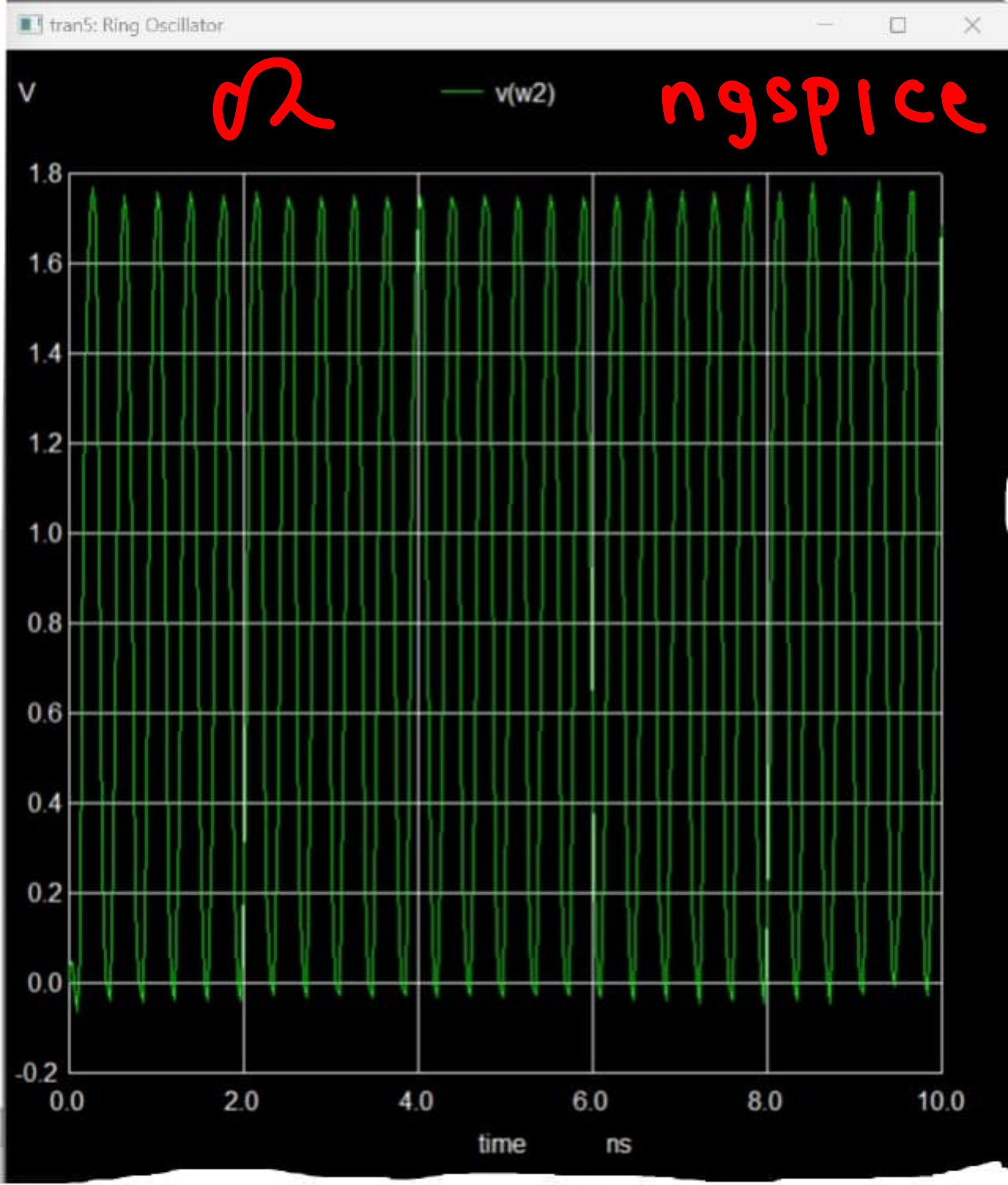
A2	A1	A0	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

majority fⁿ

$\therefore Y = (A2')(A1)(A0) + (A2)(A1')(A0) + (A2)(A1)(A0)' + (A2)(A1)(A0)$

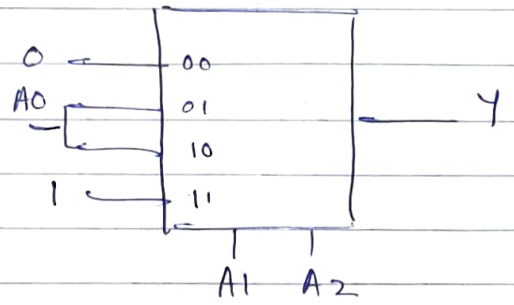
$\therefore Y = (A2')(A1')\cdot 0 + (A0)[(A1')(A2) + (A1)(A2')] + (A2)(A1)\,1.$


V
v(out)
02
magic
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
2.0
4.0
6.0
8.0
10.0
time
ns


tran5: Ring Oscillator
V
v(w2)
w2
ngspice
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
2.0
4.0
6.0
8.0
10.0
time
ns

These four terms in Y, depict the function of a 4x1 MUX where A2 & A1 are select lines

↓



Trend in delay : → delay increases with temperature because the current flowing through CMOS decreas due to increase in V_{th}

⇒ cap charges slowly so delay ↑.

Output pics attached after this page.

Q4 We need a circuit that gives absolute value of a number (3 bit — 4th bit signed)

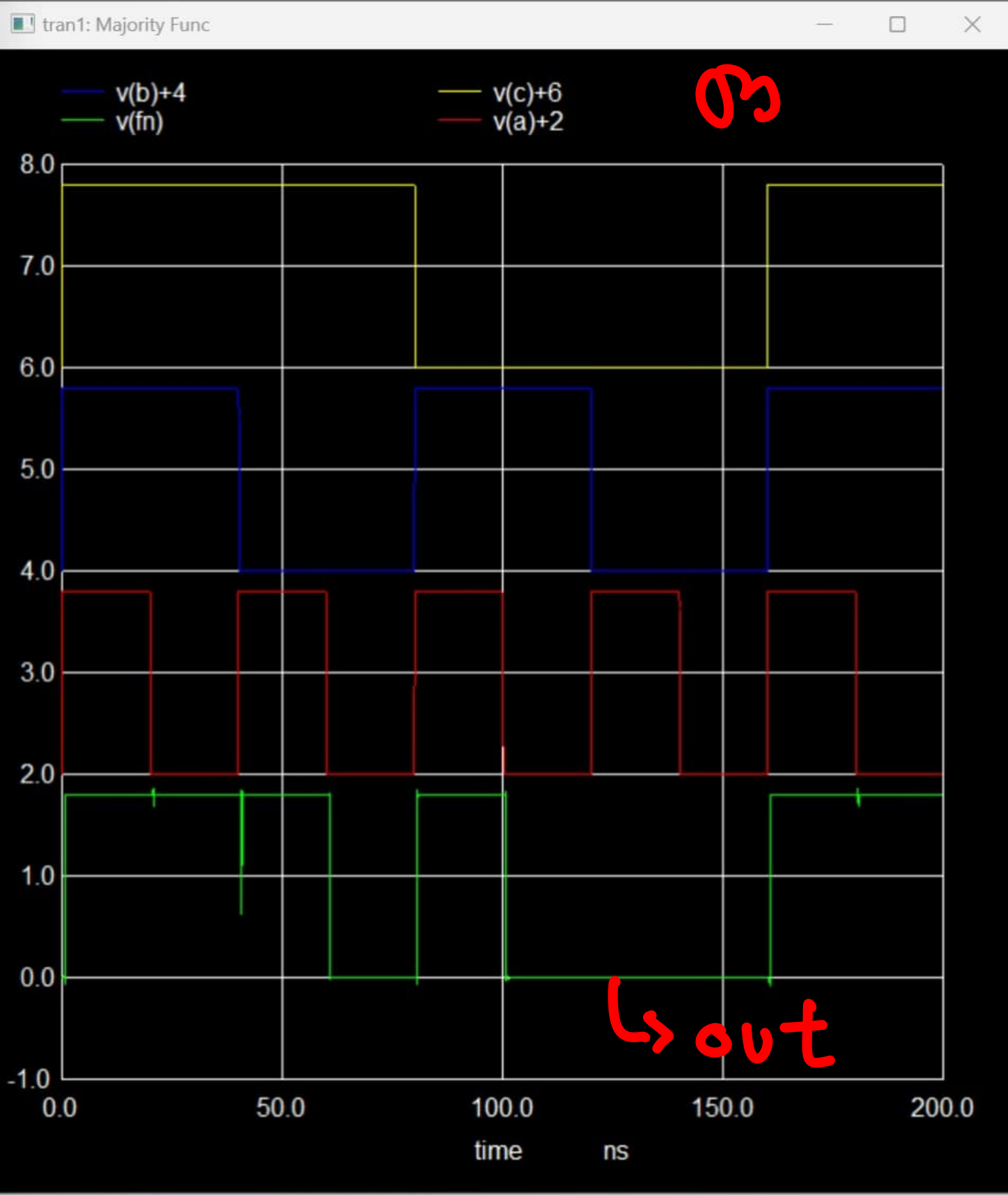
: Logic : if A_3 (4th bit) = 0

then $S_2 = A_2$, $S_1 = A_1$ & $S_0 = A$

if $A_3 = 1$

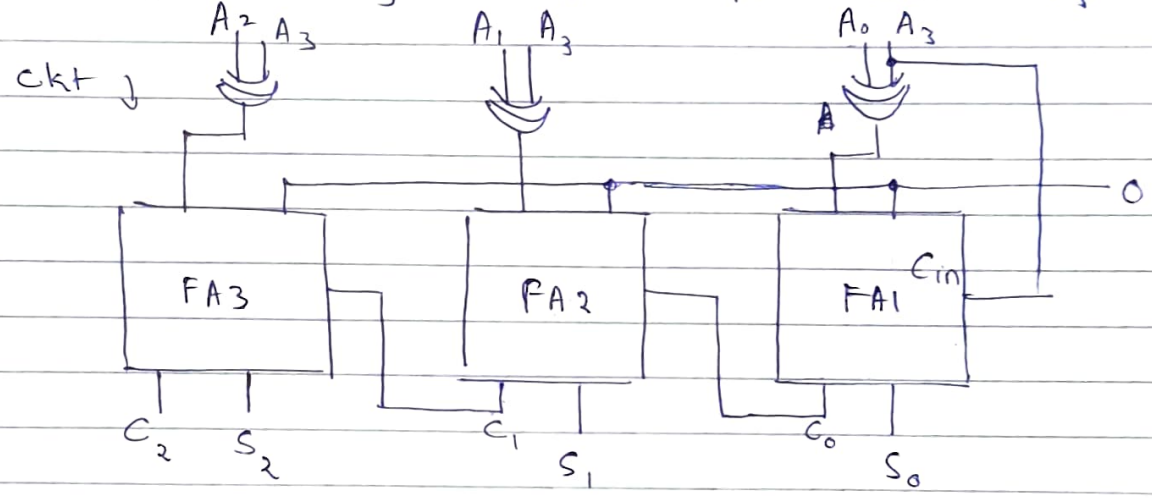
then

	A_2' ~~$\oplus A_3$~~	A_1'	A_0'
+	0	0	1
	S_2	S_1	S_0


tran1: Majority Func
v(b)+4
v(c)+6
v(fn)
v(a)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
50.0
100.0
150.0
200.0
time
ns

to get A_2' A_1' & A_0' we XOR them with A_3

Now first carry to first full adder = A_3



~~Pic~~ output after this page.

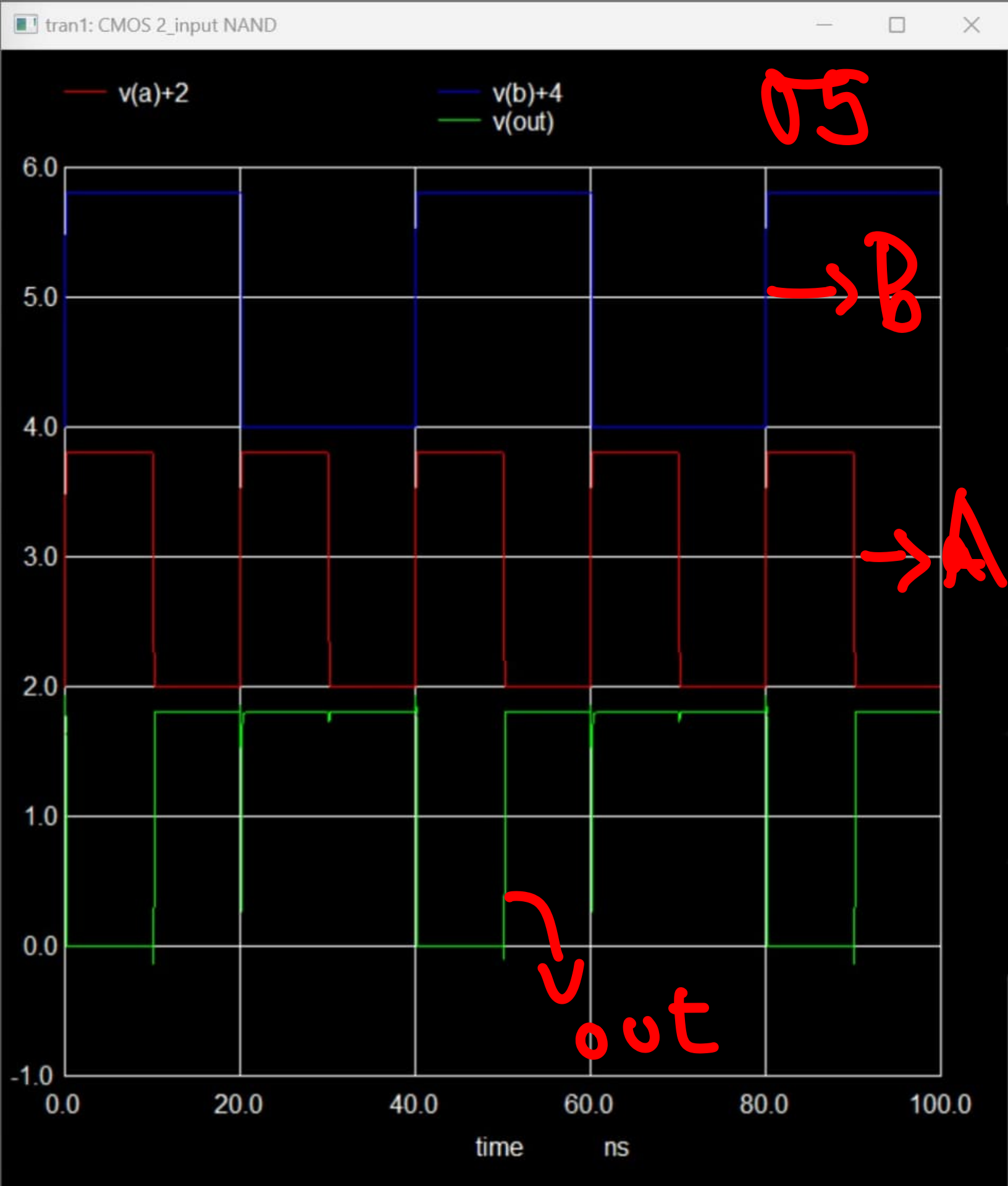
05. ~~As 1~~

(a) As temp ↑ delays ↑ because as V_{th} rises, the current reduces which essentially charges the capacitor more slowly thereby delaying the responses.

(b) delay trend as C_L ↑ → delay ↑ as C_L ↑ because $\tau = 0.67 R C_L$ ↑

C_L (fF)	delay (s)	C_L (fF)	delay (s)
2	6.74820×10^{-11}	12	9.1461×10^{-11}
4	7.22902×10^{-11}	14	9.5913×10^{-11}
6	7.75434×10^{-11}	16	1.0072×10^{-10}
8	8.3567×10^{-11}	18	10.579×10^{-10}
10	8.7143×10^{-11}	20	11.067×10^{-10}

Pic after this page.


tran1: CMOS 2_input NAND
v(a)+2
v(b)+4
v(out)
05
→B
→A
→out
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ns


tran3: Absolute Value Calculator
v(s1)+2
v(s2)+4
v(s0)
04
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
S2
S1
S0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
time
ns