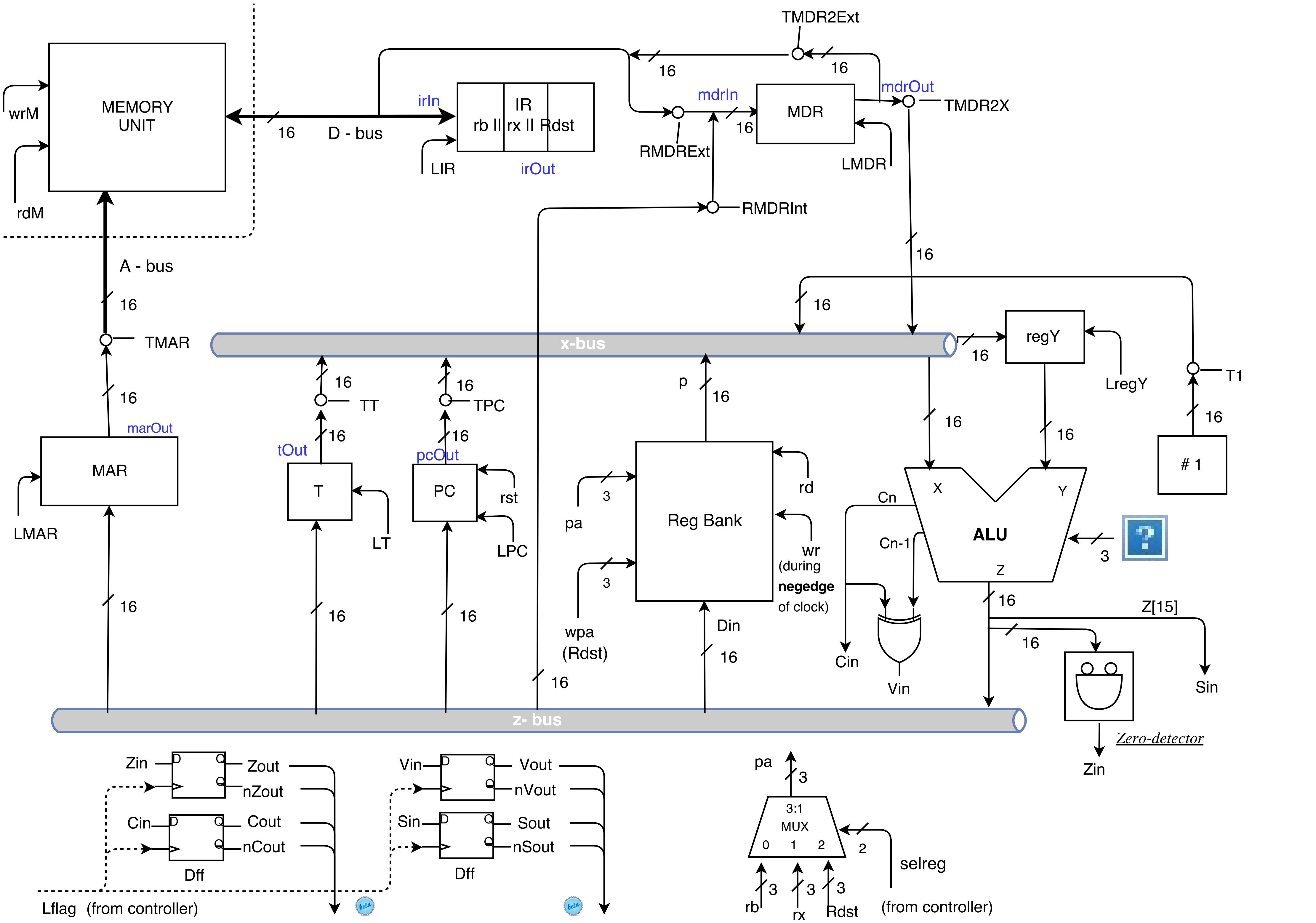
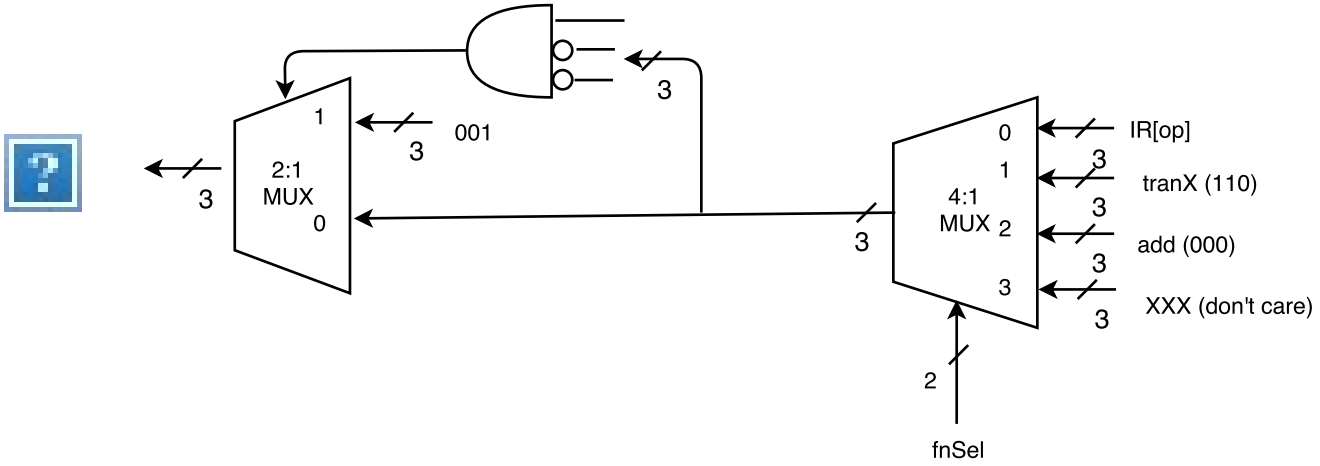
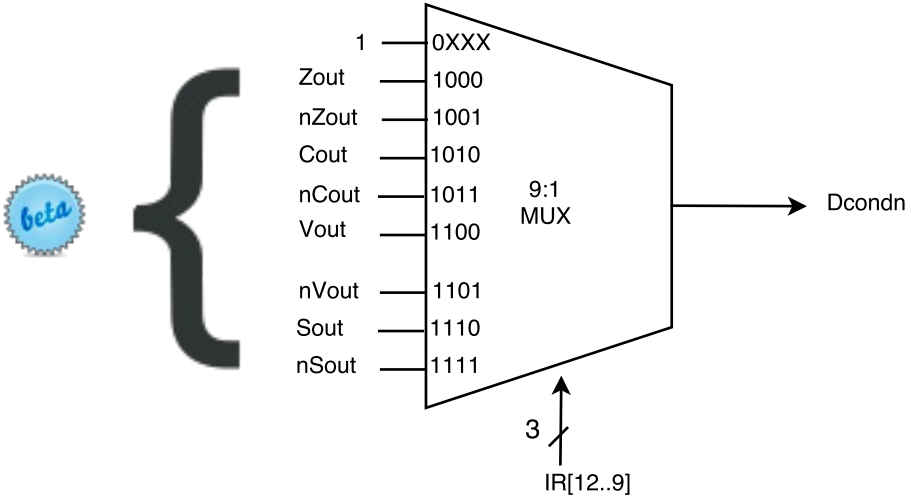


MEMORY UNIT
wrM
rdM
D - bus
16
irIn
IR
rb ll rx ll Rdst
LIR
irOut
TMDR2Ext
mdrIn
MDR
mdrOut
TMDR2X
RMDRExt
LMDR
RMDRInt
A - bus
TMAR
marOut
MAR
LMAR
x-bus
TT
tOut
T
LT
TPC
pcOut
PC
rst
LPC
p
Reg Bank
pa
rd
wr
(during
negedge
of clock)
wpa
(Rdst)
Din
regY
LregY
T1
1
Cn
Cn-1
X
Y
ALU
Z
3
Cin
Vin
Z[15]
Sin
Zero-detector
Zin
z- bus
Zin
Zout
nZout
Cin
Cout
nCout
Dff
Vin
Vout
nVout
Sin
Sout
nSout
Dff
Lflag (from controller)
pa
3:1
MUX
0 1 2
selreg
(from controller)
rb
rx
Rdst





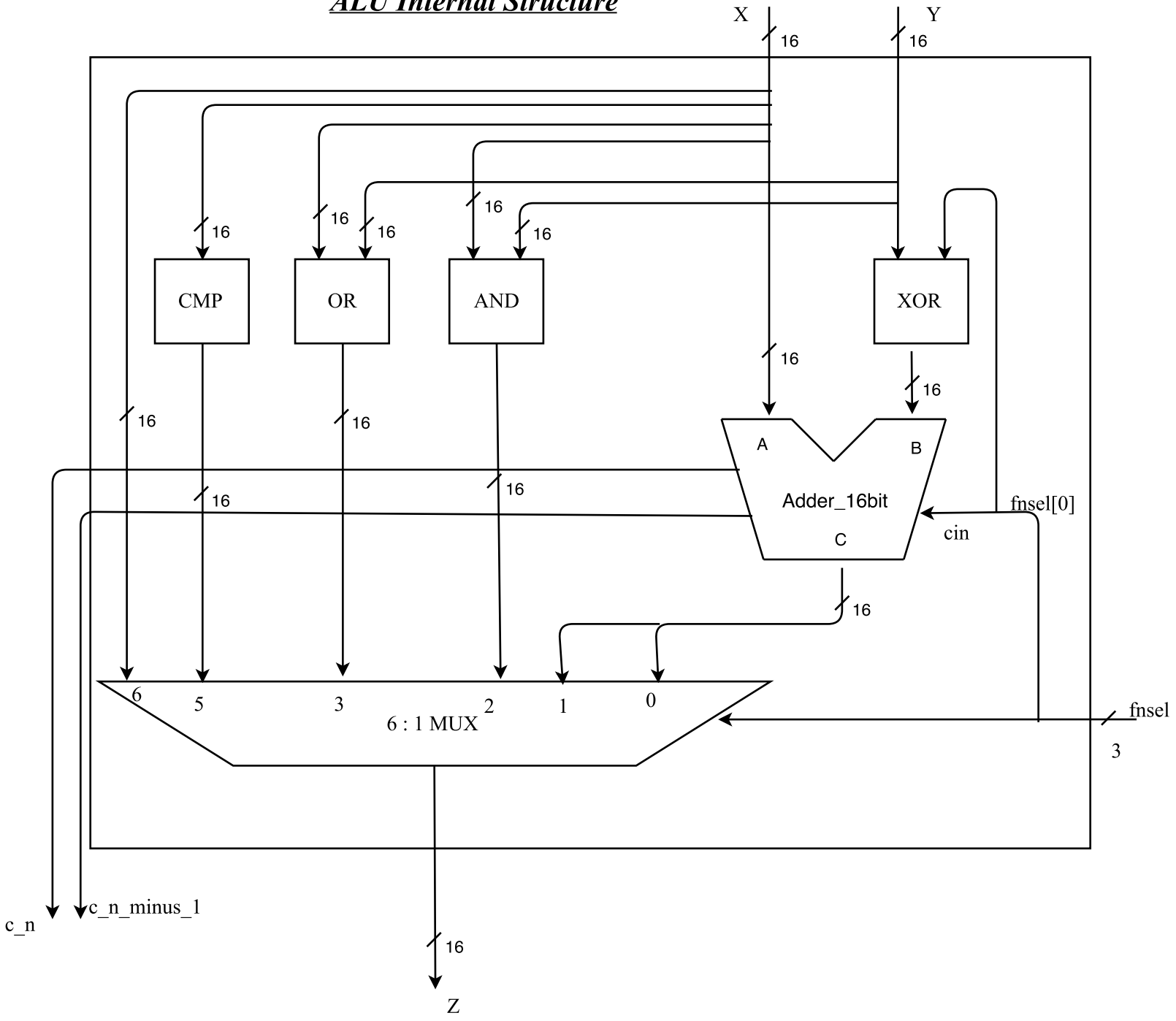
Inputs to datapath from controller :-

rd, wr, LPC, TPC, LT, TT, LMAR, TMAR, rdM, wrM, LIR, RMDRExt, RMDRInt, TMDR2X, TMDR2Ext, LMDR, LregY, T1, fnSel, Lflag, selreg, rst(this 'rst' signal from controller resets ALL the registers in the datapath)

Outputs from datapath to controller :-

Dcondn; IR[cc], IR[opcode] i.e. IR[15...9]

ALU Internal Structure



Register Bank Internal Structure