St. Cloud State University

Department of Electrical and Computer Engineering

Final Design Project

Design and Application of a Current Feedback Operational Amplifier (CFOA)

ECE 316-01 Analog Electronics – Prof. Hossain

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Objectives

To design, to simulate, to build, and to analyze a current feedback operational amplifier (CFOA) and implement it using the design procedure required. The design includes biasing, input and output stage, current mirrors, and transimpedance gain stage. These stages making a total of 24 transistors for the circuit design to enhance the amplifier performance. Besides, there are several requirements need to be achieved for the simulation and analysis.

Theory

The current feedback operational amplifier is an electronic module device used in modern analog electronics whose input is sensitive to current, rather than to voltage as in voltage feedback amplifier VFOA. See figure (1) for the basic module of CFOA. The design of CFOA differs from VFOA, which can operate at higher frequencies with very high slew rate and higher gain bandwidth product, which is independent of closed loop gain. See figure (2) for the comparison of CFOA and VFOA. They are used in high frequency applications where it performs better than the VFOA, which consumes minimum current are useful in many applications including video lines, front-end and multiplexing, DSL drivers, RF receivers, data communications, other communications, and sound system applications. However, CFOAs are power efficient amplifiers, it will have great impact in modern electronic devices, which are becoming more popular.

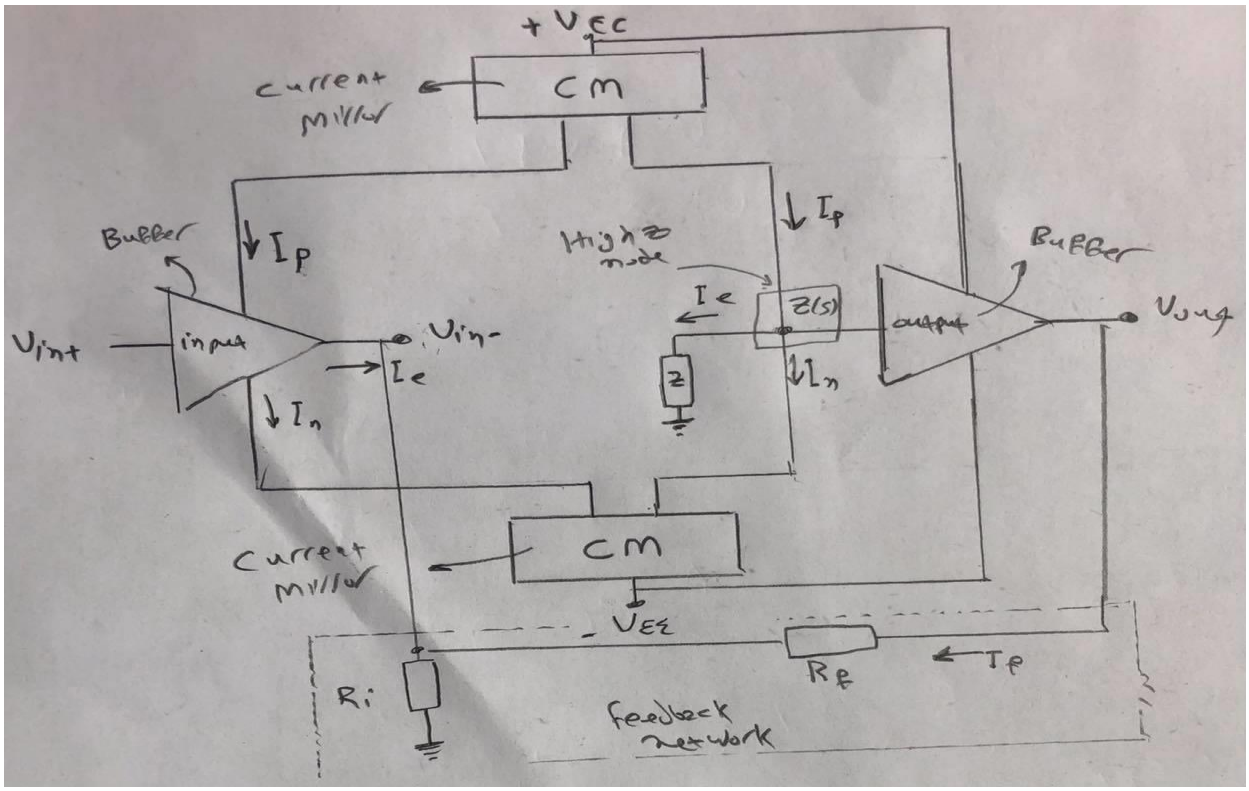


Figure (1) Basic Module of CFOA.

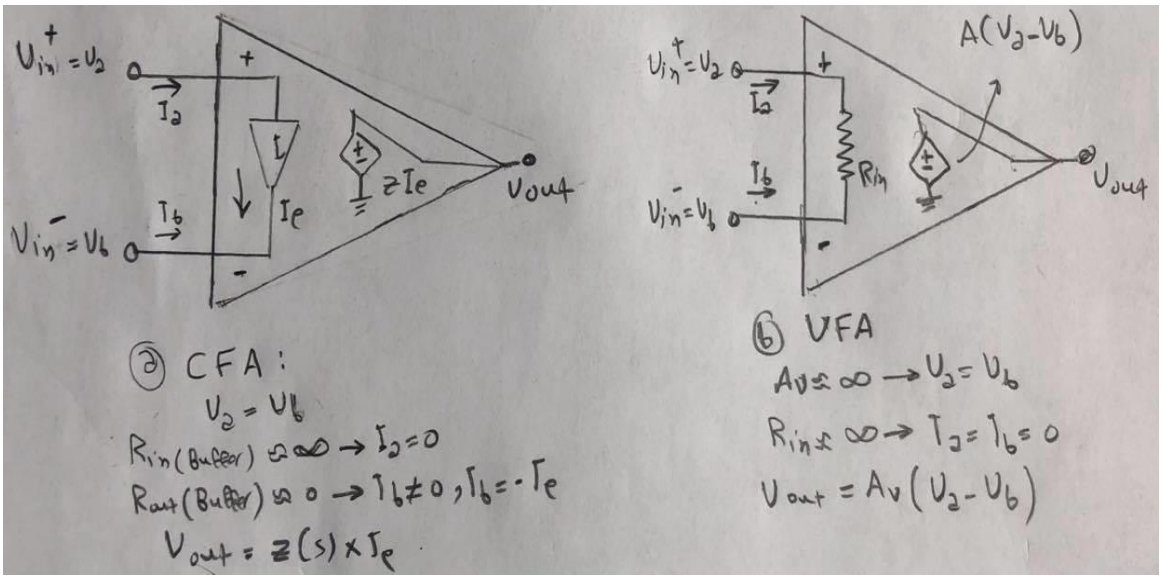


Figure (2) Comparison of CFOA with VFOA.

Design: (specifications and procedures**)**

a- The design specifications:

The specifications are DC source of VCC = 5V and VEE = -5V; it can be little higher if needed. Also, the current mirrors must be used to improve the amplifier performance. In addition, the slew rate should be 10-20 V/us in this project. The slew rate is critically important for amplifiers design. Plus, maximizing gain bandwidth product, which is relatively independent of the closed loop gain.

b- The design procedures:

i- Biasing stage and input stage:

An amplifier biasing stage includes a transistor that produces a signal for a pair of transistors within an output stage amplifier. However, the biasing stage also contains one resistive element connected to an emitter of the transistor, another resistive element connected to the base, and another is connected to a collector of the transistor. The resistances are selected to match with a voltage provided by the amplifier biasing stage, and it is also match with a temperature coefficient of the pair of transistors. In this design, the resistors are all having the same values, which is 1k**Ω**. Typically, the gain-bandwidth product is a constant and the slew-rate is limited to a maximum value determined by input stage bias current.

The design of the input stage of CFOA is responsible for determining the performance of the amplifier. It has number of advantages; it is simple, very low offset, and the biasing current in the inverting and non-inverting are matched and don’t vary with temperature. See the biasing stage and the input stage in the figure (3) below.

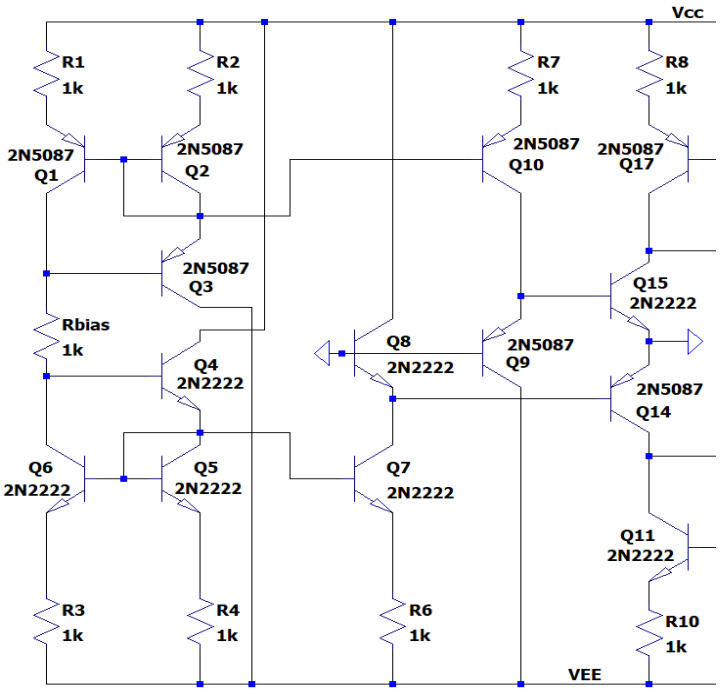


Figure (3) Input Stage and Biasing Stage of CFOA Circuit.

ii- Current mirrors:

This CFOA design contains four Wilson current mirrors type; this current mirror circuit uses three active devices that accept the current across its input and provide the copy or mirrored copy of the current to its output where $I_{C1} = I_{C2}$ and $I_{B1} = I_{B2}$. See the design capture below in figure (4) for Wilson current mirror.

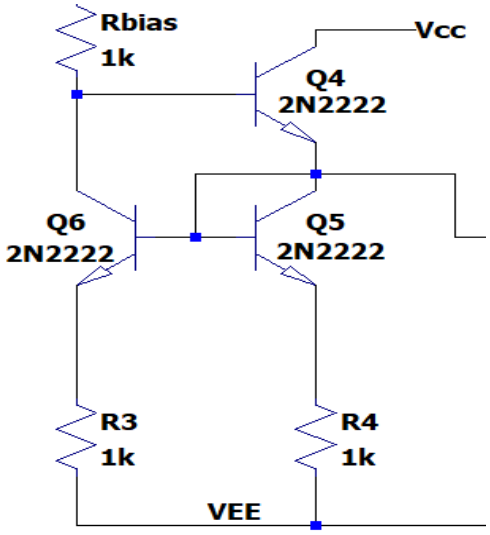


Figure (4) Current Mirror Wilson Type.

iii- Transimpedance gain stage:

From the block diagram figure (1) , the transimpedance gain block Z(i) is where the gain of the amplifier is achieved $A_0 = Z$. The ideal open loop transimpedance gain is infinity, which is intended

for closed loop applications. The transimpedance output is connected to a unity gain output buffer, which has an associated output impedance. The open loop transimpedance gain stage is used to construct the bode plot; see the simulation section below for the plot and see figure (5) for capture of the transimpedance gain stage taken from the CFOA design.

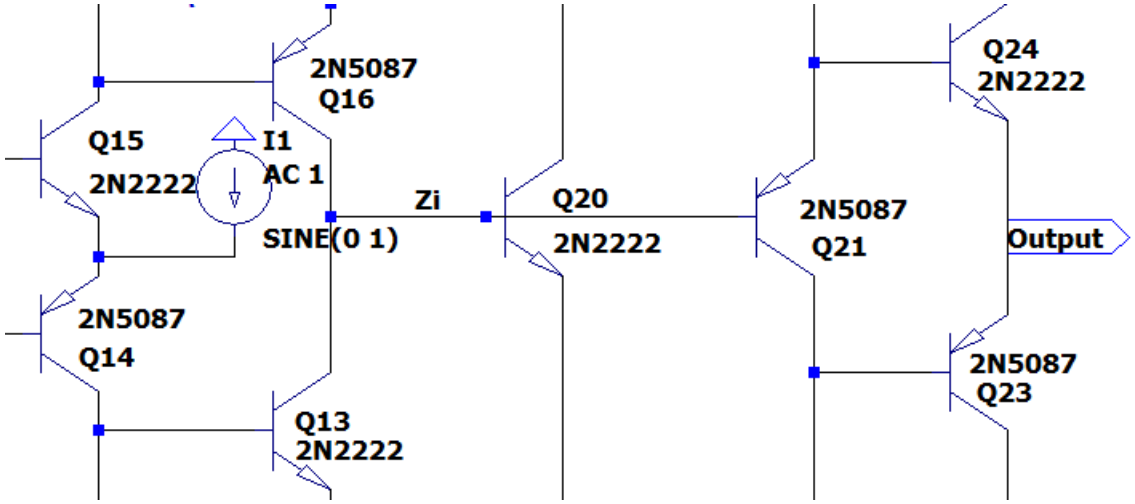


Figure (5) Transimpedance Gain Stage.

iv- Output stage:

The design of output voltage starts with common emitter output stage using BJTs which can only swing within saturation voltage; for small load current, the saturation voltage is low, but during high load current, the saturation voltage can increase. The output stage circuit helps to improve the current drive capability, and the buffer helps to decrease the output impedance. See the output stage in figure (6) below.

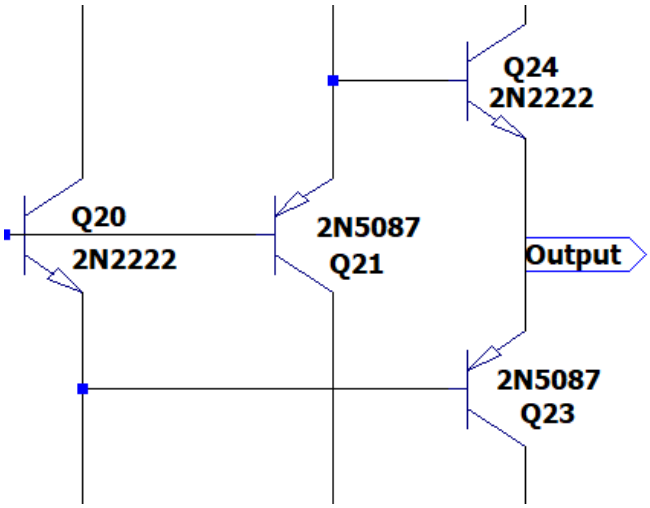
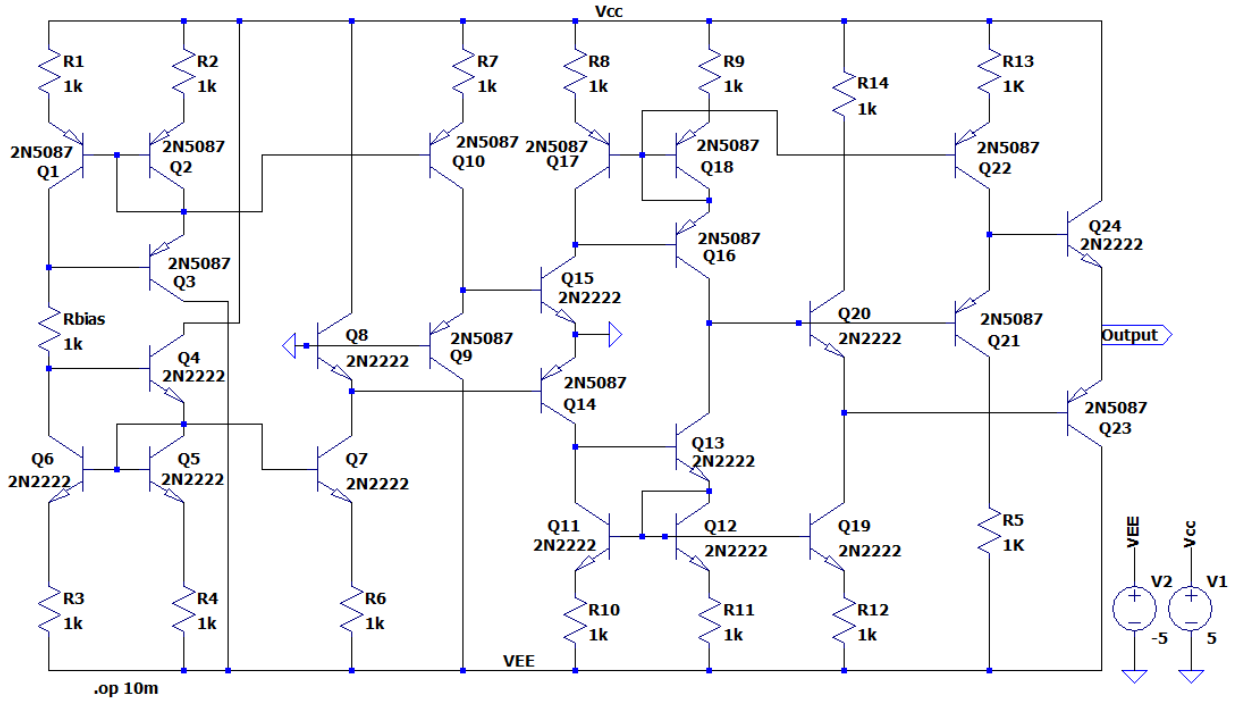


Figure (6) Output Stage.

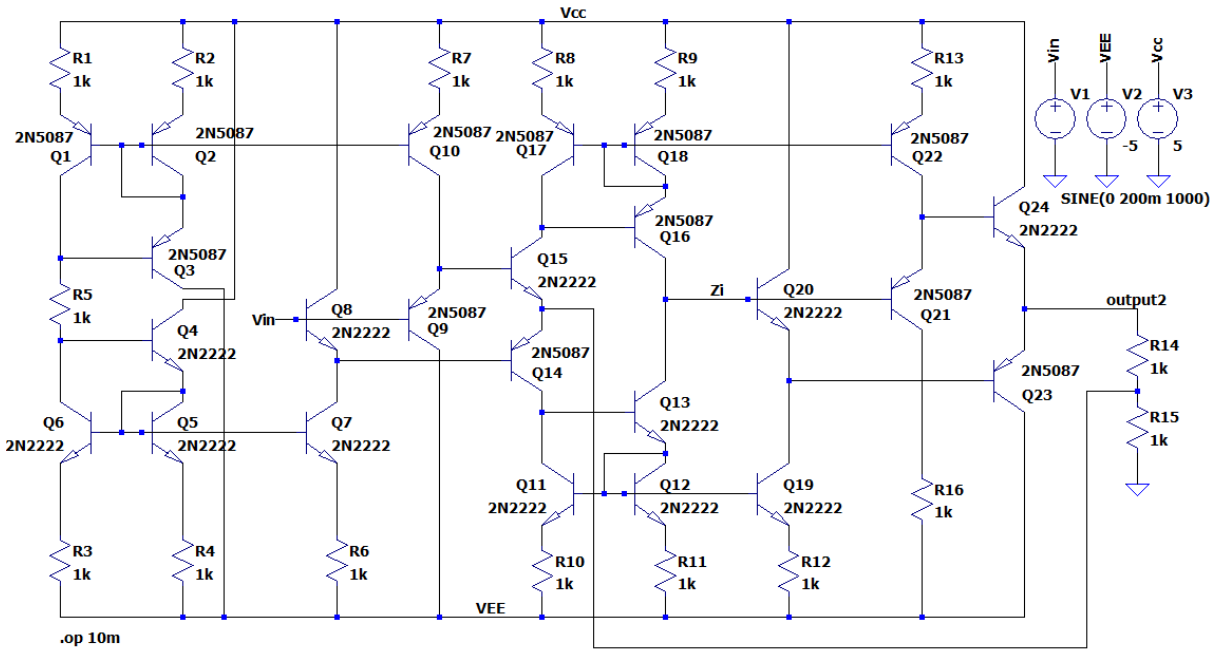
The whole design for the CFOA is including the stages mentioned above and some resistors with equal values. The design is completed with these necessary stages and combined to make the circuit work. See the complete design schematic of CFOA in figure (7) in the simulation section below.

Simulation:

The simulation is set using LTspice software; the schematic in figure (7) shows the final design used for DC simulation with voltages inputs set to ground, and the schematic in figure (8) shows the final design used for transient simulation. This schematic includes Vin voltage input and the feedback loop is connected to the output. There are four current mirrors. All resistors are chosen to be the same value, which is 1kΩ to allow the current to be mirrored or copied through the stages of the current feedback operational amplifier.



Figure(7) Schematic for Final CFOA Design using DC Simulation.



Figure(8) Schematic for Final CFOA Design using Transient Simulation.

The simulation includes the following results:

1- DC operating points:

In the figure (9) below, shows the DC operating points throughout the circuit of figure (7). The schematic in figure (7) is used to find the DC operating points of the circuit; the inputs are set to ground, and the feedback is removed. As seen from the figure (9) table, there are several voltages that have the same values. As expected, like voltages 2.576V and -3.38V are also repeated due to their node locations within the current mirrors in the circuit that has resistors and transistors that are the same throughout the circuit. Also, see operating points for the current values in Appendix A.

--- Operating Point ---

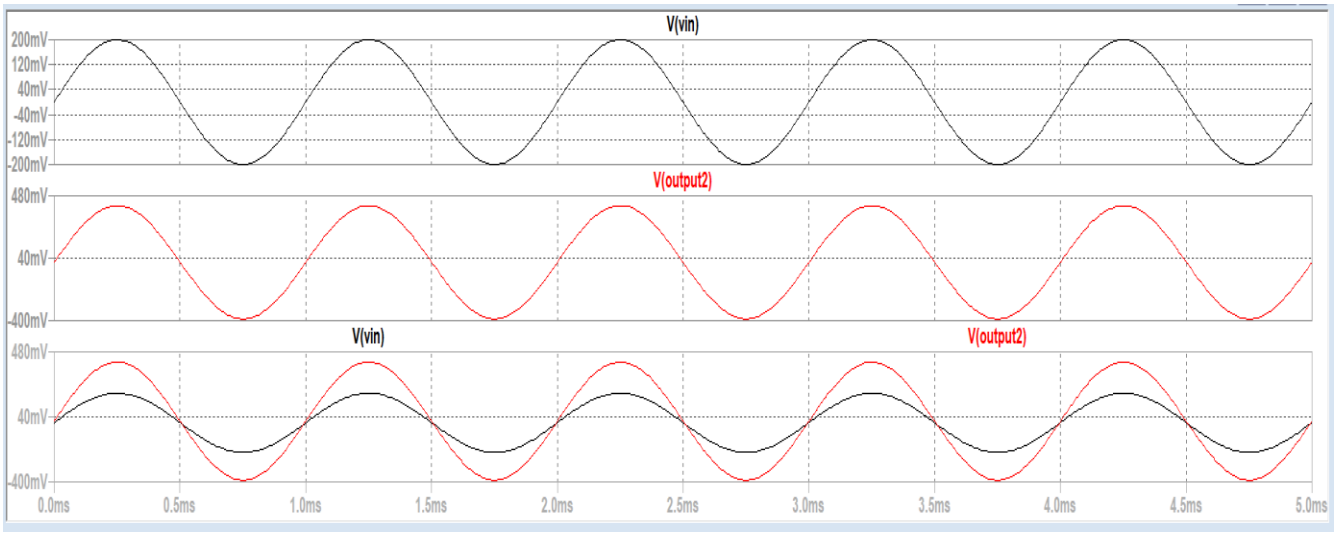
V(vcc):	5	voltage
V(n002):	2.57604	voltage
V(n003):	2.57643	voltage
V(n022):	-2.57647	voltage
V(vee):	-5	voltage
V(n023):	-2.57665	voltage
V(n011):	1.20244	voltage
V(n015):	-1.22056	voltage
V(n024):	-2.57634	voltage
V(n004):	2.57576	voltage
V(n005):	2.76672	voltage
V(n006):	2.76712	voltage
V(n025):	-3.38608	voltage
V(n026):	-3.38625	voltage
V(n027):	-3.38522	voltage
V(n007):	2.77771	voltage
V(n017):	1.39156	voltage
V(output):	2.06863	voltage
V(n009):	2.73857	voltage
V(n001):	2.08072	voltage
V(n021):	-3.08721	voltage
V(n014):	2.05891	voltage
V(n010):	1.36455	voltage
V(n012):	0.685573	voltage
V(n008):	1.88787	voltage
V(n019):	-2.05122	voltage
V(n016):	-0.677227	voltage
V(n020):	-2.71834	voltage
V(n013):	3.40708	voltage
V(n018):	-1.89795	voltage

Figure(9) DC Operating Points Voltages.

2- Transient simulation showing the input and output with closed loop and gain of 2 configuration:

In the figure (10) below, shows the transient simulation for the circuit in figure (8); using three plot panes windows to plot the input and output voltages. In the first pane, V_{in} is plotted, and it is 200mV. In the second pane, V_{out} is plotted, and V_{out} is designed to have a gain of 2 using the feedback loop. As seen in the plot, the amplitude of the output is double the amplitude of the input,

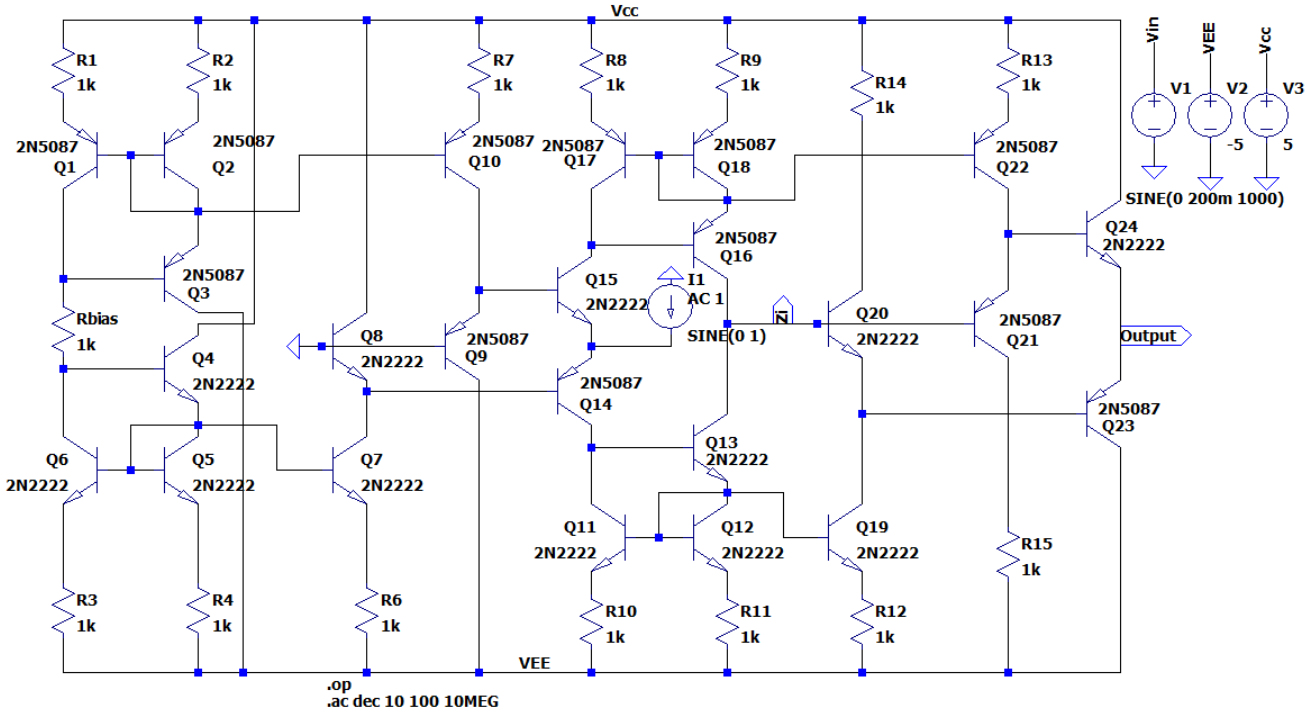
hence, this verifies the amplifier's gain of 2 configuration is amplified. The third pane is combined for V_{in} and V_{out} so that the difference can be easily seen.



Figure(10) The Transient Simulation.

3- Transimpedance versus frequency simulation:

The schematic below in figure (11) shows a simulation schematic for a current source applied to the feedback node with amplitude of 1. It is simply replacing the feedback with current source. This current source in the feedback node will show what happens at the gain node Zi or high Z node as in figure (11). The plot will show the impedance, which is Z = V/I , and A_0 = Z.



Figure(11) Simulation Schematic for Transimpedance.

The gain node has the same voltage in the Zi node and the output node, which is copied to the output node from Q20 to Q23 that is -0.7 for NPN and +0.7 PNP. The four transistors Q20, Q21, Q23, and Q24 are just copy the node Z to the output to make transimpedance with better shape. Conducting frequency analysis with Spice directive .ac dec 10 100 10MEG and see what the gain at Zi node is as in figure (12), which is about 73dB with the same value for output voltage.

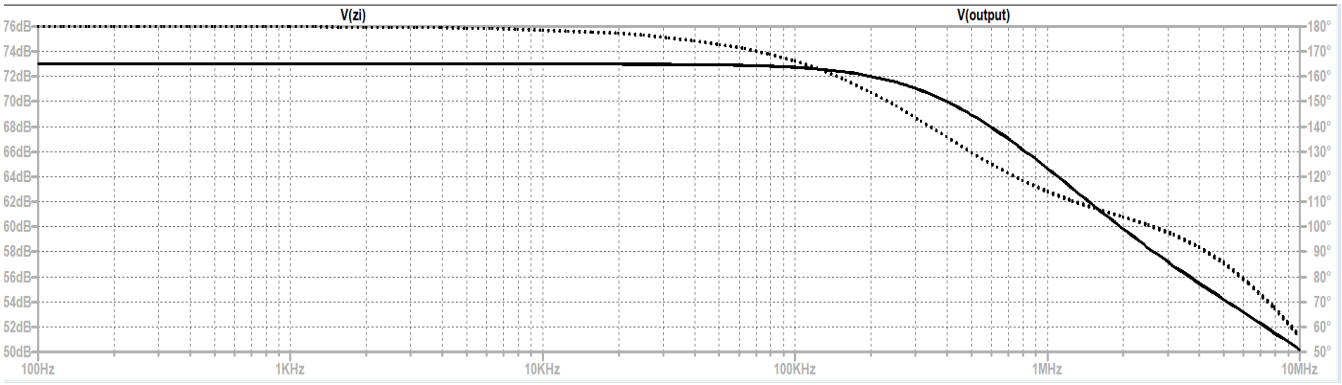
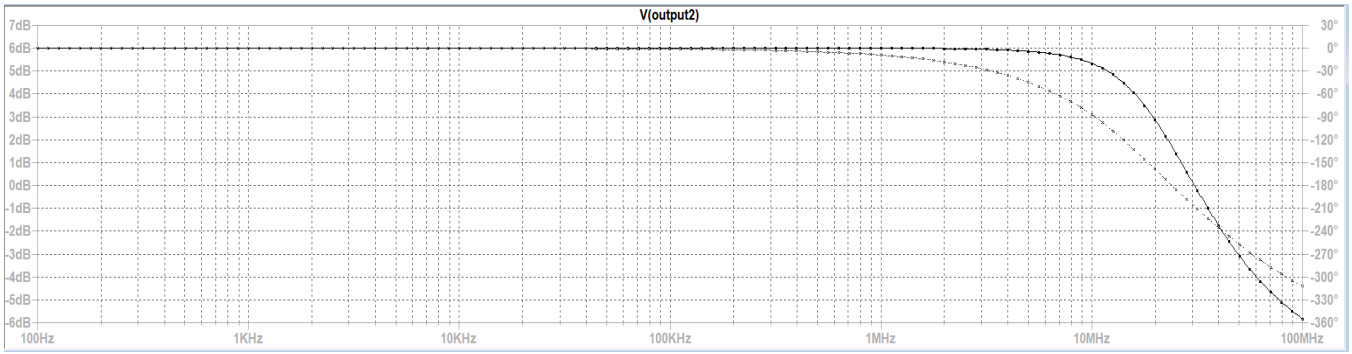
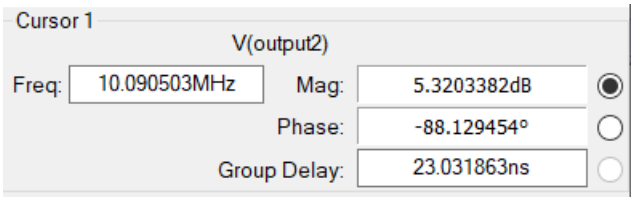


Figure (12) Transimpedance Gain.

4- Frequency simulation showing Bandwidth, Poles etc.:

The bode and phase plot of the figure (13) is for simulating the circuit in figure(8); also, showing a cursor contains magnitude and phase results. Using as analysis and setting the frequency in LTspice up to 100MHz; the plot indicates that the circuit acting like a low pass filter with cutoff frequency about 10MHz, phase about -88° and a gain of 2. Also, conducting another experiment by increasing the frequency to even higher than 100Meg, the cutoff frequency is 10MHz. This experiment indicates that the oscilloscopes cannot show more than 100Meg, but LTspice can.

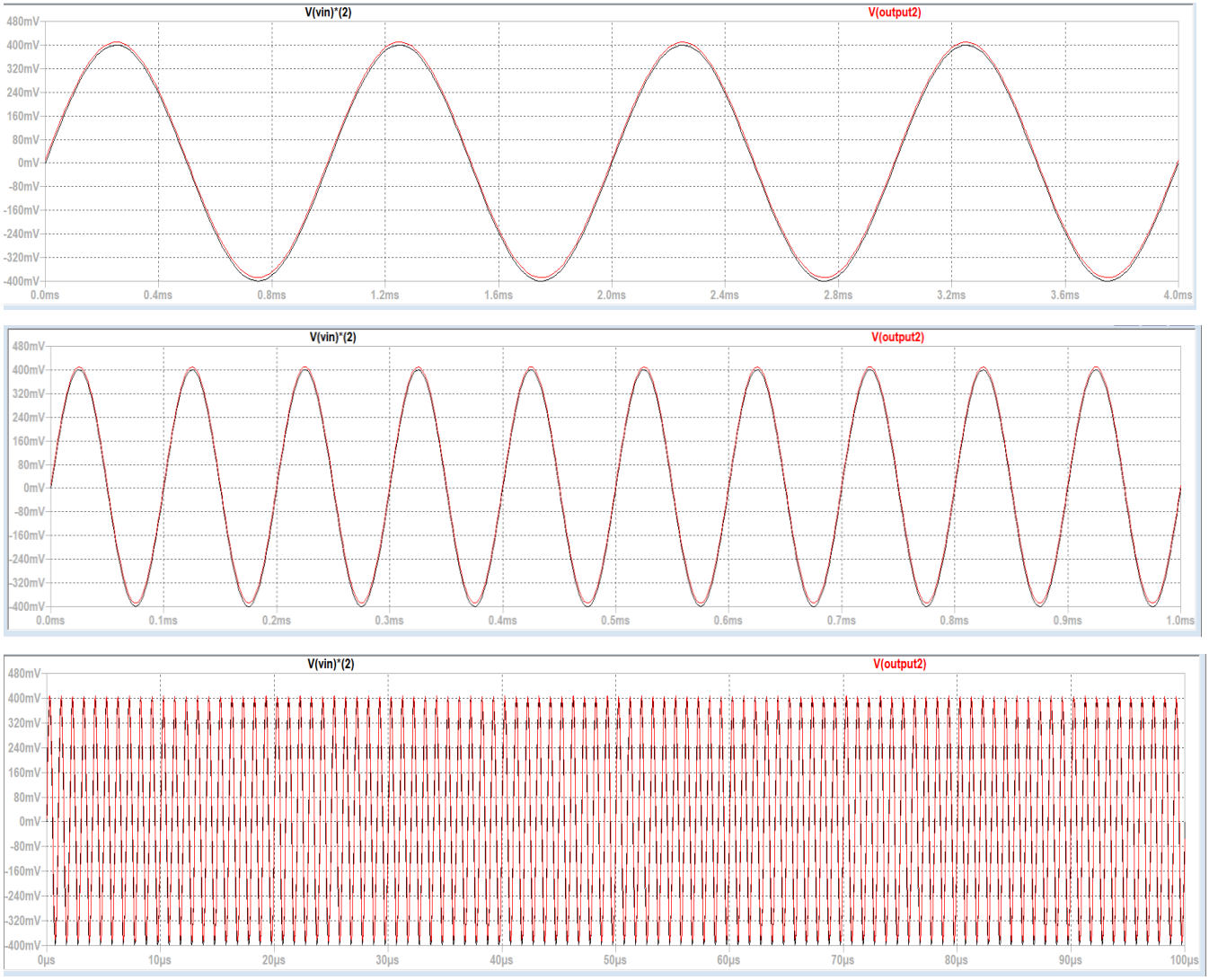




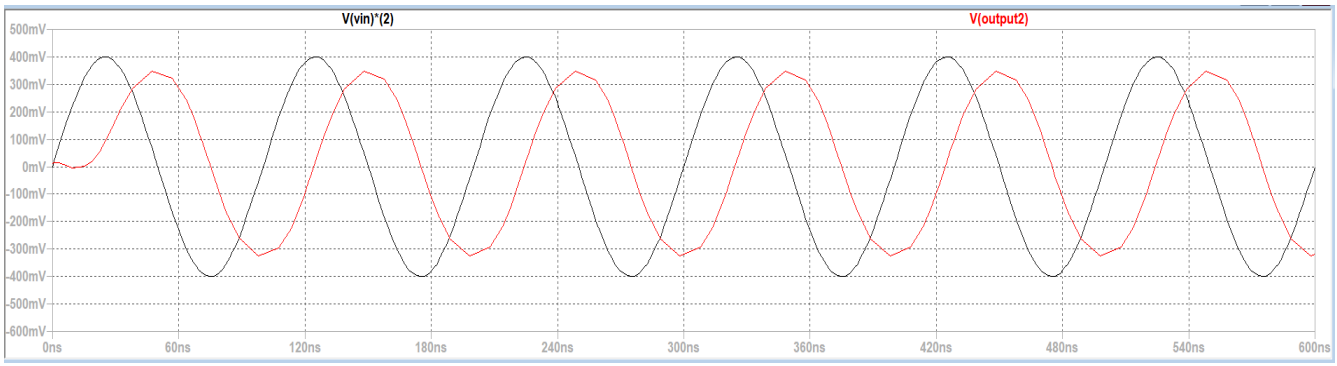
Figure(13) Bode and Phase plot with a cursor showing magnitude and phase.

5- Transient simulation and slew rate:

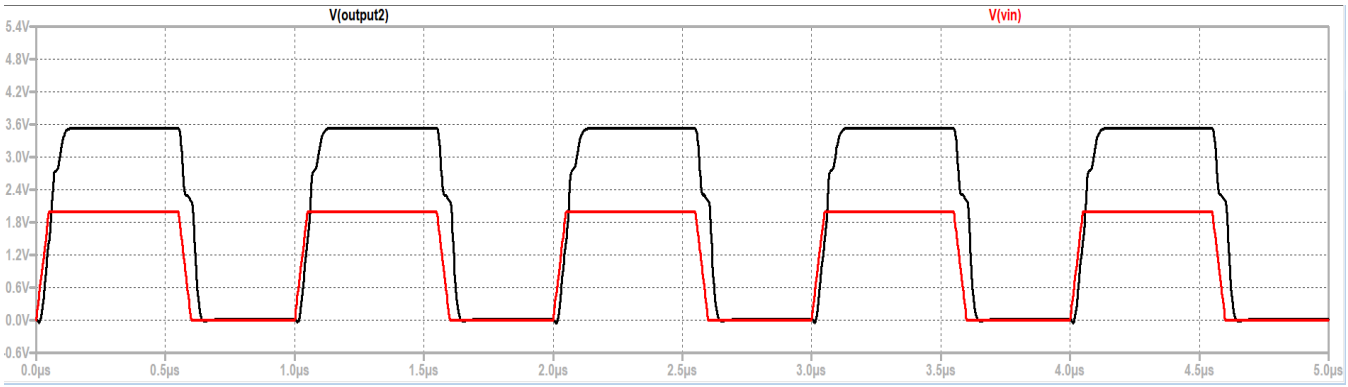
As increasing the frequency, the attenuation starts due to finite bandwidth, which is a linear phenomenon that creates a slew rate, which is non-linear distortion. Also, increasing frequency, the output become more attenuated wave. In LTspice, multiplying the input signal with the ideal amplification, which is 2 so that it matches with the output. See figure (14) for the input and output with 1kHz, 10kHz, and 1MEG is becoming more attenuated, however, changing to square wave and zooming the wave, there is an attenuation that the slew rate can be calculated; see figure (15) showing the zooming part for attenuation for sine wave and figure (16) for the square wave change and figure (17) for the wave that zoomed for slew rate calculation; from the figure (17) it can be seen from the cursors, the slew rate, which is the slope is about 34 V/us. The formula of the slew rate can be used here; the formula is SR= ΔV/Δt = 34 V/us



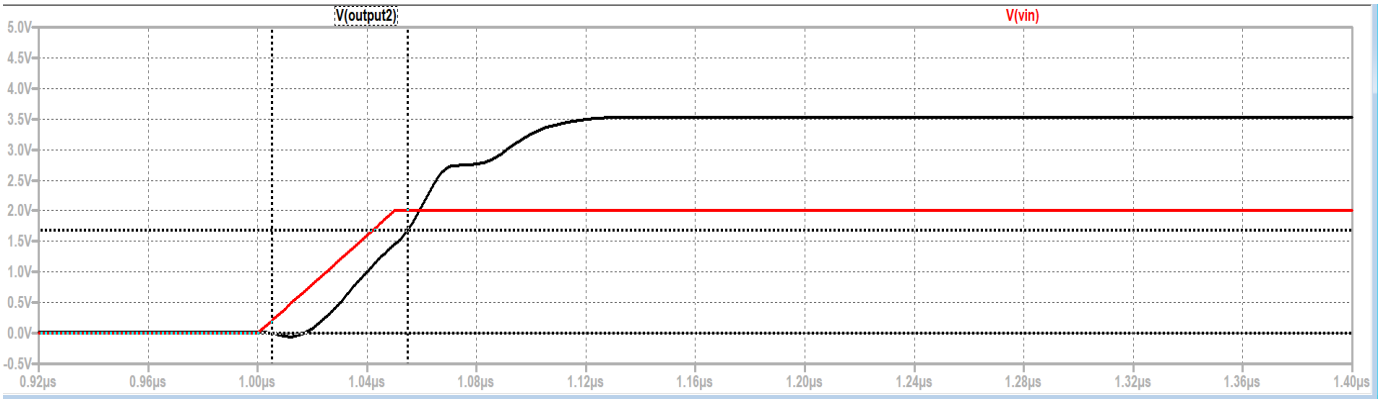
Figure(14) The waves with 1kHz, 10kHz, and 1MEG frequencies.



Figure(15) The Plot for the Attenuated waves.



Figure(16) Square Waves for Slew Rate.



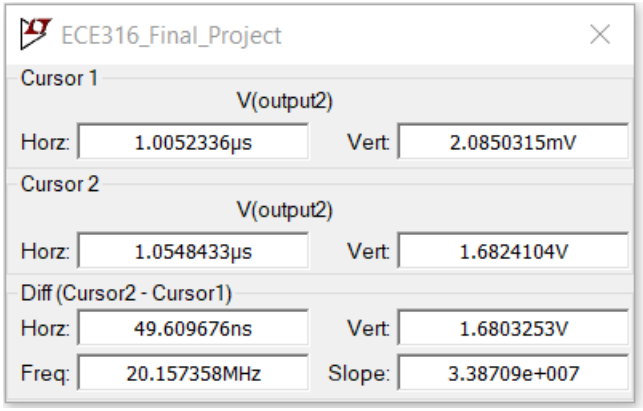


Figure (17) Slew Rate Wave and Cursors.

In Lab Experiment:

The CFOA is built in the lab using 24 BJT transistors; 12 of them are PN2222, and the other 12 are 2N5087; NPN and PNP respectively. The circuit installed in the breadboard with 24 transistors; see figure (18) for the physical built circuit. As seen in the breadboard, the upper half including the 12 PNPs and the lower half includes 12 NPNs. V_{CC} is the red wire runs through the positive trail (red rails) in the upper trail of the breadboard and the positive trail in the first right in the breadboard. The negative V_{EE} is the red wire runs through the positive trail (red rails) in the middle and lower trails of the breadboard. The ground is the green wire that runs through the negative rail in the middle of the breadboard, is used to ground the two inputs during the operation of the DC circuit and ground the voltage divider during the feedback gain of 2.

The output is in the middle of the right-hand side of the breadboard, which is the brown wire connected to the feedback white wire coming from the voltage divider.

Setting up the experiment after building the circuit; the experiment needs oscilloscope, power supply, function generator, and digital multimeter (DMM). The oscilloscope is needed to plot the waves and finding the slew rate; the power supply needed to supply the circuit with + 5V and -5V for V_{CC} and V_{EE} respectively; the function generator to provide an AC signal and to plot its output on the oscilloscope; the DMM needed to measure the voltages throughout the circuit to see if the transistors are active region or not.

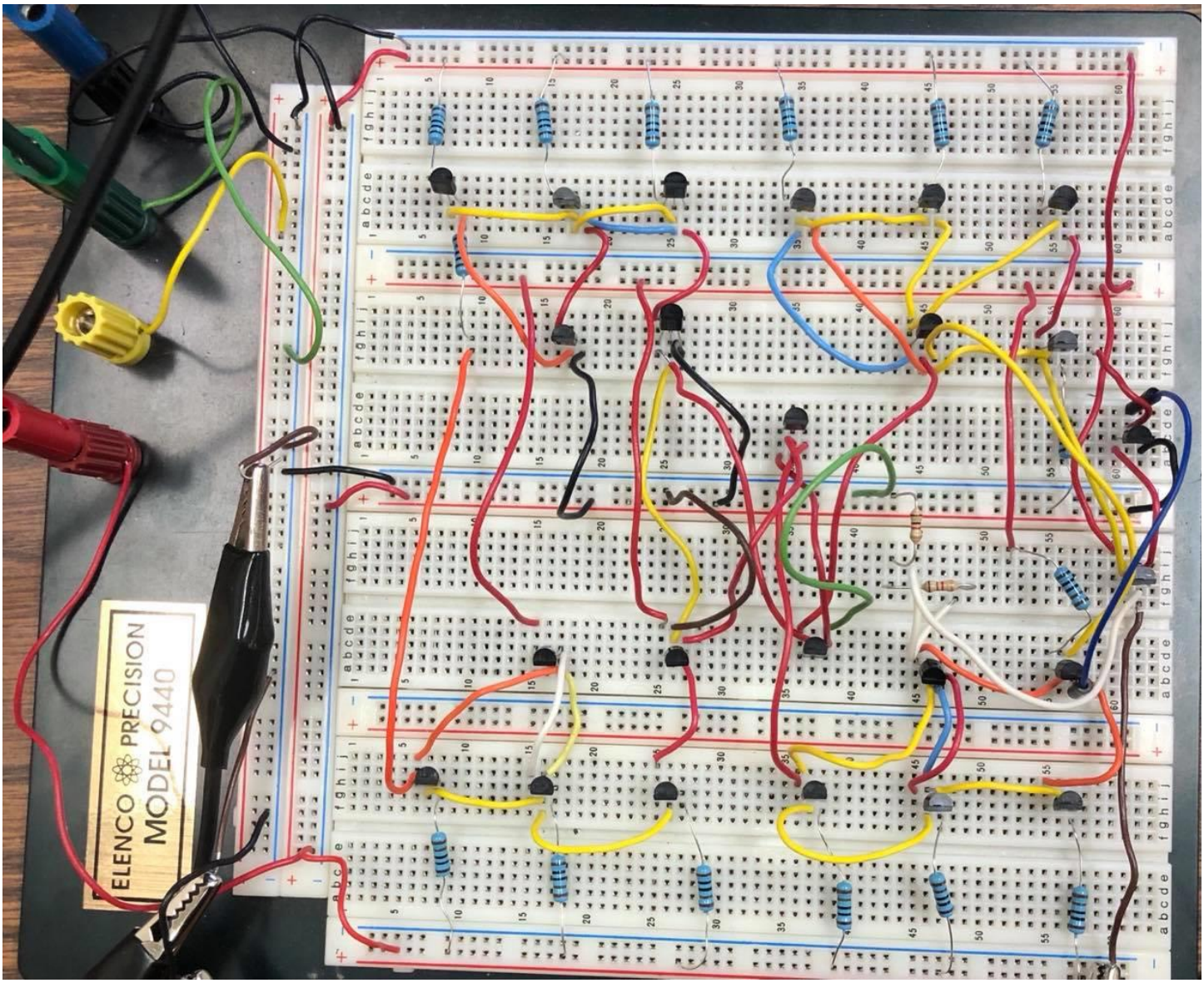
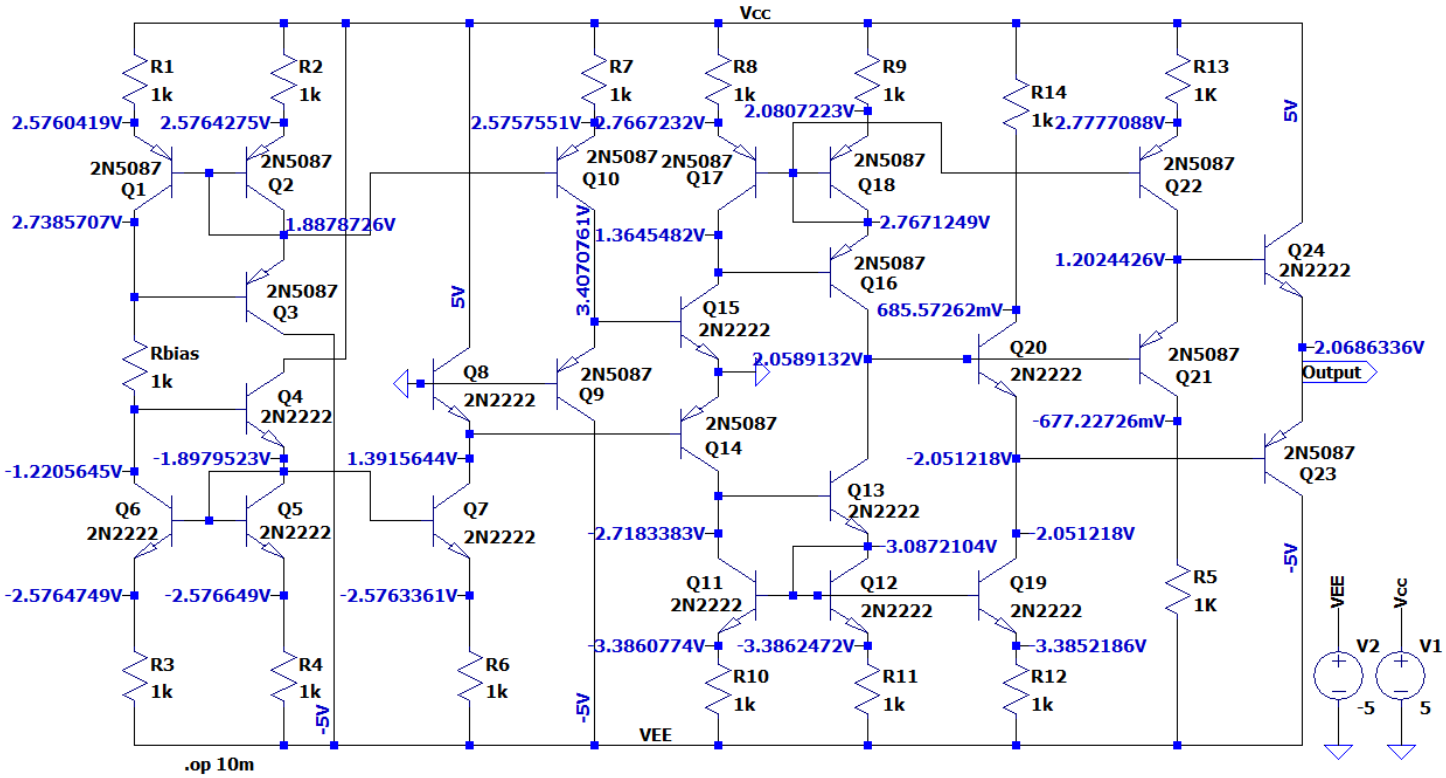


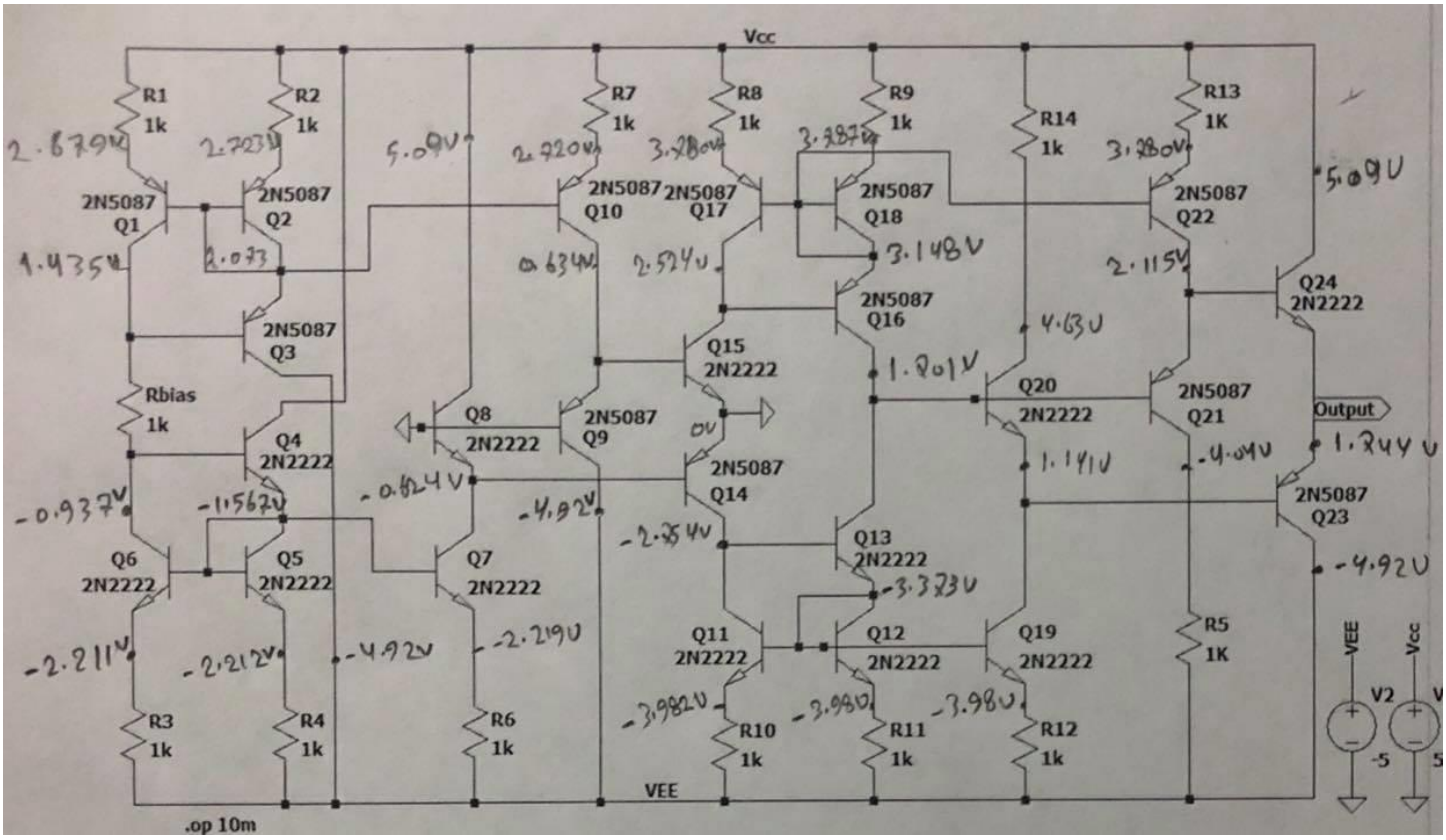
Figure (18) The Circuit of CFOA Built in the Lab.

Data and Analysis:

From simulation for operating points to show the voltages throughout the circuit and the voltages were taken in the lab are close, but there is some difference. The difference might be due to the simulation, which is not accurate because the transistors used in the lab might have different parameters than the LTspice along with the noise accruing in the lab. See figure (19) for the voltages throughout the CFOA circuit from LTspice, and figure (20) the voltages were taken in the lab; accordingly, the comparison can be made, and the circuit works correctly as expected.



Figure(19) Operating Points from LTspice.

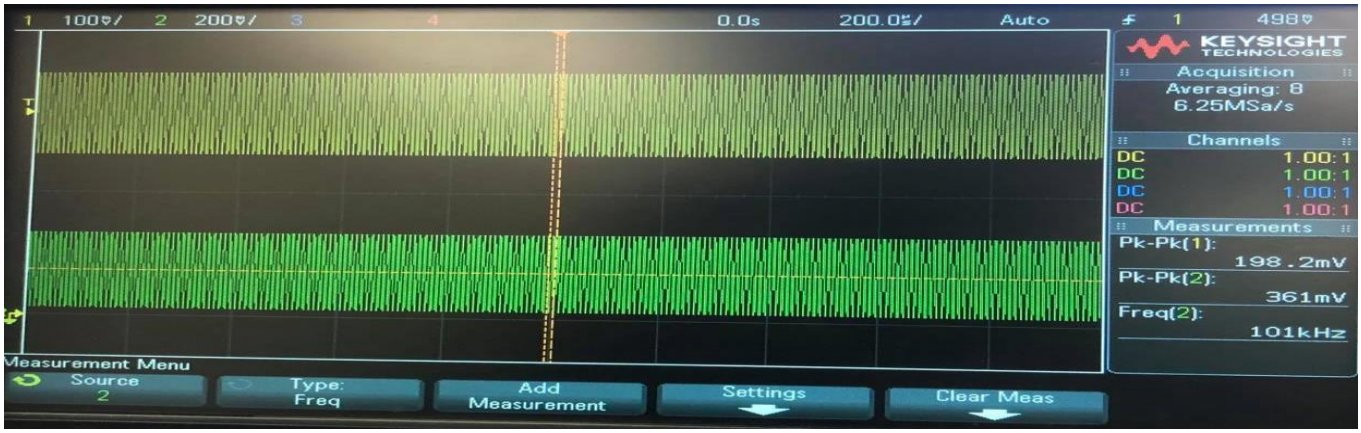


Figure(20) In Lab Voltages.

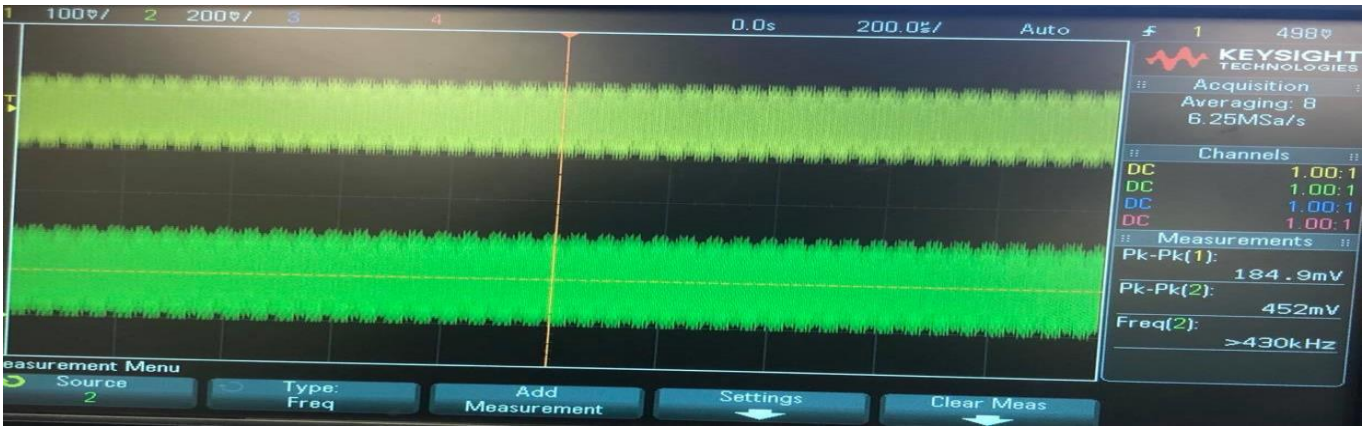
The following four oscilloscope captures in figure (21) below shows the input and output sinusoidal waves with 200mV input and varying the frequency from 1kHz. 10kHz, 100kHz and to high frequency. It shows that the waves are still having a gain of 2 until 100kHz, but the oscilloscope doesn't fit the wave for high frequency for more than 430kHz. However, after fixing the probes of the oscilloscope, it was seen that the wave getting worse and the gain shows a rapid reductions as the frequencies get higher for more than 10MHz, which is the cutoff frequency of CFOA; see figure (22) for a. the Excel data table for frequency response and gain, and b. the plot of gain vs frequency. The gain in dB was calculated using the formula $20*\log(V_{out}/V_{in})$.

(a)

(b)



(c)



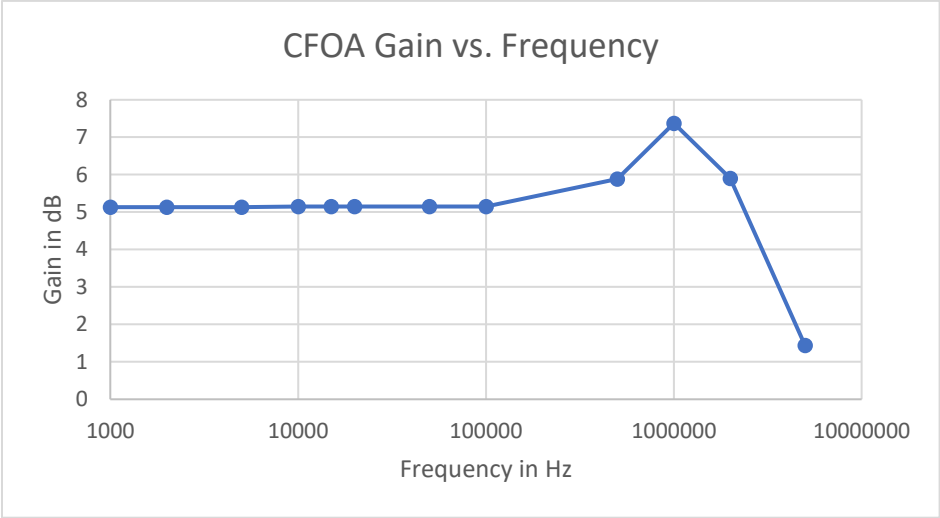
(d)

Figure (21) CFOA Sinusoidal Waves of Oscilloscope Capture:

a. 10kHz. B. 10kHz. c. 100kHz. d. >430kHz.

Frequency (in Hz)	V_{out}(in mV)	V_{in} (in mV)	Gain(V_{out}/V_{in})	Gain(dB)
1000	361	200	1.805	5.1295
2000	361	200	1.805	5.1295
5000	361	200	1.805	5.1295
10000	360	199	1.809	5.1490
15000	360	199	1.809	5.1490
20000	360	199	1.809	5.1490
50000	360	199	1.809	5.1490
100000	360	199	1.809	5.1490
500000	372	189	1.968	5.8816
1000000	430	184	2.337	7.3730
2000000	290	147	1.973	5.9016
5000000	21	17.8	1.180	1.4360

(a)



(b)

Figure (22) a. Data Table for Frequency Response and Gain. b. Plot of Gain vs Frequency.

Other Important Measurement:

a- Square Wave:

Setting the function generator to 2V with square wave, the oscilloscope shows the output of CFOA when a DC pulse is used as an input signal at allow frequency 1kHz; the square wave looks better than the higher frequency when changing to 100kHz. The square wave at 100kHz still has a gain of 2 and it has some distortion, but still not worse than increasing the frequency to 1MHz. The square wave at 1MHz changed and it became no longer a square and the gain increased to more than 2. See figure (23) for the square waves of 1KHz, 100kHz, and 1MHz below. Also, see appendix B for zoomed 1MHz square wave.

(a)

(b)

(c)

Figure (23) Square Wave for CFOA at: a.1KHz. b.100kHz. and c.1MHz.

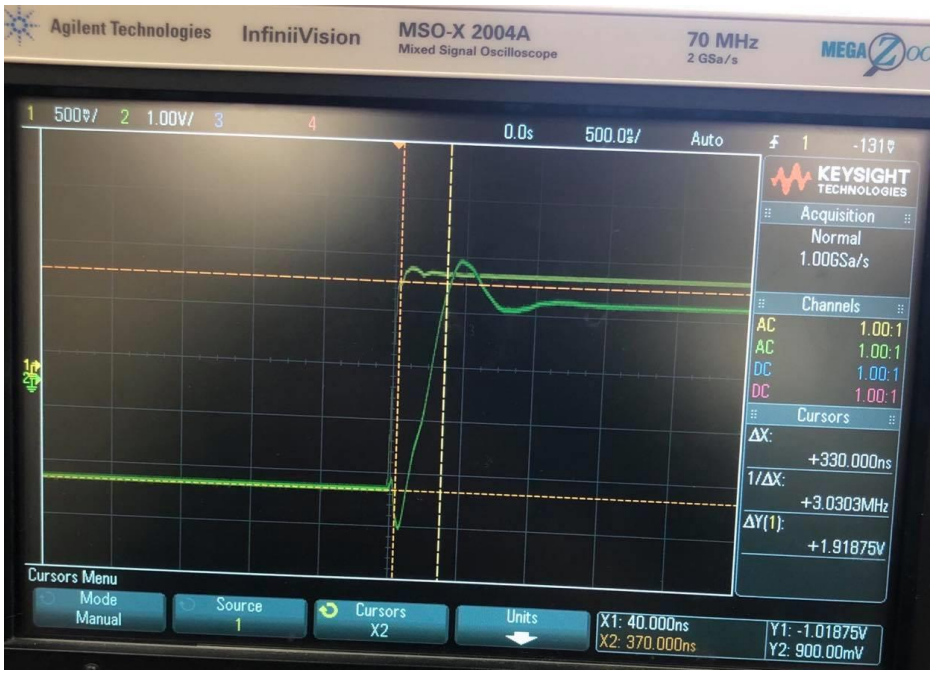
b- Slew Rate and Propagation Delay:

The slew rate is used to determine how fast the amplifier is; the ideal slew rate is usually 30V/us. In this part of experiment, the slew rate was obtained from the oscilloscope using the cursors to calculate the slope of the voltage difference per time difference. The slew rate obtained in the lab is different from the slew rate obtained from simulation. However, the output has some confusing rising edge and falling edge, which made the calculation of the slew rate little complicated. Even though with the complication of rising and falling edge, the slew rate is obtained by placing the cursor 1 to the 10% of the first rise and 90% from the peak. See figure (24a) for the slew rate from the oscilloscope for the first rise; the slew rate happened to be:

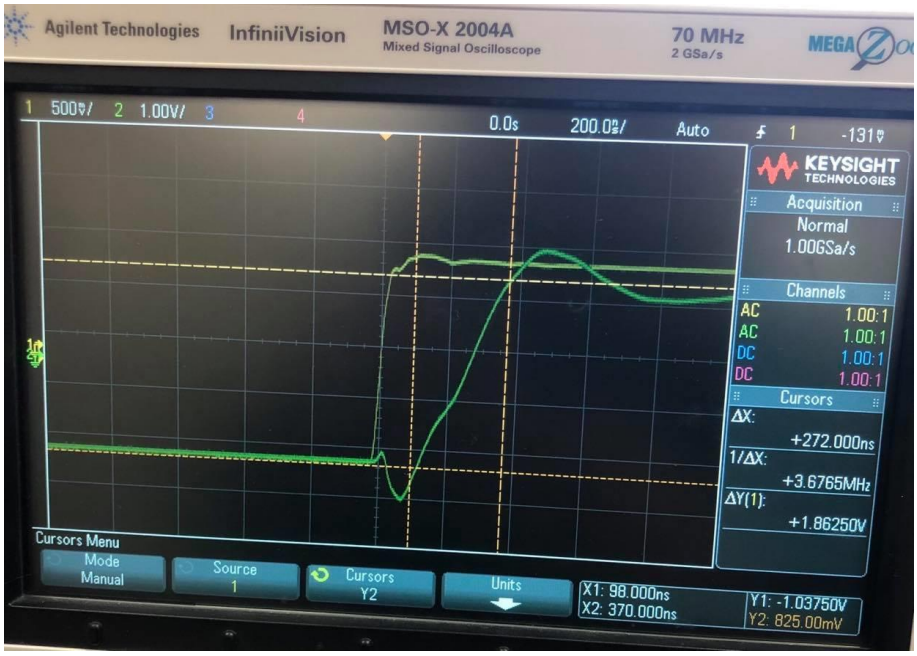
$$SR = \Delta V/\Delta t = \Delta Y/\Delta X = 1.91875V/0.330us = 5.81V/us$$

and see figure (24b) for the slew rate from the second rise; the slew rate happened to be:

$$SR = \Delta V/\Delta t = \Delta Y/\Delta X = 1.86250V/0.272us = 6.85V/us$$



(a)



(b)

Figure (24) a. Slew Rate from First Rise. b. Slew Rate from Second Rise.

The circuits usually have delay because of capacitance inside the transistors and other parasitic elements and they are ignored during the simulation. The propagation delay describes the amount of time between the input and output and is calculated at 50% of input-output transition.

There is two-time difference, which are rise and fall. The rise time (t_r) is the time during transition, when output switches from 10% to 90% of the maximum value. The fall time (t_f) is from 90% to 10% of the maximum value; see the explanation in figure (25). Many designs prefer 30% to 70% for

rise time and 70% to 30% for fall time. It varies according to the design. It is calculated using the equation $t_p = (t_{PHL} - t_{PLH})/2$.

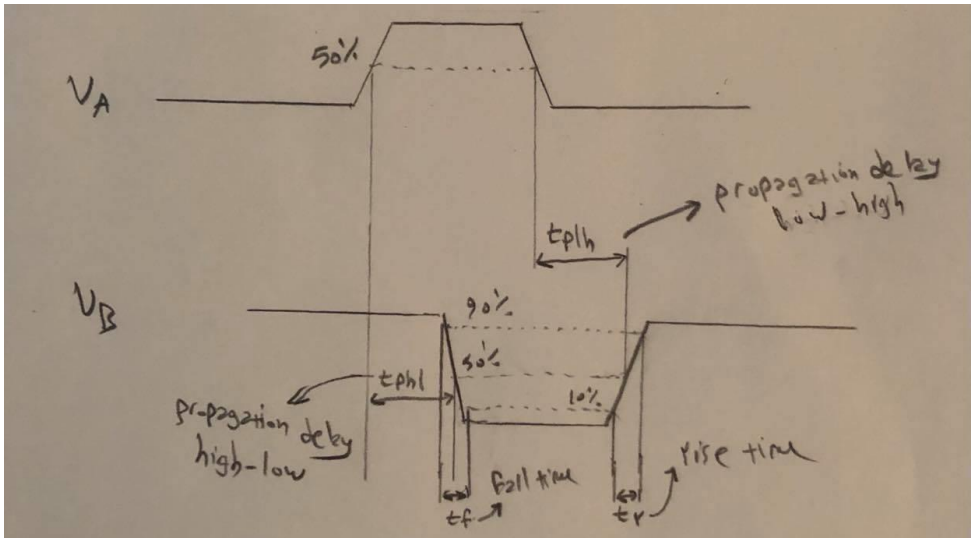


Figure (25) Propagation Delay.

c- Noise Margin:

Noise margins is the amount of noise that the transistor can handle or withstand without causing problems in the operation of the circuit. In other words, it is a safety margins that prevent the circuit from producing erroneous outputs in the presence of noisy inputs. In CFOA design, the noise margin is not a big deal since the CFOA is efficient and has less noise. See figure (26) representation of noise margins.

Noise margins are defined for low and high input levels using the following equations:

NM_L(noise margin low) = $V_{IL} - V_{OL}$

NM_H(noise margin high) = $V_{OH} - V_{IH}$

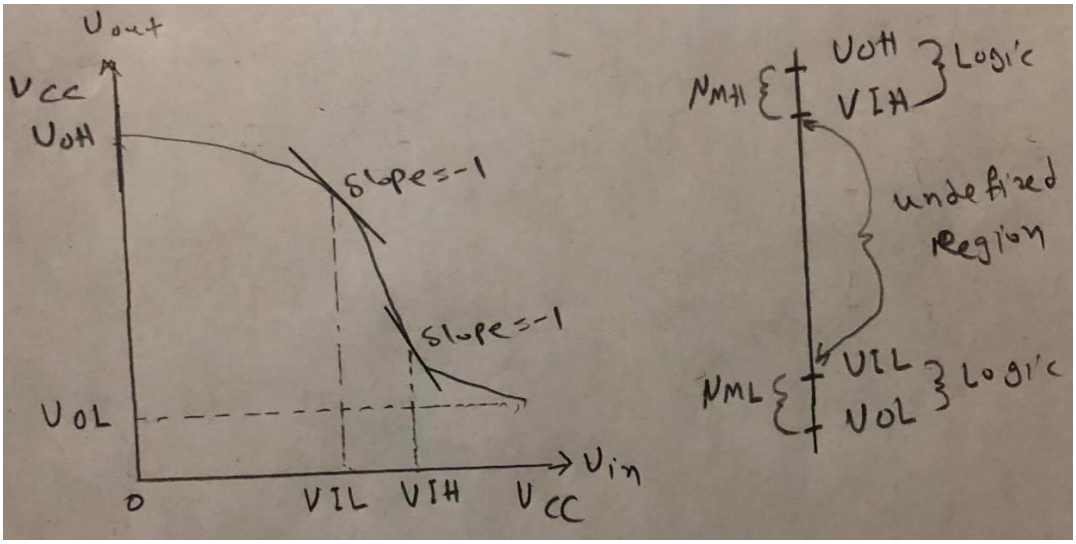


Figure (26) Representation of Noise Margin.

Discussion:

The project is interesting and beneficial for understanding the modern amplifier circuits. However, some problems during the experiment encountered like connecting the pins of the transistors but was simply resolved by the reading the datasheet for NPN2222, and PNP5087.

The plots are clear and confirmed the circuit works correctly. The gain of 2, the correct values of the voltages, and the slew rate were obtained.

Some additional research about CFOA was conducted during the project. The CFOA operates faster and efficient than the VFOA because it operates in current feedback that prevents the effect of stray node capacitances. It has several advantages comparing to VFOA; for example, the CFOA has a high slew rate, large bandwidth that relatively independent of the closed loop gain, and lower distortion; Also, CFOA circuits has less components to implement like resistors, which makes the circuit looks neat and makes it better design.

Design issues was mostly about the stability; for stable operation, the phase margin must be high. The phase margin can be obtained using high current even though high current means more power consumption. Also, unbalanced input stage due to CMRR, which tends to reduce precision, and high-speed input stage that can distort the signal if a slow output stage is connected.

Conclusion:

In conclusion, the final project of CFOA with a gain of 2 is designed, simulated, implemented, and analyzed. The circuit is simulated using LTspice and the plots and the resulting values appear as expected.

The design includes designing biasing stage, input stage, current mirrors, transimpedance, and output stage. The circuit was analyzed to find the DC operating points, frequency response, and slew rate to see how fast the amplifier can operate.

The whole project is succeeded and is met the objectives of the project requirement, which is designing, simulating, building, and analyzing the CFOA circuit. In addition, time delay and noise margin are mentioned briefly in the other important measurement since it wasn’t required for this project because the CFOA has less impact toward these two factors.

Appendices

A. DC operating points for current values.
B. A zoomed square wave of 1MHz.

A. DC operating points for current values:

```
                --- Operating Point ---

Ic(Q11):        0.0016059      device_current
Ib(Q11):        8.01875e-006   device_current
Ie(Q11):        -0.00161392    device_current
Ic(Q6):         0.00241145     device_current
Ib(Q6):         1.20718e-005   device_current
Ie(Q6):         -0.00242353    device_current
Ic(Q7):         0.00241166     device_current
Ib(Q7):         1.20075e-005   device_current
Ie(Q7):         -0.00242366    device_current
Ic(Q8):         0.00239393     device_current
Ib(Q8):         1.14864e-005   device_current
Ie(Q8):         -0.00240542    device_current
Ic(Q15):        0.00313734     device_current
Ib(Q15):        1.57429e-005   device_current
Ie(Q15):        -0.00315308    device_current
Ic(Q4):         0.00243588     device_current
Ib(Q4):         1.15538e-005   device_current
Ie(Q4):         -0.00244743    device_current
Ic(Q5):         0.0024112      device_current
Ib(Q5):         1.2153e-005    device_current
Ie(Q5):         -0.00242335    device_current
Ic(Q12):        0.00160568     device_current
Ib(Q12):        8.07141e-006   device_current
Ie(Q12):        -0.00161375    device_current
Ic(Q13):        0.0016217      device_current
Ib(Q13):        7.82886e-006   device_current
Ie(Q13):        -0.00162953    device_current
Ic(Q20):        0.00159292     device_current
Ib(Q20):        7.89987e-006   device_current
Ie(Q20):        -0.00160082    device_current
Ic(Q19):        0.00160702     device_current
Ib(Q19):        7.75766e-006   device_current
Ie(Q19):        -0.00161478    device_current
Ic(Q24):        0.00177245     device_current
Ib(Q24):        8.71636e-006   device_current
Ie(Q24):        -0.00178116    device_current
Ic(Q14):        -0.00161373    device_current
Ib(Q14):        -6.23785e-006  device_current
Ie(Q14):        0.00161997     device_current
Ic(Q9):         -0.0023905     device_current
Ib(Q9):         -8.60123e-006  device_current
Ie(Q9):         0.0023991      device_current
Ic(Q3):         -0.00243392    device_current
Ib(Q3):         -8.55414e-006  device_current
Ie(Q3):         0.00244248     device_current
Ic(Q1):         -0.00241445    device_current
Ib(Q1):         -9.50501e-006  device_current
Ie(Q1):         0.00242396     device_current
Ic(Q2):         -0.00241393    device_current
Ib(Q2):         -9.647e-006    device_current
Ie(Q2):         0.00242357     device_current
```

```
Ic(Q10):        -0.00241484    device_current
Ib(Q10):        -9.40069e-006  device_current
Ie(Q10):        0.00242424     device_current
Ic(Q16):        -0.00162275    device_current
Ib(Q16):        -0.000912804   device_current
Ie(Q16):        0.00253555     device_current
Ic(Q18):        -0.00222399    device_current
Ib(Q18):        -8.88037e-006  device_current
Ie(Q18):        0.00223287     device_current
Ic(Q17):        -0.00222453    device_current
Ib(Q17):        -8.74415e-006  device_current
Ie(Q17):        0.00223328     device_current
Ic(Q21):        -0.00191279    device_current
Ib(Q21):        -6.84965e-006  device_current
Ie(Q21):        0.00191967     device_current
Ic(Q22):        -0.00192836    device_current
Ib(Q22):        -0.000293936   device_current
Ie(Q22):        0.00222228     device_current
Ic(Q23):        -0.00177496    device_current
Ib(Q23):        -6.19997e-006  device_current
Ie(Q23):        0.00178117     device_current
I(R5):          0.00191279     device_current
I(R14):         0.00159292     device_current
I(R13):         0.00222229     device_current
I(R12):         0.00161478     device_current
I(R11):         0.00161375     device_current
I(R10):         0.00161392     device_current
I(R9):          0.00223287     device_current
I(R8):          0.00223328     device_current
I(R7):          0.00242424     device_current
I(R6):          0.00242366     device_current
I(Rbias):       0.00242301     device_current
I(R4):          0.00242335     device_current
I(R3):          0.00242353     device_current
I(R2):          0.00242357     device_current
I(R1):          0.00242396     device_current
I(V1):          -0.0221554     device_current
I(V2):          0.0206252      device_current
```

B. Zoomed square wave of 1MHz: