Power Management System Design for Power Supply and Battery Charger Controller

By

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Senior Design Progress Report

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Abstract

Solar panel, battery charger controller, and power supply are required to feed the load system. The system is battery-powered and uses solar panels for recharging, making it self-sustaining and suitable for deployment in remote locations using solar panel to charge a battery to make sure the system is powered with no outage. In this project, it is required to design and implement an electrical power system that collects solar energy via PV-panels, stores it in battery banks, and delivers power to the load. After the completion of this project, the system would be designed and implemented using Altium Designer for PCB and the system would be powered 100% from solar and would be self-contained and self-sustained.

Introduction

Background

The system will be fed from a solar panel and rechargeable battery through a power supply. The solar power will be controlled by a charger controller to charge the battery and from the battery to a buck converter of two output voltages 3.3V for Network Manager and 4V for GSM module. The current of the power supply can be programmed up to 5A. For this design, only 600mA is needed as maximum current. The purpose of having our system to be powered 100% from solar is to make the system self-contained and self-sustained.

The hardware design will be implemented separately at first. The network manager, GSM module, power supply, and charger controller are each a separate design. They will be designed using Altium Designer by creating a layout PCB. The PCB will be soldered and tested to achieve the desired purpose. After getting all hardware design implemented and worked, the motherboard will be designed and implemented as one PCB board including those separate designs. Also, an enclosure will be

designed to include our system; we probably be using a Solidworks software to create the enclosure and print it using see through material if possible.

Problem Statement

The system will be fed from the solar panel and rechargeable battery to ensure the power is available to the system load at any time.

Power Management System Design

The system needs two output voltages 3.3V for Network Manager and 4V for GSM module; Also, the maximum current of 600mA is needed. The power supply is a DC-DC buck converter is fed from a rechargeable battery and straight from solar to DC-DC power supply. The battery must be charged from a solar panel, which is controlled by a charge controller. See the block diagram in Figure 1 below for overview of solar charge controller and power supply.

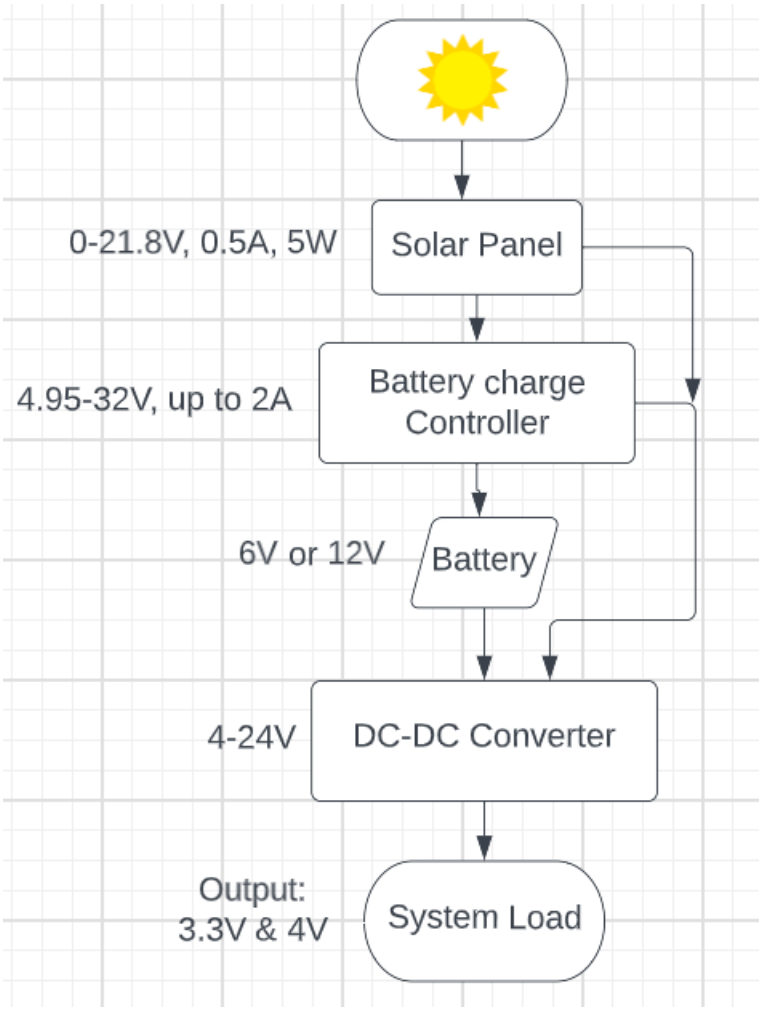

Figure 1 Power Supply Block Diagram

The block diagram above shows the starting of the system which is the solar panel of 21.8V and 0.5A to charge the battery through charge controller; the battery voltage will be bucked to 3.3V and 4V from the DC-DC converter. The system might need more two outputs one 5V for the Bluetooth and the other one will be for future extension. The two outputs are connected to the load to feed the system. The components selection of this design will be discussed next.

Main Power Management Components selection

1- **ECO-WORTHY 5W Solar Panel:**

Selecting the Specification for solar panel to feed the system based on maximum current of 0.6A to charge a battery of 6V up to 12V; this solar was chosen at random and we might need a bigger size to be compatible to charge a 2.9Ah battery. The table below shows the specification of the solar panel.

Description	Value
Rated Power	5W
The open circuit voltage V_{oc}	20.6V
Working Voltage (V_{op})	17.3V
Short circuit current (I_{sc})	0.69A
Working current (Iop)	0.58A
Output Tolerance	±3%
Temperature range	-40℃to +80℃

2- Battery Charge Controller

The Power Tracking 2A Battery Charger for Solar Power LT3652 was chosen based on its specification and features. The LT3652 is a step-down battery charger that operates from a 4.95V up to 32V input voltage range. It provides a constant-current and constant-voltage charge, with maximum charge current externally adjustable up to 2A. The charger employs a 3.3V float voltage feedback reference, so any desired battery float voltage up to 14.4V can be adjustable with a resistor divider [1]. As mentioned, the selection was made because it has the input voltage range and output charging range compatible for what the solar panel, rechargeable battery, and DC-DC converter need to be operated. Besides the voltage operation range and charging range, this chip has temperature sensing to protect the battery from high temperature and overvoltage protection to protect the battery from over charging while under-voltage

protection stops the battery from being discharging beyond its capacity. Plus, the last reason of selecting this chip is for the maximum peak power tracking MPPT, which is a method to keep the output of the solar panels as high as possible regardless of environmental factors such as varying temperature or weak sun ray.

3- **Dual, 2-Phase Synchronous Step-Down Switching Controller LTC3850**

LTC3850 is a high performance dual synchronous step-down switching regulator controller that operates in an input range from 4V up to 24V. The selection of this particular chip based on its features that are needed for this design; it includes ±1% 0.8V output voltage accuracy. These two outputs are adjustable by resister divider are needed to power the Network Manager and GSM module. Also, high efficiency up to 95%, DCR current sensing, and fixed frequency from 250KHz up to 780KHz [2].

Power Supply Design

The DC-DC converter was our priority to design and implement before the battery charger. The design was started by obtaining the information of the load that needed to be powered. The system load needs to output power one is 3.3V for Network Manager and 4V for GSM module; the maximum current needed is 0.6A. The LTC3850 step-down buck converter was the chosen chip to achieve the output to feed the system. The design started with simulation and then is implemented in PCB.

Design Calculation and Components Selection

The instructions for the design and components selection were followed by the datasheet, which provides the formula for calculating the output voltage, current, and other parameters. The maximum current used in the calculation is 2A and can exceeds this value if needed. The calculations are as follow:

1- Setting The Output Voltage (Pin V_{FB1} and Pin V_{FB2} are in pin 6 and 8)

These pins are called error amplifier feedback inputs; they receive feedback voltage from external resistive dividers; setting R_A to be 20KΩ and R_B can be found from the equation below.

V_{out} = 0.8V(1+R_B/R_A) = 3.3V = 0.8V(1+RB/20kΩ) = 63.4kΩ

2- Setting R_{sense} (Sense$^+$ and Sense$^-$ are Pin 2, 3 and Pin 11, 12)

These pins are current sense comparators which are connected to the output with a resistor to sense the current. To calculate the sense resistor values for two outputs using the equation below:

R_{sense} = $V_{sense(max)}$/I $_{load(max)}$+ΔI_L/2 =40mV/5A+1.5/2) =0.008Ω

$V_{sense(max)}$ is Maximum Current Sense Threshold can be found in the electrical characteristics in datasheet to be 40mV. I $_{load(max)}$ is the maximum load current assuming 5A. ΔI_L is peak to peak ripple current.

3- Inductors Selection

The value of the inductor is calculated and selected based on 1.75A that is 35% max. current ripple assumption of 5A; the highest value of ripple current occurs at the maximum input voltage using the formula below to obtain the value of the inductor.

$$L = \frac{V_{out}}{f \times \Delta I_{L(max)}} \times \left(1 - \frac{V_{out}}{V_{in(nom)}}\right)$$

$$L1 = \frac{3.3}{500KHz \times 1.75} \times \left(1 - \frac{3.3}{12}\right) = 2.73\mu H \approx 2.2\mu H$$

$$L2 = \frac{4}{500KHz \times 1.75} \times \left(1 - \frac{4}{12}\right) = 3.05\mu H \approx 3.3\mu H$$

For 3.3V output, the inductor is L1= 3.3µH since the calculated value is 2.73µH and the next highest standard value is 3.3µH. The output of 4V will require 3.3µH since the calculated value is 3.05µH.

Based on the value of the inductor, the ripple at nominal input voltage 12V will be:

$$\Delta I_{L(nom)} = \frac{V_{out}}{f \times L} \times \left(1 - \frac{V_{out}}{V_{in(nom)}}\right) = \frac{3.3}{500kHz \times 3.3\mu} \times \left(1 - \frac{3.3}{12}\right) = 1.45\ A$$

So, the ripple is 1.45A which is 29% ripple and channel 2 will have the same ripple since it has the same inductor. This is the maximum peak current of the inductor adding the DC value plus 50% of 1.45A of the ripple found. The typical DCR values of the inductors are chosen based on the suggestion of the datasheet; the suggestion is based on the less power loss; the range are given to "30mΩ DCR_{MAX} at 20°C and at 100°C, the estimated maximum DCR values are 26.4mΩ and 39.6mΩ"[7].

4- MOSFET Selection

The selection of the N- Channel MOSFETs is optional but has some hints from datasheet based on the $R_{DS(on)}$. The datasheet suggests a MOSFET with low $R_{DS(on)}$. The one was available is SI4936BDY-T1-E3 which has $R_{DS(on)}$ = 40mΩ, but the datasheet suggested 18.7mΩ which is out of stock. Their selection was based on power dissipation. The power loss is predicted from the DC resistance; since the two MOSFETs have 40mΩ each and R_{sense} is 8mΩ, the total is 48mΩ; then, the power loss for 3.3V and 1A current load will be I^2R = 1A×48mΩ = 48mW. This power loss is much less than the datasheet is calculated because the calculate for more current load.

5- Input capacitor and output capacitors selection

C_{in} was chosen for RMS current rating of at least 2A based on the maximum designed current and also the datasheet suggested that. CAP ALUM POLY 22UF 20% 35V SMD is the capacitor for the input and has 2.3A RMS current rating and 50mΩ ESR (Equivalent Series Resistance).

C_{out} is chosen based on ESR; the ESR is 0.05Ω or less for low output ripple. The maximum ripple voltage will be high at maximum input voltage. The output voltage ripple due to ESR can be calculated by the formula below provided in datasheet.

$V_{OutRipple} = R_{ESR} \times \Delta I_L = 0.05 \times 1.5 = 75mV$

6- Diodes selection

The Schottky diodes selection is optional; the diodes are connected from pins INTVCC which are pins on the chip that function as internal 5V regulator output that control the circuits that are powered from this regulator. These pins INTVCC are decoupled with 4.7µF capacitor with low ESR TO PGND pin. One of the importance of these diodes are to conduct between the two MOSFETs during the dead time off and on; means to prevent the bottom diodes from turning on and storing charge from the capacitor during the time that requires a reverse recovery to increase the efficiency at high Vin and when the SW pin is low. Base on the datasheet "A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance"[2]. The diode was selected to be CMDSH-3TR Diode Schottky 30V 100mA Surface Mount SOD-323. The DC reverse breakdown is greater than Vin maximum.

LTSpice Simulation for Power Supply LTC3850 Buck Converter

The simulation was done using LTSpice; as seen in Figure 2 below, the schematic of the circuit was designed based on the typical application from datasheet; the component was chosen after the required calculation according to datasheet. The output 1 and 2 is 3.3V with two capacitors of 47µF and 220µF with ESR 2mΩ and 1mΩ and 4A RMS current rating since is selected based on ESR and RMS current rating of at least 2A; the V_{FB} pins are called VOSENSE in LTSpice are connected to resistive divider to obtain the output voltages of 3.3V and 4V as mentioned in design calculation section above. The input capacitor is 22µF with ESR of 2mΩ. The input is connected to the input pin of LTCC3850 chip with 0.1µF and 10Ω resistor. Also, the input is connected to the drain of the MOSFETs; the SW1 and SW2 pins are switching pins for the MOSFETs are connected to the source of the top MOSFETs and drain of the bottom MOSFETs to the inductors. There are two Schottky diodes are connected from INTVCC pin to

Boost pins and MOSFETS through decoupling capacitor to store and discharge during the time on and off that requires diodes to conduct the MOSFETs. The selection of these diodes is explained in design calculation and selection section above.

The $sense^+$ and $sense^-$ pins are the pins for current sense comparator are connected to Rsense with a decoupling capacitor from $sense^+$ and $sense^-$ pins. Also, the Track/SS pins are for soft-start inputs and output voltage tracking are connected with decoupling capacitor for just to smooth the simulation. BG1 and BG2 pins are bottom gate driver outputs to operate the gates of the bottom N-Channel MOSFETs and swings to see the maximum and minimum difference of the voltages between PGND and INTVCC. The TG1 and TG2 are directly connected to the top MOSFETs gates for voltage output swing equal to INTVCC pin. The I_{TH1} and I_{TH2} are current control threshold and error amplifier compensation to provide the feedback mechanism and compensation. In these pins I_{TH1} and $I_{TH2,}$ a voltage divider connected to the output provides a sample of the output voltage, which is compared to a reference voltage by the error amplifier. These pins are configured by connecting resistor and capacitor in series with the output of the error amplifier and a decoupling capacitor 1000pF for I_{TH1} and 100pF for I_{TH2} before the resistor R7 and R8 10kΩ and 13kΩ respectively. FREQ/PLLFLTR (Pin 28/Pin 25/Pin 26) is the Phase-Locked Loop's Low-Pass Filter is connected to this pin to vary the frequency of the internal oscillator. This pin is connected to external resistor of 3.16KΩ and 10KΩ to PGOOD pin through 100KΩ; this PGOOD pin is to indicate all of the voltages are within correct specification and that the chip may proceed to boot and operate when the output voltages are stable or not.

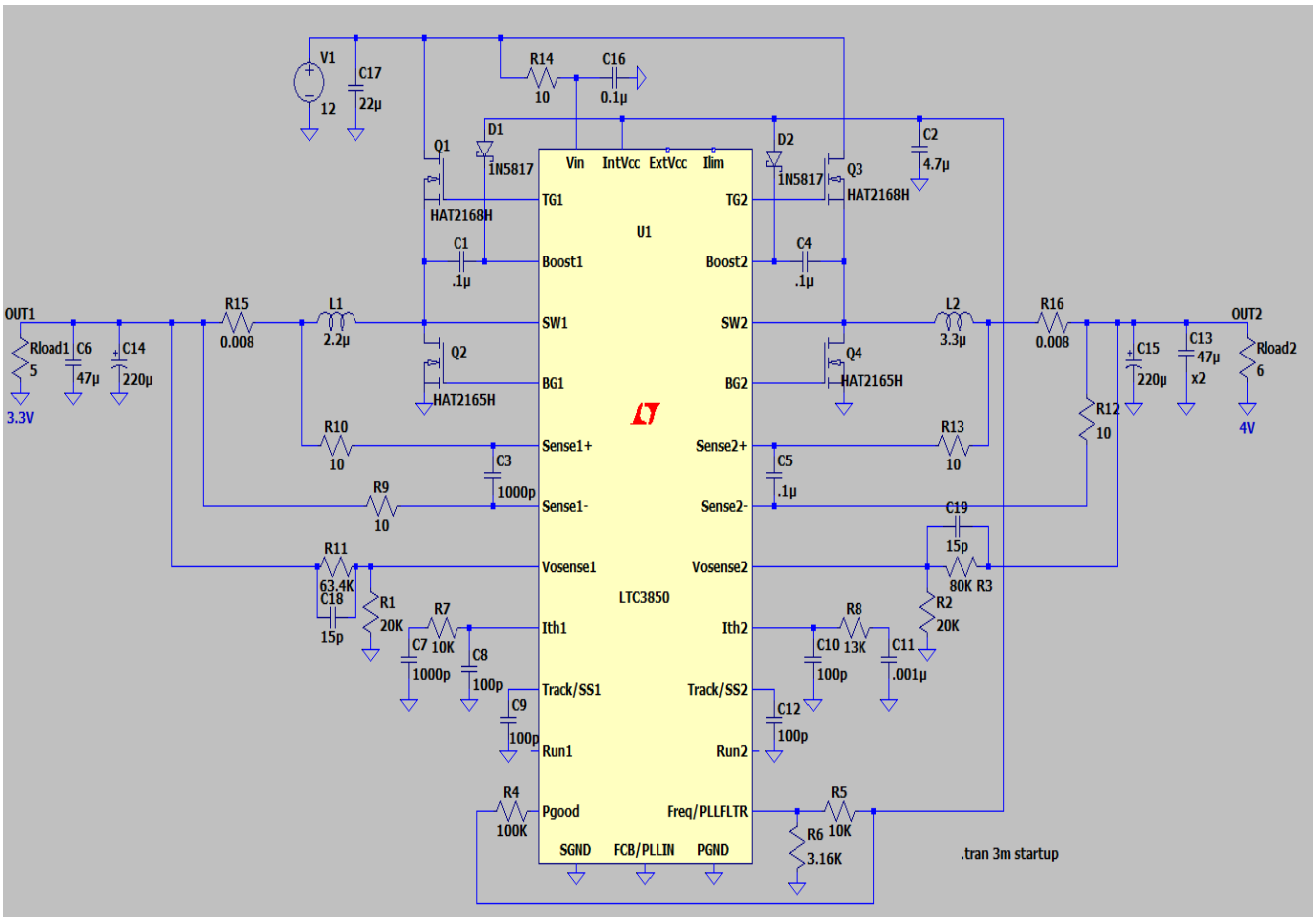

Figure 2 - LTSpice LTC3850 Circuit Schematic

The above schematic of the LTC3850 is simulated and the output voltages of 3.3V and 4V are obtained; see the plot below in Figure 3 that shows the output voltages and currents required to feed the system.

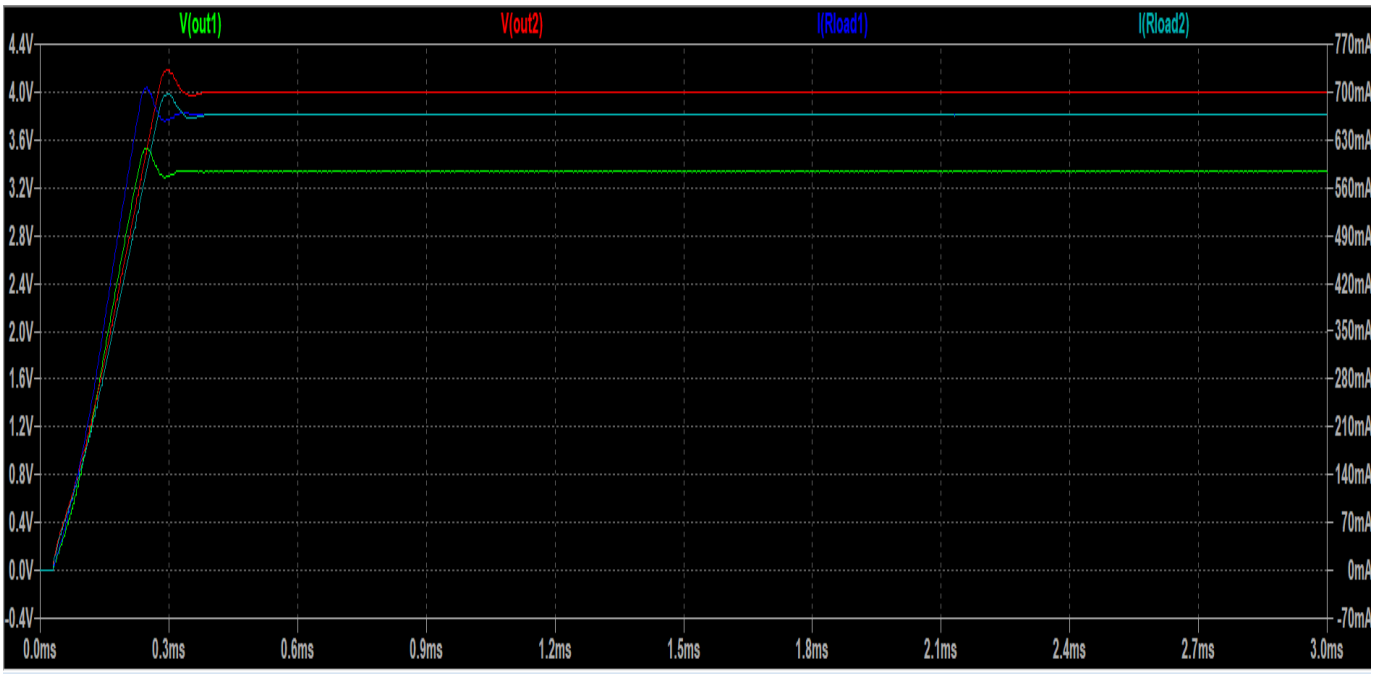

Figure 3 - LTSpice Simulation Plot for the Power Supply

Battery Charger Controller Design

The selection of a battery management system needed a consideration to ensure the battery is protected; so, the choice is Linear Technology LT3652 due to four important factors. First, temperature sensing that monitor the battery temperature to ensure that the temperature doesn't go out of the range and stop charging the battery until gets back to the proper temperature range; this will protect the battery. Second, over-voltage protection that protects the battery from over charging and over discharging. Third, power path is considered important to our system; the power path controls the power to select the source to feed the system between solar panel and battery. Finally, maximum peak power tracking (MPPT) which is an algorithm that included in charge controller used to obtain or to extract maximum available power from PV module under certain conditions. These factors are included in the selection of the chip LT3652 which is a power tracking 2A battery charger for solar power 1A solar panel powered 1-stage 12V lead-acid fast/float charger with input up to 16V and output up to 14.4V at 1A.

LT3652 Features

1- Input Range: 4.95V to 32V Including MPPT.

2- Programable charge rate up to 2A.

3- Resistor programmable float voltage up to 14.4V.

4- 1MHz fixed frequency.

5- 0.5% float voltage reference accuracy.

6- 5% charge current accuracy.

7- Operating junction temperature range -40˚C to 125˚C.

8- Absolute maximum voltage rating 40V.

LT3652 Design Calculation

The calculation will be done to charge an acid battery of 6V or 12V with float voltage of 14.4V and the solar panel of 0.5A.

1- Charge current programming

$R_1 = \frac{V_{sense}}{I_{charge(max)}} = \frac{100mV}{1A} = 100mV/1A = 100m\Omega$

Where R_1 is R_{sense}, and V_{sense} is the voltage drop will be created by sense resistor.

This sense resistor is connected to the inductor, which will be discussed next and to the output decoupling capacitors.

2- Inductor Selection

To select the inductor, the two considerations from datasheet will be applied. First, consideration is the ripple current created in the inductor. Second, its saturation current should be equal or exceeds the maximum peak current in the inductor. Using the following equation to calculate the inductor value.

$L = \frac{10 \times R_{sense}}{\frac{\Delta I_L}{I_{chg}(\max)}} \times V_{BAT(FLT)} \times \left[1 - \frac{V_{BAT(FLT)}}{V_{IN(MAX)}}\right]$

$L = \frac{10 \times 100m\Omega}{\frac{0.3A}{1A}} \times 14.4V \times \left[1 - \frac{14.4V}{21V}\right] = 15\mu H$

From the above calculation, the ripple current is set to 25% to 35% of the $I_{CHG(MAX)}$; by setting

$0.25 < \frac{\Delta I_L}{I_{CHG(MAX)}} < 0.35$.

The inductor is connected to SW pin which is the output of the charge switch. The SW pin is connected to BOOST pin via a capacitor of 1µF. the BOOST pin works as bootstrapped supply for operating range of 0V up to 8.5V; the capacitor voltage connected to SW pin is refreshed by rectifying diode with the cathode connected to BOOST pin and anode is connected to either the battery output voltage or the load source. However, the diode selected to refresh the decoupling capacitor from the battery with battery float voltages higher than 8.4V, a >100mA, is Zener diode can be put in series with the rectifying diode to prevent exceeding the BOOST pin operating voltage range.[1]

3- Battery Float Voltage Programming

The output battery float voltage $V_{BAT(FLT)}$ is programmed by external resistive divider from the battery pin to V_{FB} pin. The equivalent input resistance at V_{FB} pin is 174KΩ to compensate for bias current error and for $V_{BAT(FLT)}$ = 13.5V; so, to calculate the other resistor using the following equation.

$\frac{R_8}{R_5} = \frac{3.3V}{(V_{BAT(FLT)} - 3.3V)} = \frac{R_8}{R_5} = \frac{3.3V}{(13.5 - 3.3V)} = 0.32$

With R_8 = 100kΩ, $R_5 = \frac{R_8}{0.38} = \frac{100K\Omega}{0.38}$ = 312,500Ω ≈310kΩ

The divider equivalent resistance is

$R_5 \,||\, R_8$ = 100kΩ || 310kΩ = 75kΩ

R_7 = 250kΩ - 75kΩ = 175kΩ (Chose 175kΩ)

Where R_8 is R_{FB1} and R_5 is R_{FB2}, and R_7 is R_{FB3}.

4- MPPT System Implementation

To implement the MPPT system in order to produce the highest possible output of the solar panels, a LM234 sensor and a resistor divider are needed; based on the datasheet, the schematic of the MPPT is shown in the Figure 4 below. A MPPT system works to maintain the power as close to the peak power as possible. MPPT works by monitoring the output of the solar panels and changing the total resistance of the solar panels in order to produce the maximum output. See the implementation of the MPPT in the battery management system in the schematic in Figure 4 below.

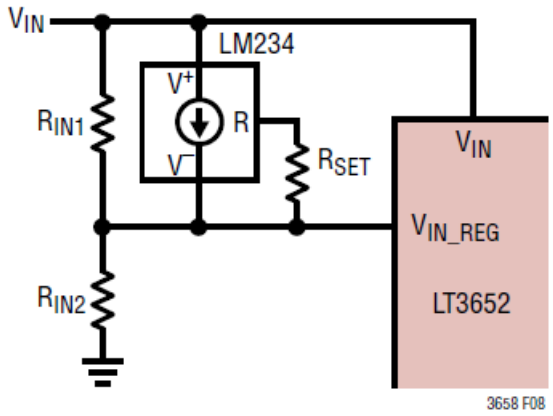

Figure 4 - MPPT Schematic Implementation

To calculate the values of RIN1 and RIN2, the following equation and example design should be used.

$R_{IN1} = -R_{SET} \bullet (TC \bullet 4405)$

$$R_{IN2} = \frac{R_{IN1}}{\left(\left\{\frac{[V_{MP(25°C)} + R_{IN1} \times (\frac{0.0674}{R_{SET}})]}{V_{IN_{REG}}}\right\} - 1\right)}$$

Where: TC = temperature coefficient (in V/°C), and

$V_{MP(25°C)}$ = maximum power voltage at 25°C

For example, the following characteristics for the solar panel are:

Open Circuit Voltage (V_{OC}) = 21.7V

Maximum Power Voltage (V_{MP}) = 17.6V

Open-Circuit Voltage Temperature Coefficient (V_{OC}) = –78mV/°C

These specifications can be inserted into the equations above setting R_{SET} = 1kΩ.

R_{IN1} = –1kΩ • (-0.078• 4405) = 344kΩ

$$R_{IN2} = \frac{344k\Omega}{\left(\left\{\frac{[17.6+344k\Omega\times(\frac{0.0674}{1k\Omega})]}{2.7}\right\}-1\right)} = 24.4k\Omega$$

In the LTSpice schematic in Figure 5 below shows the circuit simulated without MPPT system; the photocell diode is created to simulate the input voltage as a solar panel output.

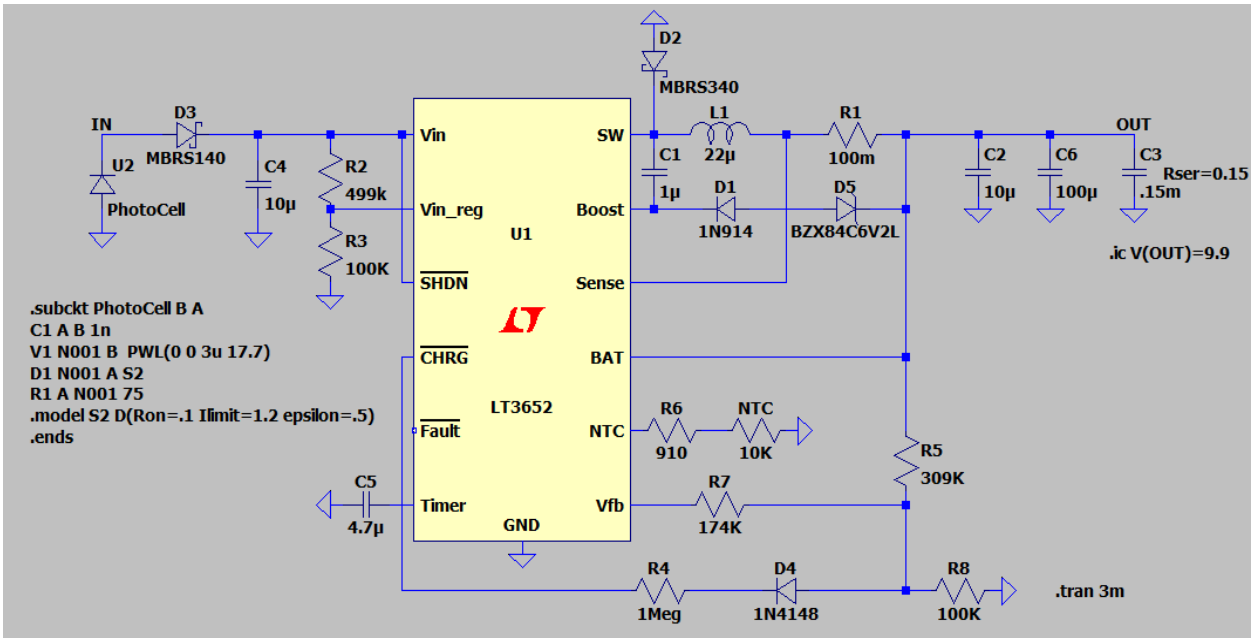

Figure 5 - LTSpice Battery Charger Controller Schematic

The simulation plot in Figure 6 below shows the charging current of 1A and float voltage of 14.4V. This simulation might be changed based on the solar panel and battery type if the current panel and battery need to be replaced with higher values.

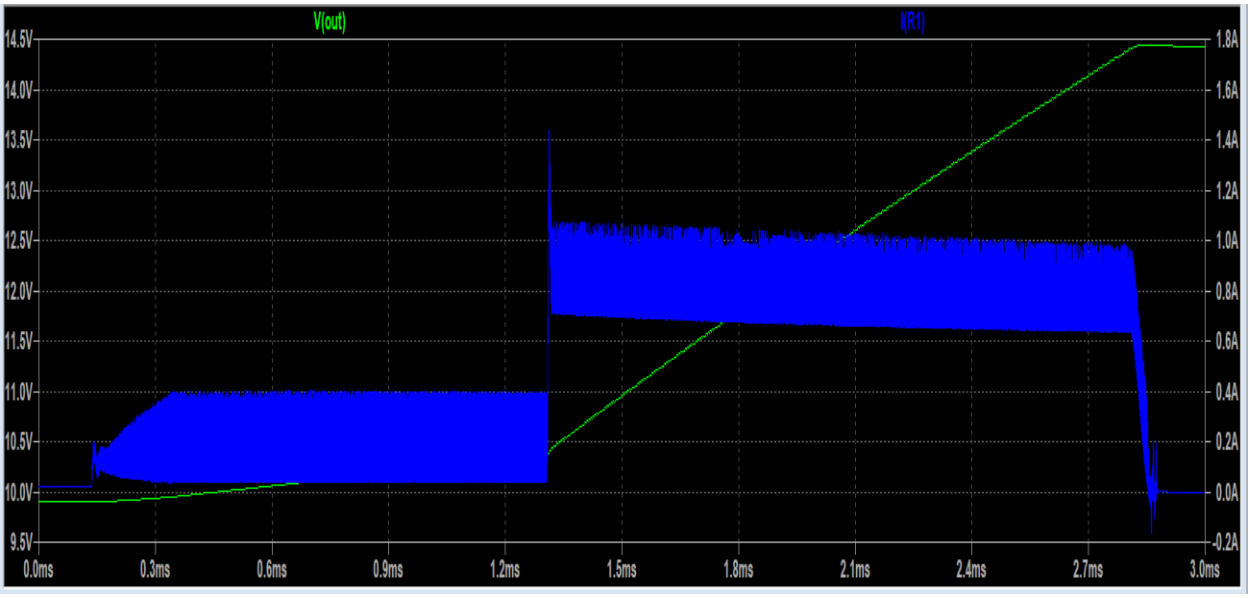

Figure 6 - LTSpice Charging Simulation Plot for Battery Charge Controller

Hardware Design

Power Supply Breakout Board

PCB Layout Implementation for Power Supply LTC3850 Buck Converter is designed using Altium Designer software. The datasheet has PCB Layout Checklist, which was followed to complete the PCB. Starting with schematic of the power supply in Figure 7 below, the design was completed according to the calculation and simulation. The schematic and footprint of the components are selected based on the design requirements. Beside the requirements, multiple test points were created in case of any issues occur during the operation to find any problem easily.

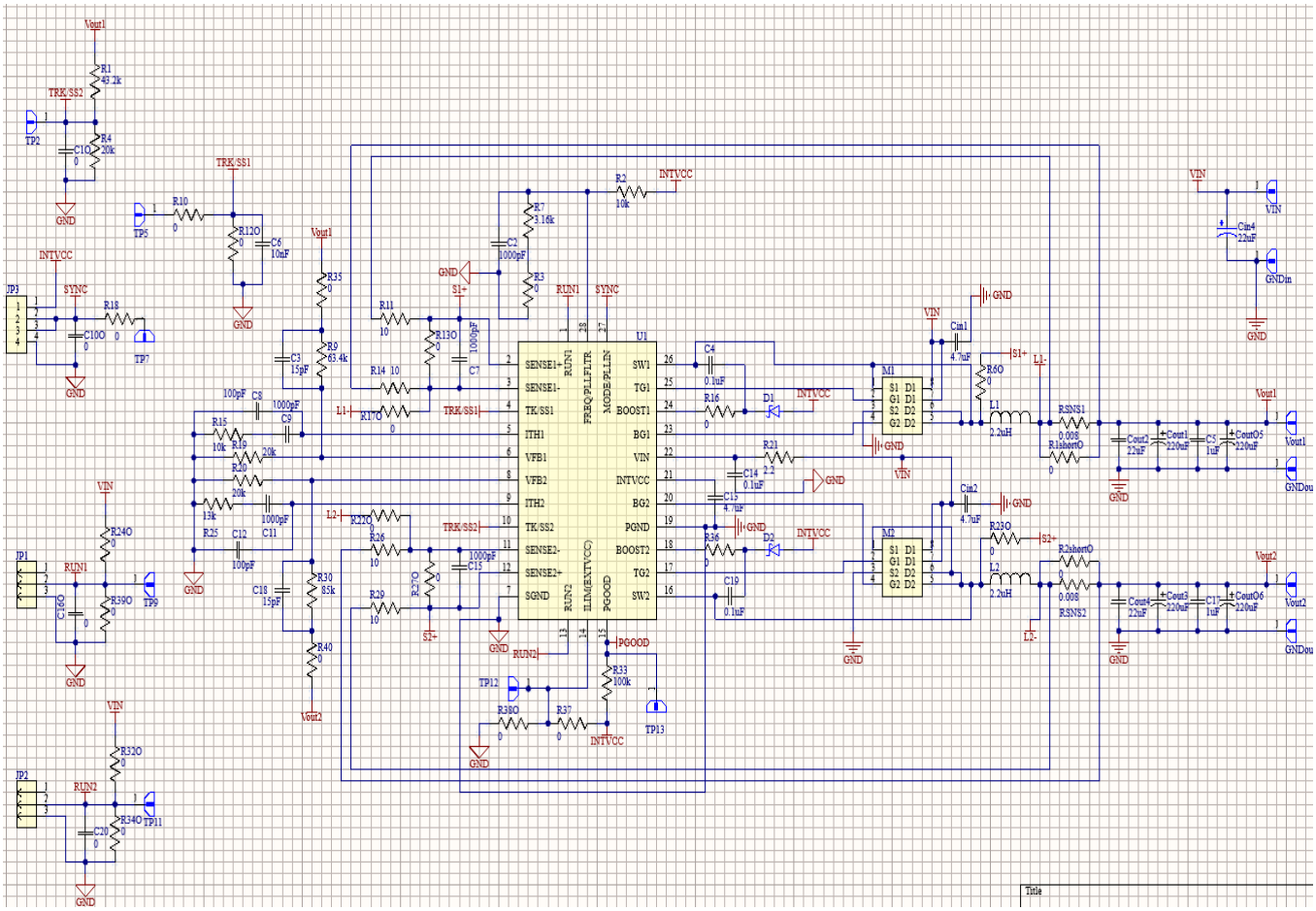

Figure 7 - Power Supply PCB Schematic

Before the PCB layout, the setting of the four layers stack up were assigned with thickness of 1.6mm (≈63mil) as seen the Figure 8 below that shows the stack of the four signal copper layers for top layer, ground, power, and bottom layer. The thickness and other parameters were selected according to JLCPCB manufacturer capabilities. Beside the stack up layers, other manufacturer's restrictions for design rules were followed such as clearance for vias, silk to silk, mask to solder, hole to hole, and components clearance; for routings, routing width, and routing and sizing vias were set in Altium Designer.

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.492mil	3.8	
1	Top Layer		Signal	1oz	1.378mil		
	Dielectric 2	PP-006	Prepreg		3.008mil	4.6	0.02
2	GND	CF-004	Signal	1/2oz	0.492mil		
	Dielectric 1	FR-4	Dielectric		49.803mil	4.6	
3	PWR	CF-004	Signal	1/2oz	0.492mil		
	Dielectric 3	PP-006	Prepreg		3.008mil	4.6	0.02
4	Bottom Layer		Signal	1oz	1.378mil		
	Bottom Solder	Solder Resist	Solder Mask		0.492mil	3.8	
	Bottom Overlay		Overlay				

Figure 8 - Layer Stackup

During the layout, some components need to be close to the IC pins according to datasheet. The size of the capacitors, resistors are 1206 (3.2 mm × 1.6 mm) are quietly large to set them close to their required spot. So, to solve this problem, some of the components were placed in the top layer and some in the bottom layer to get enough space to meet the required distances. See Figure 9 below for signal trace that shows the components; the red components are placed on top layer and blue components are placed on the bottom layer. Also, the polygon pour is connected the ground of the input to the ground of the output capacitors as separating a signal ground from power ground. The all-layer traces next to the signal trace contains multiple design layers such as ground, power, top, bottom, assembly, mechanical layer, and so on. The yellow overall layer shown is for setting the dimension for manufacturer to print the PCB. The top overlay shows the component designators and texts typed. The mechanical layer is used to place information about PCB board footprints and assembly such as physical dimension of the components, vias, assembly instructions and so on.

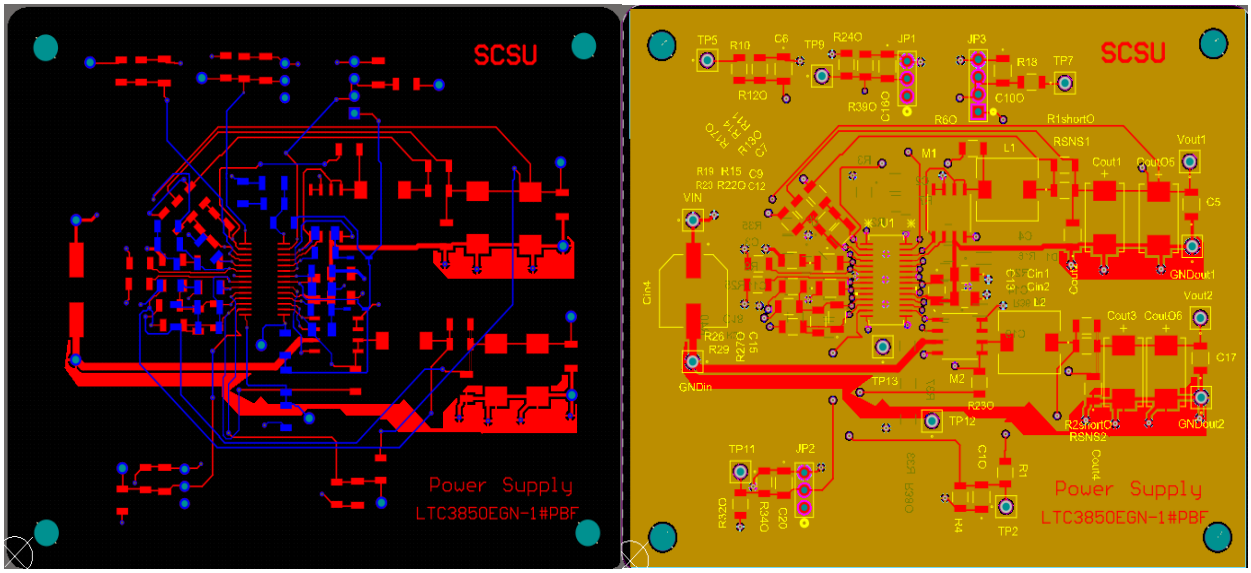

Figure 9 - Signal and Power Traces

After completing the layout above, check for any errors or rules violation. The last step is to generate Gerber files and NC drill files for the manufacturer to print the board. Importing these files using the manufacturer steps to avoid any missing requirement they need to finish printing the PCB board. The 3-d view in Altium Designer is useful to see any missing footprint, misplaced components, missing designators, texts, and so on. See Figure 10 below that shows front layer and back layer of the PCB board.

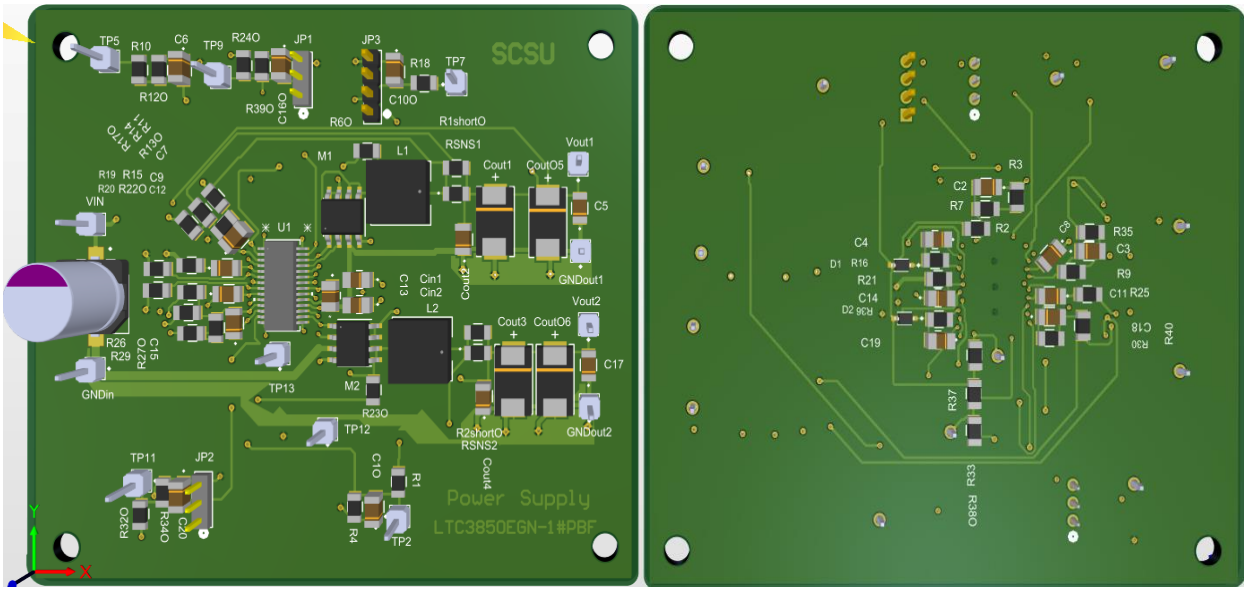

Figure 10 - 3D View of Completed PCB

Soldering the PCB after receiving the PCB from the manufacturer; using soldering paste, and hot air to solder all required components with soldering tools such as tweezers, solder wick, cleaning flux, and binoculars. The PCB of the power supply is completed and working as expected. See Figure 11 for completed PCB board for power supply. And see**Error! Reference source not found.** Figure 12 Altium Designed BOM List used in this power supply PCB.

Figure 11 Soldered and Working PCB

	Comment	Description	Designator	Footprint	LibRef	Quantity
2	0ptional	CAP CER --UF 6.3V X5R 1206	C1O, C10O, C16O, C20	CAP_1206X_AVX-L	12066D226MAT2A	4
3	1000pF	CAP CER 1UF 16V X7R 1206	C2, C9, C11, C15	1206_AVX-L	1206YC105KAT2A	4
4	15pF	CAP CER 1UF 16V X7R 1206	C3, C18	1206_AVX-L	1206YC105KAT2A	2
5	0.1uF	CAP CER 4.7UF 25V X7R 1206	C4, C14, C19	CAP_MJ316_TAY-L	TMJ316BB7475MLHT	3
6	1uF	CAP CER 1UF 16V X7R 1206	C5, C17	1206_AVX-L	1206YC105KAT2A	2
7	10nF	CAP CER 22UF 6.3V X5R 1206	C6	CAP_1206X_AVX-L	12066D226MAT2A	1
8	1000pF	CAP CER 22UF 6.3V X5R 1206	C7	CAP_1206X_AVX-L	12066D226MAT2A	1
9	100pF	CAP CER 1UF 16V X7R 1206	C8, C12	1206_AVX-L	1206YC105KAT2A	2
10	4.7uF	CAP CER 4.7UF 25V X7R 1206	C13, Cin1, Cin2	CAP_MJ316_TAY-L	TMJ316BB7475MLHT	3
11	22uF	CAP ALUM POLY 22UF 20% 35V SMD	Cin4	CAP_35SVPD22M	35SVPD22M	1
12	220uF	CAP TANT POLY 220UF 4V 2917	Cout1, Cout3, CoutO5, CoutO6	PCAP_TPE_D2E_PAN	4TPE220MF	4
13	22uF	CAP CER 22UF 6.3V X5R 1206	Cout2, Cout4	CAP_1206X_AVX-L	12066D226MAT2A	2
14	CMDSH-3TR	Diode Schottky 30V 100mA Surface-Mount SOD-323	D1, D2	SOD2512X110N	CMDSH-3TR	2
15	PH1-01-UA	Connector Header Throu-Hole 1 0.100 (2.54mm)	GNDin, GNDout1, GNDout2, TP2, TP5, TP7	ADAM-TECH_PH1-01-UA	PH1-01-UA	6
16	PH1-01-UA	Connector Header Throu-Hole 1 0.100 (2.54mm)	TP9, TP11, TP12, TP13, VIN, Vout1, Vout2	ADAM-TECH_PH1-01-UA	PH1-01-UA	7
17	TMM-103-02-L-S	Connector Header Throu-Hole 3 0.079" (2.00mm)	JP1, JP2	CONN_TMM-103-XX-XX-S_SAI	TMM-103-02-L-S	2
18	TMM-104-01-L-S	Connector Header Throu-Hole 4 0.079" (2.00mm)	JP3	TMM-104-01-G-S_SAI	TMM-104-01-L-S	1
19	2.2uH	FIXED IND 2.2UH 5.4A 12 MOHM SMD	L1, L2	IND_RLF7030T-2R2M5R4_TDK-L	RLF7030T-2R2M5R4	2
20	SI4936BDY-T1-E3	MOSFET 2N-CH 30V 6.9A 8-SOIC	M1, M2	SOIC-8_SI	SI4936BDY-T1-E3	2
21	43.2k	RES 20K OHM 1% 1/4W 1206	R1	RC1206N_YAG-L	RC1206FR-0720KL	1
22	Optional	RES -- OHM 1% 1/4W 1206	R1shortO, R2shortO, R6O, R12O, R13O, R17O	RC1206N_YAG-L	RC1206FR-0720KL	6
23	Optional	RES -- OHM 1% 1/4W 1206	R22O, R23O, R24O, R27O, R32O, R34O, R38O, R39O	RC1206N_YAG-L	RC1206FR-0720KL	8
24	20k	RES 20K OHM 1% 1/4W 1206	R4, R19, R20, R40, R35, R36, R37	RC1206N_YAG-L	RC1206FR-0720KL	7
25	3.16k	RES 3.16K OHM 1% 1/4W 1206	R7, 'R2, R15, R3, R10, R16, R18	RC1206N_YAG-L	RC1206FR-0720KL	7
26	63.4k	RES 63.4 kOHM 1% 1/4W 1206	R9	RC1206N_YAG-L	RC1206FR-0720KL	1
27	10	RES 10 OHM 1% 1/4W 1206	R11, R14, R26, R29	RC1206N_YAG-L	RC1206FR-0720KL	4
28	2.2	RES 2.2 OHM 1% 1/4W 1206	R21	RC1206N_YAG-L	RC1206FR-0720KL	1
29	13k	RES 13K OHM 1% 1/4W 1206	R25	RC1206N_YAG-L	RC1206FR-0720KL	1
30	85k	RES 85K OHM 1% 1/4W 1206	R30	RC1206N_YAG-L	RC1206FR-0720KL	1
31	100k	RES 100K OHM 1% 1/4W 1206	R33	RC1206N_YAG-L	RC1206FR-0720KL	1
32	0.008	RES 0.008 OHM 1% 1/4W 1206	RSNS1, RSNS2	RC1206N_YAG-L	RC1206FR-0720KL	2
33	LTC3850EGN-1#PBF	IC REG CTRLR BUCK 28SSOP	U1	SSOP-28_GN_LIT-L	LTC3850EGN-1#PBF	1

Figure 12 Altium Designed BOM List

Results

In lab experiments, the output voltages of 3.3V and 4V were obtained to feed the system load; the current of 0.7A is also obtained. The results of the ripple voltage were done in shieled room (Faraday's Room) in different frequencies; the current is 0.6A and input voltage of 7V. The results were acceptable for our needs to do this project. See the plots of the ripple voltages in Figure 13 below shows a ripple voltage set to 50mV and 1ms and frequency of 210kHz. The ripple voltage peak-to-peak shown in the oscilloscope is 96mV. See the other two plots Figure 14 and Figure 15 below with DC and one in faraday's cage.

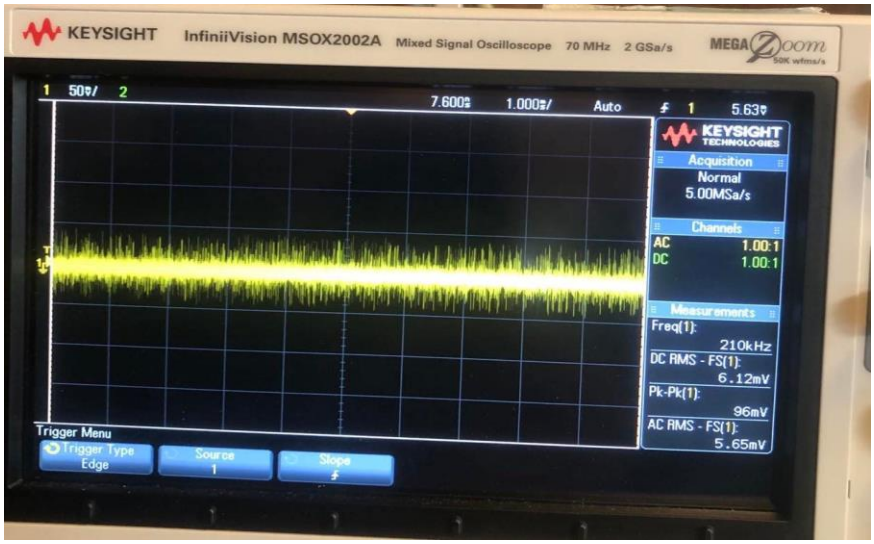

Figure 13 Voltage Ripple

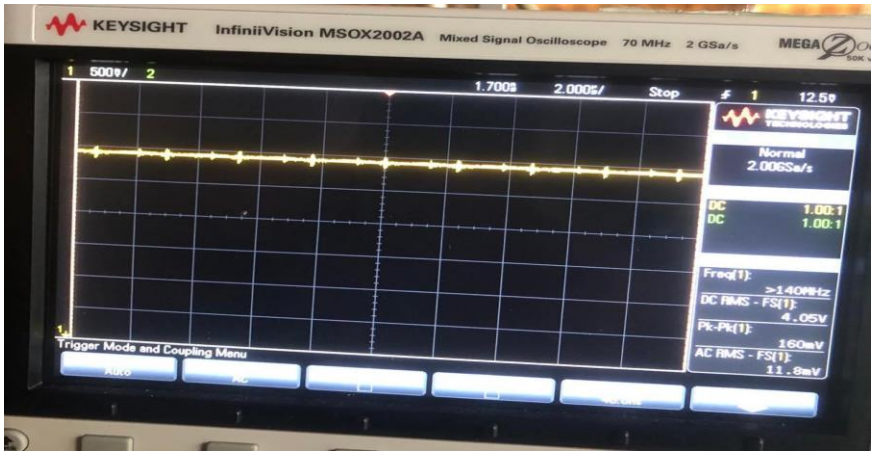

Figure 14 - Voltage Ripple with DC

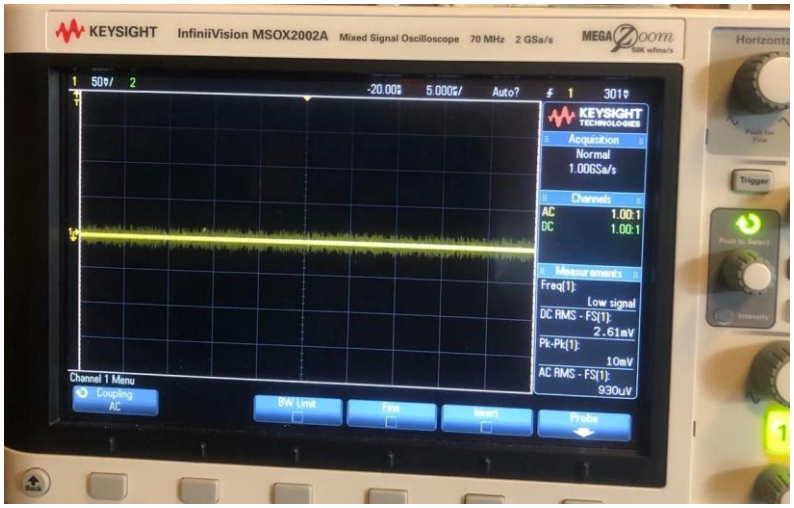

Figure 15 - Voltage Ripple in Faraday Cage

Conclusion

In conclusion, the load is powered successfully by a power supply with the two outputs required and more outputs can be added at any time for future extension. The solar panel has been tested and resulted in 21.7V and 0.3A as specified from the manufacturer. The charger controller for the battery is currently in progress; the simulation is done and currently working on board prototype and then PCB. Overall, the power management of this system was done as expected and the results were obtained.

References

1. “LT3652 - power tracking 2A Battery Charger for solar power - analog devices.” [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/3652fe.pdf. [Accessed: 09-Sep-2022].

2. “Mixed-Signal and digital signal processing ICS | Analog Devices.” [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/LTC3850-3850-1.pdf. [Accessed: 09-Oct-2022].