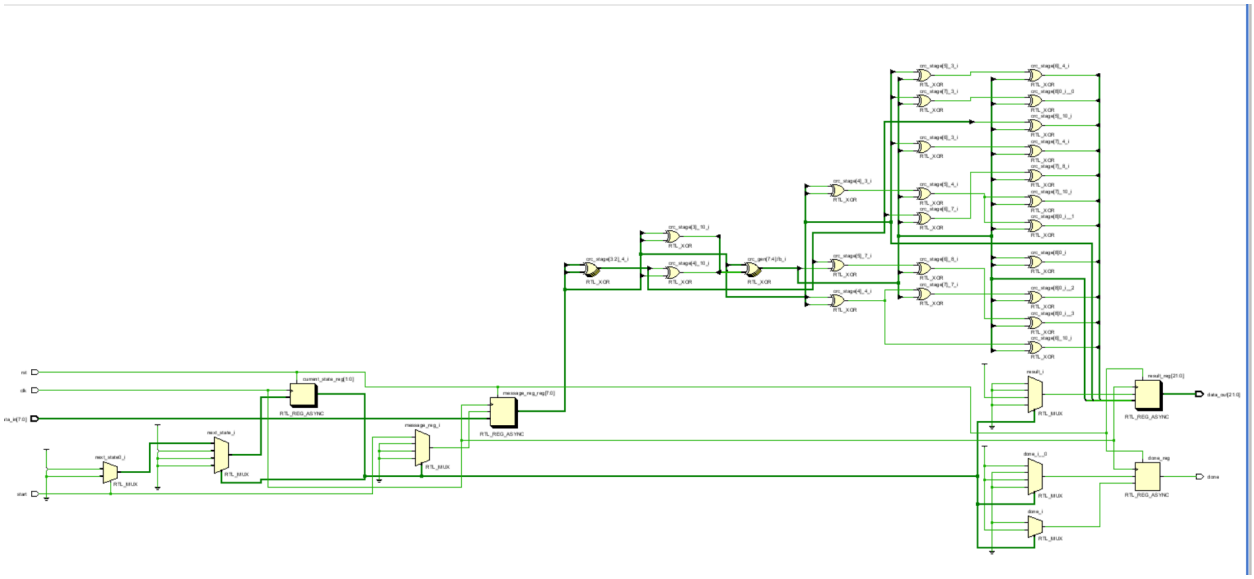
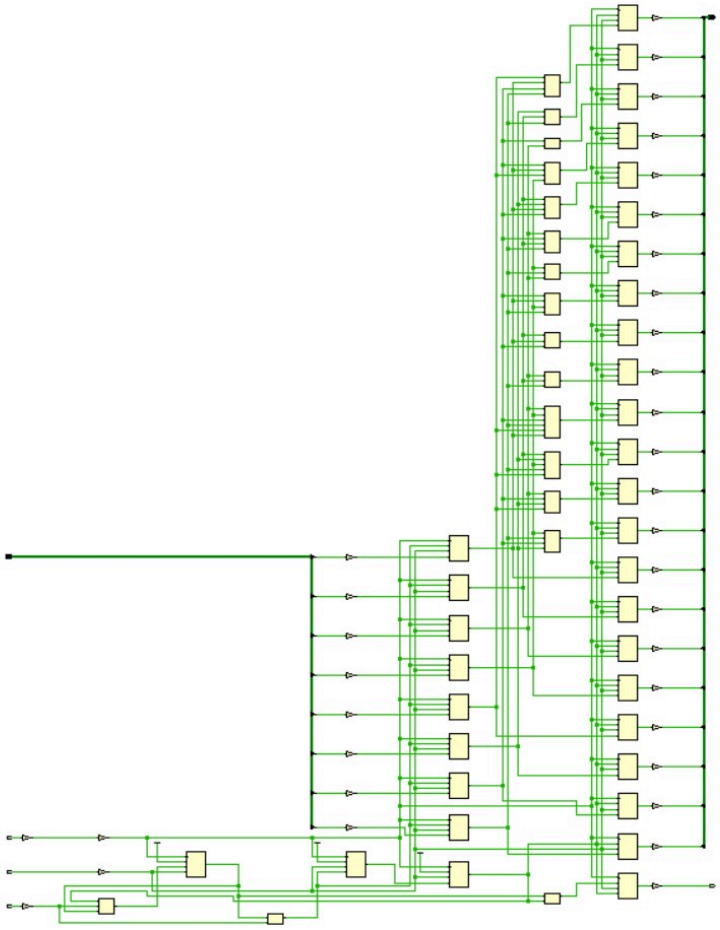
# CRC Code

## Elaborated Design



## Synthesis



## Utilization

| Name | Slice LUTs (20800) | Slice Registers (41600) | Bonded IOB (106) | BUFGCTRL (32) |
|---|---|---|---|---|
| CRC_synthesizable | 11 | 34 | 34 | 1 |

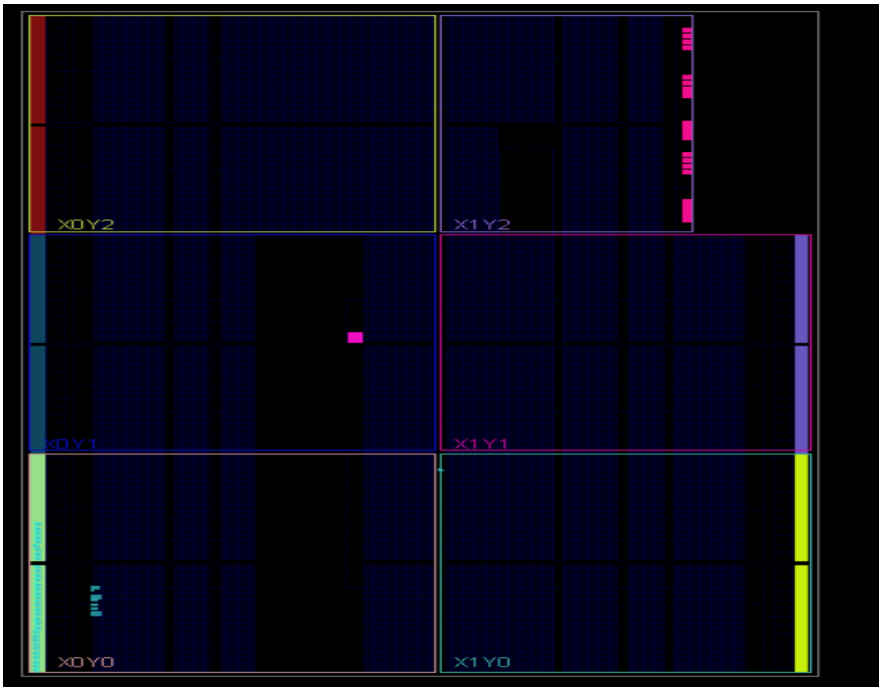
## Timing Analysis

**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 7.865 ns | Worst Hold Slack (WHS): | 0.142 ns | Worst Pulse Width Slack (WPWS): | 4.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 57 | Total Number of Endpoints: | 57 | Total Number of Endpoints: | 35 |

**All user specified timing constraints are met.**

## Implementation



# Utilization

Hierarchy

| Name | Slice LUTs (20800) | Slice Registers (41600) | Slice (8150) | LUT as Logic (20800) | LUT Flip Flop Pairs (20800) | Bonded IOB (106) | BUFGCTRL (32) |
|---|---|---|---|---|---|---|---|
| N CRC_synthesizable | 11 | 34 | 8 | 11 | 9 | 34 | 1 |

# Timing Analysis

**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 7.953 ns | Worst Hold Slack (WHS): | 0.167 ns | Worst Pulse Width Slack (WPWS): | 4.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 57 | Total Number of Endpoints: | 57 | Total Number of Endpoints: | 35 |

**All user specified timing constraints are met.**