به نام خداوند بخشنده مهربان

طراحی سیستم های دیجیتال

دانشکده مهندسی کامپیوتر

دکتر فصحتی
بهار ۱۴۰۳

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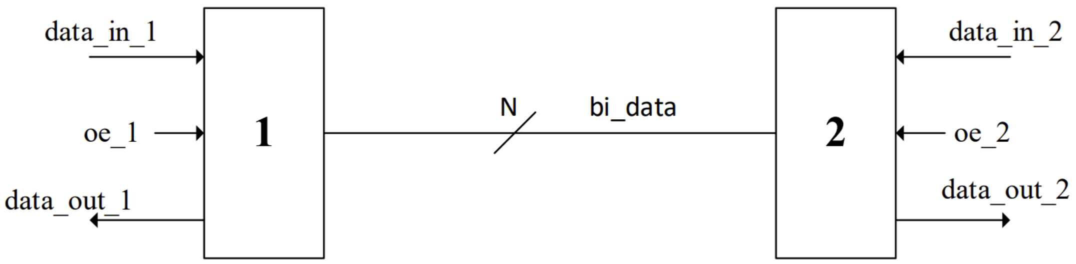
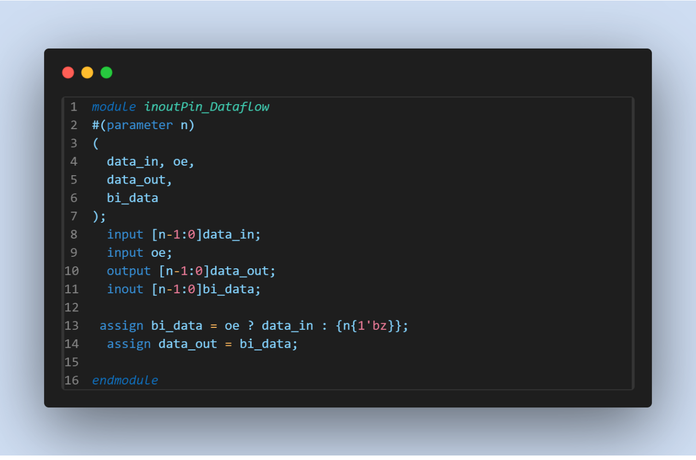
تمرین دوم

سوال ۱

۱- گذرگاه دوطرفه زیر را به عرض N بیت با روش مدل‌سازی جریان داده[1] طراحی کنید (اگر OE یک باشد داده روی گذرگاه ارسال می‌شود و اگر OE صفر باشد داده از گذرگاه دریافت می‌شود).

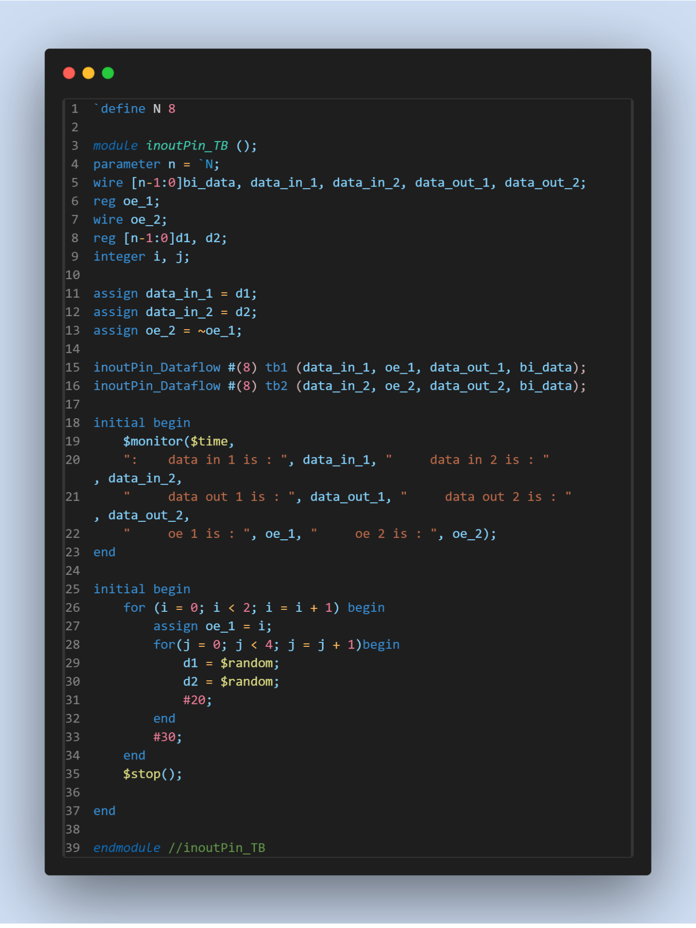
راهنمایی: برای اینکه پیاده‌سازی خود را برای N بیت امکان‌پذیر کنید؛ از پارامتر در زبان وریلاگ استفاده کنید.





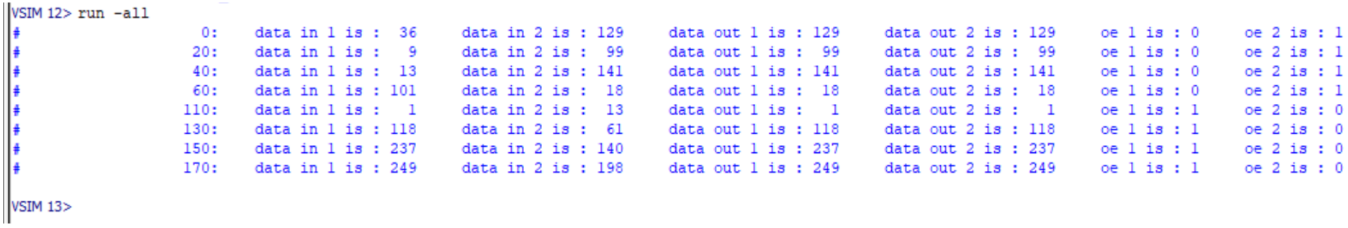
```
module inoutPin_Dataflow
#(parameter n)
(
  data_in, oe,
  data_out,
  bi_data
);
  input [n-1:0]data_in;
  input oe;
  output [n-1:0]data_out;
  inout [n-1:0]bi_data;

 assign bi_data = oe ? data_in : {n{1'bz}};
  assign data_out = bi_data;

endmodule
```

در بالا کد این بلاک را مشاهده می کنید، در واقع چیزی که مدل شده یکی از بلوک های ۱ یا ۲ است و در تست بنچ این دو به هم متصل می شوند و مدار داده شده حاصل می شود.
در این کد با استفاده از عملگر ؟ مقدار دهی bi_data انجام شده است و خروجی نیز متصل به همین سیم است.



```verilog
`define N 8

module inoutPin_TB ();
parameter n = `N;
wire [n-1:0]bi_data, data_in_1, data_in_2, data_out_1, data_out_2;
reg oe_1;
wire oe_2;
reg [n-1:0]d1, d2;
integer i, j;

assign data_in_1 = d1;
assign data_in_2 = d2;
assign oe_2 = ~oe_1;

inoutPin_Dataflow #(8) tb1 (data_in_1, oe_1, data_out_1, bi_data);
inoutPin_Dataflow #(8) tb2 (data_in_2, oe_2, data_out_2, bi_data);

initial begin
    $monitor($time,
    ":    data in 1 is : ", data_in_1, "     data in 2 is : "
, data_in_2,
    "     data out 1 is : ", data_out_1, "     data out 2 is : "
, data_out_2,
    "     oe 1 is : ", oe_1, "     oe 2 is : ", oe_2);
end

initial begin
    for (i = 0; i < 2; i = i + 1) begin
        assign oe_1 = i;
        for(j = 0; j < 4; j = j + 1)begin
            d1 = $random;
            d2 = $random;
            #20;
        end
        #30;
    end
    $stop();

end

endmodule //inoutPin_TB
```

و خروجی آن نیز به این صورت است:



```
VSIM 12> run -all
#                    0:    data in 1 is :  36     data in 2 is : 129     data out 1 is : 129     data out 2 is : 129     oe 1 is : 0     oe 2 is : 1
#                   20:    data in 1 is :   9     data in 2 is :  99     data out 1 is :  99     data out 2 is :  99     oe 1 is : 0     oe 2 is : 1
#                   40:    data in 1 is :  13     data in 2 is : 141     data out 1 is : 141     data out 2 is : 141     oe 1 is : 0     oe 2 is : 1
#                   60:    data in 1 is : 101     data in 2 is :  18     data out 1 is :  18     data out 2 is :  18     oe 1 is : 0     oe 2 is : 1
#                  110:    data in 1 is :   1     data in 2 is :  13     data out 1 is :   1     data out 2 is :   1     oe 1 is : 1     oe 2 is : 0
#                  130:    data in 1 is : 118     data in 2 is :  61     data out 1 is : 118     data out 2 is : 118     oe 1 is : 1     oe 2 is : 0
#                  150:    data in 1 is : 237     data in 2 is : 140     data out 1 is : 237     data out 2 is : 237     oe 1 is : 1     oe 2 is : 0
#                  170:    data in 1 is : 249     data in 2 is : 198     data out 1 is : 249     data out 2 is : 249     oe 1 is : 1     oe 2 is : 0

VSIM 13>
```

چون یکی از oe ها همواره not دیگری است هیچگاه حالت مساوی رخ نمی دهد.

سوال ۲

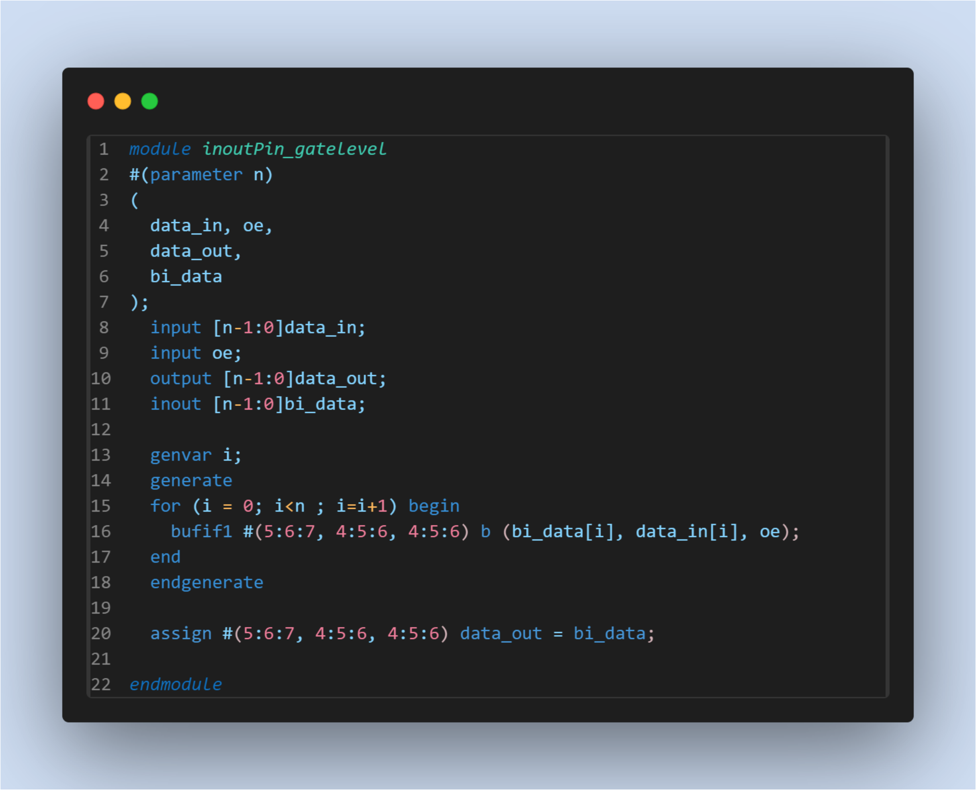
۲- این گذرگاه را با مدل‌سازی سطح گیت[۲] هم طراحی کنید. اگر تأخیر گیت‌های وارون و بافرسه‌حالته مطابق با جدول ۱ باشند، با استفاده از شبیه‌سازی، تأخیر برای انتقال ۸ بیت را در سه حالت کمینه، عمومی[۳] و بیشینه به دست آورید.

جدول ۱- جدول تأخیر گیت‌ها[+]

کمینه		عمومی		بیشینه	
Not	Tristate Buffer	Not	Tristate Buffer	Not	Tristate Buffer
2,1	5,4,4	3,2	6,5,5	4,3	7,6,6

+ به ترتیب از چپ به راست تأخیرها برابر است با Rise، Fall و Turn off

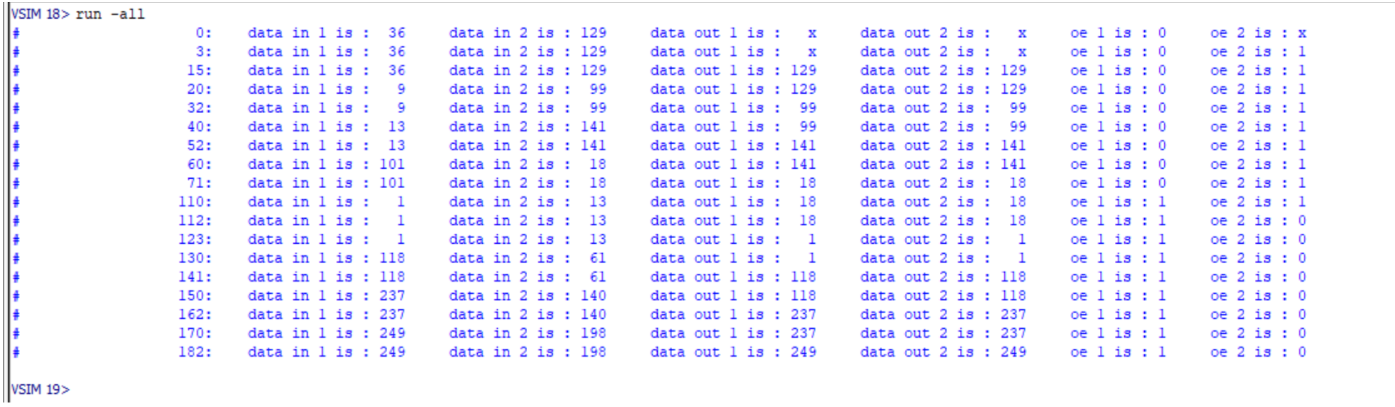
طراحی به این صورت است:



```verilog
module inoutPin_gatelevel
#(parameter n)
(
  data_in, oe,
  data_out,
  bi_data
);
  input [n-1:0]data_in;
  input oe;
  output [n-1:0]data_out;
  inout [n-1:0]bi_data;

  genvar i;
  generate
  for (i = 0; i<n ; i=i+1) begin
    bufif1 #(5:6:7, 4:5:6, 4:5:6) b (bi_data[i], data_in[i], oe);
  end
  endgenerate

  assign #(5:6:7, 4:5:6, 4:5:6) data_out = bi_data;

endmodule
```

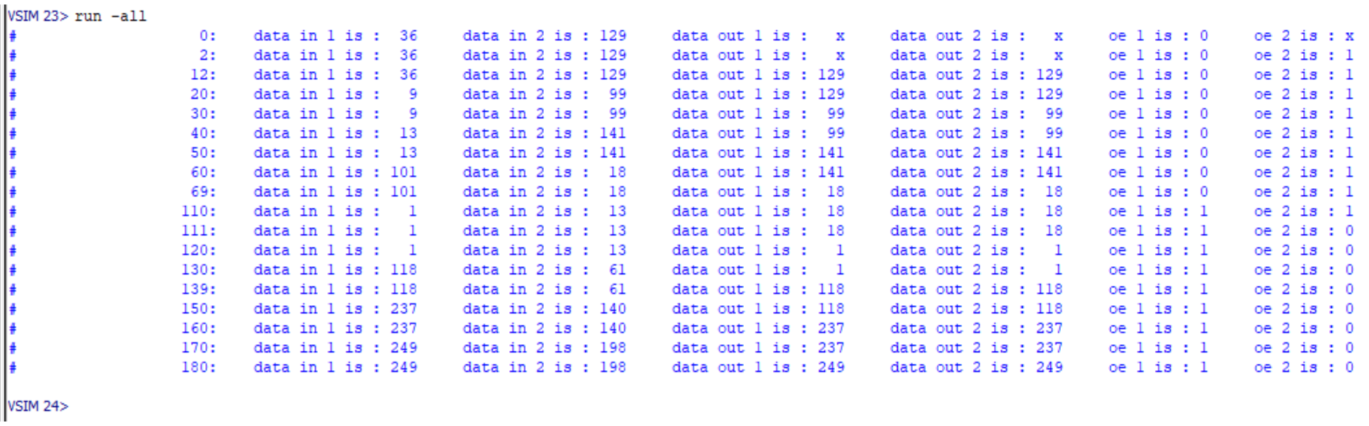
تاخیر ها نیز در زیر آورده شده است.

تاخیر ها در حالت دیفالت.



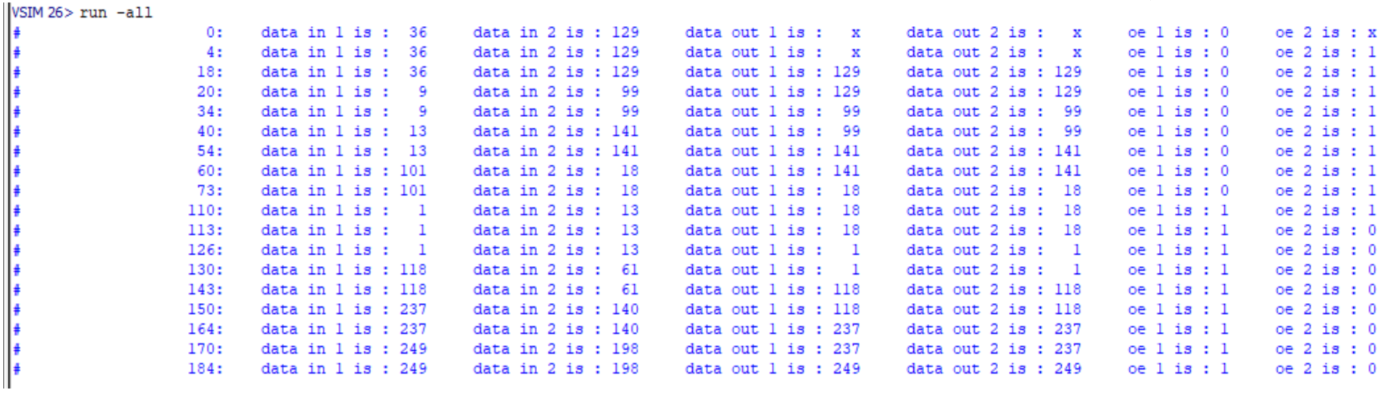
```
VSIM 18> run -all
#                    0:    data in 1 is :  36    data in 2 is : 129    data out 1 is :   x    data out 2 is :   x    oe 1 is : 0    oe 2 is : x
#                    3:    data in 1 is :  36    data in 2 is : 129    data out 1 is :   x    data out 2 is :   x    oe 1 is : 0    oe 2 is : 1
#                   15:    data in 1 is :  36    data in 2 is : 129    data out 1 is : 129    data out 2 is : 129    oe 1 is : 0    oe 2 is : 1
#                   20:    data in 1 is :   9    data in 2 is :  99    data out 1 is : 129    data out 2 is : 129    oe 1 is : 0    oe 2 is : 1
#                   32:    data in 1 is :   9    data in 2 is :  99    data out 1 is :  99    data out 2 is :  99    oe 1 is : 0    oe 2 is : 1
#                   40:    data in 1 is :  13    data in 2 is : 141    data out 1 is :  99    data out 2 is :  99    oe 1 is : 0    oe 2 is : 1
#                   52:    data in 1 is :  13    data in 2 is : 141    data out 1 is : 141    data out 2 is : 141    oe 1 is : 0    oe 2 is : 1
#                   60:    data in 1 is : 101    data in 2 is :  18    data out 1 is : 141    data out 2 is : 141    oe 1 is : 0    oe 2 is : 1
#                   71:    data in 1 is : 101    data in 2 is :  18    data out 1 is :  18    data out 2 is :  18    oe 1 is : 0    oe 2 is : 1
#                  110:    data in 1 is :   1    data in 2 is :  13    data out 1 is :  18    data out 2 is :  18    oe 1 is : 1    oe 2 is : 1
#                  112:    data in 1 is :   1    data in 2 is :  13    data out 1 is :  18    data out 2 is :  18    oe 1 is : 1    oe 2 is : 0
#                  123:    data in 1 is :   1    data in 2 is :  13    data out 1 is :   1    data out 2 is :   1    oe 1 is : 1    oe 2 is : 0
#                  130:    data in 1 is : 118    data in 2 is :  61    data out 1 is :   1    data out 2 is :   1    oe 1 is : 1    oe 2 is : 0
#                  141:    data in 1 is : 118    data in 2 is :  61    data out 1 is : 118    data out 2 is : 118    oe 1 is : 1    oe 2 is : 0
#                  150:    data in 1 is : 237    data in 2 is : 140    data out 1 is : 118    data out 2 is : 118    oe 1 is : 1    oe 2 is : 0
#                  162:    data in 1 is : 237    data in 2 is : 140    data out 1 is : 237    data out 2 is : 237    oe 1 is : 1    oe 2 is : 0
#                  170:    data in 1 is : 249    data in 2 is : 198    data out 1 is : 237    data out 2 is : 237    oe 1 is : 1    oe 2 is : 0
#                  182:    data in 1 is : 249    data in 2 is : 198    data out 1 is : 249    data out 2 is : 249    oe 1 is : 1    oe 2 is : 0

VSIM 19>
```

تاخیر ها در حالت مینیمم.



```
VSIM 23> run -all
#                   0:    data in 1 is :  36    data in 2 is : 129    data out 1 is :   x    data out 2 is :   x    oe 1 is : 0    oe 2 is : x
#                   2:    data in 1 is :  36    data in 2 is : 129    data out 1 is :   x    data out 2 is :   x    oe 1 is : 0    oe 2 is : 1
#                  12:    data in 1 is :  36    data in 2 is : 129    data out 1 is : 129    data out 2 is : 129    oe 1 is : 0    oe 2 is : 1
#                  20:    data in 1 is :   9    data in 2 is :  99    data out 1 is : 129    data out 2 is : 129    oe 1 is : 0    oe 2 is : 1
#                  30:    data in 1 is :   9    data in 2 is :  99    data out 1 is :  99    data out 2 is :  99    oe 1 is : 0    oe 2 is : 1
#                  40:    data in 1 is :  13    data in 2 is : 141    data out 1 is :  99    data out 2 is :  99    oe 1 is : 0    oe 2 is : 1
#                  50:    data in 1 is :  13    data in 2 is : 141    data out 1 is : 141    data out 2 is : 141    oe 1 is : 0    oe 2 is : 1
#                  60:    data in 1 is : 101    data in 2 is :  18    data out 1 is : 141    data out 2 is : 141    oe 1 is : 0    oe 2 is : 1
#                  69:    data in 1 is : 101    data in 2 is :  18    data out 1 is :  18    data out 2 is :  18    oe 1 is : 0    oe 2 is : 1
#                 110:    data in 1 is :   1    data in 2 is :  13    data out 1 is :  18    data out 2 is :  18    oe 1 is : 1    oe 2 is : 1
#                 111:    data in 1 is :   1    data in 2 is :  13    data out 1 is :  18    data out 2 is :  18    oe 1 is : 1    oe 2 is : 0
#                 120:    data in 1 is :   1    data in 2 is :  13    data out 1 is :   1    data out 2 is :   1    oe 1 is : 1    oe 2 is : 0
#                 130:    data in 1 is : 118    data in 2 is :  61    data out 1 is :   1    data out 2 is :   1    oe 1 is : 1    oe 2 is : 0
#                 139:    data in 1 is : 118    data in 2 is :  61    data out 1 is : 118    data out 2 is : 118    oe 1 is : 1    oe 2 is : 0
#                 150:    data in 1 is : 237    data in 2 is : 140    data out 1 is : 118    data out 2 is : 118    oe 1 is : 1    oe 2 is : 0
#                 160:    data in 1 is : 237    data in 2 is : 140    data out 1 is : 237    data out 2 is : 237    oe 1 is : 1    oe 2 is : 0
#                 170:    data in 1 is : 249    data in 2 is : 198    data out 1 is : 237    data out 2 is : 237    oe 1 is : 1    oe 2 is : 0
#                 180:    data in 1 is : 249    data in 2 is : 198    data out 1 is : 249    data out 2 is : 249    oe 1 is : 1    oe 2 is : 0

VSIM 24>
```

تاخیر ها در حالت ماکسیمم.

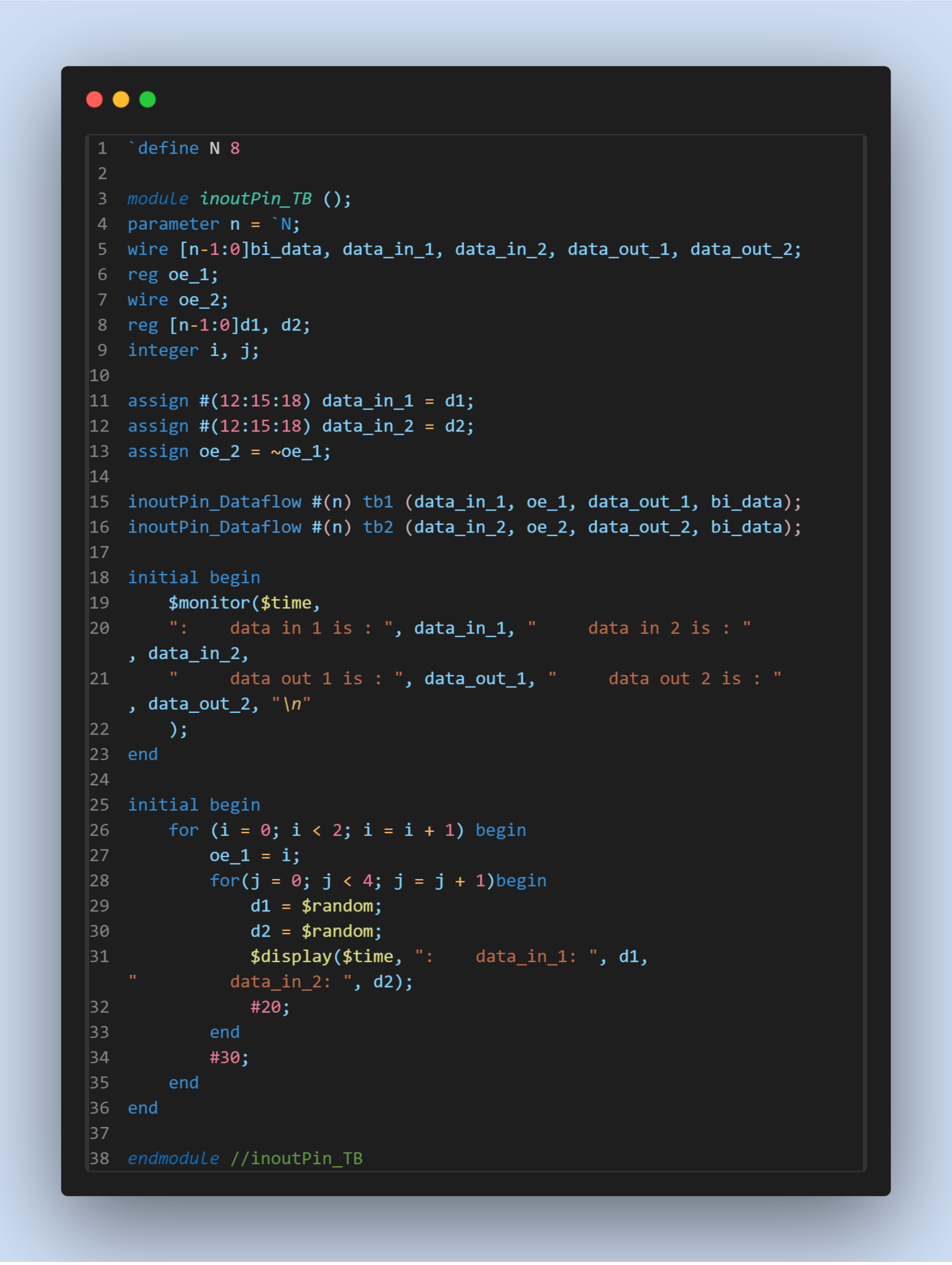


```
VSIM 26> run -all
#                   0:    data in 1 is :  36    data in 2 is : 129    data out 1 is :   x    data out 2 is :   x    oe 1 is : 0    oe 2 is : x
#                   4:    data in 1 is :  36    data in 2 is : 129    data out 1 is :   x    data out 2 is :   x    oe 1 is : 0    oe 2 is : 1
#                  18:    data in 1 is :  36    data in 2 is : 129    data out 1 is : 129    data out 2 is : 129    oe 1 is : 0    oe 2 is : 1
#                  20:    data in 1 is :   9    data in 2 is :  99    data out 1 is : 129    data out 2 is : 129    oe 1 is : 0    oe 2 is : 1
#                  34:    data in 1 is :   9    data in 2 is :  99    data out 1 is :  99    data out 2 is :  99    oe 1 is : 0    oe 2 is : 1
#                  40:    data in 1 is :  13    data in 2 is : 141    data out 1 is :  99    data out 2 is :  99    oe 1 is : 0    oe 2 is : 1
#                  54:    data in 1 is :  13    data in 2 is : 141    data out 1 is : 141    data out 2 is : 141    oe 1 is : 0    oe 2 is : 1
#                  60:    data in 1 is : 101    data in 2 is :  18    data out 1 is : 141    data out 2 is : 141    oe 1 is : 0    oe 2 is : 1
#                  73:    data in 1 is : 101    data in 2 is :  18    data out 1 is :  18    data out 2 is :  18    oe 1 is : 0    oe 2 is : 1
#                 110:    data in 1 is :   1    data in 2 is :  13    data out 1 is :  18    data out 2 is :  18    oe 1 is : 1    oe 2 is : 1
#                 113:    data in 1 is :   1    data in 2 is :  13    data out 1 is :  18    data out 2 is :  18    oe 1 is : 1    oe 2 is : 0
#                 126:    data in 1 is :   1    data in 2 is :  13    data out 1 is :   1    data out 2 is :   1    oe 1 is : 1    oe 2 is : 0
#                 130:    data in 1 is : 118    data in 2 is :  61    data out 1 is :   1    data out 2 is :   1    oe 1 is : 1    oe 2 is : 0
#                 143:    data in 1 is : 118    data in 2 is :  61    data out 1 is : 118    data out 2 is : 118    oe 1 is : 1    oe 2 is : 0
#                 150:    data in 1 is : 237    data in 2 is : 140    data out 1 is : 118    data out 2 is : 118    oe 1 is : 1    oe 2 is : 0
#                 164:    data in 1 is : 237    data in 2 is : 140    data out 1 is : 237    data out 2 is : 237    oe 1 is : 1    oe 2 is : 0
#                 170:    data in 1 is : 249    data in 2 is : 198    data out 1 is : 237    data out 2 is : 237    oe 1 is : 1    oe 2 is : 0
#                 184:    data in 1 is : 249    data in 2 is : 198    data out 1 is : 249    data out 2 is : 249    oe 1 is : 1    oe 2 is : 0
```

سوال ۳

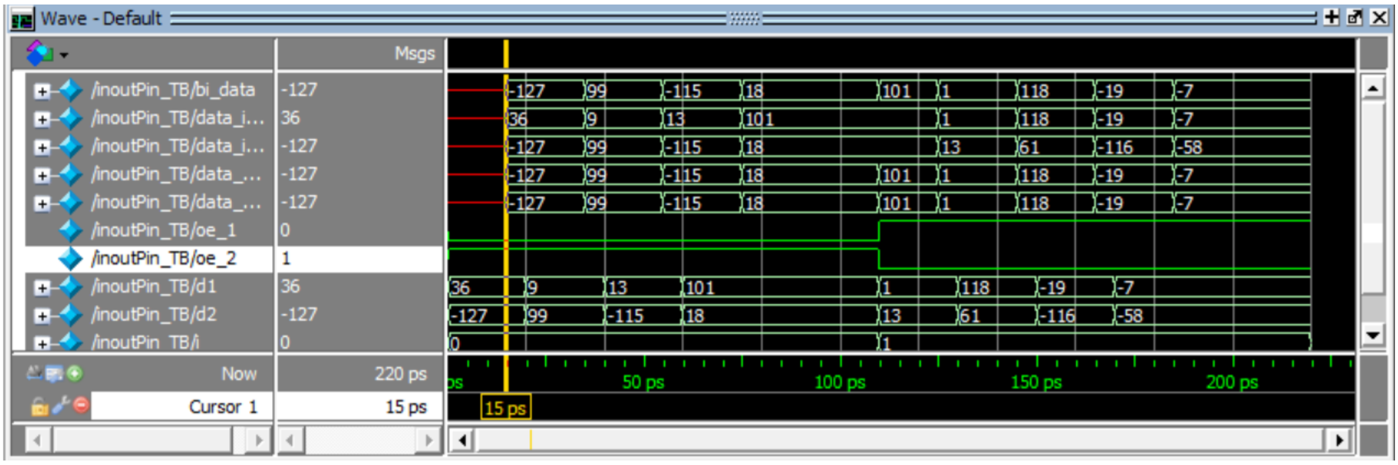
۳- با استفاده از گزارش‌های تأخیر در روش مدل‌سازی سطح گیت، تأخیرهای مناسب برای انتقال ۸ بیت را در طراحی مدل‌سازی جریان داده خود اعمال کنید و طراحی خود را شبیه‌سازی نمایید.

در مدل سازی تاخیر در روش مدل سازی جریان داده به صورت زیر، ماکسیمم تاخیر برای هر مرحله که در حالت مینیمم، ۱۲، در حالت عمومی ۱۵ و در حالت ماکسیمم ۱۸ بوده را به عنوان تاخیر پین به پین آن مرحله می نویسیم، به این صورت:

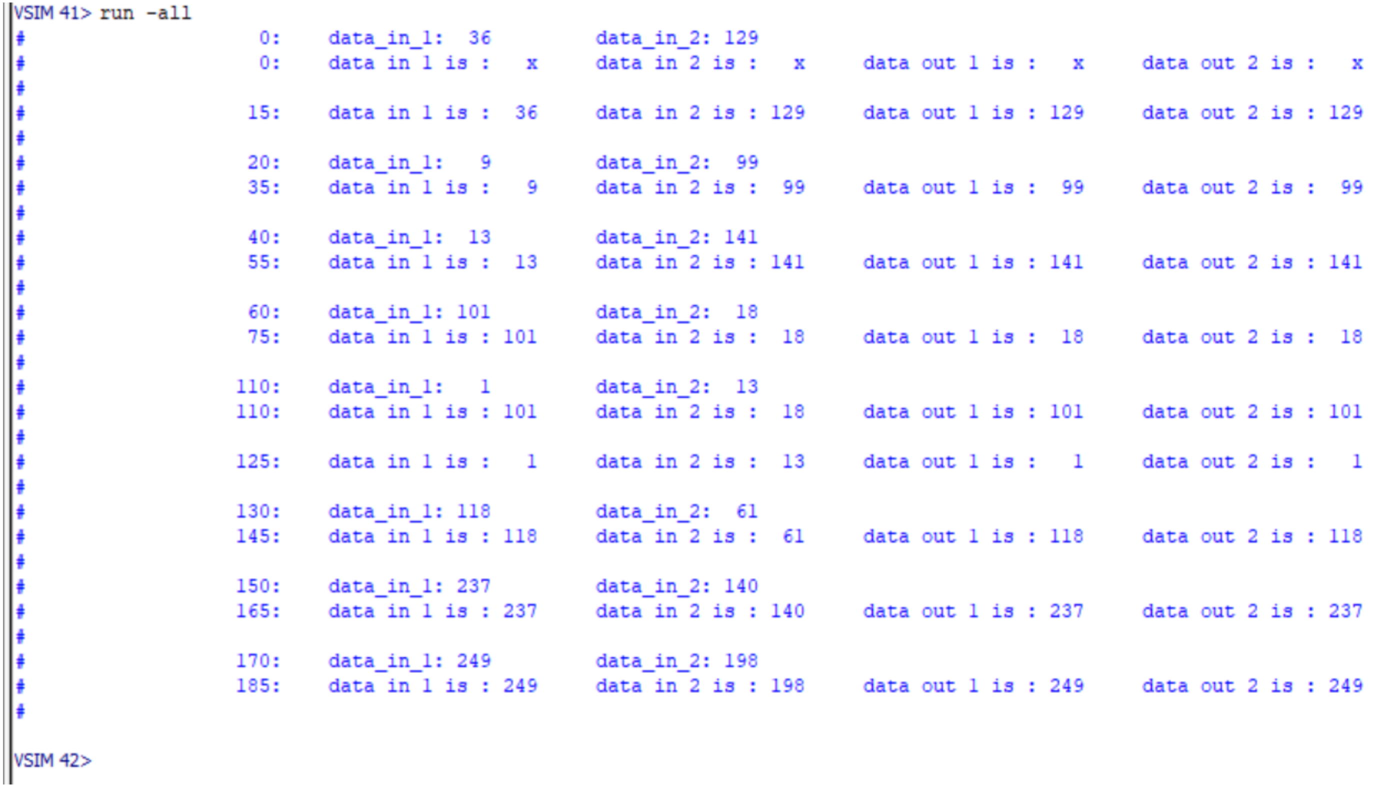


```
`define N 8

module inoutPin_TB ();
parameter n = `N;
wire [n-1:0]bi_data, data_in_1, data_in_2, data_out_1, data_out_2;
reg oe_1;
wire oe_2;
reg [n-1:0]d1, d2;
integer i, j;

assign #(12:15:18) data_in_1 = d1;
assign #(12:15:18) data_in_2 = d2;
assign oe_2 = ~oe_1;

inoutPin_Dataflow #(n) tb1 (data_in_1, oe_1, data_out_1, bi_data);
inoutPin_Dataflow #(n) tb2 (data_in_2, oe_2, data_out_2, bi_data);

initial begin
    $monitor($time,
    ":     data in 1 is : ", data_in_1, "     data in 2 is : ", data_in_2,
    "      data out 1 is : ", data_out_1, "     data out 2 is : ", data_out_2, "\n"
    );
end

initial begin
    for (i = 0; i < 2; i = i + 1) begin
        oe_1 = i;
        for(j = 0; j < 4; j = j + 1)begin
            d1 = $random;
            d2 = $random;
            $display($time, ":    data_in_1: ", d1, "        data_in_2: ", d2);
            #20;
        end
        #30;
    end
end

endmodule //inoutPin_TB
```

و حاصل آن را در حالت تاخیر دیفالت، به صورت فرم موج زیر می بینیم:



و به صورت خروجی در ترمینال:



```
VSIM 41> run -all
#                  0:    data_in_1:  36      data_in_2: 129
#                  0:    data in 1 is :   x    data in 2 is :   x    data out 1 is :   x    data out 2 is :   x
#
#                 15:    data in 1 is :  36    data in 2 is : 129    data out 1 is : 129    data out 2 is : 129
#
#                 20:    data_in_1:   9      data_in_2:  99
#                 35:    data in 1 is :   9    data in 2 is :  99    data out 1 is :  99    data out 2 is :  99
#
#                 40:    data_in_1:  13      data_in_2: 141
#                 55:    data in 1 is :  13    data in 2 is : 141    data out 1 is : 141    data out 2 is : 141
#
#                 60:    data_in_1: 101      data_in_2:  18
#                 75:    data in 1 is : 101    data in 2 is :  18    data out 1 is :  18    data out 2 is :  18
#
#                110:    data_in_1:   1      data_in_2:  13
#                110:    data in 1 is : 101    data in 2 is :  18    data out 1 is : 101    data out 2 is : 101
#
#                125:    data in 1 is :   1    data in 2 is :  13    data out 1 is :   1    data out 2 is :   1
#
#                130:    data_in_1: 118      data_in_2:  61
#                145:    data in 1 is : 118    data in 2 is :  61    data out 1 is : 118    data out 2 is : 118
#
#                150:    data_in_1: 237      data_in_2: 140
#                165:    data in 1 is : 237    data in 2 is : 140    data out 1 is : 237    data out 2 is : 237
#
#                170:    data_in_1: 249      data_in_2: 198
#                185:    data in 1 is : 249    data in 2 is : 198    data out 1 is : 249    data out 2 is : 249
#

VSIM 42>
```

سوال ۴

۴- باتوجه‌به تجربیات خود در این تمرین، مدل‌سازی سطح گیت و مدل‌سازی جریان داده را با هم مقایسه کنید.

با استفاده از مدل سازی سطح گیت، دست باز بیشتری در طراحی و ایجاد جزئیات داریم، و تمرکز اصلی مان روی ارتباط گیت ها و مدار فیزیکی است در صورتی که در سطح مدل سازی جریان بیشتر تمرکز بر روی عملکرد است. در طراحی گیت لول، دقت بیشتری در تعیین زمان عملیات ها داریم و همچنین مدل سازی جریان داده سادگی بیشتری در نوشتن کد دارد.