**8.3 Feature Description**

**8.3.1 Multiplexer**

The device contains a very flexible input multiplexer, as shown in Figure 38. Either four single-ended signals, two differential signals, or a combination of two single-ended signals and one differential signal can be measured. The multiplexer is configured by four bits (MUX[3:0]) in the configuration register. When single-ended signals are measured, the negative ADC input (AINN) is internally connected to AVSS by a switch within the multiplexer. For system-monitoring purposes, the analog supply (AVDD – AVSS) / 4 or the currently-selected external reference voltage (V(REFPx) – V(REFNx)) / 4 can be selected as inputs to the ADC. The multiplexer also offers the possibility to route any of the two programmable current sources to any analog input (AINx) or to any dedicated reference pin (REFP0, REFN0).

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by Equation 4: AVSS – 0.3 V < V(AINx) < AVDD + 0.3 V (4) If the voltages on the input pins have any potential to violate these conditions, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unused input on the device may affect conversions taking place on other input pins. If any overdrive on unused inputs is possible, TI recommends clamping the signal with external Schottky diodes.

**8.3.2 Low-Noise PGA**

The device features a low-noise, low-drift, high input impedance, programmable gain amplifier (PGA). The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Three bits (GAIN[2:0]) in the configuration register are used to configure the gain. A simplified diagram of the PGA is shown in Figure 39. The PGA consists of two chopperstabilized amplifiers (A1 and A2) and a resistor feedback network that sets the PGA gain. The PGA input is equipped with an electromagnetic interference (EMI) filter.

VIN denotes the differential input voltage VIN = (V(AINP) – V(AINN)). The gain of the PGA can be calculated with Equation 5:

Gain = 1 + 2 · RF / RG (5)

Gain is changed inside the device using a variable resistor, RG. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in Equation 6:

FSR = ±Vref / Gain (6)

Table 9 shows the corresponding full-scale ranges when using the internal 2.048-V reference.

***8.3.2.1 PGA Common-Mode Voltage Requirements***

To stay within the linear operating range of the PGA, the input signals must meet certain requirements that are discussed in this section. The outputs of both amplifiers (A1 and A2) in Figure 39 can not swing closer to the supplies (AVSS and AVDD) than 200 mV. If the outputs OUTP and OUTN are driven to within 200 mV of the supply rails, the amplifiers saturate and consequently become nonlinear. To prevent this nonlinear operating condition the output voltages must meet Equation 7:

AVSS + 0.2 V ≤ V(OUTN), V(OUTP) ≤ AVDD – 0.2 V (7)

Translating the requirements of Equation 7 into requirements referred to the PGA inputs (AINP and AINN) is beneficial because there is no direct access to the outputs of the PGA. The PGA employs a symmetrical design, therefore the common-mode voltage at the output of the PGA can be assumed to be the same as the commonmode voltage of the input signal, as shown in Figure 40.

The common-mode voltage is calculated using Equation 8:

VCM = ½ (V(AINP) + V(AINN)) = ½ (V(OUTP) + V(OUTN)) (8)

The voltages at the PGA inputs (AINP and AINN) can be expressed as Equation 9 and Equation 10:

V(AINP) = VCM + ½ VIN (9)

V(AINN) = VCM – ½ VIN (10)

The output voltages (V(OUTP) and V(OUTN)) can then be calculated as Equation 11 and Equation 12:

V(OUTP) = VCM + ½ Gain · VIN (11)

V(OUTN) = VCM – ½ Gain · VIN (12)

The requirements for the output voltages of amplifiers A1 and A2 (Equation 7) can now be translated into requirements for the input common-mode voltage range using Equation 11 and Equation 12, which are given in Equation 13 and Equation 14:

VCM (MIN) ≥ AVSS + 0.2 V + ½ Gain · VIN (MAX) (13)

VCM (MAX) ≤ AVDD – 0.2 V – ½ Gain · VIN (MAX) (14)

In order to calculate the minimum and maximum common-mode voltage limits, the maximum differential input voltage (VIN (MAX)) that occurs in the application must be used. VIN (MAX) can be less than the maximum possible FS value. In addition to Equation 13, the minimum VCM must also meet Equation 15 because of the specific design implementation of the PGA.

VCM (MIN) ≥ AVSS + ¼ (AVDD – AVSS) (15)

Figure 41 and Figure 42 show a graphical representation of the common-mode voltage limits for AVDD = 3.3 V and AVSS = 0 V, with gain = 1 and gain = 16, respectively.

The following discussion explains how to apply Equation 13 through Equation 15 to a hypothetical application. The setup for this example is AVDD = 3.3 V, AVSS = 0 V, and gain = 16, using an external reference, Vref = 2.5 V. The maximum possible differential input voltage VIN = (V(AINP) – V(AINN)) that can be applied is then limited to the full-scale range of FSR = ±2.5 V / 16 = ±0.156 V. Consequently, Equation 13 through Equation 15 yield an allowed VCM range of 1.45 V ≤ VCM ≤ 1.85 V. If the sensor signal connected to the inputs in this hypothetical application does not make use of the entire fullscale range but is limited to VIN (MAX) = ±0.1 V, for example, then this reduced input signal amplitude relaxes the VCM restriction to 1.0 V ≤ VCM ≤ 2.3 V. In the case of a fully-differential sensor signal, each input (AINP, AINN) can swing up to ±50 mV around the common-mode voltage (V(AINP) + V(AINN)) / 2, which must remain between the limits of 1.0 V and 2.3 V. The output of a symmetrical wheatstone bridge is an example of a fully-differential signal. Figure 43 shows a situation where the common-mode voltage of the input signal is at the lowest limit. V(OUTN) is exactly at 0.2 V in this case. Any further decrease in common-mode voltage (VCM) or increase in differential input voltage (VIN) drives V(OUTN) below 0.2 V and saturates amplifier A2.

In contrast, the signal of an RTD is of a pseudo-differential nature (if implemented as shown in the *RTD Measurement* section), where the negative input is held at a constant voltage other than 0 V and only the voltage on the positive input changes. When a pseudo-differential signal must be measured, the negative input in this example must be biased at a voltage between 0.95 V and 2.25 V. The positive input can then swing up to VIN (MAX) = 100 mV above the negative input. Note that in this case the common-mode voltage changes at the same time the voltage on the positive input changes. That is, while the input signal swings between 0 V ≤ VIN ≤ VIN (MAX), the common-mode voltage swings between V(AINN) ≤ VCM ≤ V(AINN) + ½ VIN (MAX). Satisfying the common-mode voltage requirements for the maximum input voltage VIN (MAX) ensures the requirements are met throughout the entire signal range. Figure 44 and Figure 45 show examples of both fully-differential and pseudo-differential signals, respectively.

Remember, common-mode voltage requirements with PGA enabled (Equation 13 to Equation 15) are as follows:

• VCM (MIN) ≥ AVSS + ¼ (AVDD – AVSS)

• VCM (MIN) ≥ AVSS + 0.2 V + ½ Gain · VIN (MAX)

• VCM (MAX) ≤ AVDD – 0.2 V – ½ Gain · VIN (MAX)

***8.3.2.2 Bypassing the PGA***

At gains of 1, 2, and 4, the device can be configured to disable and bypass the low-noise PGA by setting the PGA\_BYPASS bit in the configuration register. Disabling the PGA lowers the overall power consumption and also removes the restrictions of Equation 13 through Equation 15 for the common-mode input voltage range, VCM. The usable absolute and common-mode input voltage range is (AVSS – 0.1 V ≤ V(AINx), VCM ≤ AVDD + 0.1 V) when the PGA is disabled. In order to measure single-ended signals that are referenced to AVSS (AINP = VIN, AINN = AVSS), the PGA must be bypassed. Configure the device for single-ended measurements by either connecting one of the analog inputs to AVSS externally or by using the internal AVSS connection of the multiplexer (MUX[3:0] settings 1000 through 1011). When configuring the internal multiplexer for settings where AINN = AVSS (MUX[3:0] = 1000 through 1011) the PGA is automatically bypassed and disabled irrespective of the PGA\_BYPASS setting and gain is limited to 1, 2, and 4. In case gain is set to greater than 4, the device limits gain to 4. When the PGA is disabled, the device uses a buffered switched-capacitor stage to obtain gains of 1, 2, and 4. An internal buffer in front of the switched-capacitor stage ensures that the effect on the input loading resulting from the capacitor charging and discharging is minimal. See Figure 21 to Figure 26 for the typical values of absolute input currents (current flowing into or out of each input) and differential input currents (difference in absolute current between positive and negative input) when the PGA is disabled. For signal sources with high output impedance, external buffering may still be necessary. Note that active buffers introduce noise and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

**8.3.3 Modulator**

A ΔΣ modulator is used in the ADS1220 to convert the analog input voltage into a pulse code modulated (PCM) data stream. The modulator runs at a modulator clock frequency of f(MOD) = f(CLK) / 16 in normal and duty-cycle mode and f(MOD) = f(CLK) / 8 in turbo mode, where f(CLK) is either provided by the internal oscillator or the external clock source. Table 10 shows the modulator frequency for each operating mode using either the internal oscillator or an external clock of 4.096 MHz.

**8.3.4 Digital Filter**

The device uses a linear-phase finite impulse response (FIR) digital filter that performs both filtering and decimation of the digital data stream coming from the modulator. The digital filter is automatically adjusted for the different data rates and always settles within a single cycle. At data rates of 5 SPS and 20 SPS, the filter can be configured to reject 50-Hz or 60-Hz line frequencies or to simultaneously reject 50 Hz and 60 Hz. Two bits (50/60[1:0]) in the configuration register are used to configure the filter accordingly. The frequency responses of the digital filter are illustrated in Figure 46 to Figure 59 for different output data rates using the internal oscillator or an external 4.096-MHz clock. The filter notches and output data rate scale proportionally with the clock frequency. For example, a notch that appears at 20 Hz when using a 4.096-MHz clock appears at 10 Hz if a 2.048-MHz clock is used. Note that the internal oscillator can vary over temperature as specified in the *Electrical Characteristics* table. The data rate or conversion time, respectively, and filter notches consequently vary by the same amount. Consider using an external precision clock source if a digital filter notch at a specific frequency with a tighter tolerance is required.

**8.3.5 Output Data Rate**

Table 11 shows the actual conversion times for each data rate setting. The values provided are in terms of t(CLK) cycles using an external clock with a clock frequency of f(CLK) = 4.096 MHz. The data rates scale proportionally in case an external clock with a frequency other than 4.096 MHz is used. Continuous conversion mode data rates are timed from one DRDY falling edge to the next DRDY falling edge. The first conversion starts 210 · t(CLK) (normal mode, duty-cycle mode) or 114 · t(CLK) (turbo mode) after the last SCLK falling edge of the START/SYNC command. Single-shot mode data rates are timed from the last SCLK falling edge of the START/SYNC command to the DRDY falling edge and rounded to the next t(CLK). In case the internal oscillator is used, an additional oscillator wake-up time of up to 50 μs (normal mode, duty-cycle mode) or 25 μs (turbo mode) must be added in single-shot mode. The internal oscillator starts to power up at the first SCLK rising edge of the START/SYNC command. If an SCLK frequency higher than 160 kHz (normal mode, duty-cycle mode) or 320 kHz (turbo mode) is used, the oscillator may not be fully powered up at the end of the START/SYNC command. The ADC then waits until the internal oscillator is fully powered up before starting a conversion. Single-shot conversion times in duty-cycle mode are the same as in normal mode. See the *Duty-Cycle Mode* section for more details on duty-cycle mode operation.

**8.3.6 Voltage Reference**

The device offers an integrated low-drift, 2.048-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the device offers two differential reference input pairs (REFP0, REFN0 and REFP1, REFN1). In addition, the analog supply (AVDD) can be used as a reference. The reference source is selected by two bits (VREF[1:0]) in the configuration register. By default, the internal reference is selected. The internal voltage reference requires less than 25 μs to fully settle after power-up, when coming out of power-down mode, or when switching from an external reference source to the internal reference. The differential reference inputs allow freedom in the reference common-mode voltage. REFP0 and REFN0 are dedicated reference inputs whereas REFP1 and REFN1 are shared with inputs AIN0 and AIN3, respectively. All reference inputs are internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference. When used in ratiometric applications, the reference inputs do not load the external circuitry. Note that the analog supply current increases when using an external reference because the reference buffers are enabled. In most cases the conversion result is directly proportional to the stability of the reference source. Any noise and drift of the voltage reference is reflected in the conversion result.

**8.3.7 Clock Source**

The device system clock can either be provided by the internal low-drift oscillator or by an external clock source on the CLK input. Connect the CLK pin to DGND before power-up or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator after two rising edges on the CLK pin are detected. The device then operates on the external clock. After the ADS1220 switches to the external clock, the device can only be switched back to the internal oscillator by cycling the power supplies or by sending a RESET command.

**8.3.8 Excitation Current Sources**

The device provides two matched programmable excitation current sources (IDACs) for RTD applications. The output current of the current sources can be programmed to 10 μA, 50 μA, 100 μA, 250 μA, 500 μA, 1000 μA, or 1500 μA using the respective bits (IDAC[2:0]) in the configuration register. Each current source can be connected to any of the analog inputs (AINx) as well as to any of the dedicated reference inputs (REFP0 and REFN0). Both current sources can also be connected to the same pin. Routing of the IDACs is configured by bits (I1MUX[2:0], I2MUX[2:0]) in the configuration register. Care must be taken not to exceed the compliance voltage of the IDACs. In other words, limit the voltage on the pin where the IDAC is routed to ≤ (AVDD – 0.9 V), otherwise the specified accuracy of the IDAC current is not met. For three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *3-Wire RTD Measurement* section for more details). The IDACs require up to 200 μs to start up after the IDAC current is programmed to the respective value using bits IDAC[2:0]. If configuration registers 2 and 3 are not written during the same WREG command, TI recommends to first set the IDAC current to the respective value using bits IDAC[2:0] and thereafter select the routing for each IDAC (I1MUX[2:0], I2MUX[2:0]). In single-shot mode, the IDACs remain active between any two conversions if the IDAC[2:0] bits are set to a value other than 000. However, the IDACs are powered down whenever the POWERDOWN command is issued. Note that the analog supply current increases when enabling the IDACs (that is, when the IDAC[2:0] bits are set to a value other than 000). The IDAC circuit needs this bias current to operate even when the IDACs are not routed to any pin (I1MUX[2:0] = I2MUX[2:0] = 000). In addition, the selected output current is drawn from the analog supply when I1MUX[2:0] or I2MUX[2:0] are set to a value other than 000.

**8.3.9 Low-Side Power Switch**

A low-side power switch with low on-resistance connected between the analog input AIN3/REFN1 and AVSS is integrated in the device as well. This power switch can be used to reduce system power consumption in bridge sensor applications by powering down the bridge circuit between conversions. When the respective bit (PSW) in the configuration register is set, the switch automatically closes when the START/SYNC command is sent and opens when the POWERDOWN command is issued. Note that the switch stays closed between conversions in single-shot mode in case the PSW bit is set to 1. The switch can be opened at any time by setting the PSW bit to 0. By default, the switch is always open.

**8.3.10 Sensor Detection** To help detect a possible sensor malfunction, the device provides internal 10-μA, burn-out current sources. When enabled by setting the respective bit (BCS) in the configuration register, one current source sources current to the positive analog input (AINP) currently selected while the other current source sinks current form the selected negative analog input (AINN). In case of an open circuit in the sensor, these burn-out current sources pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading may also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading may indicate a shorted sensor. Note that the absolute value of the burn-out current sources typically varies by ±10% and the internal multiplexer adds a small series resistance. Therefore, distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. In other words, even if the sensor is shorted, the voltage drop across the external filter resistance and the residual resistance of the multiplexer causes the output to read a value higher than zero. Keep in mind that ADC readings of a functional sensor may be corrupted when the burn-out current sources are enabled. TI recommends disabling the burn-out current sources when preforming the precision measurement, and only enabling them to test for sensor fault conditions.

**8.3.11 System Monitor**

The device provides some means for monitoring the analog power supply and the external voltage reference. To select a monitoring voltage, the internal multiplexer (MUX[3:0]) must be configured accordingly in the configuration register. The device automatically bypasses the PGA and sets the gain to 1, irrespective of the configuration register settings while the monitoring feature is used. Note that the system monitor function only provides a coarse result and is not meant to be a precision measurement. When measuring the analog power supply (MUX[3:0] = 1101), the resulting conversion is approximately (AVDD – AVSS) / 4. The device uses the internal 2.048-V reference for the measurement regardless of what reference source is selected in the configuration register (VREF[1:0]). When monitoring one of the two possible external reference voltage sources (MUX[3:0] = 1100), the result is approximately (V(REFPx) – V(REFNx)) / 4. REFPx and REFNx denote the external reference input pair selected in the configuration register (VREF[1:0]). The device automatically uses the internal reference for the measurement.

**8.3.12 Offset Calibration**

The internal multiplexer offers the option to short both PGA inputs (AINP and AINN) to mid-supply (AVDD + AVSS) / 2. This option can be used to measure and calibrate the device offset voltage by storing the result of the shorted input voltage reading in a microcontroller and consequently subtracting the result from each following reading. TI recommends taking multiple readings with the inputs shorted and averaging the result to reduce the effect of noise.

**8.3.13 Temperature Sensor**

The ADS1220 offers an integrated precision temperature sensor. The temperature sensor mode is enabled by setting bit TS = 1 in the configuration register. When in temperature sensor mode, the settings of configuration register 0 have no effect and the device uses the internal reference for measurement, regardless of the selected voltage reference source. Temperature readings follow the same process as the analog inputs for starting and reading conversion results. Temperature data are represented as a 14-bit result that is left-justified within the 24- bit conversion result. Data are output starting with the most significant byte (MSB). When reading the three data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format, as shown in Table 12.

***8.3.13.1 Converting from Temperature to Digital Codes***

**8.3.13.1.1 For Positive Temperatures (for Example, 50°C):**

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left-justified format with the MSB = 0 to denote the positive sign. Example: 50°C / (0.03125°C per count) = 1600 = 0640h = 00 0110 0100 0000

**8.3.13.1.2 For Negative Temperatures (for Example, –25°C):**

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1. Example: |–25°C| / (0.03125°C per count) = 800 = 0320h = 00 0011 0010 0000 Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

***8.3.13.2 Converting from Digital Codes to Temperature***

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all bits. Then, multiply the result by –0.03125°C. Example: The device reads back 0960h: 0960h has an MSB = 0. 0960h · 0.03125°C = 2400 · 0.03125°C = 75°C Example: The device reads back 3CE0h: 3CE0h has an MSB = 1. Subtract 1 and complement the result: 3CE0h → 0320h 0320h · (–0.03125°C) = 800 · (–0.03125°C) = –25°C

**8.4 Device Functional Modes**

**8.4.1 Power-Up and Reset**

When the device powers up, a reset is performed. The reset process takes approximately 50 μs. After this power-up reset time, all internal circuitry (including the voltage reference) are stable and communication with the device is possible. As part of the reset process, the device sets all bits in the configuration registers to the respective default settings. By default, the device is set to single-shot mode. After power-up, the device performs a single conversion using the default register settings and then enters a low-power state. When the conversion is complete, the DRDY pin transitions from high to low. The high-to-low transition of the DRDY pin can be used to signal that the ADS1220 is operational and ready to use. The power-up behavior is intended to prevent systems with tight power-supply requirements from encountering a current surge during power-up.

**8.4.2 Conversion Modes**

The device can be operated in one of two conversion modes that can be selected by the CM bit in the configuration register. These conversion modes are single-shot and continuous conversion mode.

***8.4.2.1 Single-Shot Mode***

In single-shot mode, the device only performs a conversion when a START/SYNC command is issued. The device consequently performs one single conversion and returns to a low-power state afterwards. The internal oscillator and all analog circuitry (except for the excitation current sources) are turned off while the device waits in this low-power state until the next conversion is started. In addition, every write access to any configuration register also starts a new conversion. Writing to any configuration register while a conversion is ongoing functions as a new START/SYNC command that stops the current conversion and restarts a single new conversion. Each conversion is fully settled (assuming the analog input signal settles to its final value before the conversion starts) because the device digital filter settles within a single cycle.

***8.4.2.2 Continuous Conversion Mode***

In continuous conversion mode, the device continuously performs conversions. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion. In order to start continuous conversion mode, the CM bit must be set to 1 followed by a START/SYNC command. The first conversion starts 210 · t(CLK) (normal mode, duty-cycle mode) or 114 · t(CLK) (turbo mode) after the last SCLK falling edge of the START/SYNC command. Writing to any configuration register during an ongoing conversion restarts the current conversion. TI recommends always sending a START/SYNC command immediately after the CM bit is set to 1.

**8.4.3 Operating Modes**

In addition to the different conversion modes, the device can also be operated in different operating modes that can be selected to trade-off power consumption, noise performance, and output data rate. These modes are: normal mode, duty-cycle mode, turbo mode, and power-down mode.

***8.4.3.1 Normal Mode***

Normal mode is the default mode of operation after power-up. In this mode, the internal modulator of the ΔΣ ADC runs at a modulator clock frequency of f(MOD) = f(CLK) / 16, where the system clock (f(CLK)) is either provided by the internal oscillator or the external clock source. The modulator frequency is 256 kHz when using the internal oscillator. Normal mode offers output data rate options ranging from 20 SPS to 1 kSPS with the internal oscillator. The data rate is selected by the DR[2:0] bits in the configuration register. In case an external clock source with a clock frequency other than 4.096 MHz is used, the data rates scale accordingly. For example, using an external clock with f(CLK) = 2.048 MHz yields data rates ranging from 10 SPS to 500 SPS.

***8.4.3.2 Duty-Cycle Mode***

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the device supports an automatic duty-cycle mode that can yield significant power savings by periodically entering a low-power state between conversions. In principle, the device runs in normal mode with a duty cycle of 25%. This functionality means the device performs one conversion in the same manner as when running in normal mode but then automatically enters a low power-state for three consecutive conversion cycles. The noise performance in duty-cycle mode is therefore comparable to the noise performance in normal mode at four times the data rate. Data rates in duty-cycle mode range from 5 SPS to 250 SPS with the internal oscillator.

***8.4.3.3 Turbo Mode***

Applications that require higher data rates up to 2 kSPS can operate the device in turbo mode. In this mode, the internal modulator runs at a higher frequency of f(MOD) = f(CLK) / 8. f(MOD) equals 512 kHz when the internal oscillator or an external 4.096-MHz clock is used. Note that the device power consumption increases because the modulator runs at a higher frequency. Running the ADS1220 in turbo mode at a comparable output data rate as in normal mode yields better noise performance. For example, the input-referred noise at 90 SPS in turbo mode is lower than the input-referred noise at 90 SPS in normal mode.

***8.4.3.4 Power-Down Mode***

When the POWERDOWN command is issued, the device enters power-down mode after completing the current conversion. In this mode, all analog circuitry (including the voltage reference and both IDACs) are powered down, the low-side power switch is opened, and the device typically only uses 400 nA of current. While in powerdown mode, the device holds the configuration register settings and responds to commands, but does not perform any data conversions. Issuing a START/SYNC command wakes up the device and either starts a single conversion or starts continuous conversion mode, depending on the conversion mode selected by the CM bit. Note that writing to any configuration register wakes up the device as well, but only starts a single conversion regardless of the selected conversion mode (CM).

**8.5 Programming**

**8.5.1 Serial Interface**

The SPI-compatible serial interface of the device is used to read conversion data, read and write the device configuration registers, and control device operation. Only SPI mode 1 (CPOL = 0, CPHA = 1) is supported. The interface consists of five control lines (CS, SCLK, DIN, DOUT/DRDY, and DRDY) but can be used with only four or even three control signals as well. The dedicated data-ready signal (DRDY) can be configured to be shared with DOUT/DRDY. If the serial bus is not shared with any other device, CS can be tied low permanently so that only signals SCLK, DIN, and DOUT/DRDY are required to communicate with the device.

***8.5.1.1 Chip Select (CS)***

Chip select (CS) is an active-low input that selects the device for SPI communication. This feature is useful when multiple devices share the same serial bus. CS must remain low for the duration of the serial communication. When CS is taken high, the serial interface is reset, SCLK is ignored, and DOUT/DRDY enters a high-impedance state; as such, DOUT/DRDY cannot indicate when data are ready. In situations where multiple devices are present on the bus, the dedicated DRDY pin can provide an uninterrupted monitor of the conversion status. If the serial bus is not shared with another peripheral, CS can be tied low.

***8.5.1.2 Serial Clock (SCLK)***

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data into and out of the device on the DIN and DOUT/DRDY pins, respectively. Even though the input has hysteresis, TI recommends keeping the SCLK signal as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

***8.5.1.3 Data Ready (DRDY)***

DRDY indicates when a new conversion result is ready for retrieval. When DRDY falls low, new conversion data are ready. DRDY transitions back high on the next SCLK rising edge. When no data are read during continuous conversion mode, DRDY remains low but pulses high for a duration of 2 · t(MOD) prior to the next DRDY falling edge. The DRDY pin is always actively driven, even when CS is high.

***8.5.1.4 Data Input (DIN)***

The data input pin (DIN) is used along with SCLK to send data (commands and register data) to the device. The device latches data on DIN on the SCLK falling edge. The device never drives the DIN pin.

***8.5.1.5 Data Output and Data Ready (DOUT/DRDY)***

DOUT/DRDY serves a dual-purpose function. This pin is used with SCLK to read conversion and register data from the device. Data on DOUT/DRDY are shifted out on the SCLK rising edge. DOUT/DRDY goes to a highimpedance state when CS is high. In addition, the DOUT/DRDY pin can also be configured as a data-ready indicator by setting the DRDYM bit high in the configuration register. DOUT/DRDY then transitions low at the same time that the DRDY pin goes low to indicate new conversion data are available. Both signals can be used to detect if new data are ready. However, because DOUT/DRDY is disabled when CS is high, the recommended method of monitoring the end of a conversion when multiple devices are present on the SPI bus is to use the dedicated DRDY pin.

***8.5.1.6 SPI Timeout***

The ADS1220 offers an SPI timeout feature that can be used to recover communication when a serial interface transmission is interrupted. This feature is especially useful in applications where CS is permanently tied low and is not used to frame a communication sequence. Whenever a complete command is not sent within 13955 · t(MOD) (normal mode, duty-cycle mode) or 27910 · t(MOD) (turbo mode), the serial interface resets and the next SCLK pulse starts a new communication cycle. See the *Modulator* section for details on the modulator frequency (f(MOD) = 1 / t(MOD)) in the different operating modes. For the RREG and WREG commands, a *complete command* includes the command byte itself plus the register bytes that are read or written.

**8.5.2 Data Format**

The device provides 24 bits of data in binary twos complement format. The size of one code (LSB) is calculated using Equation 16. 1 LSB = (2 · Vref / Gain) / 224 = +FS / 223 (16) A positive full-scale input [VIN ≥ (+FS – 1 LSB) = (Vref / Gain – 1 LSB)] produces an output code of 7FFFFFh and a negative full-scale input (VIN ≤ –FS = –Vref / Gain) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale. Table 13 summarizes the ideal output codes for different input signals.

**8.5.3 Commands**

The device offers six different commands to control device operation, as shown in Table 14. Four commands are stand-alone instructions (RESET, START/SYNC, POWERDOWN, and RDATA). The commands to read (RREG) and write (WREG) configuration register data from and to the device require additional information as part of the instruction.

***8.5.3.1 RESET (0000 011x)***

Resets the device to the default values. Wait at least (50 μs + 32 · t(CLK)) after the RESET command is sent before sending any other command.

***8.5.3.2 START/SYNC (0000 100x)***

In single-shot mode, the START/SYNC command is used to start a single conversion, or (when sent during an ongoing conversion) to reset the digital filter, and then restarts a single new conversion. When the device is set to continuous conversion mode, the START/SYNC command must be issued one time to start converting continuously. Sending the START/SYNC command while converting in continuous conversion mode resets the digital filter and restarts continuous conversions.

***8.5.3.3 POWERDOWN (0000 001x)***

The POWERDOWN command places the device into power-down mode. This command shuts down all internal analog components, opens the low-side switch, turns off both IDACs, but holds all register values. In case the POWERDOWN command is issued while a conversion is ongoing, the conversion completes before the ADS1220 enters power-down mode. As soon as a START/SYNC command is issued, all analog components return to their previous states.

***8.5.3.4 RDATA (0001 xxxx)***

The RDATA command loads the output shift register with the most recent conversion result. This command can be used when DOUT/DRDY or DRDY are not monitored to indicate that a new conversion result is available. If a conversion finishes in the middle of the RDATA command byte, the state of the DRDY pin at the end of the read operation signals whether the old or the new result is loaded. If the old result is loaded, DRDY stays low, indicating that the new result is not read out. The new conversion result loads when DRDY is high.

***8.5.3.5 RREG (0010 rrnn)***

The RREG command reads the number of bytes specified by *nn* (number of bytes to be read – 1) from the device configuration register, starting at register address rr. The command is completed after nn + 1 bytes are clocked out after the RREG command byte. For example, the command to read three bytes (nn = 10) starting at configuration register 1 (rr = 01) is 0010 0110.

***8.5.3.6 WREG (0100 rrnn)***

The WREG command writes the number of bytes specified by *nn* (number of bytes to be written – 1) to the device configuration register, starting at register address rr. The command is completed after nn + 1 bytes are clocked in after the WREG command byte. For example, the command to write two bytes (nn = 01) starting at configuration register 0 (rr = 00) is 0100 0001. The configuration registers are updated on the last SCLK falling edge.

**8.5.4 Reading Data**

Output pins DRDY and DOUT/DRDY (if the DRDYM bit is set high in the configuration register) transition low when new data are ready for retrieval. The conversion data are written to an internal data buffer. Data can be read directly from this buffer on DOUT/DRDY when DRDY falls low without concern of data corruption. An RDATA command does not have to be sent. Data are shifted out on the SCLK rising edges, MSB first, and consist of three bytes of data. Figure 61 to Figure 63 show the timing diagrams for reading conversion data in continuous conversion mode and single-shot mode when not using the RDATA command. Data can also be read at any time without synchronizing to the DRDY signal using the RDATA command. When an RDATA command is issued, the conversion result currently stored in the data buffer is shifted out on DOUT/DRDY on the following SCLK rising edges. Data can be read continuously with the RDATA command as an alternative to monitoring DRDY or DOUT/DRDY. The DRDY pin can be polled after the LSB is clocked out to determine if a new conversion result was loaded. If a new conversion completes during the read operation but data from the previous conversion are read, then DRDY is low. Otherwise, if the most recent result is read, DRDY is high. Figure 64 and Figure 65 illustrate the behavior for both cases.

**8.5.5 Sending Commands**

The device serial interface is capable of full-duplex operation while reading conversion data when not using the RDATA command. Full-duplex operation means commands are decoded at the same time that conversion data are read. Commands can be sent on any 8-bit data boundary during a data read operation. When a RREG or RDATA command is recognized, the current data read operation is aborted and the conversion data are corrupted, unless the command is sent while the last byte of the conversion result is retrieved. The device starts to output the requested data on DOUT/DRDY at the first SCLK rising edge after the command byte. To read data without interruption, keep DIN low while clocking out data. A WREG command can be sent without corrupting an ongoing read operation. Figure 66 shows an example for sending a WREG command to write two configuration registers while reading conversion data in continuous conversion mode. After the command is clocked in (after the 32nd SCLK falling edge), the device resets the digital filter and starts converting with the new register settings. The WREG command can be sent on any of the 8-bit boundaries.

Note that the serial interface does not decode commands while an RDATA or RREG command is executed. That is, all 24 bits of the conversion result must be read after the RDATA command is issued and all requested registers must be read after a RREG command is sent before a new command can be issued.

**8.5.6 Interfacing with Multiple Devices**

When connecting multiple ADS1220 devices to a single SPI bus, SCLK, DIN, and DOUT/DRDY can be safely shared by using a dedicated chip-select (CS) line for each SPI-enabled device. When CS transitions high for the respective device, DOUT/DRDY enters a 3-state mode. Therefore, DOUT/DRDY cannot be used to indicate when new data are available if CS is high, regardless of the DRDYM bit setting in the configuration register. Only the dedicated DRDY pin indicates that new data are available, because the DRDY pin is actively driven even when CS is high. In some cases the DRDY pin cannot be interfaced to the microcontroller. This scenario can occur if there are insufficient GPIO channels available on the microcontroller or if the serial interface must be galvanically isolated and thus the amount of channels must be limited. Therefore, in order to evaluate when a new conversion of one of the devices is ready, the microcontroller can periodically drop CS to the respective device and poll the state of the DOUT/DRDY pin. When CS goes low, the DOUT/DRDY pin immediately drives either high or low, provided that the DRDYM bit is configured to 1. If the DOUT/DRDY line drives low, when CS is taken low, new data are currently available. If the DOUT/DRDY line drives high, no new data are available. This procedure requires that DOUT/DRDY is high after reading each conversion result and before taking CS high. To make sure DOUT/DRDY is taken high, send 8 additional SCLKs with DIN held low after each data read operation. DOUT/DRDY reads high during the eight SCLKs after the conversion result is read, as shown in Figure 67. Alternatively, valid data can be retrieved from the device at any time without concern of data corruption by using the RDATA command.

**8.6 Register Map**

**8.6.1 Configuration Registers**

The device has four 8-bit configuration registers that are accessible through the serial interface using the RREG and WREG commands. The configuration registers control how the device operates and can be changed at any time without causing data corruption. After power-up or reset, all registers are set to the default values (which are all 0). All registers retain their values during power-down mode. Table 15 shows the register map of the configuration registers.

***8.6.1.1 Configuration Register 0 (offset = 00h) [reset = 00h]***

***8.6.1.2 Configuration Register 1 (offset = 01h) [reset = 00h]***

***8.6.1.3 Configuration Register 2 (offset = 02h) [reset = 00h]***

***8.6.1.4 Configuration Register 3 (offset = 03h) [reset = 00h]***

**6.6 SPI Timing Requirements**

over operating ambient temperature range and DVDD = 2.3 V to 5.5 V (unless otherwise noted)

**PARAMTER ; MIN ; MAX ; UNIT**

td(CSSC) Delay time, CS falling edge to first SCLK rising edge(1) ; 50 ; ; ns

td(SCCS) Delay time, final SCLK falling edge to CS rising edge ; 25 ; ; ns

tw(CSH) Pulse duration, CS high ; 50 ; ; ns

tc(SC) SCLK period ; 150 ; ; ns

tw(SCH) Pulse duration, SCLK high ; 60 ; ; ns

tw(SCL) Pulse duration, SCLK low ; 60 ; ; ns

tsu(DI) Setup time, DIN valid before SCLK falling edge ; 50 ; ; ns

th(DI) Hold time, DIN valid after SCLK falling edge ; 25 ; ; ns

SPI timeout(2) Normal mode, duty-cycle mode ; ; 13955 ; t(MOD)

Turbo mode ; ; 27910 ; t(MOD)

(1) CS can be tied low permanently in case the serial bus is not shared with any other device. (2) See the *SPI Timeout* section for more information.

t(MOD) = 1 / f(MOD). Modulator frequency f(MOD) = 256 kHz (normal mode, duty-cycle mode) and 512 kHz (turbo mode), when using the internal oscillator or an external 4.096-MHz clock.

**6.7 SPI Switching Characteristics**

over operating ambient temperature range, DVDD = 2.3 V to 5.5 V (unless otherwise noted)

**PARAMETER ; TEST CONDITIONS ; MIN ; TYP ; MAX ; UNIT**

tp(CSDO) Propagation delay time, CS falling edge to DOUT driven ; DOUT load = 20 pF || 10 kΩ to DGND ; ; ; 50 ; ns

tp(SCDO) Propagation delay time, SCLK rising edge to valid new DOUT ; DOUT load = 20 pF || 10 kΩ to DGND ; 0 ; ; 50 ; ns

tp(CSDOZ) Propagation delay time, CS rising edge to DOUT high impedance ; DOUT load = 20 pF || 10 kΩ to DGND ; ; ; 50 ; ns

**9.2 Typical Applications**

**9.2.1 K-Type Thermocouple Measurement (–200°C to +1250°C)**

Figure 74 shows the basic connections of a thermocouple measurement system when using the internal highprecision temperature sensor for cold-junction compensation. Apart from the thermocouple itself, the only external circuitry required are two biasing resistors, a simple low-pass, antialiasing filter, and the power-supply decoupling capacitors.

***9.2.1.1 Design Requirements***

***Table 21. Design Requirements***

***DESIGN PARAMETER ; VALUE***

***Supply voltage ; 3.3 V***

***Reference voltage ; Internal 2.048-V reference***

***Update rate ; ≥10 readings per second***

***Thermocouple type ; K***

***Temperature measurement range ; –200°C to +1250°C***

***Measurement accuracy at TA = 25°C(1) ; ±0.2°C***

***9.2.1.2 Detailed Design Procedure***

The biasing resistors RB1 and RB2 are used to set the common-mode voltage of the thermocouple to within the specified common-mode voltage range of the PGA (in this example, to mid-supply AVDD / 2). If the application requires the thermocouple to be biased to GND, either a bipolar supply (for example, AVDD = 2.5 V and AVSS = –2.5 V) must be used for the device to meet the common-mode voltage requirement of the PGA, or the PGA must be bypassed. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

In addition to biasing the thermocouple, RB1 and RB2 are also useful for detecting an open thermocouple lead. When one of the thermocouple leads fails open, the biasing resistors pull the analog inputs (AIN0 and AIN1) to AVDD and AVSS, respectively. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition. Although the device digital filter attenuates high-frequency components of noise, TI recommends providing a firstorder, passive RC filter at the inputs to further improve performance. The differential RC filter formed by RF1, RF2, and the differential capacitor CDIF offers a cutoff frequency that is calculated using Equation 17. fC = 1 / [2π · (RF1 + RF2) · CDIF] (17) Two common-mode filter capacitors (CM1 and CM2) are also added to offer attenuation of high-frequency, common-mode noise components. TI recommends that the differential capacitor CDIF be at least an order of magnitude (10x) larger than the common-mode capacitors (CM1 and CM2) because mismatches in the commonmode capacitors can convert common-mode noise into differential noise. The filter resistors RF1 and RF2 also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AIN0 and AIN1) of the device to safe levels if an overvoltage on the inputs occur. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. TI recommends limiting the filter resistor values to below 1 kΩ. The filter component values used in this design are: RF1 = RF2 = 1 kΩ, CDIF = 100 nF, and CCM1 = CCM2 = 10 nF. The highest measurement resolution is achieved when matching the largest potential input signal to the FSR of the ADC by choosing the highest possible gain. From the design requirement, the maximum thermocouple voltage occurs at T(TC) = 1250°C and is V(TC) = 50.644 mV as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature of T(CJ) = 0°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at T(TC) = 1250°C produces an output voltage of V(TC) = 50.644 mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of T(CJ) = –40°C. The maximum gain that can be applied when using the internal 2.048-V reference is then calculated as (2.048 V / 52.171 mV) = 39.3. The next smaller PGA gain setting the device offers is 32. The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. To measure the internal temperature of the ADS1220, the device must be set to internal temperature sensor mode by setting the TS bit to 1 in the configuration register. For best performance, careful board layout is critical to achieve good thermal conductivity between the cold junction and the device package. However, the device does not perform automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces to the device. The microcontroller requests one or multiple readings of the thermocouple voltage from the device and then sets the device to internal temperature sensor mode (TS = 1) to acquire the temperature of the cold junction. An algorithm similar to the following must be implemented on the microcontroller to compensate for the cold-junction temperature: 1. Measure the thermocouple voltage, V(TC), between AIN0 and AIN1. 2. Measure the temperature of the cold junction, T(CJ), using the temperature sensor mode of the ADS1220. 3. Convert the cold-junction temperature into an equivalent thermoelectric voltage, V(CJ), using the tables or equations provided by NIST. 4. Add V(TC) and V(CJ) and translate the summation back into a thermocouple temperature using the NIST tables or equations again. In some applications, the integrated temperature sensor of the ADS1220 cannot be used (for example, if the accuracy is not high enough or if the device cannot be placed close enough to the cold junction). The additional analog input channels of the device can be used in this case to measure the cold-junction temperature with a thermistor, RTD, or an analog temperature sensor. To get an approximation of the achievable temperature resolution, the rms-Noise of the ADS1220 at Gain = 32 and DR = 20 SPS (0.23 μVrms) is divided by the average sensitivity of a K-type thermocouple (41 μV/°C), as shown in Equation 18. Temperature Resolution = 0.23 μV / 41 μV/°C = 0.006°C (18)

***9.2.1.3 Application Curves***

Figure 75 and Figure 76 show the measurement results. The measurements are taken at TA = T(CJ) = 25°C. A system offset calibration is performed at T(TC) = 25°C, which translates to a V(TC) = 0 V when T(CJ) = 25°C. No gain calibration is implemented. The data in Figure 75 are taken using a precision voltage source as the input signal instead of a thermocouple. The respective temperature measurement error in Figure 76 is calculated from the data in Figure 75 using the NIST tables. The design meets the required temperature measurement accuracy given in Table 21. Note that the measurement error shown in Figure 76 does not include the error of the thermocouple itself and the measurement error of the cold-junction temperature. Those two error sources are in general larger than 0.2°C and therefore, in many cases, dominate the overall system measurement accuracy.

**9.2.2 3-Wire RTD Measurement (–200°C to +850°C)**

The ADS1220 integrates all necessary features (such as dual-matched programmable current sources, buffered reference inputs, and a PGA) to ease the implementation of ratiometric 2-, 3-, and 4-wire RTD measurements. Figure 77 shows a typical implementation of a ratiometric 3-wire RTD measurement using the excitation current sources integrated in the device to excite the RTD as well as to implement automatic RTD lead-resistance compensation.

**9.2.2.1 Design Requirements**

**Table 23. Design Requirements**

**DESIGN PARAMETER ; VALUE**

Supply voltage ; 3.3 V

Update rate ; 20 readings per second

RTD type ; 3-wire Pt100

Maximum RTD lead resistance ; 15 Ω

RTD excitation current ; 500 μA

Temperature measurement range ; –200°C to +850°C

Measurement accuracy at TA = 25°C(1) ; ±0.2°C

***9.2.2.2 Detailed Design Procedure***

The circuit in Figure 77 employs a ratiometric measurement approach. In other words, the sensor signal (that is, the voltage across the RTD in this case) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise of the excitation source cancel out because these errors are common to both the sensor signal and the reference.

In order to implement a ratiometric 3-wire RTD measurement using the device, IDAC1 is routed to one of the leads of the RTD and IDAC2 is routed to the second RTD lead. Both currents have the same value, which is programmable by the IDAC[2:0] bits in the configuration register. The design of the device ensures that both IDAC values are closely matched, even across temperature. The sum of both currents flows through a precision, low-drift reference resistor, RREF. The voltage, Vref, generated across the reference resistor (as shown in Equation 19) is used as the ADC reference voltage. Equation 19 reduces to Equation 20 because IIDAC1 = IIDAC2. Vref = (IIDAC1 + IIDAC2) · RREF (19) Vref = 2 · IIDAC1 · RREF (20) To simplify the following discussion, the individual lead resistance values of the RTD (RLEADx) are set to zero. Only IDAC1 excites the RTD to produce a voltage (VRTD) proportional to the temperature-dependable RTD value and the IDAC1 value, as shown in Equation 21. VRTD = RRTD (at temperature) · IIDAC1 (21) The device internally amplifies the voltage across the RTD using the PGA and compares the resulting voltage against the reference voltage to produce a digital output code proportional to Equation 22 through Equation 24: Code ∝ VRTD · Gain / Vref (22) Code ∝ (RRTD (at temperature) · IIDAC1 · Gain) / (2 · IIDAC1 · RREF) (23) Code ∝ (RRTD (at temperature) · Gain) / (2 · RREF) (24) As can be seen from Equation 24, the output code only depends on the value of the RTD, the PGA gain, and the reference resistor (RREF), but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter. However, because the value of the reference resistor directly affects the measurement result, choosing a reference resistor with a very low temperature coefficient is important to limit errors introduced by the temperature drift of RREF. The second IDAC2 is used to compensate for errors introduced by the voltage drop across the lead resistance of the RTD. All three leads of a 3-wire RTD typically have the same length and, thus, the same lead resistance. Also, IDAC1 and IDAC2 have the same value. Taking the lead resistance into account, the differential voltage (VIN) across the ADC inputs, AIN0 and AIN1, is calculated using Equation 25: VIN = IIDAC1 · (RRTD + RLEAD1) – IIDAC2 · RLEAD2 (25) When RLEAD1 = RLEAD2 and IIDAC1 = IIDAC2, Equation 25 reduces to Equation 26: VIN = IIDAC1 · RRTD (26) In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated, as long as the lead resistance values and the IDAC values are well matched. A first-order differential and common-mode RC filter (RF1, RF2, CDIF1, CCM1, and CCM2) is placed on the ADC inputs, as well as on the reference inputs (RF3, RF4, CDIF2, CCM3, and CCM4). The same guidelines for designing the input filter apply as described in the *Thermocouple Measurement* section. For best performance, TI recommends matching the corner frequencies of the input and reference filter. More detailed information on matching the input and reference filter can be found in application report *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248* (SBAA201). The reference resistor RREF not only serves to generate the reference voltage for the device, but also sets the common-mode voltage of the RTD to within the specified common-mode voltage range of the PGA. When designing the circuit, care must also be taken to meet the compliance voltage requirement of the IDACs. The IDACs require that the maximum voltage drop developed across the current path to AVSS be equal or less than AVDD – 0.9 V in order to operate accurately. This requirement means that Equation 27 must be met at all times. AVSS + IIDAC1 · (RLEAD1 + RRTD) + (IIDAC1 + IIDAC2) · (RLEAD3 + RREF) ≤ AVDD – 0.9 V (27) The device also offers the possibility to route the IDACs to the same inputs used for measurement. If the filter resistor values RF1 and RF2 are small enough and well matched, IDAC1 can be routed to AIN1 and IDAC2 to AIN0 in Figure 77. In this manner, even two 3-wire RTDs sharing the same reference resistor can be measured with a single device.

This design example discusses the implementation of a 3-wire Pt100 measurement to be used to measure temperatures ranging from –200°C to +850°C as stated in Table 23. The excitation current for the Pt100 is chosen as IIDAC1 = 500 μA, which means a combined current of 1 mA is flowing through the reference resistor, RREF. As mentioned previously, besides creating the reference voltage for the ADS1220, the voltage across RREF also sets the common-mode voltage for the RTD measurement. In general, choose the largest reference voltage possible while still maintaining the compliance voltage of the IDACs as well as meeting the common-mode voltage requirement of the PGA. TI recommends setting the common-mode voltage at or near half the analog supply (in this case 3.3 V / 2 = 1.65 V), which in most cases satisfies the common-mode voltage requirements of the PGA. The value for RREF is then calculated by Equation 28: RREF = Vref / (IIDAC1 + IIDAC2) = 1.65 V / 1 mA = 1.65 kΩ (28) The stability of RREF is critical to achieve good measurement accuracy over temperature and time. Choosing a reference resistor with a temperature coefficient of ±10 ppm/°C or better is advisable. If a 1.65 kΩ value is not readily available, another value near 1.65 kΩ (such as 1.62 kΩ or 1.69 kΩ) can certainly be used as well. As a last step, the PGA gain must be selected in order to match the maximum input signal to the FSR of the ADC. The resistance of a Pt100 increases with temperature. Therefore, the maximum voltage to be measured (VIN(MAX)) occurs at the positive temperature extreme. At 850°C, a Pt100 has an equivalent resistance of approximately 391 Ω as per the NIST tables. The voltage across the Pt100 equates to Equation 29: VIN (MAX) = VRTD (at 850°C) = RRTD (at 850°C) · IIDAC1 = 391 Ω · 500 μA = 195.5 mV (29) The maximum gain that can be applied when using a 1.65-V reference is then calculated as (1.65 V / 195.5 mV) = 8.4. The next smaller PGA gain setting available in the ADS1220 is 8. At a gain of 8, the ADS1220 offers a FSR value as described in Equation 30: FSR = ±Vref / Gain = ±1.65 V / 8 = ±206.25 mV (30) This range allows for margin with respect to initial accuracy and drift of the IDACs and reference resistor. After selecting the values for the IDACs, RREF, and PGA gain, make sure to double check that the settings meet the common-mode voltage requirements of the PGA and the compliance voltage of the IDACs. To determine the true common-mode voltage at the ADC inputs (AIN0 and AIN1) the lead resistance must be taken into account as well. The smallest common-mode voltage occurs at the lowest measurement temperature (–200°C) with RLEADx = 0 Ω and is calculated using Equation 31 and Equation 32. VCM (MIN) = Vref + (IIDAC1 + IIDAC2) · RLEAD3 + IIDAC2 · RLEAD2 + ½ IIDAC1 · RRTD (at –200°C) (31) VCM (MIN) = 1.65 V + ½ 500 μA · 18.52 Ω = 1.655 V (32) Actually, assuming VCM (MIN) = Vref is a sufficient approximation. VCM (MIN) must meet two requirements: Equation 15 requires VCM (MIN) to be larger than AVDD / 4 = 3.3 V / 4 = 0.825 V and Equation 13 requires VCM (MIN) to meet Equation 33: VCM (MIN) ≥ AVSS + 0.2 V + ½ Gain · VIN (MAX) = 0 V + 0.2 V + ( ½ · 8 · 195.5 mV) = 982 mV (33) Both restrictions are satisfied in this design with a VCM (MIN) = 1.65 V. The largest common-mode voltage occurs at the highest measurement temperature (850°C) and is calculated using Equation 34 and Equation 35. VCM (MAX) = Vref + (IIDAC1 + IIDAC2) · RLEAD3 + IIDAC2 · RLEAD2 + ½ IIDAC1 · RRTD (at 850°C) (34) VCM (MAX) = 1.65 V + 1 mA · 15 Ω + 500 μA · 15 Ω + ½ 500 μA · 391 Ω = 1.77 V (35) VCM (MAX) does meet the requirement given by Equation 14, which in this design equates to Equation 36: VCM (MAX) ≤ AVDD – 0.2 V – ½ Gain · VIN (MAX) = 3.3 V – 0.2 V – ( ½ · 8 · 195.5 mV) = 2.318 V (36) Finally, the maximum voltage that can occur on input AIN1 must be calculated to determine if the compliance voltage (AVDD – 0.9 V = 3.3 V – 0.9 V = 2.4 V) of IDAC1 is met. Note that the voltage on input AIN0 is smaller than the one on input AIN1. Equation 37 and Equation 38 show that the voltage on AIN1 is less than 2.4 V, even when taking the worst-case lead resistance into account. VAIN1 (MAX) = Vref + (IIDAC1 + IIDAC2) · RLEAD3 + IIDAC1 · (RRTD (at 850°C) + RLEAD1) (37) VAIN1 (MAX) = 1.65 V + 1 mA · 15 Ω + 500 μA · (391 Ω + 15 Ω) = 1.868 V (38)

The register settings for this design are shown in Table 24.

**Table 24. Register Settings**

**REGISTER ; SETTING ; DESCRIPTION**

00h ; 66h ; AINP = AIN1, AINN = AIN0, gain = 8, PGA enabled

01h ; 04h ; DR = 20 SPS, normal mode, continuous conversion mode

02h ; 55h ; External reference (REFP0, REFN0), simultaneous 50-Hz and 60-Hz rejection, IDAC = 500 μA

03h ; 70h ; IDAC1 = AIN2, IDAC2 = AIN3

**9.2.2.2.1 Design Variations for 2-Wire and 4-Wire RTD Measurements**

Implementing a 2- or 4-wire RTD measurement is very similar to the 3-wire RTD measurement illustrated in Figure 77, except that only one IDAC is required. Figure 78 shows a typical circuit implementation of a 2-wire RTD measurement. The main difference compared to a 3-wire RTD measurement is with respect to the lead resistance compensation. The voltage drop across the lead resistors, RLEAD1 and RLEAD2, in this configuration is directly part of the measurement (as shown in Equation 39) because there is no means to compensate the lead resistance by use of the second current source. Any compensation must be done by calibration. VIN = IIDAC1 · (RLEAD1 + RRTD + RLEAD2) (39)

Figure 79 shows a typical circuit implementation of a 4-wire RTD measurement. Similar to the 2-wire RTD measurement, only one IDAC is required for exciting and measuring a 4-wire RTD in a ratiometric manner. The main benefit of using a 4-wire RTD is that the ADC inputs are connected to the RTD in the form of a Kelvin connection. Apart from the input leakage currents of the ADC, there is no current flow through the lead resistors RLEAD2 and RLEAD3 and therefore no voltage drop is created across them. The voltage at the ADC inputs consequently equals the voltage across the RTD and the lead resistance is of no concern.

Note that because only one IDAC is used and flows through the reference resistor, RREF, the transfer function of a 2- and 4-wire RTD measurement differs compared to the one of a 3-wire RTD measurement by a factor of 2, as shown in Equation 40. Code ∝ (RRTD (at Temperature) · Gain) / RREF (40) In addition, the common-mode and reference voltage is reduced compared to the 3-wire RTD configuration. Therefore, some further modifications may be required in case the 3-wire RTD design is used to measure 2- and 4-wire RTDs as well. If the decreased common-mode voltage does not meet the VCM (MIN) requirements of the PGA anymore, either increase the value of RREF by switching in a larger resistor or, alternatively, increase the excitation current while decreasing the gain at the same time.

***9.2.2.3 Application Curves***

Figure 80 and Figure 81 show the measurement results. The measurements are taken at TA = 25°C. A system offset calibration is performed using a reference resistor of 100 Ω. No gain calibration is implemented. The data in Figure 80 are taken using precision resistors instead of a 3-wire Pt100. The respective temperature measurement error in Figure 81 is calculated from the data in Figure 80 using the NIST tables. The design meets the required temperature measurement accuracy given in Table 23. Note that the measurement error shown in Figure 81 does not include the error of the RTD itself.

**9.2.3 Resistive Bridge Measurement**

The device offers several features to ease the implementation of ratiometric bridge measurements (such as a PGA with gains up to 128, buffered, differential reference inputs, and a low-side power switch).

***9.2.3.1 Design Requirements***

**Table 25. Design Requirements**

**DESIGN PARAMETER ; VALUE**

Analog supply voltage ; 5.0 V

Digital supply voltage ; 3.3 V

Load cell type ; 4-wire load cell

Load cell maximum capacity ; 1 kg

Load cell sensitivity ; 3 mV/V

Excitation voltage ; 5 V

Repeatability ; 50 mg

***9.2.3.2 Detailed Design Procedure***

To implement a ratiometric bridge measurement, the bridge excitation voltage is simultaneously used as the reference voltage for the ADC, as shown in Figure 82. With this configuration, any drift in excitation voltage also shows up on the reference voltage, consequently canceling out drift error. Either of the two device reference input pairs can be connected to the bridge excitation voltage. However, only the negative reference input (REFN1) can be internally routed to a low-side power switch. By connecting the low side of the bridge to REFN1, the device can automatically power-down the bridge by opening the low-side power switch. When the PSW bit in the configuration register is set to 1, the device opens the switch every time a POWERDOWN command is issued and closes the switch again when a START/SYNC command is sent. The PGA offers gains up to 128, which helps amplify the small differential bridge output signal to make optimal use of the ADC full-scale range. Using a symmetrical bridge with the excitation voltage equal to the supply voltage of the device ensures that the output signal of the bridge meets the common-mode voltage requirement of the PGA.

Note that the maximum input voltage of ADS1220 is limited to VIN (MAX) = ±[(AVDD – AVSS) – 0.4 V] / Gain, which means the entire full-scale range, FSR = ±(AVDD – AVSS) / Gain, cannot be used in this configuration. This limitation is a result of the output drive capability of the PGA amplifiers (A1 and A2); see Figure 39. The output of each amplifier must stay 200 mV away from the rails (AVDD and AVSS), otherwise the PGA becomes nonlinear. Consequently, the maximum output swing of the PGA is limited to VOUT = ±[(AVDD – AVSS) – 0.4 V]. Using a 3-mV/V load cell with a 5-V excitation yields a maximum differential output voltage of VIN (MAX) = ±15 mV, which meets Equation 41 when using a gain of 128. VIN (MAX) ≤ ±[(AVDD – AVSS) – 0.4 V] / Gain = ±(5 V – 0.4 V) / 128 = ±36 mV (41) A first-order differential and common-mode RC filter (RF1, RF2, CDIF1, CCM1, and CCM2) is placed on the ADC inputs. The reference has an additional capacitor CDIF2 to limit reference noise. Care must be taken to maintain a limited amount of filtering or the measurement is no longer ratiometric. To find the repeatability of the readings, perform the following calculation. The load cell produces an output voltage of 15 mV at the maximum load of 1 kg. At a Gain = 128 and DR = 20 SPS the ADS1220 offers a noisefree resolution of 0.41 μVpp. The repeatability is then calculated as shown in Equation 42. Repeatability = (1 kg / 15 mV) · 0.41 μV = 27 mg (42) The register settings for this design are shown in Table 26.

**Table 26. Register Settings**

**REGISTER ; SETTING ; DESCRIPTION**

00h ; 3Eh ; AINP = AIN1, AINN = AIN2, gain = 128, PGA enabled

01h ; 04h ; DR = 20 SPS, normal mode, continuous conversion mode

02h ; 98h ; External reference (REFP1, REFN1), simultaneous 50-Hz and 60-Hz rejection, PSW = 1

03h ; 00h ; No IDACs used

**7 Parameter Measurement Information**

**7.1 Noise Performance**

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the inputreferred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals. Table 1 to Table 8 summarize the device noise performance. Data are representative of typical noise performance at TA = 25°C using the internal 2.048-V reference. Data shown are the result of averaging readings from a single device over a time period of approximately 0.75 seconds and are measured with the inputs internally shorted together. Table 1, Table 3, Table 5 and Table 7 list the input-referred noise in units of μVRMS for the conditions shown. Note that μVPP values are shown in parenthesis. Table 2, Table 4, Table 6 and Table 8 list the corresponding data in effective number of bits (ENOB) calculated from μVRMS values using Equation 1. Note that noise-free bits calculated from peak-to-peak noise values using Equation 2 are shown in parenthesis. The input-referred noise (Table 1, Table 3, Table 5 and Table 7) only changes marginally when using an external low-noise reference, such as the REF5020. To calculate ENOB numbers and noise-free bits when using a reference voltage other than 2.048 V, use Equation 1 to Equation 3: ENOB = ln (Full-Scale Range / VRMS-Noise) / ln(2) (1) Noise-Free Bits = ln (Full-Scale Range / VPP-Noise) / ln(2) (2) Full-Scale Range = 2 · Vref / Gain (3)