Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Systems ENCS2340

Verilog HDL Project Report

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Sec1

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Introduction:

BCD Subtraction using 10s Complement method:

This method subtracts by adding the minuend to the 10's complement of the subtrahend and ignoring any carry. First, find the 10's complement of the negative number. Then, add this to the minuend using BCD addition. If no carry occurs, take the 10's complement of the result to get the final answer. This approach simplifies subtraction by using addition instead.

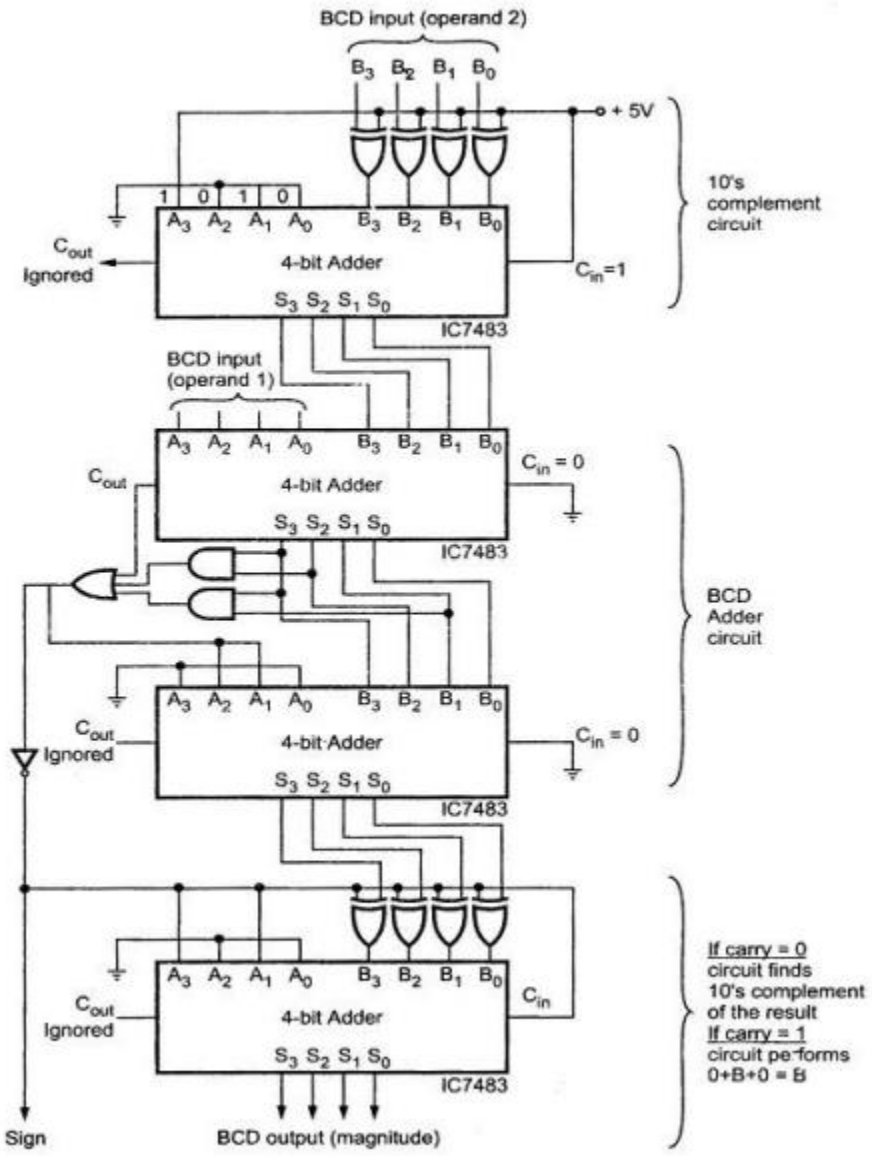

Figure 1:1-digit BCD subtraction using the 10's complement

One-bit full adder:

Full adder is a combinational circuit that adds 3 input states and produce 2 output states (sum, carry).

The full adder logic circuit can be constructed using 2 AND gates, 2 XOR gates with one OR gate.

Verilog structural code:

../project/Full_adder.v

```
1  module Full_adder(input in1,in2,in3 , output sum,carryout);
2   wire wire1, wire2 ,wire3;
3   xor xor1(wire1, in1, in2);
4   xor xor2(sum, wire1, in3);
5   and and1(wire2, in1, in2);
6   and and2(wire3, wire1, in3);
7   or (carryout, wire3, wire2);
8   endmodule
```

Figure 2: one-bit full adder verilog structural code.

Simulation:

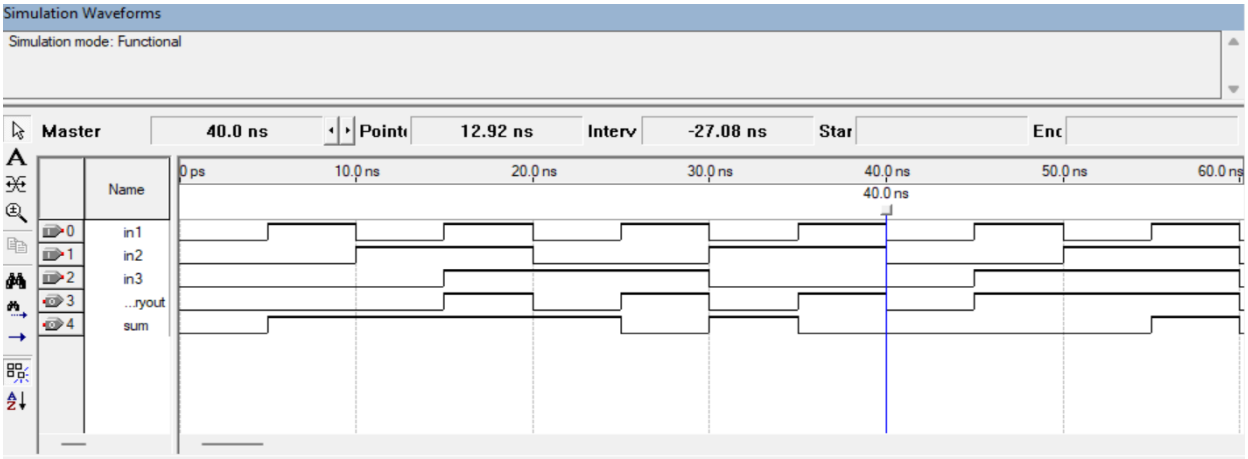

Figure 3: One-bit full adder simulation

Symbol:

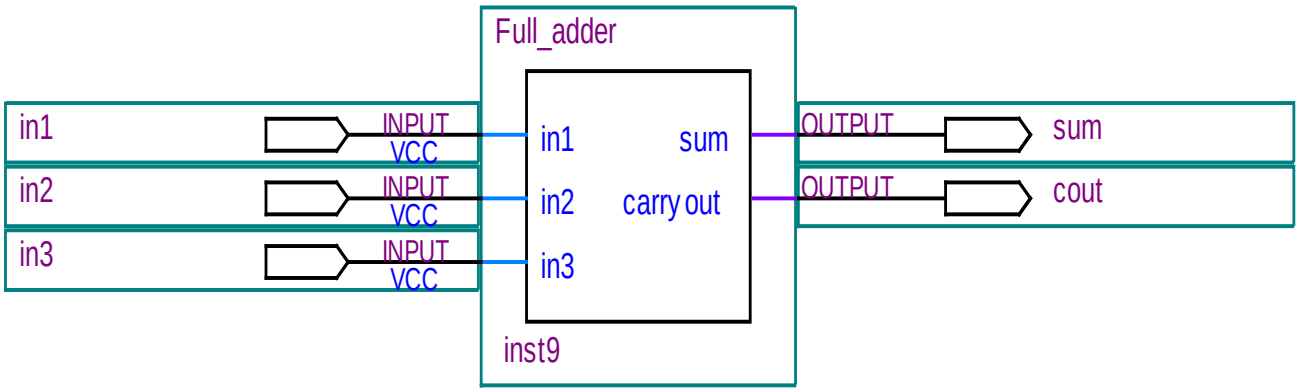

Figure 4: One-bit full adder symbol.

4-bit ripple adder:

Is a combinational logic circuit, used for purpose of adding two 4-bit binary numbers.

The 4-bit ripple adder logic circuit can be constructed using 4 full adder logic circuits, each full adder takes the carry in as input and produce carry out and sum bit as output, the carry out produced by a full adder serves as carry in for its adjacent most significant full adder. When cin becomes available to the full adder, it activates it and comes into operation.

Verilog structural code:

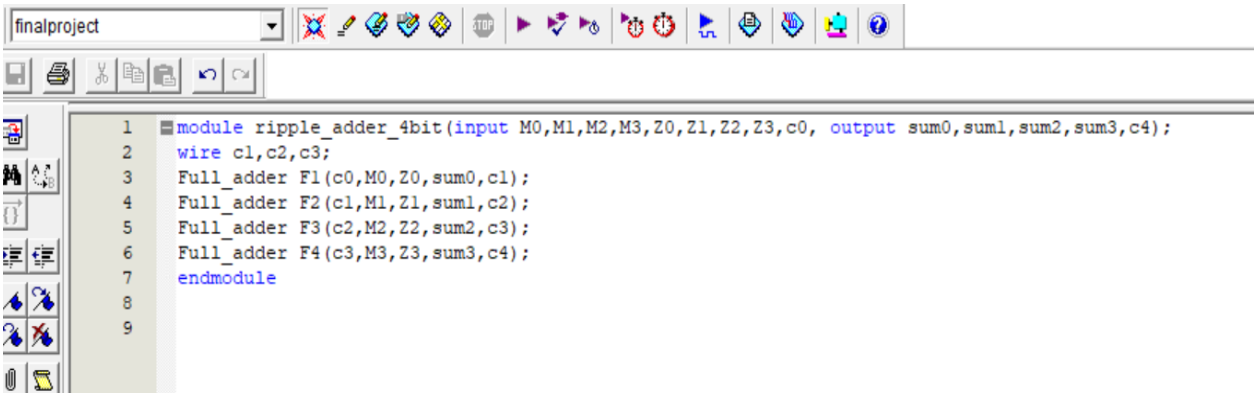

Figure 5: 4-bit ripple adder verilog structural code.

Simulation:

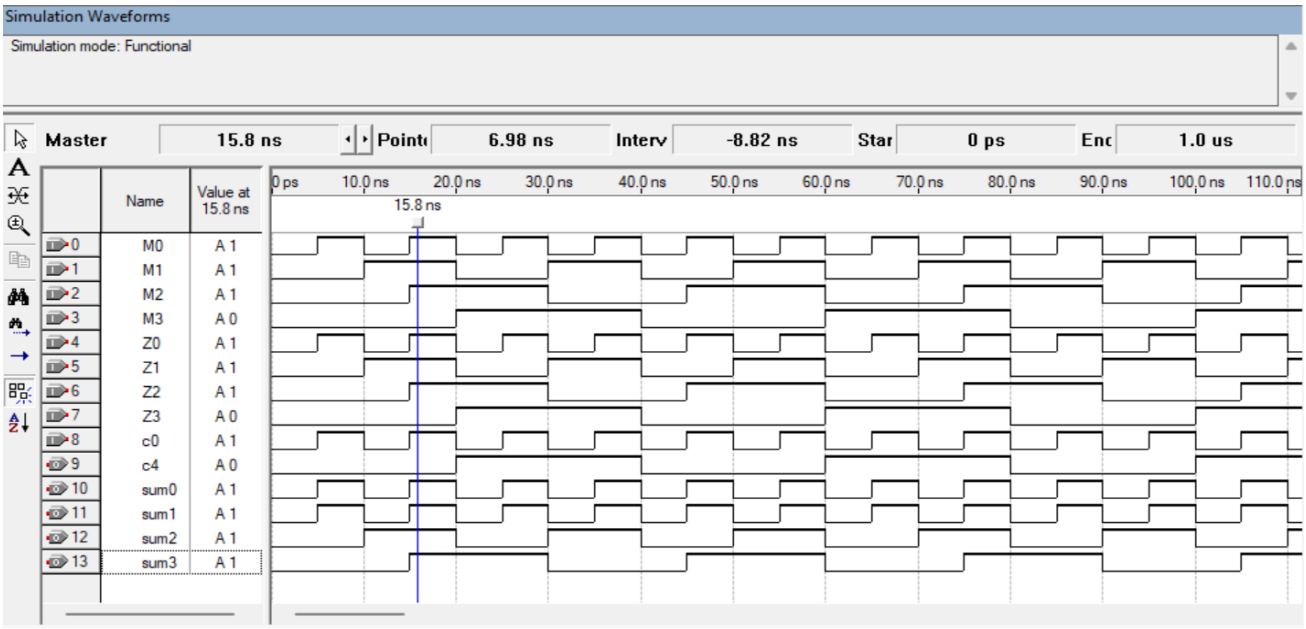

Figure 6: 4-bit ripple adder simulation

Symbol:

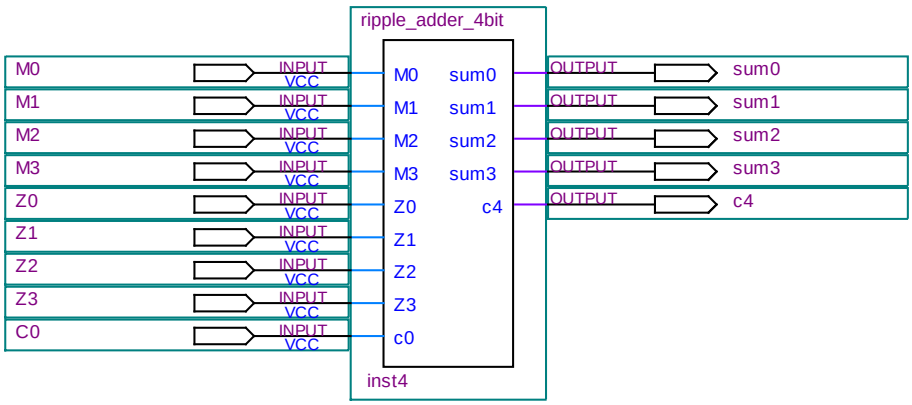

Figure 7: 4-bit ripple adder symbol

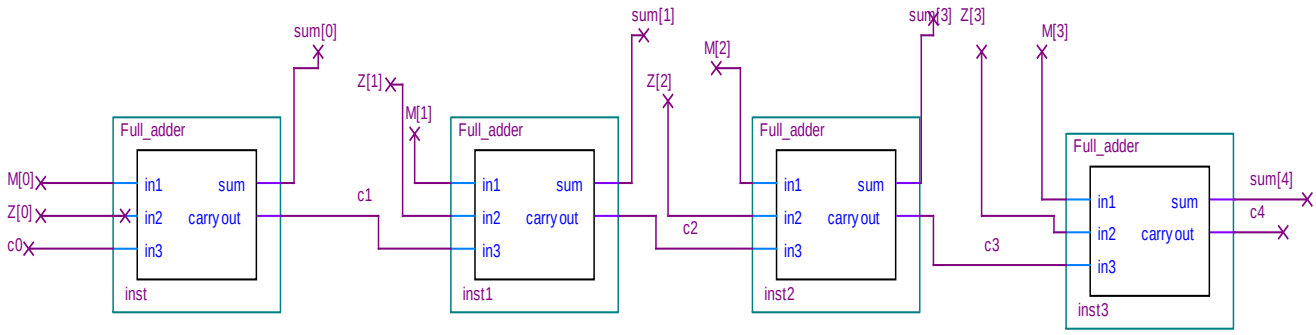

Figure 8: 4-bit ripple adder symbol with 4 full adder

1-digit BCD subtraction using the 10’s complement:

Schematic design:

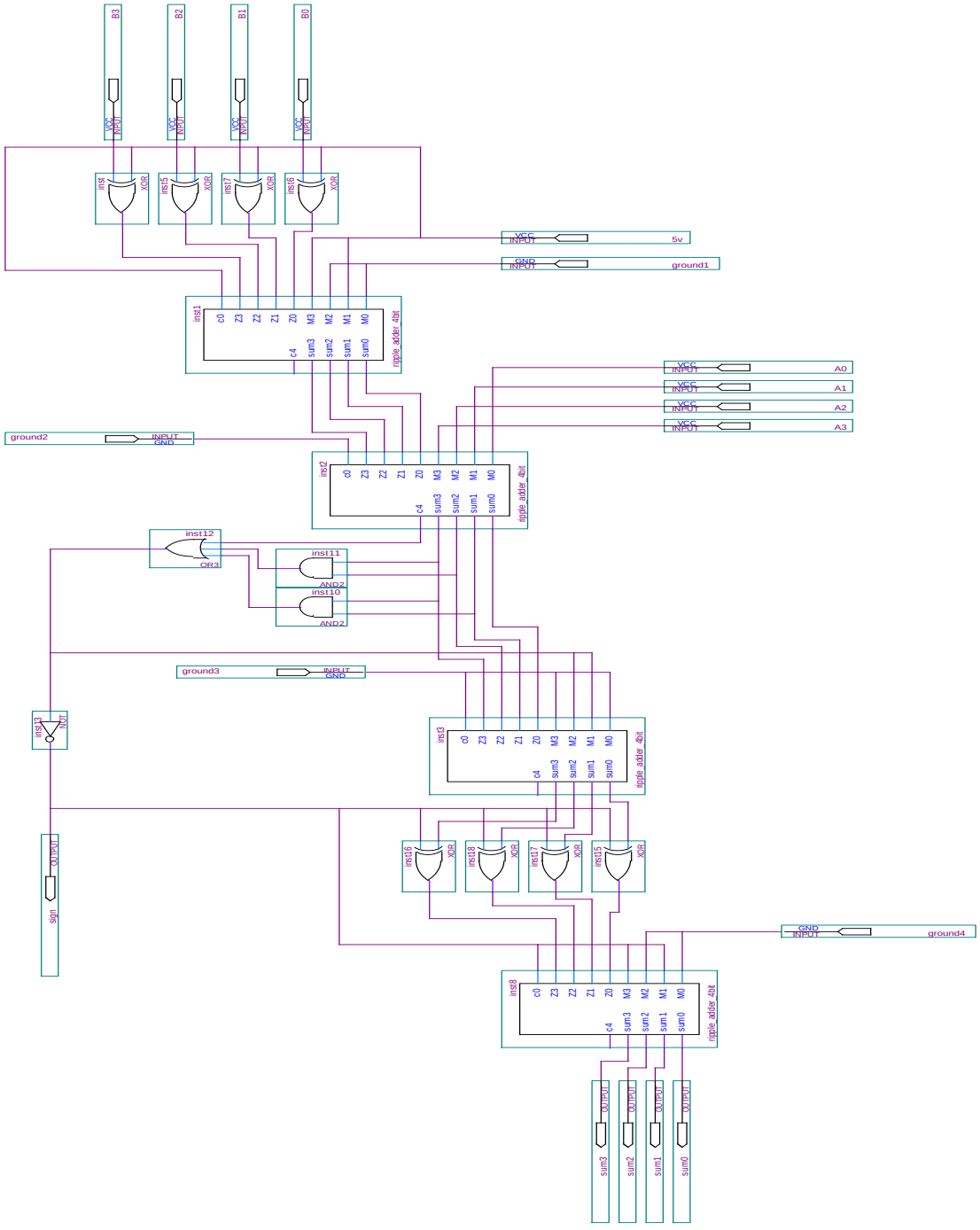

Figure 9: 1-digit BCD subtraction using 10's complement schematic design

Simulation:

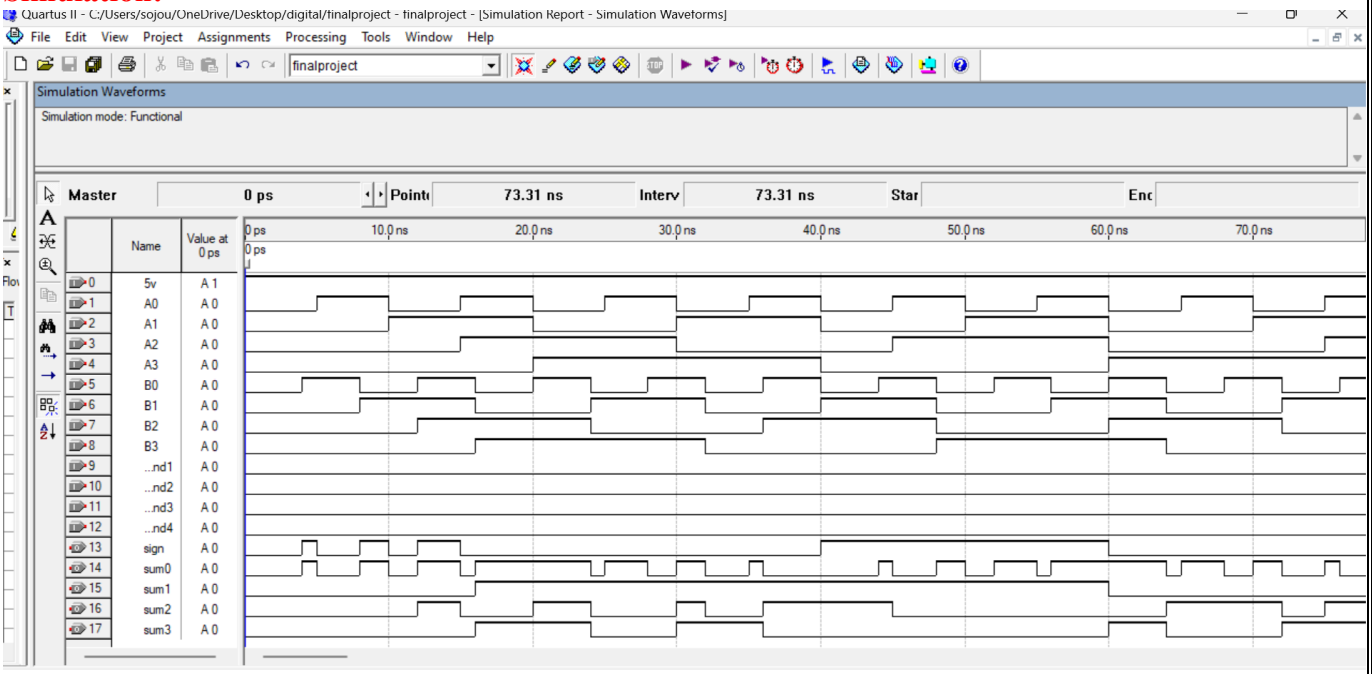

Figure 10: 1-digit BCD subtraction test

Conclusion:

There are many steps to perform 1-digit BCD subtraction using 10's complement. As shown in the Fig.9, first binary adder finds the 10s Complement of the subtracted. Next two 4-bit binary adders perform the BCD addition. Finally, last 4-bit binary adder finds the 10's complement of the number if carry is not generated after BCD addition.

Also as shown in Fig.10 if we subtract a negative number from a positive number, the sign is zero, but if we subtract a positive number from a negative number, the sign is 1.

Finally since the BCD only one digit, the circuit will only enter the BCD numbers (1-9).