Birzeit University

Faculty of Engineering and Technology
Electrical and Computer Engineering Department
Digital Systems ENCS2340
Verilog HDL Project
BCD Subtraction using 10s Complement

Due: Thursday, August 22, 2024

This project is to be completed individually.

Requirements:

1. Submit your Verilog code.

2. Write a report that includes your code, simulation results, and testing for each component as well as the entire system.

Project Description:

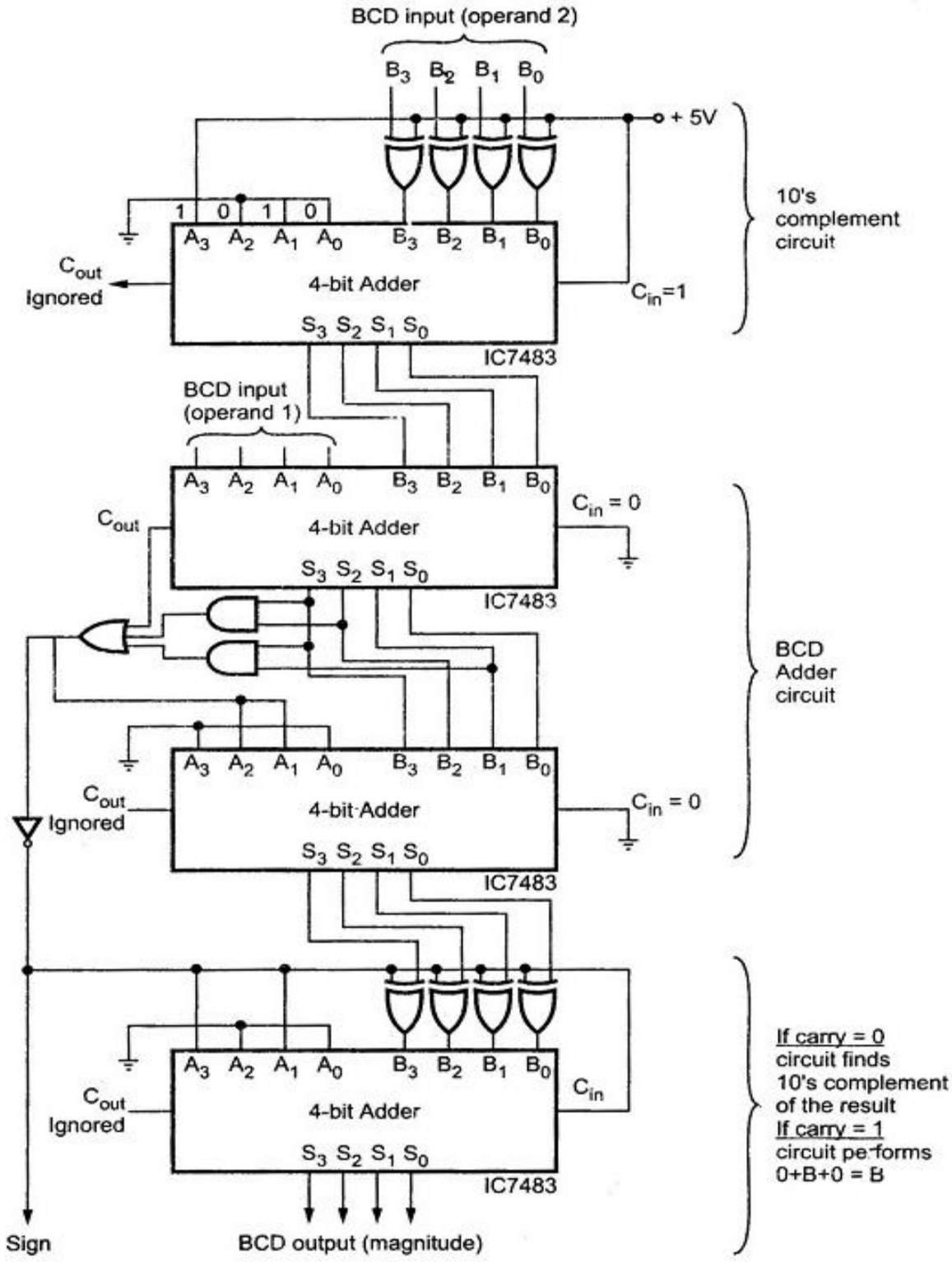
The project focuses on implementing 1-digit BCD subtraction using the 10's complement method. This method involves subtracting by adding the minuend to the 10's complement of the subtrahend and then discarding the carry. The procedure is as follows:

1. Calculate the 10's complement of the negative number.

2. Perform BCD addition with the two numbers.

3. If no carry is generated, find the 10's complement of the result.

The diagram below illustrates the complete circuit for 1-digit BCD subtraction using the 10's complement.


BCD input (operand 2)
B3 B2 B1 B0
+ 5V
10's complement circuit
1 0 1 0
A3 A2 A1 A0 B3 B2 B1 B0
Cout Ignored
4-bit Adder
S3 S2 S1 S0
Cin=1
IC7483
BCD input (operand 1)
A3 A2 A1 A0 B3 B2 B1 B0
Cout
4-bit Adder
Cin = 0
S3 S2 S1 S0
IC7483
BCD Adder circuit
A3 A2 A1 A0 B3 B2 B1 B0
Cout Ignored
4-bit Adder
Cin = 0
S3 S2 S1 S0
IC7483
A3 A2 A1 A0 B3 B2 B1 B0
Cout Ignored
4-bit Adder
Cin
S3 S2 S1 S0
IC7483
If carry = 0 circuit finds 10's complement of the result
If carry = 1 circuit performs 0+B+0 = B
Sign
BCD output (magnitude)

Tasks:

1. Develop a one-bit full adder using Verilog structural code.

2. Test the one-bit full adder.

3. Create a symbol for the one-bit full adder.

4. Build a 4-bit ripple adder using Verilog structural code.

5. Test the 4-bit ripple adder.

6. Create a symbol for the 4-bit ripple adder.

7. Implement the 1-digit BCD subtraction using the 10's complement in Quartus using schematic design.

8. Test the entire system.

Grading:

Task	Grade
Build, test, and create symbol for one-bit full adder using Verilog structural code.	2
Build, test, and create symbol for a 4-bit ripple adder using Verilog structural code.	2
Implement and test the 1-digit BCD subtraction using the 10's complement.	4
Report	2
Total	10