

Name	Value
clk	0
SW14	0
rst	0
BTNL	0
BTNR	0
> unit1[3:0]	6
> ten1[3:0]	1
> unit2[3:0]	6
> ten2[3:0]	0
TbS...ded	0
TbPeriod	1000 ps

The timing diagram displays various digital signals over a 1,000 ns period. The signals are as follows:

- clk**: A constant low signal.
- SW14**: A constant low signal.
- rst**: A pulse at approximately 10 ns, followed by a constant low signal.
- BTNL**: A periodic square wave with a period of approximately 80 ns.
- BTNR**: A periodic square wave with a period of approximately 40 ns.
- unit1[3:0]**: A 4-bit bus that changes value at specific intervals, indicated by numbered markers (0 through 6).
- ten1[3:0]**: A 4-bit bus that changes value at specific intervals, indicated by numbered markers (0 through 5).
- unit2[3:0]**: A 4-bit bus that changes value at specific intervals, indicated by numbered markers (0 through 6).
- ten2[3:0]**: A 4-bit bus that remains at 0 throughout the simulation.
- TbS...ded**: A constant low signal.
- TbPeriod**: A constant value of 1000 ps.

Name	Value	0.000 ns	100.000 ns	200.000 ns	290.000 ns	300.000 ns	400.000 ns	500.000 ns	600.000 ns	700.000 ns	800.000 ns	900.000 ns	
clk	0												
/tb_goal_counter/clk	1												
rst	0												
BTNL	0												
BTNR	1												
> unit1[3:0]	7	0 1 2 3 4 5 6 7 6 5 4 3 2 1 0											
> ten1[3:0]	0	0											
> unit2[3:0]	6	0 1 2 3 4 5 6 5 4 3 2 1 0											
> ten2[3:0]	0	0											
TbS...dec	0	0											
TbPeriod	1000 ps	1000 ps											