International Institute of Information Technology Bangalore

LDO WITH HIGH PSRR
VL804 : ANALOG POWER IC DESIGN

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❑ CONTENTS

❑ Key Challenges Addressed

- Increase PSRR Value by using suitable value of Cc Miller Capacitance
- Enhance the value of PSRR at High Frequency (MHz) range
- Implemented paper A 65-nm CMOS Low Dropout Regulator Featuring >60-dB PSRR Over 10-MHz Frequency Range and 100-mA Load Current Range

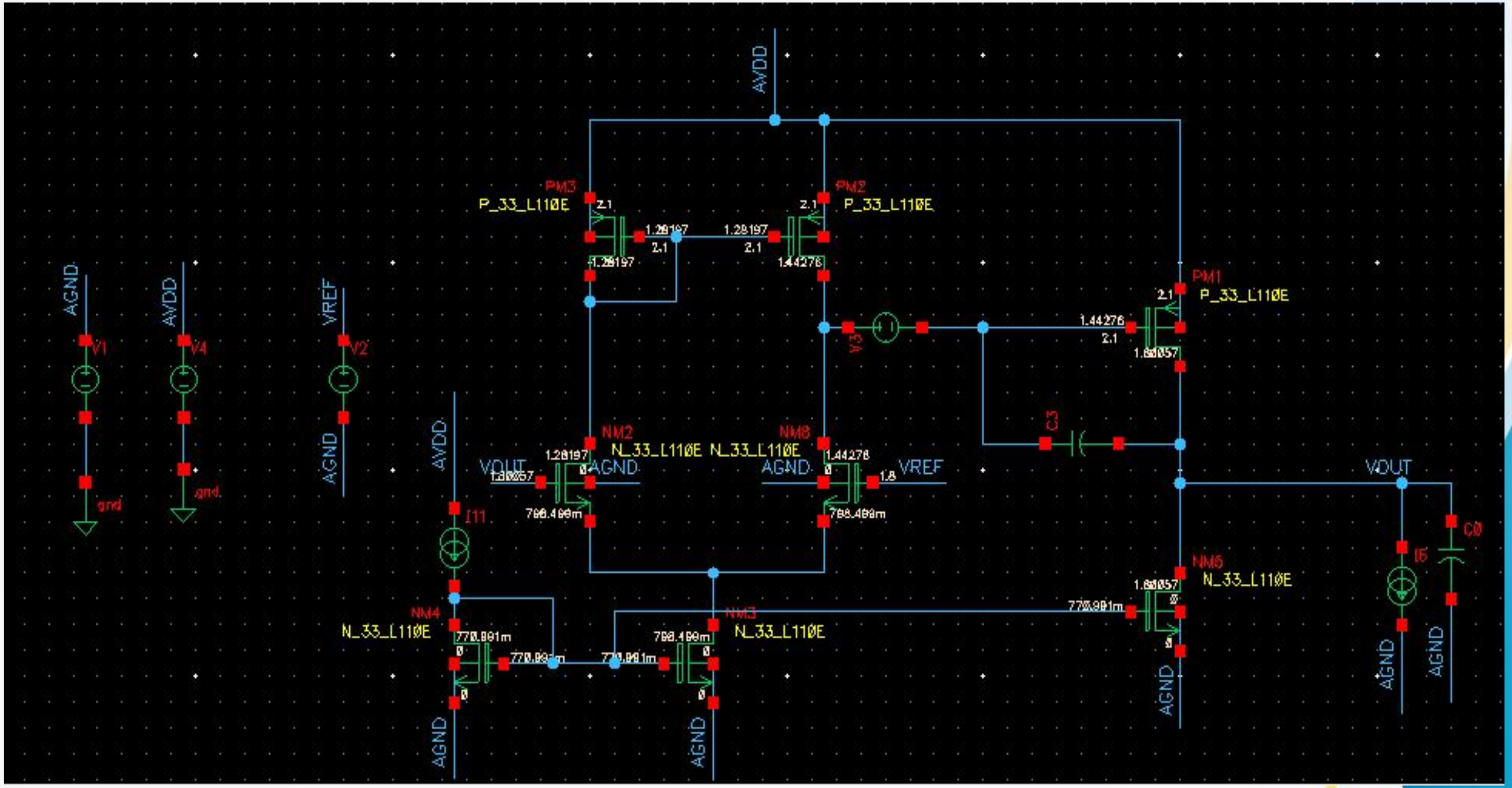
❑ Reference Paper Specification Table

		Units	Paper 1	Paper 2	Paper 3	Paper 4	Paper 5	Paper 6
Techniques								
Technology		nm	65	180	130	180	90	180
Power Transistor			NMOS					PMOS
Maximium ILoad		mA	100		25	200	140	
Nominal Vin		V	1.2	8-45	>1.15	1.8-2.5	>1.15	
Vout		V	1	5	1	1.6-2.5	1	
Minimum Dropout		V	80		>0.15	0.2	>0.15	0.178
Cout		uF	4.7			1		
Load Regulation		uV/mA	10					
Quiescent Current		uA	40		50	0.6-160	33-145	5.6-35.6
Overshoot		mV	2					28.7
Undershoot		mV	4					36.36
PSRR Heavy Load	**ILoad**	mA	100	50	25	200		250
	100KHz	dB	89		60		53	80
	1MHz	dB	70	70	67	40.5	62	70
	10MHz	dB	62	57	56		56	60
PSRR Light Load	**ILoad=**	uA	100					
	100kHz	dB	81					
	1MHz	dB	75					
	10MHz	dB	91					
Area		mm^2	0.048		0.0049	0.037	0.015	0.12
Iout(max)		mA	50					
Line Regulation		mV/V		0.0397	26	4.86		
Load Regulation		mV/mA		0.00018	0.048	0.055	0.043	0.112

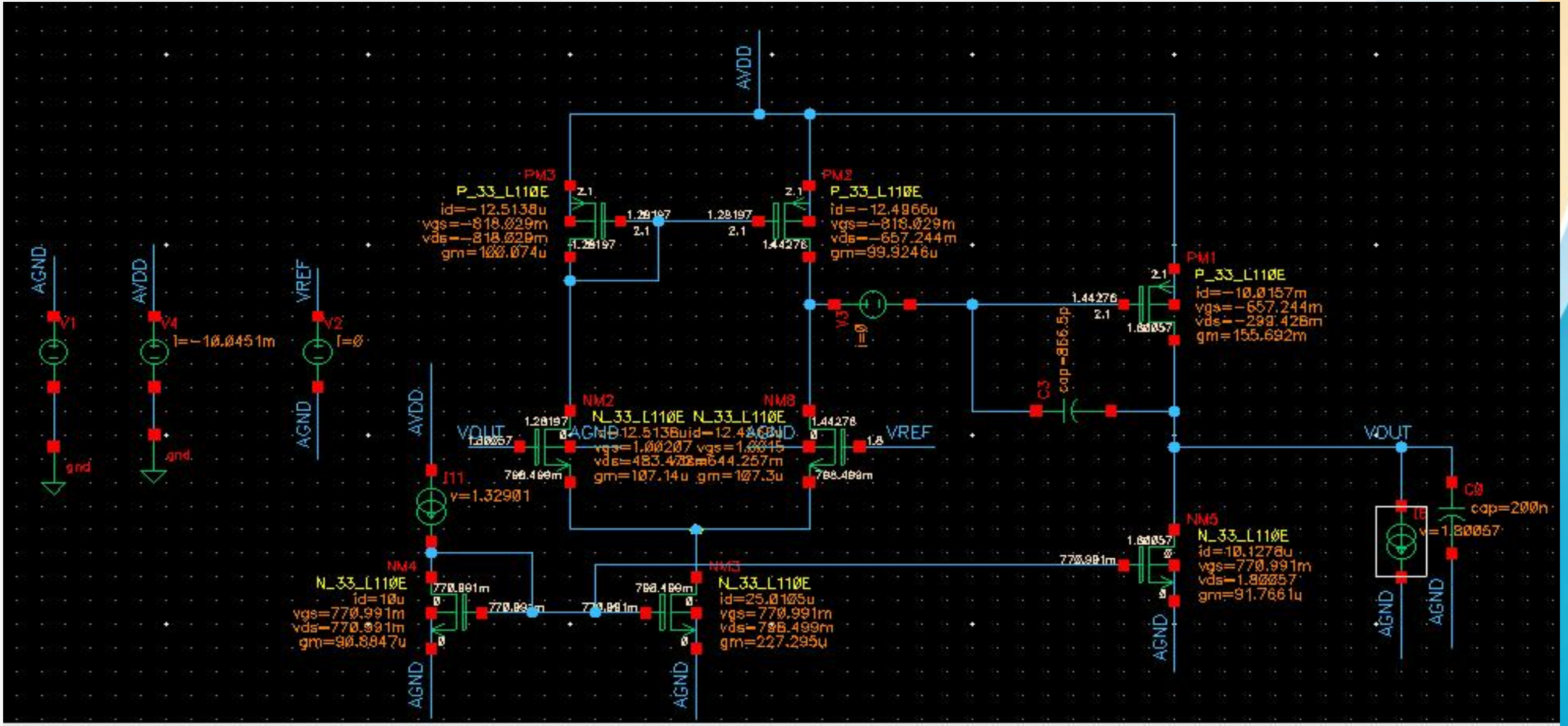
Used Specification Table

Parameters	Units	Values
Supply Voltage	V	2.1
Output Voltage	V	1.8
Dropout Voltage	V	0.2
Dropout Voltage	V	0.2
C_Load	nF	200
Quiescent Current	uA	25
I_Load(maximum)	mA	50
I_Load(minimum)	mA	10
PSRR(@ High Frequency)	dB	40.9
PSRR(@ Low Frequency)	dB	70.8

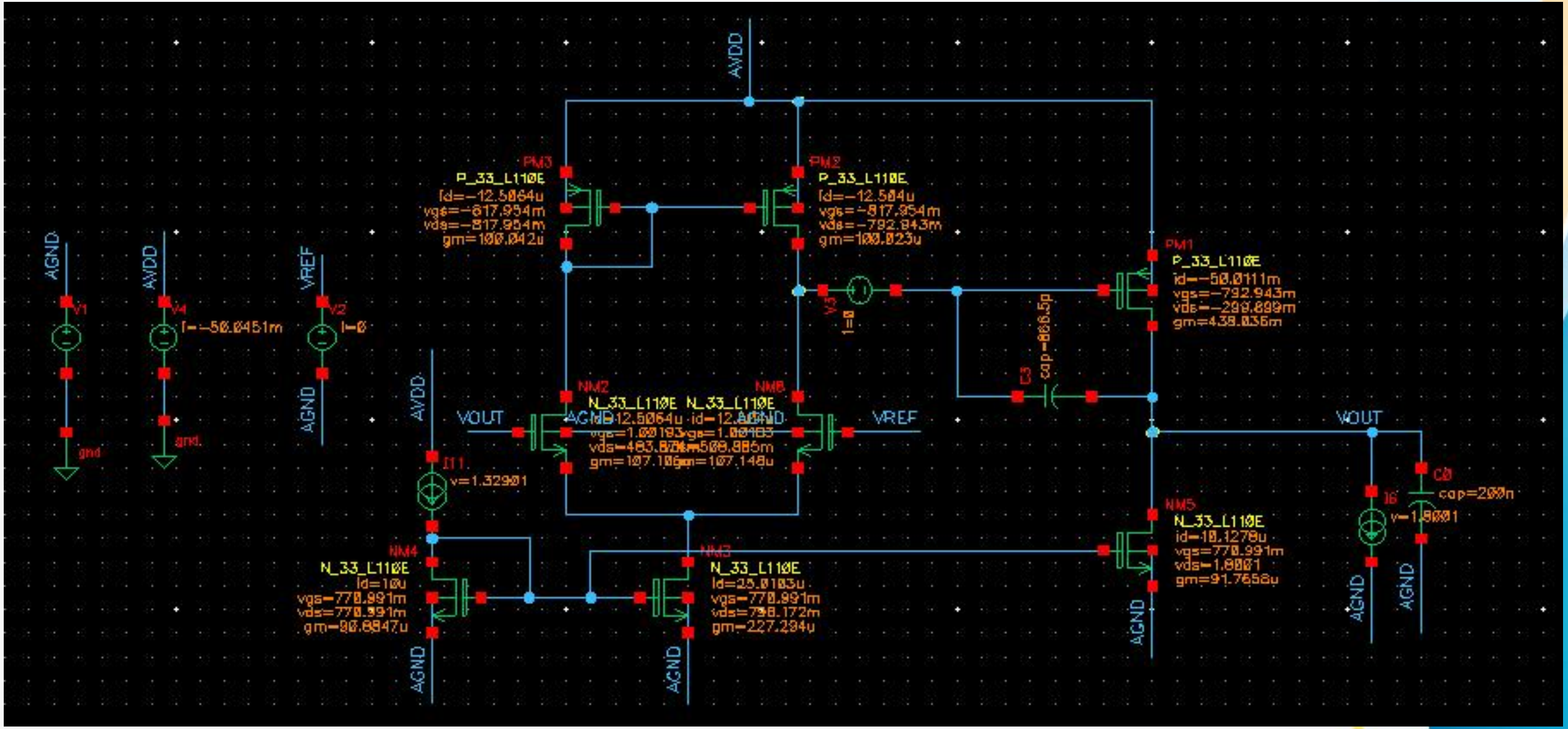
❑ Circuit Diagram(Schematic)



❑ Simulation Result-1 (DC Operating Points for Compensated 10mA)



❑ Simulation Result-1 (DC Operating Points for Compensated 50mA)



❑ Theoretical Analysis or Design Approach

❑ DC_Operating_Point_Values_of_All_Transistor_at _ILoad=50mA

Mosfet	NM5	NM2	NM4	NM3	NM1	NM0	PM3	PM2	PM0	PM1	PM7
Vov(V)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Vth(V)	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6
Vgs(V)	7.71E-01	7.68E-01	7.71E-01	7.68E-01	7.74E-01	7.74E-01	7.89E-01	7.89E-01	7.89E-01	7.89E-01	7.76E-01
Vds(V)	7.71E-01	7.68E-01	2.26E-01	7.68E-01	1.85E-01	1.85E-01	4.32E-01	7.89E-01	7.89E-01	7.76E-01	2.00E-01
rout(ohm)	6.49E+06	1.32E+06	3.37E+04	1.32E+06	2.53E+04	2.53E+04	7.88E+05	2.65E+06	2.65E+06	7.96E+05	2.03E+05
Vgt(V)	1.86E-01	1.82E-01	1.86E-01	1.82E-01	1.88E-01	1.88E-01	1.96E-01	1.96E-01	1.96E-01	1.96E-01	1.83E-01
Ids(A)	1.00E-05	4.85E-05	9.74E-05	4.85E-05	4.87E-05	4.87E-05	4.85E-05	4.87E-05	4.87E-05	4.87E-05	8.34E-06
gm(S)	9.08E-05	4.46E-04	8.69E-04	4.46E-04	4.17E-04	4.17E-04	4.36E-04	4.37E-04	4.37E-04	4.35E-04	7.63E-05
Cgs(F)	6.86E-13	3.42E-12	6.83E-12	3.42E-15	3.36E-12	3.36E-12	1.16E-11	1.16E-11	1.16E-11	1.16E-11	2.29E-12
Cgd(F)	8.78E-15	4.39E-14	4.93E-13	4.39E-14	4.61E-13	4.61E-13	2.39E-13	2.03E-13	2.03E-13	2.04E-13	1.34E-13
region	2	2	2	2	2	2	2	2	2	2	2
Vds (sat) (V)	1.64E-01	1.61E-01	1.64E-01	1.61E-01	1.65E-01	1.65E-01	1.66E-01	1.66E-01	1.66E-01	1.66E-01	1.57E-01
self gain	589.23	592.976	29.273	592.97	10.57	10.57	345.961	1.15E+03	1.15E+03	1.14E+03	15.5135

❑ Light Load ILoad=10mA with Compensation Theoretical Calculation

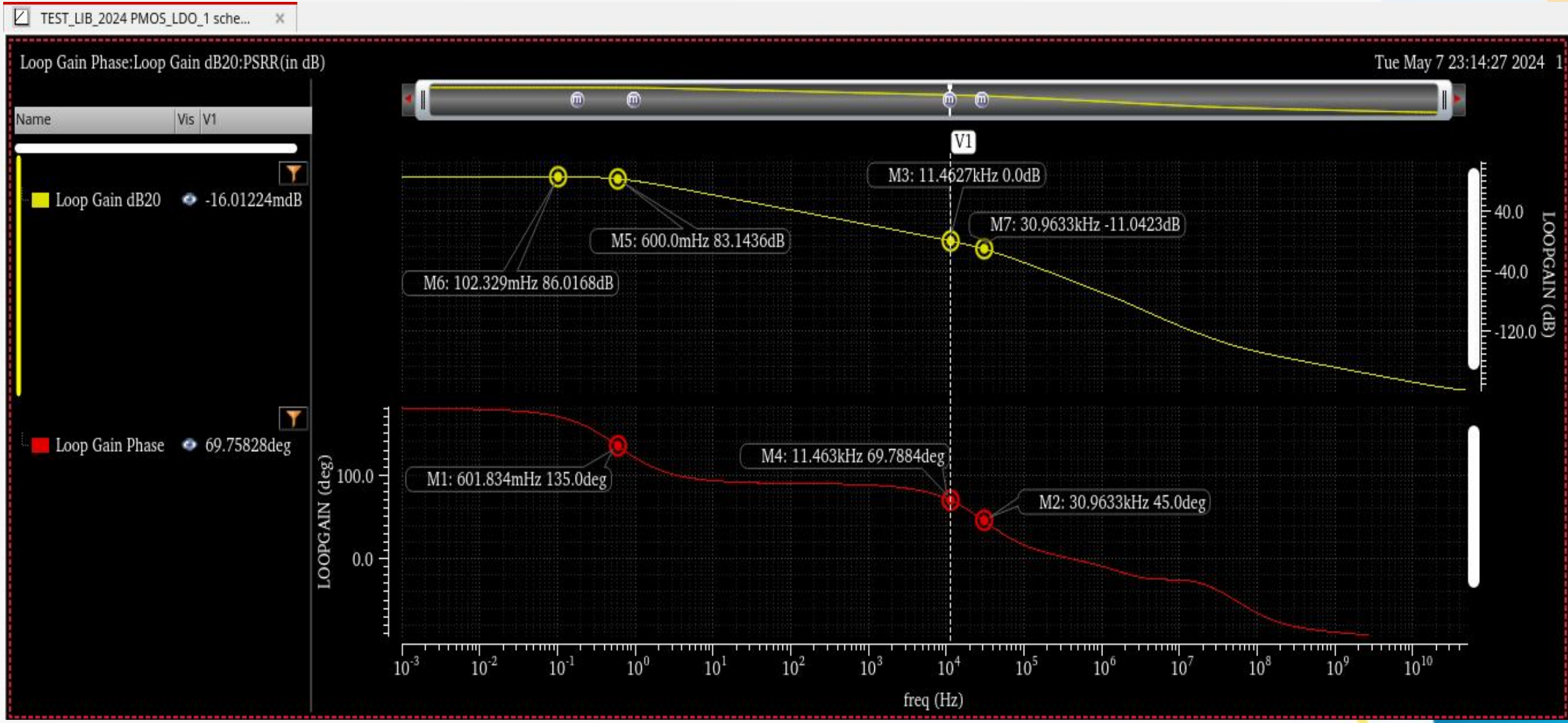
Light Load with Compensation								
Pole 1-(Inside)(Hz)	1/((((1+Apass)*Cc)+Cgd(PM2)+Cgd(NM8)+Cgg(PM1))*(rout(NM8)||rout(PM2)))						1.088075235	0.173260388
	3.174E-07	2895570.311	rout(NM8)		4.54E+06	rout(PM2)		7.99E+06
Pole 2- near Cload(Hz)	gm(PM1)/Cload							
	gm(PM1)	1.56E-01	Cload		2.00E-07		778460	
							123958.5987	
Mirror Pole (Hz)	1/((Cgd(NM2)+Cgs(PM3)+Cgg(PM2))*(rout(NM2)||rout(PM3)||1/gm(PM3)))						18905852.26	3010486.029
	5.31713E-12	9947.782887	rout(NM2)		2.80E+06	rout(PM3)		1.07E+07
Passfet Zero (Hz)	gm(PM1)/Cgd(PM1)		653152661.8		104005200.9			
	gm(PM1)	1.56E-01		Cgd(PM1)			2.38E-10	
Zero at input (Hz)	gm(NM2)/Cgd(NM2)		8831481420		1406286850			
	gm(NM2)	1.07E-04	Cgd(NM2)		1.21E-14			
Gain-Opamp (dB)	gm(NM2)*(rout(NM8)||rout(PM2		rout(NM8)		4.54E+06	rout(PM2)		7.99E+06
	gm(NM2)	1.07E-04	2895570.311		310.2314031			
Gain-passfet (dB)	gm(PM1)*(rout(PM1)||rout(NM5		rout(PM1)		2.26E+03	rout(NM5)		8.90E+06
	gm(PM1)	1.56E-01	2254.428665		350.9965077			
Total Gain					108890.1391			112689.6352
					100.73 dB			
w(ugf) (Hz)	18866.34772							

❑ Heavy Load ILoad=50mA with Compensation Theoretical Calculation & Cc Parameterization

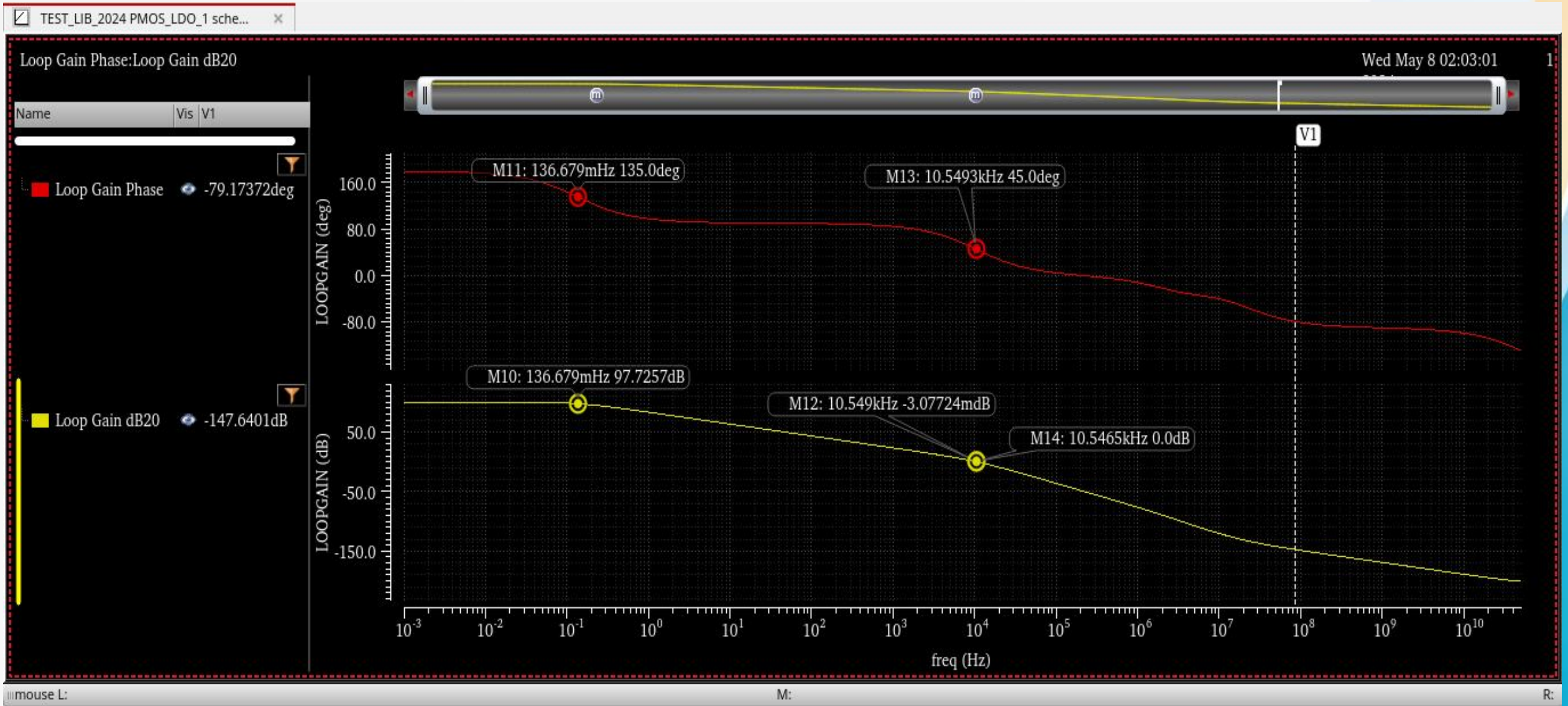
Heavy Load with Compensation								
Pole 1-(Inside)(Hz)	1/((((1+Apass)*Cc)+Cgd(PM2)+Cgd(NM8)+Cgg(PM1))*(rout(NM8)||rout(PM2)))					4.982269383	0.793354997	
	8.39864E-08	2389813.85	rout(NM8)		3.11E+06	rout(PM2)		1.03E+07
Pole 2- near Cload(Hz)	gm(PM1)/Cload							
	gm(PM1)	Cload						
	4.38E-01	2.00E-07	2190180		348754.7771			
Mirror Pole (Hz)	1/((Cgd(NM2)+Cgs(PM3)+Cgg(PM2))*(rout(NM2)||rout(PM3)||1/gm(PM3)))					41883356.44	6669324.274	
	2.40012E-12	9947.77027	rout(NM2)		2.80E+06	rout(PM3)		1.07E+07
			gm(PM3)		1.00E-04	9992.605472		
Passfet Zero (Hz)	gm(PM1)/Cgd(PM1)		gm(PM1)	Cgd(PM1)				
			4.38E-01		3.33E-10	1315648625	209498188.6	
Zero at input (Hz)	gm(NM2)/Cgd(NM2)		gm(NM2)	Cgd(NM2)				
			1.07E-04		1.21E-14	8837775394	1407289075	
Gain-Opamp (dB)	gm(NM2)*(rout(NM8)||rout(PM2		gm(NM2)	ROUT				
			1.07E-04		2389813.85	255.9610124		
Gain-passfet (dB)	gm(PM1)*(rout(PM1)||rout(NM5		gm(PM1)	rout(PM1)		rout(NM5)		
			4.38E-01		180.817	8.89E+06		
					180.8133224	79.20274448		
Total Gain	20272.81466	86.138 dB						
Wugb(Hz)	16083.53882							

Cload	2.24E-07
gmpass	4.38E-01
gm(NM2)	1.07E-04
Cgd	2.38E-10
gmpass/CL	1955517.857
(gmpass/CL)/2.2	888871.7532
((gmpass/CL)/2.2)/gm(NM2)	8299068701
1/(((gmpass/CL)/2.2)/gm(NM2))	1.20495E-10
Cc	-1.1787E-10
	64.0219 pF
Cc from parameterization	866.5p

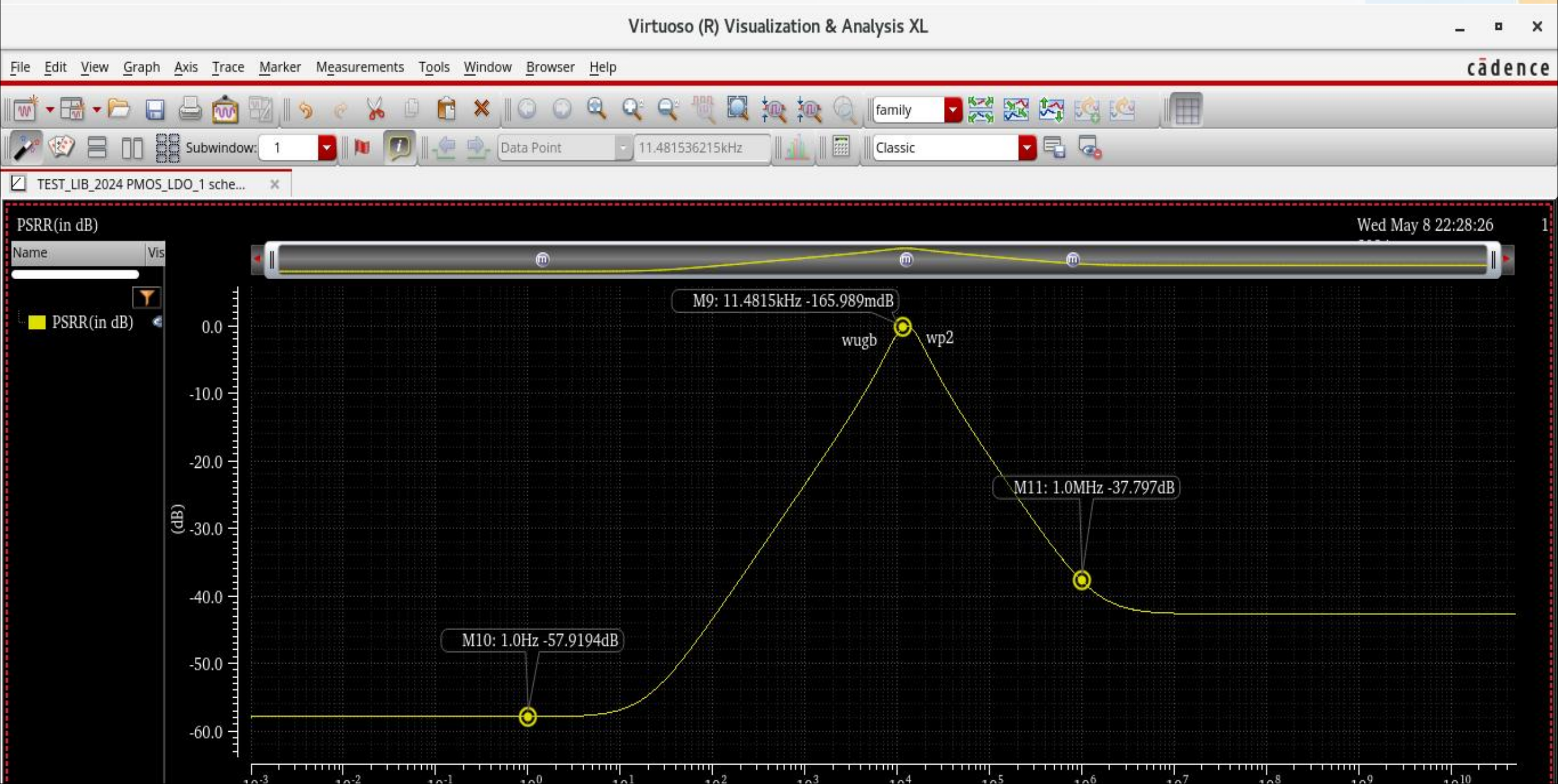
❑ Simulation Result-2 (Gain & Phase Plots For Compensated ILoad=50mA)



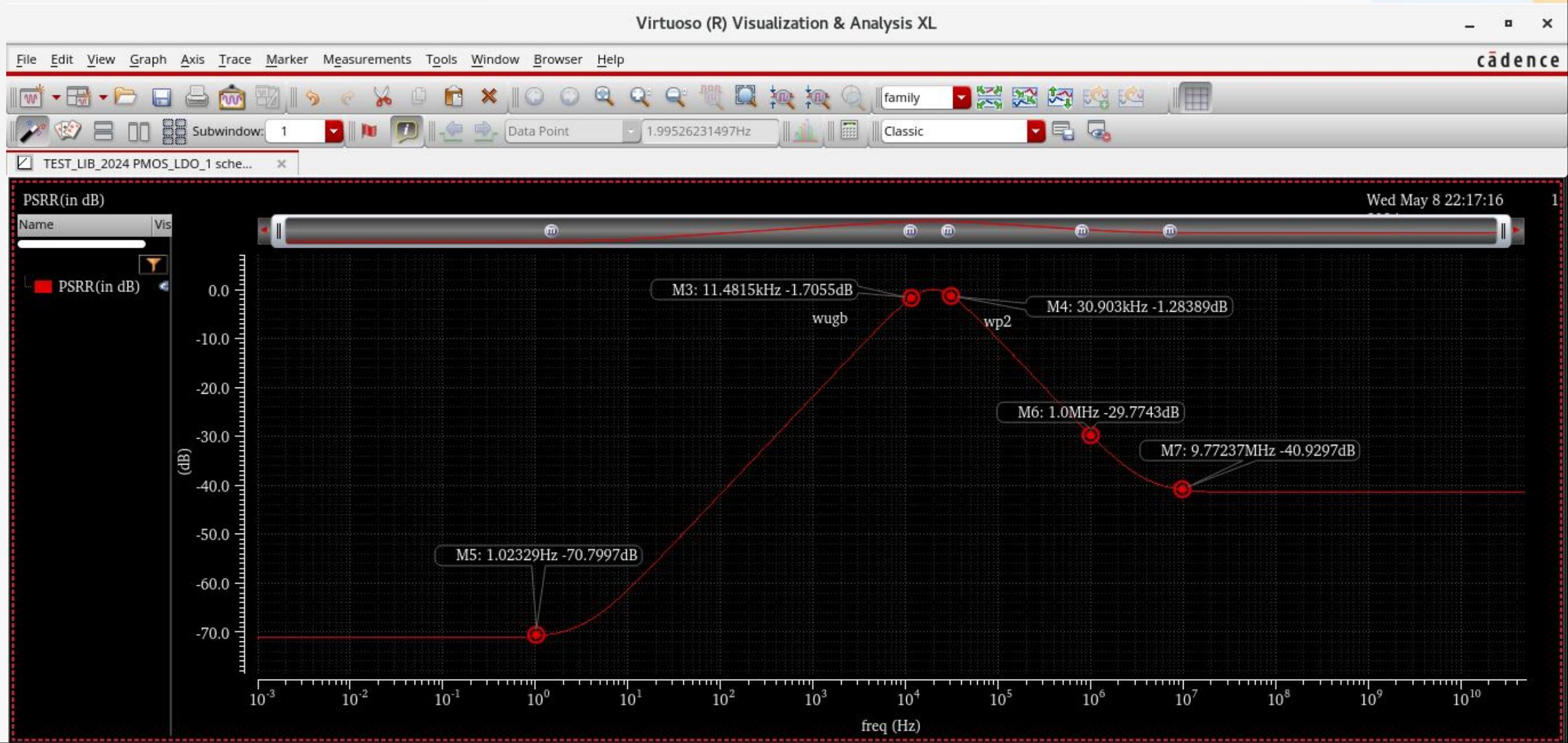
❑ Simulation Result-2 (Gain & Phase Plots For Compensated ILoad=10mA)



❑ Simulation Result-3 PSRR at ILoad=10mA

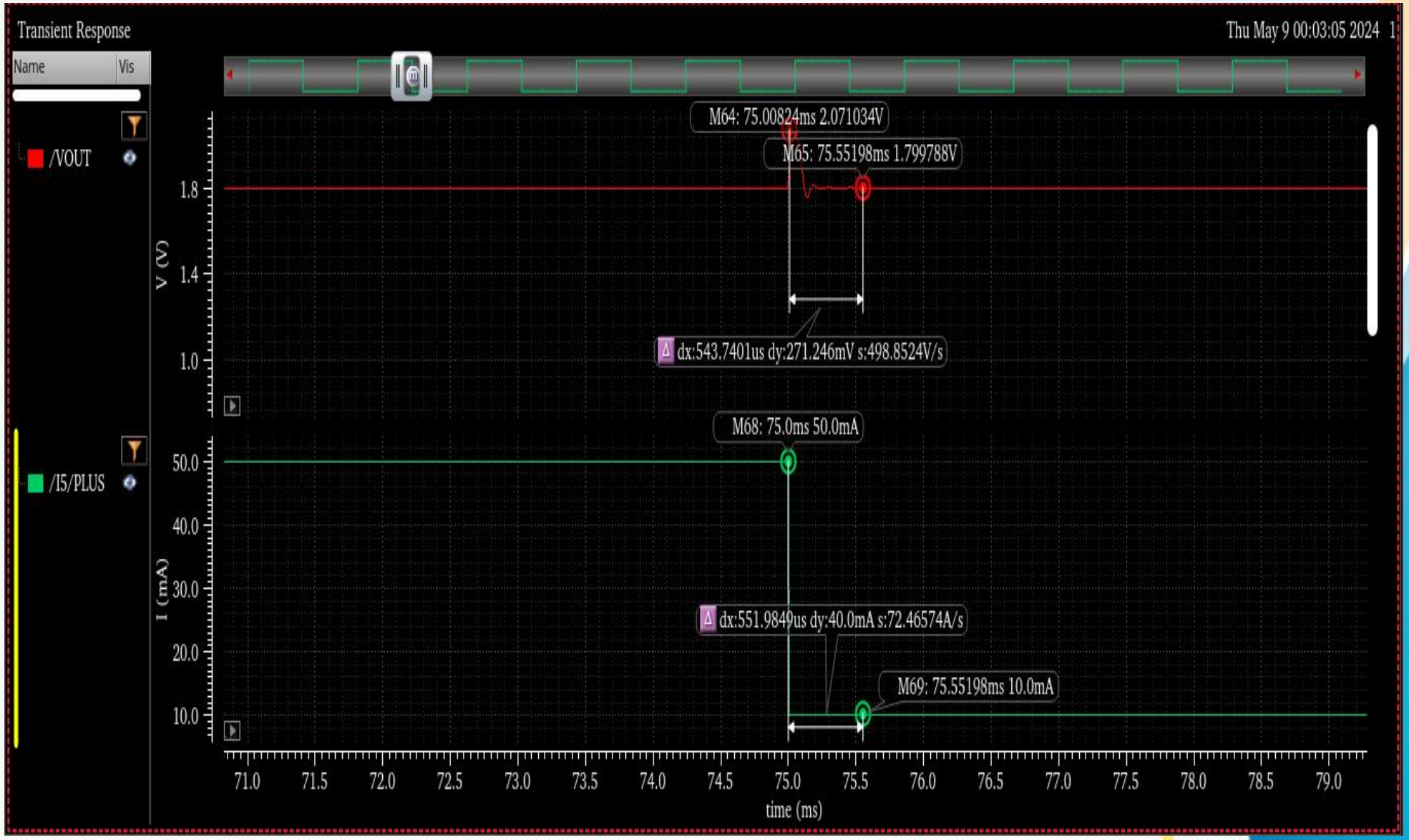


❑ Simulation Result-3 PSRR at ILoad=50mA



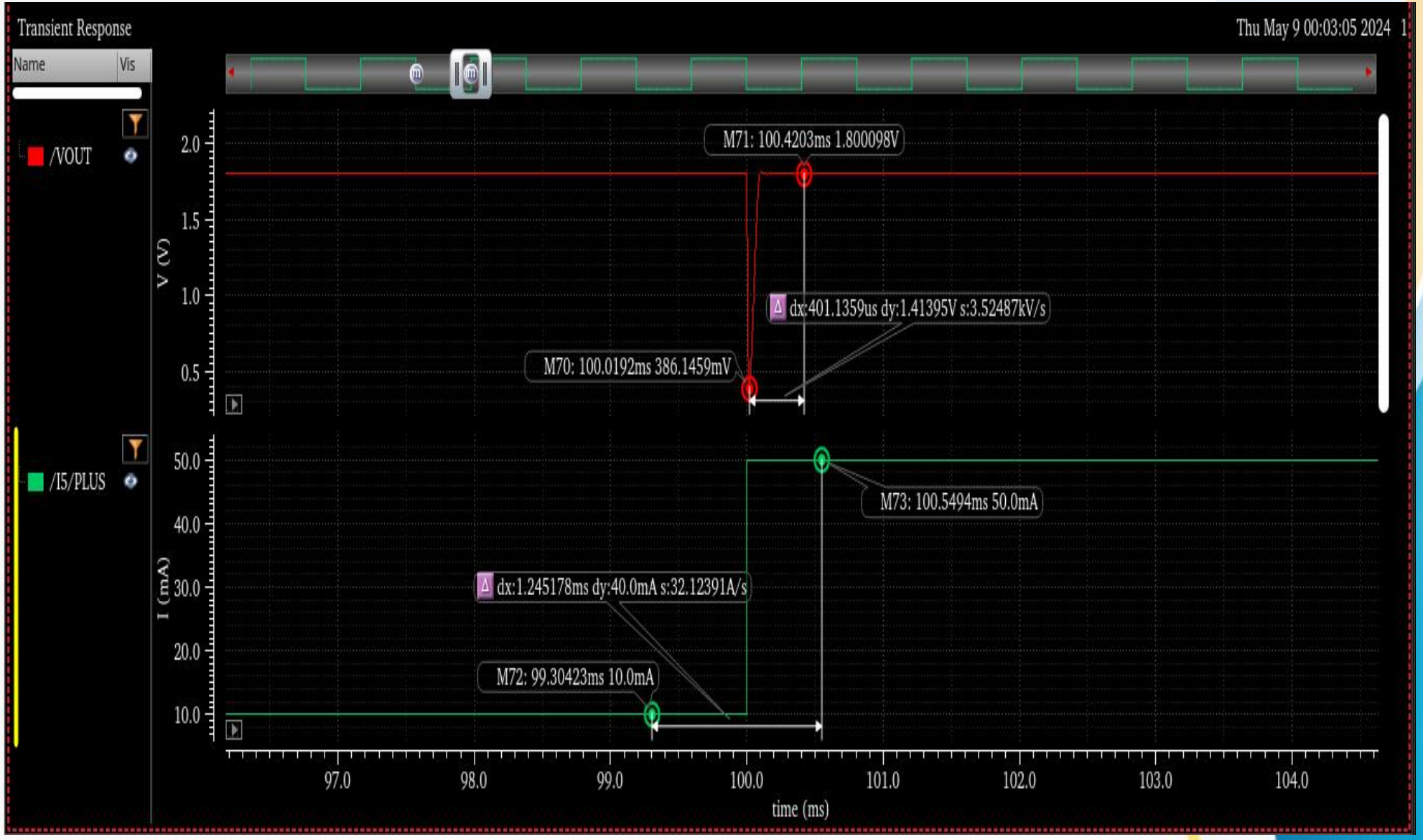
❑ Simulation Result-4 Load Transient(ILoad=50mA to 10 mA)

OVERSHOOT	
Delta(VOUT) (V)	0.271
Delta(ILoad) (A)	0.04
Rout(DVOUT/DILoad) (ohm)	6.775



❑ Simulation Result-4 Load Transient(ILoad=10mA to 50 mA)

UNDERSHOOT	
Delta(VOUT) (V)	1.414
Delta(ILoad) (A)	0.04
Rout(DVOUT/DILoad) (ohm)	35.35

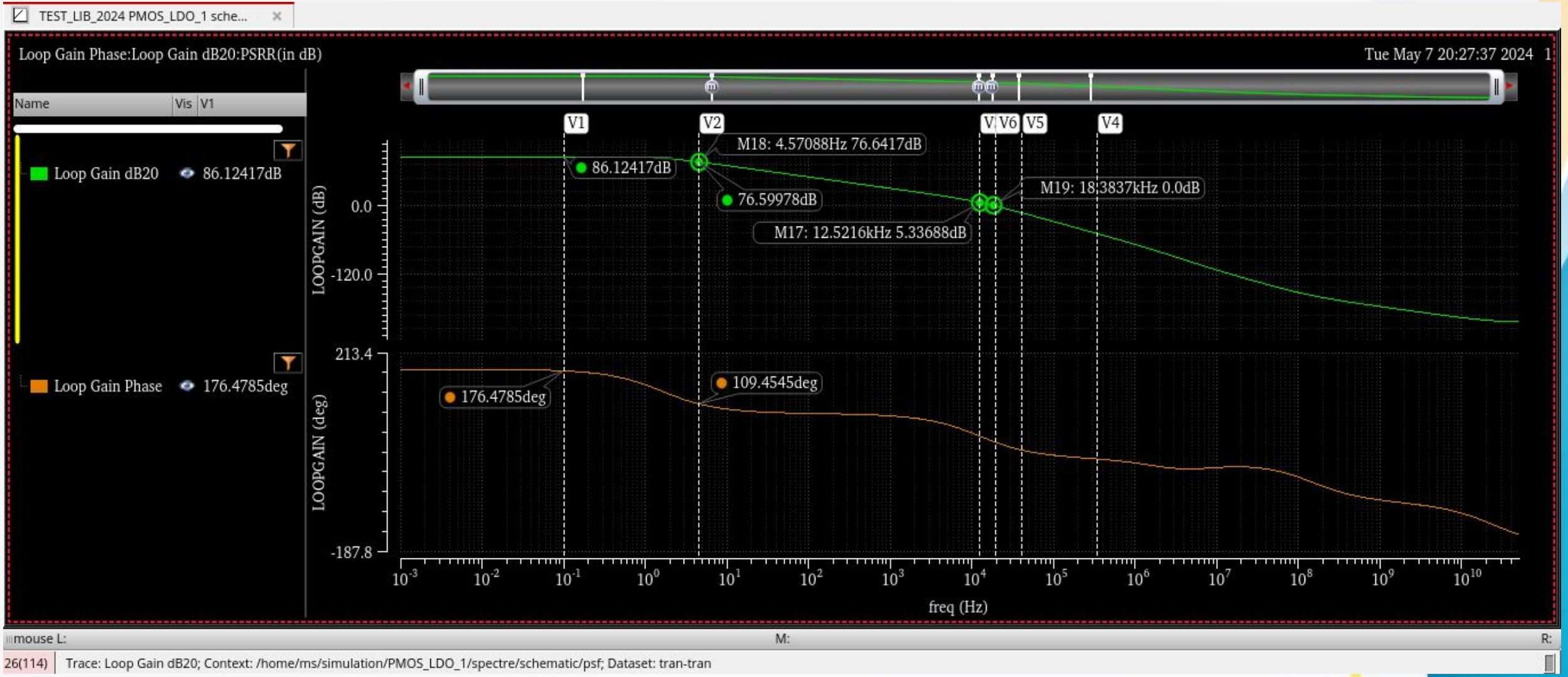


❑ Simulation Results Table

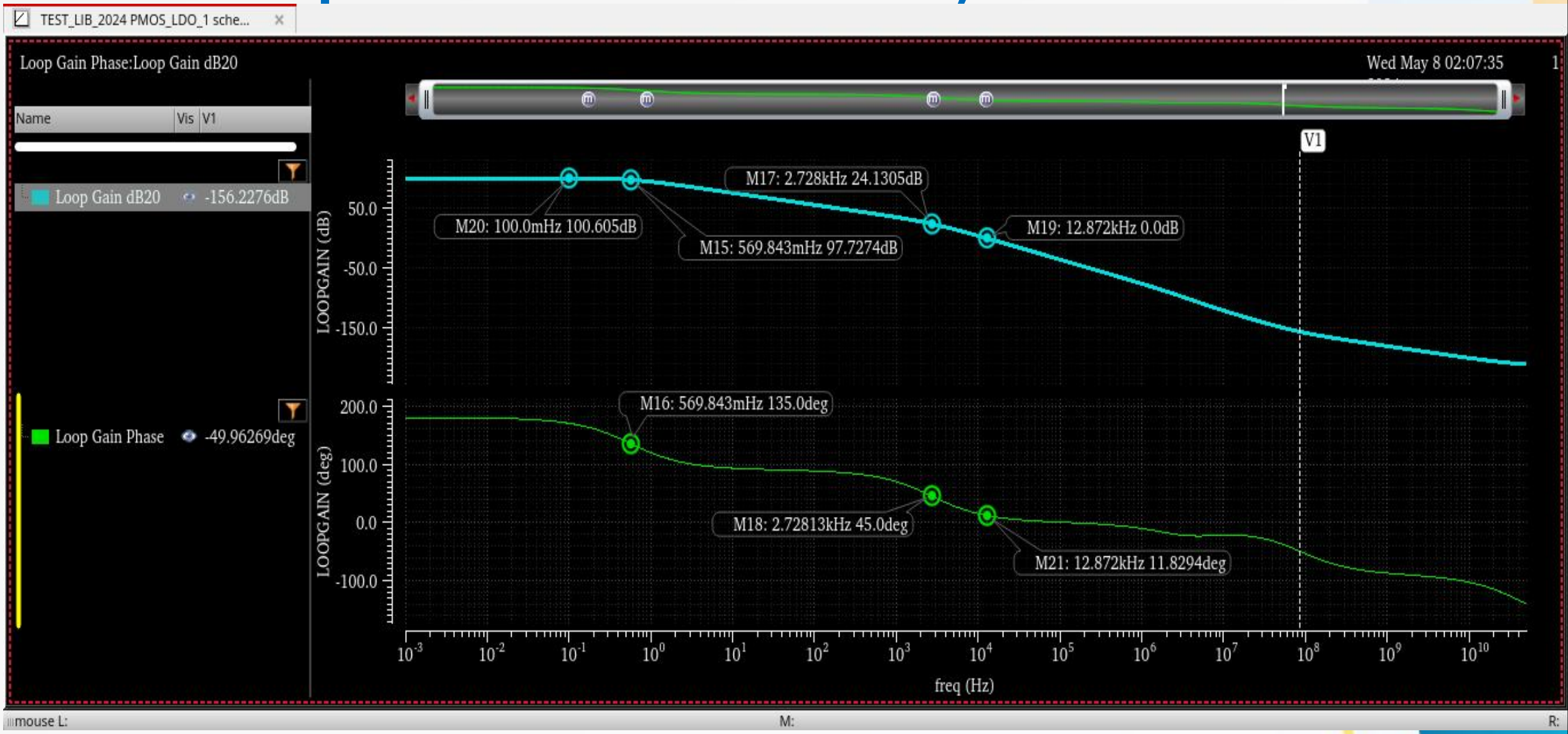
SIMULATION RESULTS	
Technology	110nm
Input Voltage (Vin)	2.1V
Load Current Max(ILoad_max)	50mA
Load Current Min(ILoad_min)	10mA
Output Voltage(VOUT)	1.8V
Load Capacitance(Cout)	200nF
Compesation Scheme	Miller(Internal) Compensation Cc
PSRR @ 1Hz	70.80dB
PSRR @ 1MHz	29.77dB
PSRR @10MHz	41dB
Load Overshoot Rout(ILoad=10mA to 50mA)	6.775 ohm
Load Undershoot Rout(ILoad=50mA to 10mA)	35.35ohm

Backup Slides

❑ Simulation Result-2 (Gain & Phase Plots For Uncompensated ILoad=50mA)



❑ Simulation Result-2 (Gain & Phase Plots For Uncompensated ILoad=10mA)



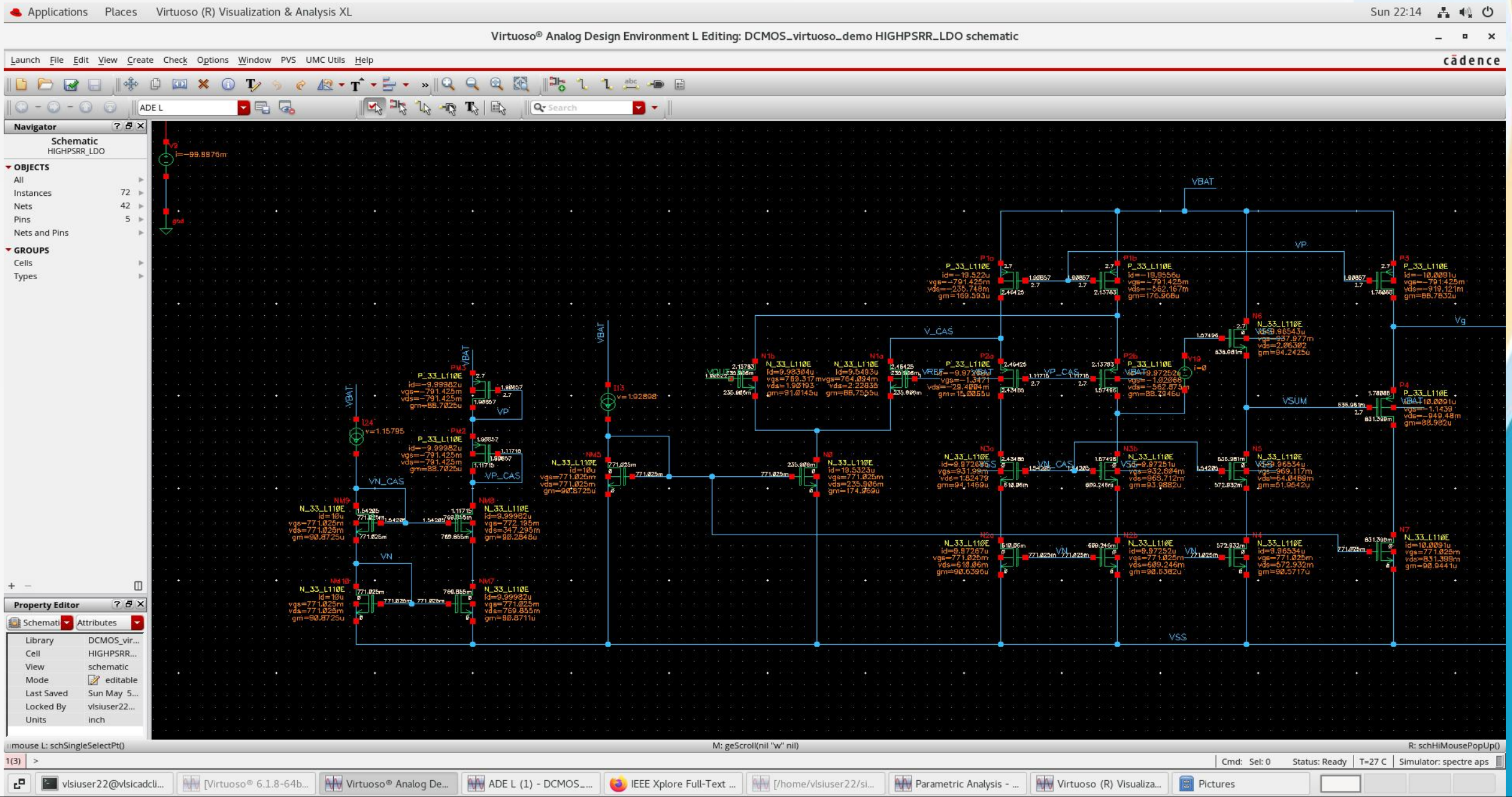
Reference Paper 1: A 65-nm CMOS Low Dropout Regulator Featuring >60-dB PSRR Over 10-MHz Frequency Range and 100-mA Load Current Range

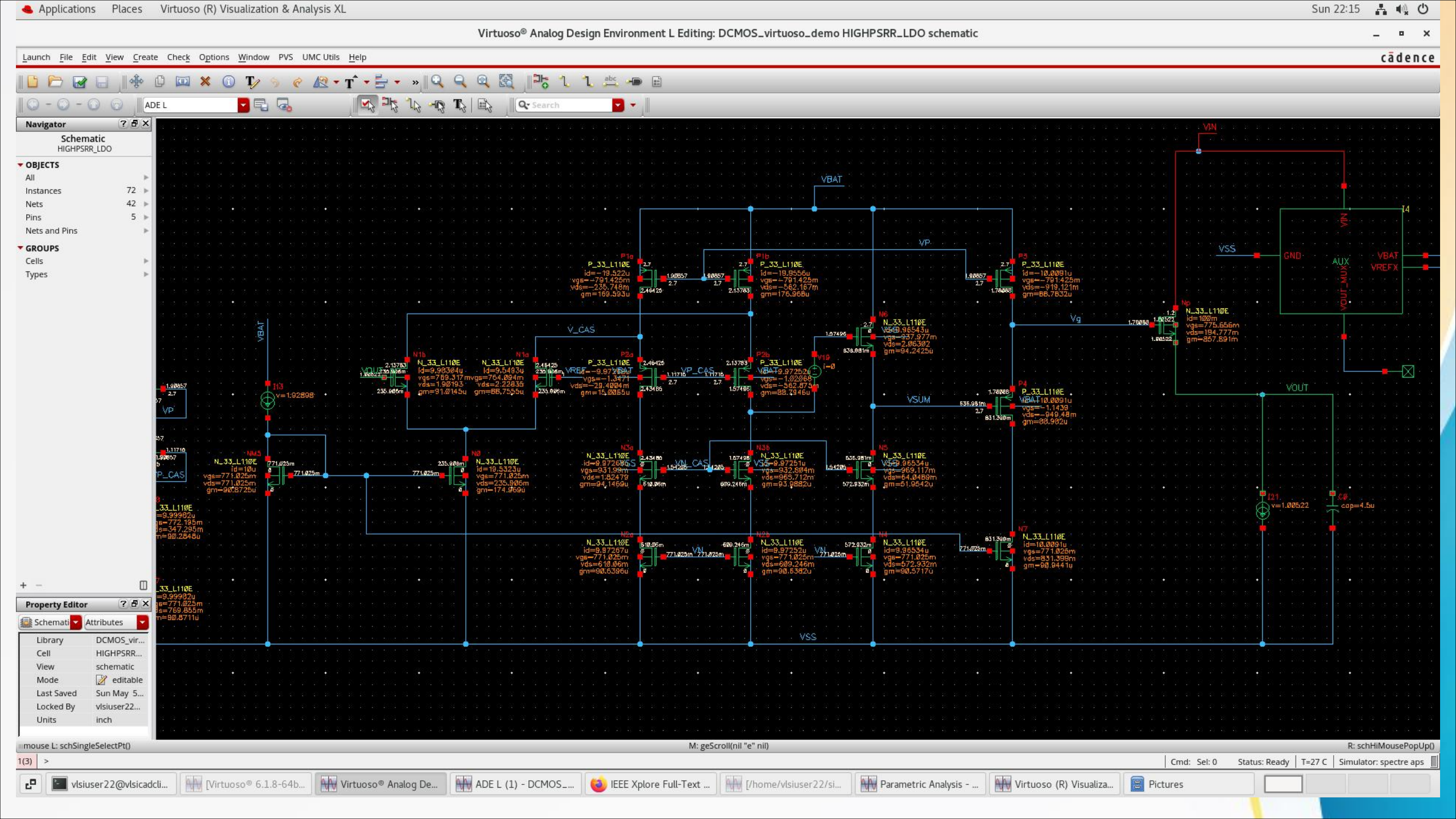
- This paper presents an NMOS Passfet LDO, realized in 65-nm CMOS, featuring >60-dB PSRR over a 10-MHz frequency range and a 100-mA large load current range.

- The high PSRR is achieved by anadaptive feed forward ripple cancellation (FFRC) technique embodying an adaptive load current tracking scheme.

- By means of embodying an NMOS-based power stage, the LDO alsoachieves very low dropout voltage of 80 mV and features very small overshoot and undershoot of 2 and 4 mV respectively.

❑ DC OPERATING POINT




Applications
Places
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VOUT_MUX
V_CAS
Vg
VSUM
VOUT
VN_CAS
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M: geScroll(nil "e" nil)
R: schHiMousePopUp()
Cmd: Sel: 0
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IEEE Xplore Full-Text ...
[/home/vlsiuser22/si...
Parametric Analysis - ...
Virtuoso (R) Visualiza...
Pictures

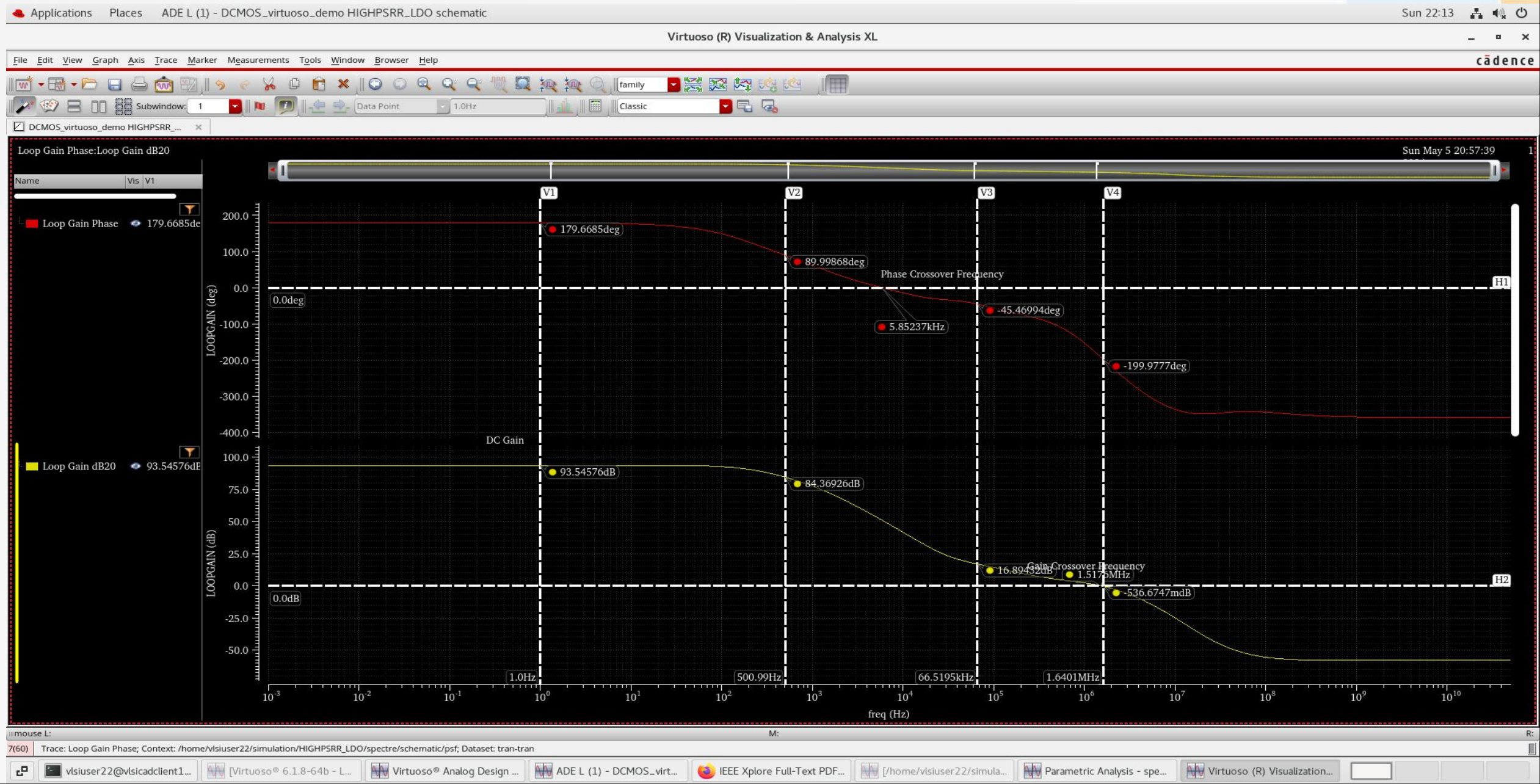
❑ Theory Calculations

MOSFET	I(A)	W(m)	L(m)
nmos	1.00E-05	30.98u	8u
pmos	1.00E-05	115.971u	8u
nmos	1.40E-05	43.38u	8u
pmos	1.40E-05	162.36u	8u
nmos	8.00E-06	24.791u	8u
pmos	8.00E-06	92.77u	8u

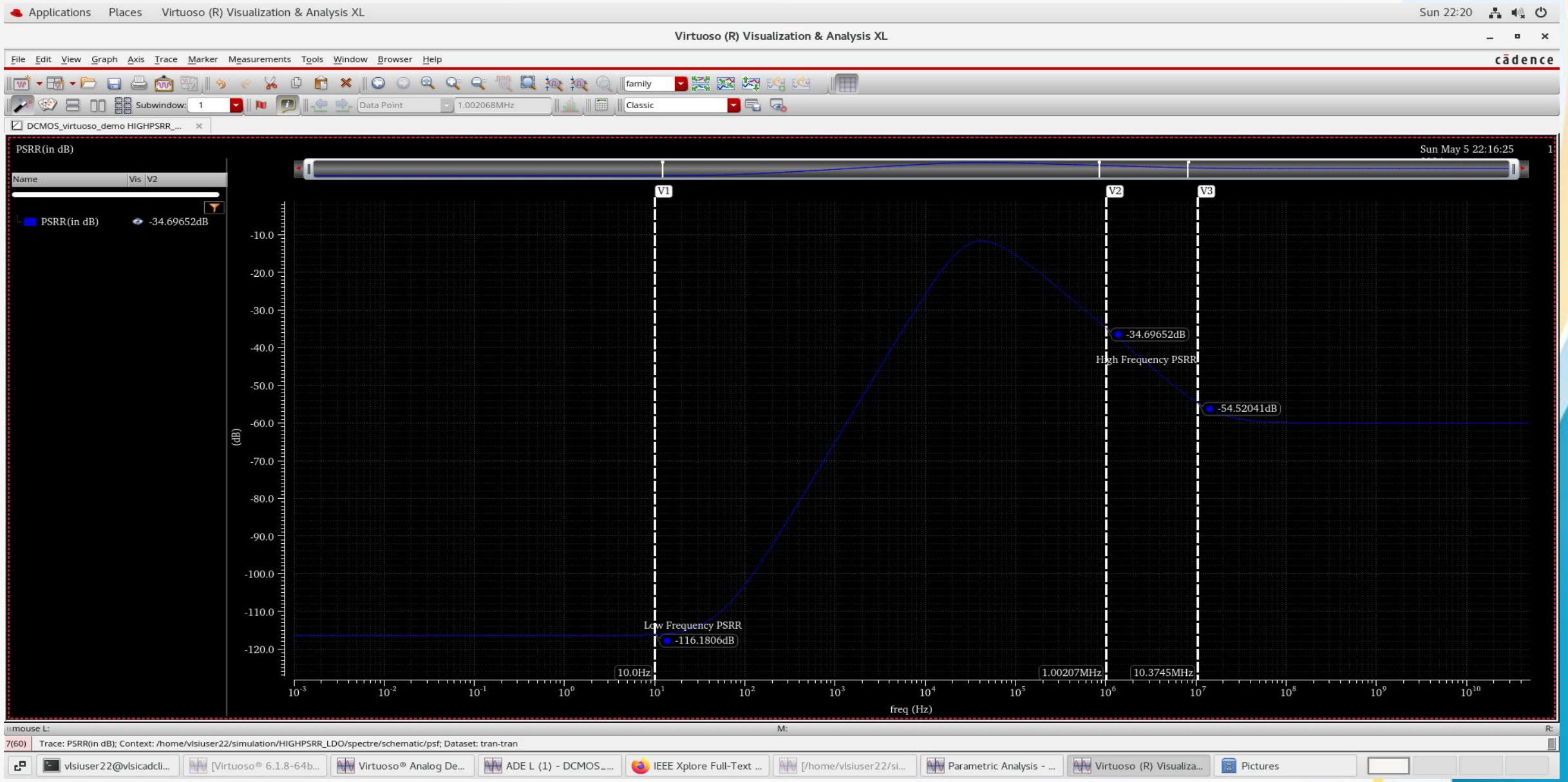
	Rout	Cout	Rout*Cout	1/(Rout*Cout)	
Pole (1st)	4740395.2388	8.352735E-13	3.959527E-06	252555.44328	Hz
Pole (2nd)	2297537.6922	4.162239E-12	9.562901E-06	104570.77841	Hz
Pole (3rd)	8807104.4042	7.411472E-09	0.0652736095	15.320127199	Hz
Pole (4th)	327.111	4.505755E-06	0.001473882	678.48035586	Hz
	GM	Cgs	gm/Cgs		
Zero(1st)	3.08E-01	5.76E-09	53499443.981	Hz	
		Cgd			
Zero(2nd)	9.10E-05	5.50E-15	16545564611	Hz	

DC gain of 1st stage	gm(N1b)*(rout(P1b+P2b)||(N3b+N2b))	rout(p1b)	rout(p2b)	rout(N3b)	rout(N2b)	gm(N1b)	Rout1	Rout2	Rout	Gain(v/v)
		3.88E+06	1.34E+07	6.53E+06	5.24E+06	9.10E-05	17275000	6533140	4740395.2388192	431.44707266
DC gain of 2nd stage	gm(N6)*(rout(N5+N4)||(N6))	rout(N6)	rout(N5)	rout(N4)		gm(N6)				
		9.74E+06	3.22E+03	3.00E+06		9.33E-05	3007079.36	9.74E+06	2297537.69223913	214.34717072
DC gain of 3rd stage	gm(P4)*(rout(P3)||(P4+N7))	rout(P4)	rout(N7)	rout(P3)		gm((P4)				
		1.29E+07	7.14E+06	1.57E+07		8.89E-05	19995890	1.57E+07	8807104.40420547	782.67679988
DC gain of 4th stage	gm(Np)(Np)	rout(Np)				gm(Np)				
		327.111				3.08E-01	327.111			100.7174769

❑ GAIN PLOT AND PHASE PLOT(Without AUX)



❑ PSRR PLOT(Without AUX)



REFERENCE_TABLE_PAPER

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6. https://ieeexplore.ieee.org/document/9036907

THANK YOU