An Ultra-Low Phase Noise Low-Power 10-GHz LC VCO with High-Q Common-Mode Harmonic Resonance for 5G Systems

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***Abstract*—This paper presents an ultra-low phase noise and low-power CMOS LC VCO intended for 5G applications. The proposed design adopts a class-B voltage-biased topology besides incorporating high Q common mode harmonic resonance for ultra-low phase noise performance. Moreover, the design exploits the inherent current reuse mechanism of the complementary cross-coupled configuration to attain a low power consumption level. Furthermore, targeting a sufficient wide tuning range for wideband operation, the designed VCO incorporates both continuous tuning using a low k_{vco} controllable varactor and discrete capacitive tuning through a proposed optimal NMOS-based digitally controlled varactor bank. Designed and simulated in a standard 65 nm RF CMOS technology, the proposed VCO achieves a 16% wide tuning range from 9.2 GHz to 10.8 GHz while consuming a total current of 2.4 mA from a 1 V power supply. Simulated phase noise results showed ultra-low thermal phase noise levels of -124.8 dBc/Hz and -144.8 dBc/Hz at 1 MHz and 10 MHz frequency offsets respectively, while additionally achieving an ultra-low flicker phase noise of -57 dBc/Hz at 1kHz with an outstanding 3.5 kHz $1/f^3$ corner frequency. Accordingly, the designed VCO successfully achieves a superior state-of-the-art peak FoM of 201.7 dBc/Hz and a corresponding 205.7 dBc/Hz FoMT at 1 MHz offsets, which are remarkably the best simulated VCO FoMs of the recently published 10 GHz VCOs.**

***Index Terms*—Low phase noise, Low power, Common-mode resonance, Switched Varactor Bank, Voltage biased, Cross coupled, LC VCO, Microwave, RFIC, 5G.**

I. Introduction

Due to the rapidly growing demand for low power high data rate wireless communications driving the incoming 5G era, a low power high performance Voltage Controlled Oscillator (VCO) becomes a great necessity. This necessity arises as the VCO phase noise adversely limits the modulation Error Vector Magnitude (EVM) for any digital wireless communication system, limiting its performance and the SNR in high-speed data converters. This issue becomes particularly critical in mobile applications where low-power operation is highly demanded.

Recently, many VCO designs have been reported seeking simultaneous low power and low PN operations while providing a sufficient wide tuning range. However, the unavoidable tradeoff between these key parameters establishes a big challenge. Investigating some of these works, almost all of them have deployed extra electronics in their designs trying to mitigate some noise sources. However, these additional components imply a larger area and even introduce other types of noises. For shaping the tail current, [1] introduced two additional capacitors and transistors which moreover needed an external DC bias through two large resistors. All these extra added components despite being introduced to evade some noise sources or mechanisms, their added noises incorporated into the total PN, resulting in an insufficient noise improvement. Meanwhile, [2] proposed a high Q center-tapped inductor while using large sensitive varactors for continuous tuning, which surely loaded the inductor causing a Q degradation and hence minimizing PN enhancement. Also, the use of a switched capacitor bank in [3], sets a lower bound on PN due to Q degradation by bank switches. So, the critical necessity for the simultaneous low PN and low power VCO design still exists. Such simultaneous constraints on PN performance, power consumption level, and tuning range introduce various challenges in the design.

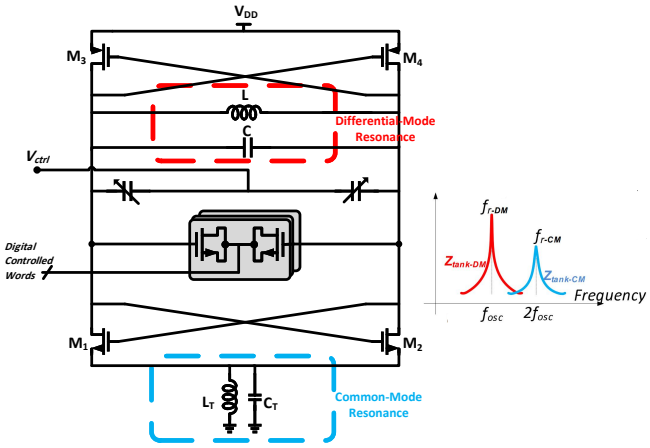

Fig. 1. Simplified schematic of the proposed complementary cross-coupled class-B VCO with resulting differential-and common-mode resonances.

Consequently, in this paper, a low-power VCO with excellent phase noise performance and wideband operation is presented for 5G LO generation in typical 5G transceiver systems [4]. Simultaneously, addressing an ultra-low PN design with a sufficient wide tuning range, while strictly maintaining a low power consumption level, the design demonstrated high Q common mode harmonic resonance for PN reduction, besides adopting a carefully balanced current reuse topology for power minimization. Also, the design is optimized to

operate without a current source, evading its injected noise and consequently achieving lower PN. Moreover, an optimal NMOS-based varactor bank was adopted for maintaining an almost constant undegraded PN performance across the tuning range. Additionally, it had been considered to greatly minimize the current variation during the varactor tuning across the band. Besides these low PN and power consumption levels, the advantages of maintaining both less variant power and PN levels had been verified and reported in the paper.

Following this introduction, section II describes the proposed design and its incorporated techniques. Afterward, section III presents the simulation results and a comparison with the latest published works. Finally, section IV concludes the paper.

II. Proposed Design

Targeting both PN and power consumption reductions had been achieved by acting on the oscillator topology, circuit techniques, and quality factor (Q) enhancement. Owing to the cross-coupled LC VCOs superior PN performance and also seeking the lowest possible power consumption, the complementary cross-coupled current-reuse topology is selected for this LC VCO design. As shown in Fig. 1, the proposed VCO adopted the complementary P-N topology as the VCO core, where the current is reused by the PMOS transistors achieving a higher transconductance for a certain bias current. This advantage consequently enables less power consumption needed for a given LC tank to attain oscillation. Exploiting its inherent current reuse mechanism, the design saves 75% of the current consumed by the conventional NMOS or PMOS-only cross-coupled topologies.

Also, the class-B configuration is preferred due to its simplicity and robustness. However, its PN and power efficiency could be degraded significantly with the tail current source if not designed properly. Resolving this issue and in order to reduce the PN level and improve power efficiency, the voltage-biased topology was adopted removing the tail bias current, which is a major contributor to the VCO PN as seen in the well-known PN equation.

$$\mathcal{L} = 10\log\left[\frac{kT}{Q^2}\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{I_{\text{bias}}^2 R}\frac{\pi^2}{8}(1+\gamma+F)\right] \quad (1)$$

Where $\mathcal{L}$ represents the phase noise, T is the absolute temperature, K is the Boltzmann constant, Q is the loaded quality factor of the tank, f_0 is the oscillation frequency, Δf is the frequency offset, I_{bias} is the bias current, R is the equivalent parallel resistance of the tank, γ is the noise factor of the MOS transistor operating in the active region, and F is a factor accounting for the bias current noise injected into the tank. The proposed design is optimized without a tail current source evading its flicker and thermal noise, moreover avoiding the frequency modulation due to its injected noise. Consequently, the total phase noise performance and power efficiency have been greatly enhanced. Another PN issue of class B operation is encountered during a part of the oscillation period when the gm-devices M_{1-2} enter the deep triode region loading the tank and degrading its quality factor. Addressing this loading issue, the design demonstrates an efficient noise filtering technique by achieving high Q common-mode harmonic resonance through L_T and C_T, shown in Fig. 1 [5,6]. Achieving both high Q differential and common mode resonances, shown in Fig. 2, has successfully guaranteed the targeted ultra-low PN performance.

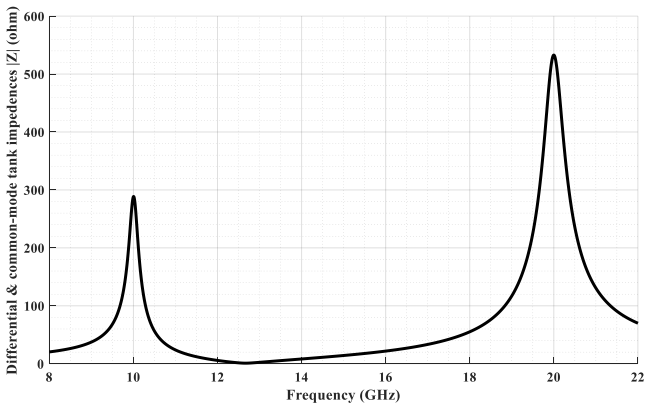

Fig. 2. Simulated differential-and common-mode resonances

Accounting for the advantageous wideband operation, a proposed optimal NMOS-based varactor bank was adopted for discrete tuning which enabled achieving a calculated tuning range with the minimum possible degradation in phase noise performance. Besides the low k_{vco} analog controlled varactors used for the continuous tuning, the bank is digitally switched through 64 thermometer codes to achieve a calculated wide tuning range [7]. Switching the small bank varactors capacitances, each with a value of C_u, adjusts the oscillation frequency from $f_{\min}$ to $f_{\max}$ according to the following equations [8],

$$f_{\min} = \frac{1}{2\pi\sqrt{L\left(C_{\max} + C_{par} + nC_u\right)}} \quad (2)$$

$$f_{\max} = \frac{1}{2\pi\sqrt{L\left(C_{\min} + C_{par}\right)}} \quad (3)$$

Where $C_{\max}$ and $C_{\min}$ are the maximum and minimum analog varactors capacitances respectively, and C_{par} is the core parasitic capacitance. Besides all these mentioned topologies and techniques that have been adopted to achieve ultra-low PN performance along with the minimum possible power consumption and sufficient tuning range, the proposed tank is optimized in terms of its quality factor, avoiding the loading effects degrading its performance. An optimized resonator tank, of both the inductor and varactors, efficiently guaranteed a less variant PN performance during varactor tuning.

III. Simulation results

The proposed cross-coupled LC VCO has been designed and simulated in 65 nm RF CMOS technology. Designed with a 16 % tuning range, the designed VCO exhibits a tunability from 9.2 GHz to 10.8 GHz through 64 overlapping subbands. Fig. 3 depicts the tuning curves of the upper and

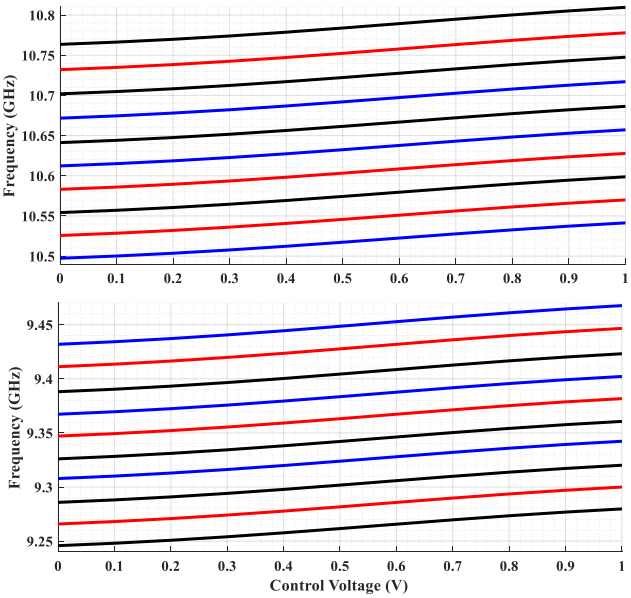

Fig. 3. Upper and lower bands tuning curves

lower bands, showing only 10 subbands for each. Switching the varactor bank branches enables jumping between the 64 subbands which were optimally designed and adjusted with an average overlap of 33%.

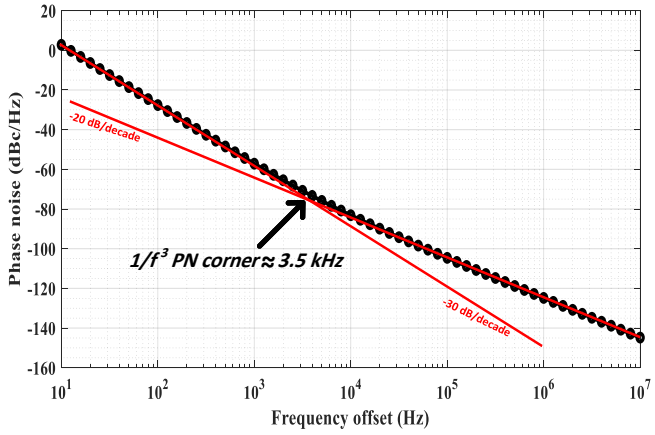

Fig. 4. Simulated phase noise

Evaluating the phase noise performance, the best simulated phase noise of the proposed VCO is displayed in Fig. 4. The figure shows a phase noise of -124.8 dBc/Hz and -144.8 dBc/Hz at offset frequencies of 1 MHz and 10 MHz, respectively. The close-in phase noise is also indicated revealing a very low level of -57 dBc/Hz at 1 kHz offset. As indicated in Fig. 4, an excellent $1/f^3$ PN of 3.5 kHz has been achieved, which is amongst the best-reported VCO $1/f^3$ PN corners. Furthermore, these phase noise levels were displayed across the control voltage range as depicted in Fig. 5. This figure demonstrates a clear indication of the phase noise variation that is kept almost constant across the range, ensuring the preserved undegraded phase noise performance. Advantageously, this notice proves the success of meeting the

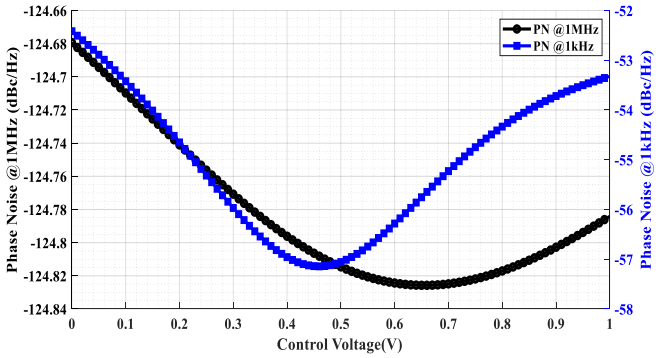

Fig. 5. Simulated phase noise at 1 MHz and 1kHz offsets across the control voltage range

targeted challenging goal of not only lowering the phase noise but moreover keeping its performance undegraded across the fine-tuning range.

In order to verify the low power advantage of the designed VCO, its total DC power consumption has been simulated and reported in Fig. 6. This figure depicts the simulated power consumption across the control voltage range, indicating power consumption of no more than 2.4 mW. Also, this reported figure proves the advantage of minimizing the current variation over each tuning subband.

The most popular widely used VCOs benchmarking parameter, FoM, has been used for evaluating the overall performance of the proposed design in order to fairly compare it with other published designs. FoM is expressed as,

$$FoM = -L(\Delta f) + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (4)$$

where P_{DC} is the DC power consumption. The design competitively could achieve an outstanding state-of-the-art peak FoM of 201.7 dBc/Hz at 1 MHz offset. Also, accounting for the Frequency Tuning Range (FTR), a corresponding FoMT of 205.7 dBc/Hz was achieved. Moreover, fig. 7 clearly depicts the achieved FoM at 1 MHz over the entire upper tuning subband.

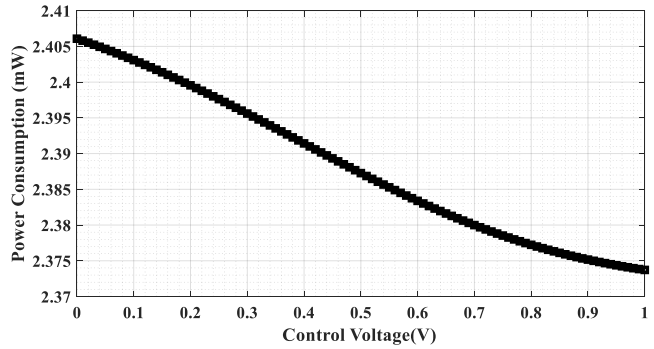

Fig. 6. Simulated power consumption across the control voltage range

According to the aforementioned simulation results, Table I summarizes the overall performance of the proposed VCO and provides a summarized comparison with some of the beof

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH LATEST STATE-OF-THE-ART 10 GHZ VCOS

specification	AICSP'18 [1]*	MWCL'20 [2]	TCAS-II'20 [3]	MWCL'15 [9]	ISCAS'16 [10]*	This work*
CMOS Technology (nm)	180	180	65	65	130	65
Power Supply (V)	1.8	1	0.45	1.2	0.6	1
Power Consumption (mW)	1.45	4	2.7	2.2	1.64	2.4
Center Frequency (GHz)	10	12.7	9.66-11.07	11.2	9.7-10.93	9.2-10.8
FTR $(\%)$	N.A.	16	13.6	9.6	11.9	16
Phase Noise @ 1 KHZ (dBc/Hz)	-27	29*	N.A.	N.A.	-29	-57
Phase Noise @ 1 MHZ (dBc/Hz)	-107.8	-107.7*	-115.4*	-109.7*/-107.7	-112.9	-124.8
Phase Noise @ 10 MHZ (dBc/Hz)	-129	-126.13*	-136.3*	N.A.	-133.3	-144.8
FoM @ 1 MHZ (dBc/Hz)	186.2	184.4	191.4	185	190.5	201.7
FoMT @ 1 MHZ (dBc/Hz)	N.A.	188.5	192.3	185	190.9	205.7
Simulation/Measurement	Sim.	Meas.	Meas.	Meas.	Sim.	Sim.

* Simulation results

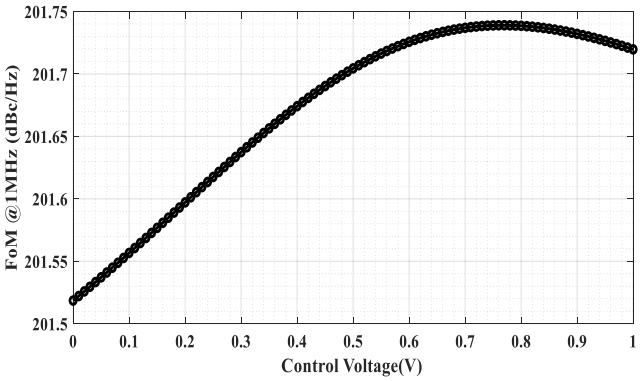

Fig. 7. Achieved FoM at 1 MHz across the control voltage range

st latest state-of-the-art relevant 10 GHz designs. Compared to the referenced designs, the designed VCO achieves the best phase noise performance with competitively low power consumption, hence the best FOM, as well. Results of both [1] and [10] are simulation results just as the case in this paper. However, the reported results of [2,3,9] are measurement results but their simulated phase noise results were reported instead of the measured ones to provide a fair comparison of phase noise performances. Clearly, the presented comparison proves the superiority of this work showing that all FoMs of the mentioned works are significantly far enough from these of the proposed design.

IV. CONCLUSION

In this paper, an ultra-low phase noise, low-power LC VCO in 65 nm RF CMOS is presented. The low phase noise is attributed to the use of a class-B, tail-current free VCO topology, in addition to the use of high Q common-mode harmonic resonance. On the other hand, the low power is attributed to the current reuse mechanism of the designed VCO Complementary P-N configuration. The design achieves a wide tuning range by incorporating a low k_{vco} analog controllable varactor for continuous tuning, together with a proposed optimal NMOS-based digitally controlled varactor bank discrete capacitive tuning. The designed VCO achieves phase noise of -124.8 dBc/Hz and -144.8 dBc/Hz at 1 and 10 MHz frequency offsets, respectively, with a tuning range of 16% while consuming no moore than 2.4 mW. In addition, the design outstandingly achieves an ultra-low $1/f^3$ PN of -57 dBc/Hz with a 3.5 kHz $1/f^3$ PN corner frequency. Accordingly, the designed VCO achieves a superior state-of-the-art FoM of 201.7 dBc/Hz and 205.7dBc/Hz FoMT at 1 MHz offsets. To the authors' knowledge, this is the highest published simulated VCO FoM.

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