A Low Phase Noise 11.8-15.3 GHz CMOS LC-VCO with High-Q Inductor

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***Abstract*—This work presents a 14GHz LC voltage controlled oscillator (VCO) by using high quality (Q) factor inductors. The LC-VCO consists of a NMOS cross-coupled pair and differential buffer for test purposes. To increase the VCO phase noise performance, double-turn parallel single-width inductor is used to achieve high tank quality factor. With 5-bit control bits, the VCO has a wide frequency tuning range (FTR) of 25.9% (i.e. from 11.8 GHz to 15.3 GHz). At 14.64 GHz, the measured phase noise is -136.57 dBc/Hz @10 MHz offset frequency, which corresponds to a figure of merit (FoM) of -188.25 dBc/Hz. Fabricated in a 65 nm CMOS process, the core VCO has an area of 210 µm × 360 µm.**

Keywords—CMOS, VCO, low phase noise, wide tuning range.

I. INTRODUCTION

Due to the rapidly increasing demand for high data rate communication, it is very critical to realize the low phase noise PLL. As a key building block of the PLL, the voltage controlled oscillator (VCO) typically limits the PLL phase noise and tuning range performance.

Typically, a well-performing VCO requires a small chip area, low phase noise, and wide tuning range. Therefore, many factors should be considered during the design process. To address these issues, targeting at 5G communication, this paper introduces a 11.8-15.3 GHz cross-coupled LC-VCO with wide tuning range and low phase noise. With 5-bits switch capacitors, the VCO achieves a 3.5GHz tuning range (i.e. from 11.8 to 15.3GHz), and a phase noise of -136.57 dBc/Hz at 10MHz offset from 14.64 GHz.

This paper is organized as follows. In Section II, the proposed complementary cross-coupled VCO circuit topology is discussed. Then Section III discusses the measurement results. Finally, conclusions are drawn in Section IV.

II. CIRCUIT DESIGN

A. VCO toplogy

As shown in Fig.1, with easy startup advantage, the cross-coupled oscillator topology is widely used in wireless communication, in which the cross-coupled transistor pair generates the negative Gm and compensates the tank loss. As shown in Fig. 2, the output buffer amplifier is realized with a two-stage self-biased CMOS inverter to drive the 50 Ω load[1]. Since the buffer amplifier reduces the Q-factor of LC-tank, the size of the transistors in the first buffer stage and that of the capacitors need to optimized to suppress their effect on the phase noise.

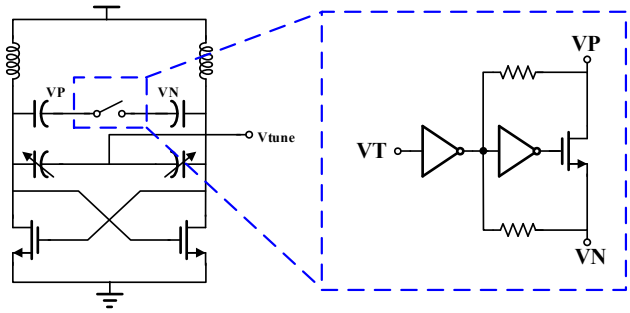

Fig. 1. The VCO toplogy

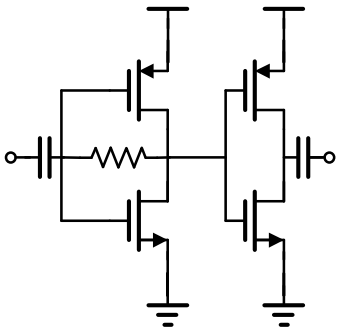

Fig. 2. The schematic of the output buffer

B. Inductor

As discussed in [2], the transistor and passive LC tank directly contributes to the phase noise, which is captured by the Leeson formula [3,4].

$$L(\Delta\omega) \propto F\frac{4KTR_{\text{Tank}}}{V_0^2}\left(\frac{\omega_0}{2Q_{\text{Tank}}\Delta\omega}\right)^2 \qquad (1)$$

where F is the noise factor, K is Boltzmann's constant, T is the temperature, V_0 is the output signal amplitude, R_{Tank} is the tank parallel characteristic resistance, Q_{Tank} is the tank Q-

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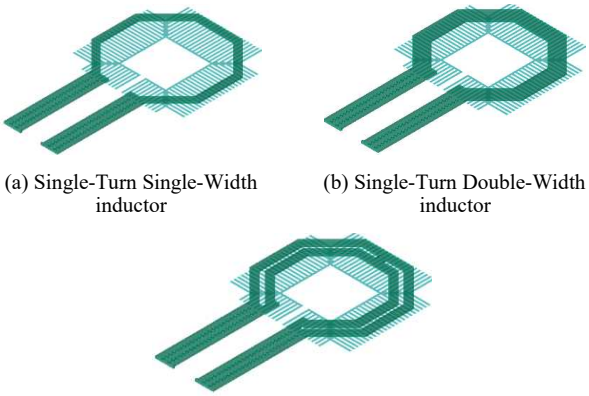
factor, ω_0 is the oscillation frequency, and $\Delta\omega$ is the offset frequency. According to this formula, the tank Q-factor should be maximized to increase the phase noise performance. In 10 GHz frequency range, the Q-factor of the on-chip capacitor is significantly higher than that of the on-chip inductor. In other words, the Q-factor of the inductor determines the quality of the overall LC resonator [2]. In CMOS process, on-chip planar spiral structures are usually realized with top metals, in both symmetrical and asymmetrical forms, for its benefits in low parasitic [3].



(a) Single-Turn Single-Width inductor

(b) Single-Turn Double-Width inductor

(c) Double-Turn Parallel Single-Width inductor

Fig. 3. The inductor implementation

In this paper, to increase the tank quality factor several inductor implementations are investigated. To relax the substrate loss, a float metal shielding scheme is used. As shown in Fig. 3, with simulations it is found that the conventional Single-Turn Single-Width inductor has a higher inductance and higher loss. To reduce the ohmic loss, a Single-Turn Double-Width inductor can be used, as shown in Fig. 3(b). Compared with Fig. 3 (a), the inductor in Fig. 3(b) has a higher quality factor. However, due to skin effect [5,6], its quality factor is limited at higher frequency range. To solve this issue, in Fig. 3(c) a Double-Turn Parallel Single-Width inductor is proposed. Compared with the inductor in Fig. 3(b), the inductor in Fig. 3(c) has a similar DC resistance, but it can relax the skin effect, thereby increasing the quality factor.

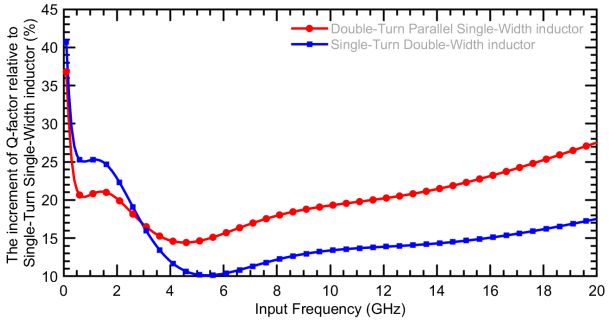


Fig. 4. Comparison of Q-factor increments

To compare the quality factor of different inductor, Fig. 4 shows the performance comparison of the inductors in Fig. 3. Clearly, compared with the conventional Single-Turn Single-Width inductor, due to wide metal the quality factor of the Single-Turn Double-Width inductor is improved by about 15% from 10 to 18GHz. In contrast, on top of large width, due to relaxed skin effect the quality factor of the Double-Turn Parallel Single-Width inductor is improved by about 25% over that of the conventional Single-Turn Single-Width inductor. As a result, in this design the Double-Turn Parallel Single-Width inductor in Fig. 3 (c) is used for the VCO design.

III. MEASUREMENT RESULTS

Fig. 5 shows the chip micrograph of the VCO. It is implemented in a 65-nm CMOS process, and its core area is about 0.56×0.60 mm^2. The VCO consumes a dc power consumption of about 14.4 mW from a 1.2-V supply.

With the Rohde & Schwarz phase noise analyzer equipment, the oscillator tuning range, the output power, and the phase noise are measured. The VCO has a 5-bit control bit and covers the frequency band from 11.8 to 15.3 GHz. At 14.46 GHz, Fig. 6 shows the VCO output spectrum and phase noise performance. The VCO achieves a phase noise of −136.57 dBc/Hz at 10-MHz offset. Across the tuning range, the measured output power is about -9.3 dBm, which includes a line loss of about 2.5 dB.

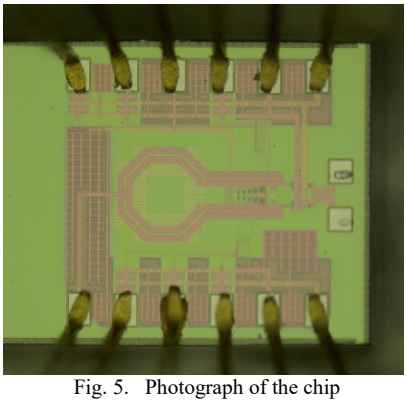
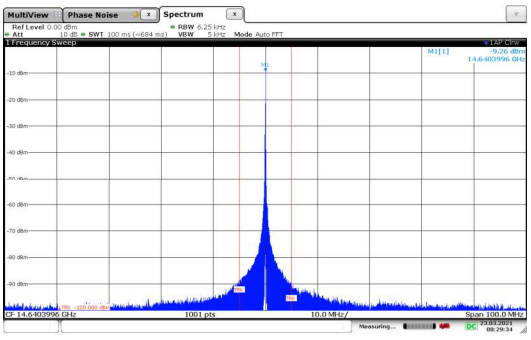
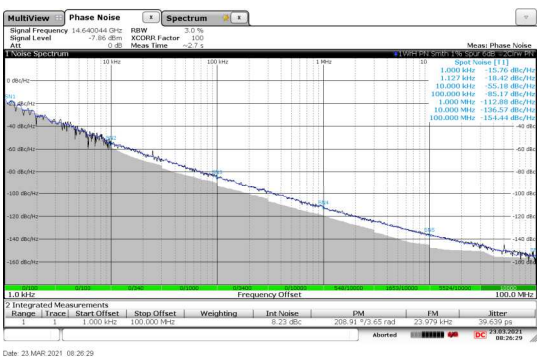


Fig. 5. Photograph of the chip



(a)



(b)

Fig. 6. Phase Noise (a) and its output spectrum (b) at 14.64 GHz.

Table I summarizes the comparison with state-of-the-art results. With the high Q-factor inductor, the oscillator achieves better noise performance at 10 MHz offset with a large tuning range, resulting in an Figure of Merit of −188.25 dBc/Hz at 10MHz offset.

TABLE I. PERFORMANCE COMPARISON OF VCOs

Ref	***[1]***	***[7]***	***[8]***	***THIS WORK***
Technology	56 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Supply voltage(V)	0.5	1.2	2	1.2
Frequency (GHz)	8.66-10.90	8.5-10.5	10.6 - 11.7	11.8 -15.3
Power (mW)	5.32	15.84	32	14.4
Phase Noise (dBc/Hz)	-119.02 @5 MHz	-127.54 @10 MHz	-116 @1 MHz	-136.57 @10MHz
FoM	-176.0	-185	-178	-188.25

$$FoM = PNoise - 20\log(f_0 / \Delta f) + 10\log(P_{DISS} / 1mW)$$

IV. CONCLUSION

In this paper, a 14GHz LC voltage controlled oscillator (VCO) is realized in a 65 nm CMOS process. To increase the phase noise performance, a double-turn parallel single-width inductor with the slow wave shielding is proposed, which relaxes the skin effect at the operating frequency range and improves the tank quality factor. The VCO has a measured tuning range (FTR) of 25.9% (i.e. from 11.8 GHz to 15.3 GHz). At 14.64 GHz, the measured phase noise is -136.57 dBc/Hz @10 MHz offset frequency, which corresponds to a figure of merit (FoM) of -188.25 dBc/Hz.

ACKNOWLEDGMENT

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