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Design of 6.7 GHz ~7. 518 GHz Cross Coupled LC-VCO in 180nm CMOS technology

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Abstract—**This paper discusses the analysis and design of LC VCO in 180nm CMOS technology with 7 GHz resonating frequency using Cadence Virtuoso environment. The designed circuit works at 1.8 V supply voltage. VCOs are the main component of PLL that is used in the generation of IR pulses in UWB systems. The designed LC – VCO with a bandwidth of 6.711 GHz - 7.518 GHz is to be used in the IR-UWB system that generates short pulses using indirect IR-UWB method. The gain K_{VCO} of LC VCO designed was 484 Mhz/V. The output power P (mw) was 2.25mw. The observed Phase noise at 1MHz is -103.2dbc/Hz and at 10 MHz is -131.5dbc/Hz. The resonating frequency was verified using PSS analysis, which gives a resonating frequency of 7 GHz. The FOM of the designed VCO is -136.98 8 dbc/Hz.**

Index- LC-VCO,CMOS, UWB,Phase Noise,PMOS Capacitor, Tuning Range

I. INTRODUCTION

The emerging demand for the wireless products that are low in cost, compact in size, high frequency and have a low power consumption has increased in the field of wireless communication. Recent advances in integrated circuit design enabled the development of high frequency VCOs, an important part of PLL. PLL's are part of a majority communication receivers. UWB technology is a technique that has been evolved for short-range communication. The release of wideband spectral masks uses unlicensed 3.1GHz to 10.6GHz with a minimum bandwidth of 500MHZ[1][2]. Several VCOs in SiGe BiCMOS technology have already been reported for high-speed applications. Large phase noise appears on their output signals[3][4] that gives rise to spectral overlap or reciprocal mixing . The Power dissipation was more [5] and Low tuning range[3][6]. Designing of high-speed LC VCO is challenging as the speed of operation of CMOS are lower that of SiGe.VCO based application form the fundamental components of any communication System on Chip (SoC). CMOS technology has the potential advantage of being able to integrate peripheral circuitry on a massive scale on the transceiver chipset which provides high density; hence implementation of wireless systems is efficient. CMOS technology is good choice since reduces cost and low power compared to other technologies.

The most widely used oscillator structures are Ring oscillator and *LC* oscillator. Considering the Phase noise parameter is better for LC oscillator compared to poor phase noise of ring oscillator in this paper we choose LC oscillator for implementation. A number of CMOS, PMOS only, NMOS only LC-VCOs have been reported in the literature [3-5]. The topology of PMOS only circuit has similarity with the NMOS only topology. However, with the variations in the mobility, the size of transistors is twice greater than nmos transistor to achieve the similar transconductance. Hence PMOS cross coupled VCO consume more power when compared to other two topologies [5][8]. Compared to PMOS cross coupled VCO , NMOS cross coupled VCO consumes less power and low phase noise[5].

By using the complementary oscillator circuit to generate the negative resistance reduces the noise up conversion properties [3][4]. Advantages of CMOS cross coupled VCOs compared to other two are, CMOS cross coupled VCOs gives double the output amplitude compared to the NMOS cross coupled circuit[5][7], power consumed is less[6][7], low Phase noise[8][9] and higher transconductance[10] . These oscillators can be modelled in two ways, feedback model and the negative-resistance model. Generation of negative resistance for a differential VCO by the use of cross-coupled transistors

In this paper we confine ourselves to designing and implementing the CMOS cross coupled oscillator as shown in figure 1. The purpose of this paper is to get a clear understanding of the important analysis and parameters that are needed to be measured before actually implementing the entire VCO core.

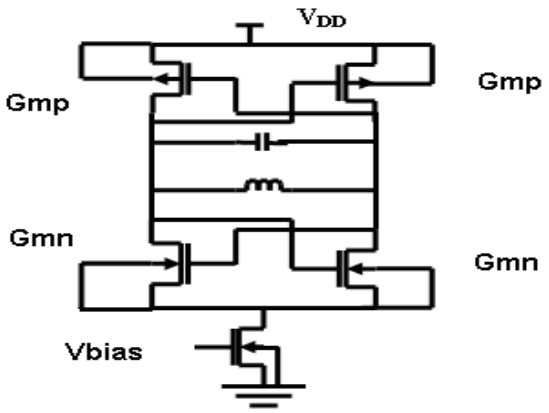

Figure. 1. Simple CMOS complementary -G_m oscillator

II. Analysis and parameters measured before actually implementing the entire LC VCO.

The main analyses involved in designing the VCO are AC and transient analysis. Before actually implementing the entire CMOS cross coupled LC VCO, analyzing the ac and transient behavior of the basic parallel resonator circuit is important.

A. AC Analysis of basic parallel Resonator.

In the AC analysis the important parameters measured are the resonating frequency and the Losses in the tank circuit i.e. Rp, the total resistance of the tank circuit. The Schematic of a parallel LC in 180nm CMOS technology using Cadence Virtuoso environment is shown in figure 2. The AC response is observed by giving a sine wave at the input and measuring the resonating frequency (f_{res}). It is a plot of current verses frequency. The cadence virtuso setup for the plots is as shown in figure 3. As in parallel resonator the resonating frequency i.e. f_{res} is measured by selecting the current of the entire circuit. This is the frequency which gives minimum current as shown in figure 4.

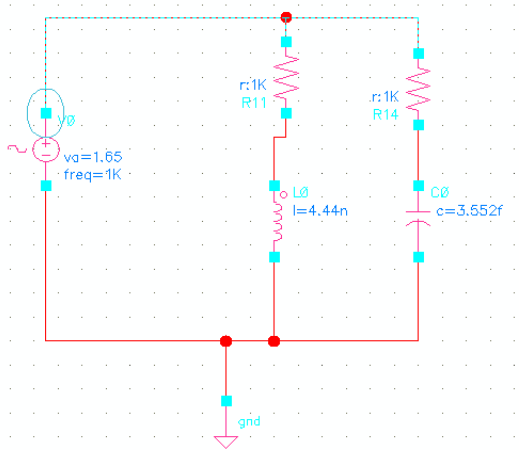

Figure 2 : Schematic of a parallel LC parallel LC to measure F_{res}

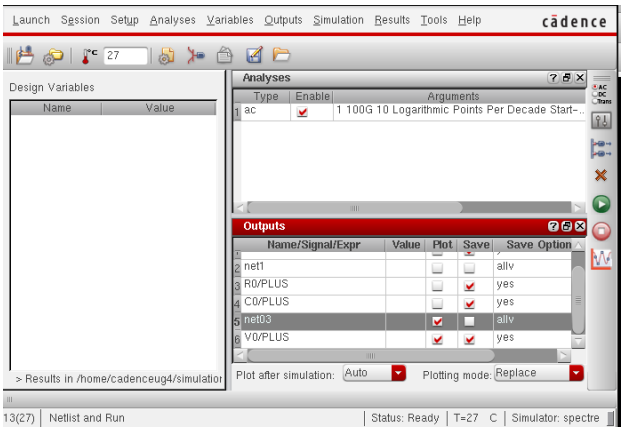

Figure 3 : Virtuso ADE setup of a parallel LC

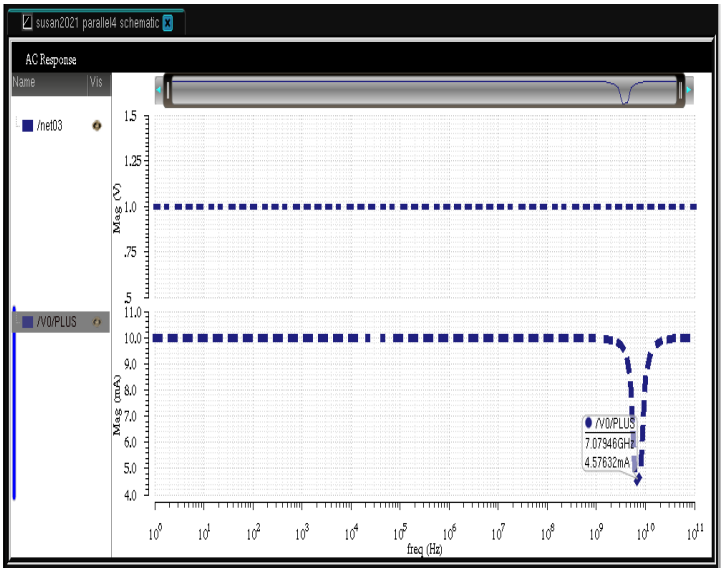

Figure 4 : Resonating frequency plot of a parallel LC

In the AC analysis the total resistance i.e. Rp of the tank circuit is also measured as shown in figure 5. This parameter is helpful to cancel the loss using CMOS cross coupled in the VCO design. To get the plot of Rp select both input current and voltage of parallel resonator. Then by following the procedure outlined for measuring current resonating frequency and the voltage across the resonator (indicated in Figure 6) are obtained as shown in figure 7.

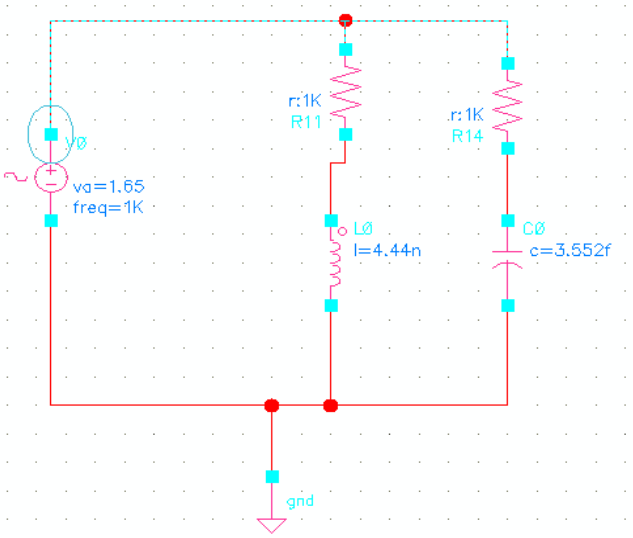

Figure 5 : Schematic of a simple parallel LC to measure Rp

Plot of Rp is obtained by simulating the circuit shown in Fig. 5

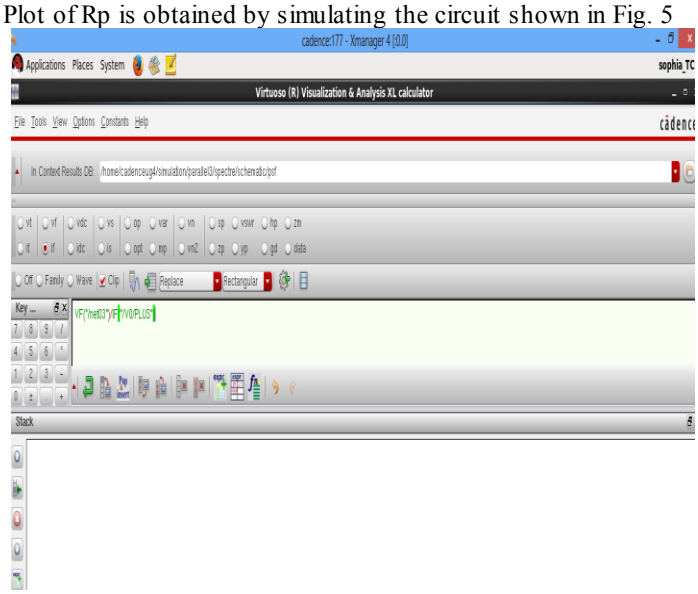

Figure 6 : Calculator tool to calculate Rp of a simple parallel LC

Once the above circuit is simulated, to calculate and plot Rp use calculator from tool. A plot will be generated as shown in Fig. 7. This plot gives the Loss in the tank circuit i.e. Rp the total resistance of the tank circuit.

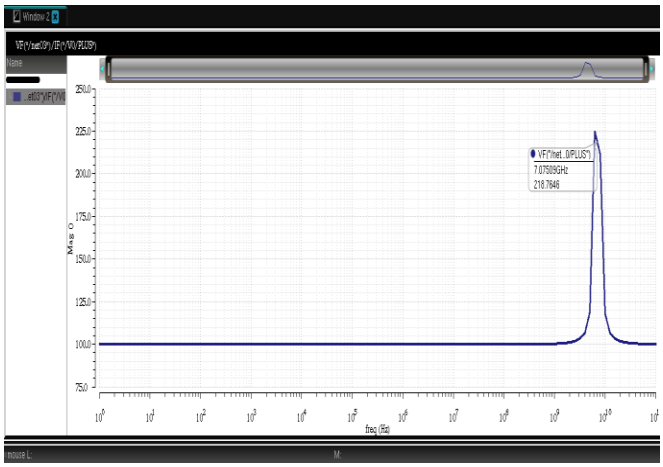

Figure 7:Plot of Rp the total resistance of the tank circuit.

B. Transient Analysis of basic parallel Resonator .

From the ac analysis we obtain the resonating frequency of the tank circuit as well as the Rp. To get the desired resonating frequency we adjust the values of C and L. Once the resonating frequency is obtained by adjusting the values of L and C ($\omega = \frac{1}{2\pi\sqrt{LC}}$). We need to check whether the oscillation is self sustaining by removing the ac input. The modified schematic is shown in figure 8. In real world noise will act as the input for the start of oscillation. As the software is a noiseless environment we have to use initial conditions to start the oscillation. We can give intial condition at a node in two methods. In the first method the initial condition is given by using a capacitor connected in parallel with the basic resonator as shown in figure 8. Initially, the capacitor is given a default voltage, which will act as the initial node voltage, with time the voltage on the capacitor will discharge and it will have no effect on the operation of the circuit. The other method is to use initial conditions option provided by cadence virtuoso ADE. In simulation option on the tool bar we have to select Convergence aids which has initial condition option. After selecting the initial condition option then click on the node for setting the initial value and set the value. The observed parameter are the oscillating waveform (figure 10) and the voltage of the capacitor with initial condition. The initial value of the capacitor gradually becomes zero, which does not have any impact on the circuit as shown in figure 9.

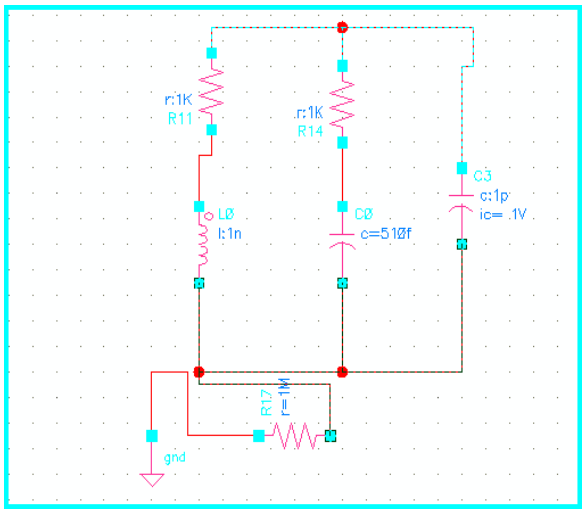

Figure 8: Schematic of a simple parallel LC without ac input

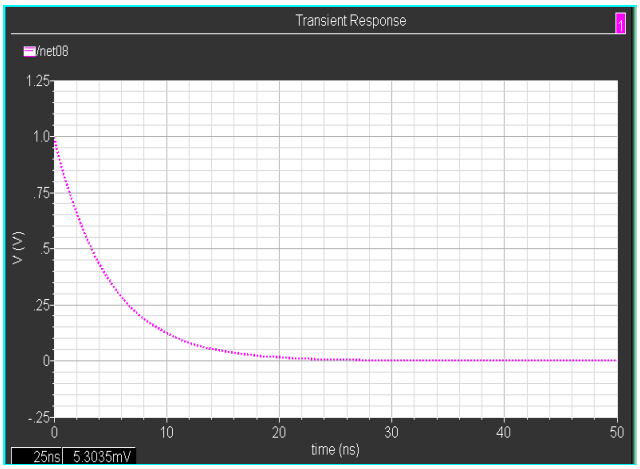

Figure 9: Plot of the voltage of the capacitor with initial condition

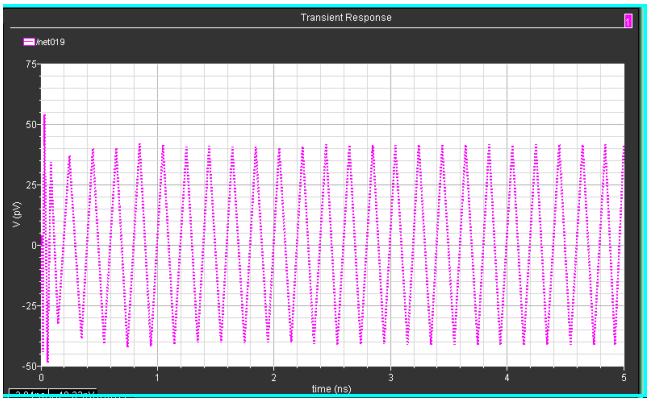

Figure 10: Plot of the oscillating waveform with initial condition

C. *AC Analysis of basic parallel Resonator by using PMOS capacitors to increase the tuning range*

In this paper to increase the tuning range the capacitors are replaced by PMOS capacitors with centertap as shown in Fig. 11. The cadence virtuoso setup for the plots will be similar as shown in figure 3. The AC response, which gives minimum current is obtained is also similar to figure 4.

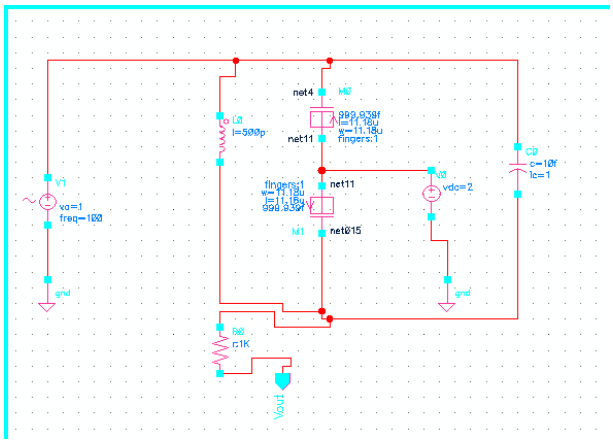

Figure 11: Schematic of *parallel Resonator by using PMOS capacitors*

These are the analysis and parameters needed to be measured before actually implementing the entire VCO.

III. Design Specifications

CMOS Technology	:	180nm
VCO	:	7 GHz
V_{dd}	:	1.8 V
V_{cnt}	:	0.1V to 1.35V
VCO Tuning range	:	800 Mhz
VCO frequency gain	:	500 Mhz/volts
Phase noise	:	<-100dBc/Hz @1MHz
Power of VCO	:	< 4mw
FOM	:	<-130 dBc/Hz

IV. DESIGN , IMPLEMENTATION AND RESULTS

A . Design

In this work the parameter values chosen are:

V_{dd} =1.8V ,V_{bias}=500mV

Design:

For f_{res}=7GHz

Choose L=1nH

C_{in} = 10fF

C_1=C_2= 1pF

The variable capacitance is given by equation 1

$C_{var}=(C_1C_2)/(C_1+C_2)$ (1)

Therefore C_{var} = 0.5pF

Therefore $C_{total}= C_{in}+C_{var}$= 10fF+0.5pF=510fF

$Q = f_{res}/BW$ (2)

Where Q=Quality factor

F_{res}= Resonating frequency
BW= Bandwidth= f_h-f_l
Also $Q=R_p \sqrt{(C_{total}/L)}$ (3)
Where R_p= LC parallel Resistance
Hence $G_{tank}=1/R_p$ (4)

To ensure the oscillation to occur , the G_m associated with the active device (PMOS and NMOS) should be greater than G_{tank}. A safety factor need to be considered to satisfy that condition.
In a parallel cross-coupled pair the negative transconductance G_m is given by equation 5 :

$$G_m = \left(\frac{G_{mn} + G_{mp}}{2} \right) \qquad (5)$$

The transconductance G_{mn} and G_{mp} *are* associated with the NMOS and PMOS transistors, respectively. Choosing G_{mn} be equal to G_{mp} to achieve symmetry in the output of the VCO.
The MOS devices are sized, i.e., the W/L ratio of the NMOS and PMOS devices constituting the *-Gm* core are computed using the relations indicated in equation 6 and 7 respectively.

$$G_{mn} = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{th}) \qquad \mathbf{(6)}$$

$$G_{mp} = \mu_p C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{th}) \qquad \mathbf{(7)}$$

B.IMPLEMENTATION

In this section Schematic (figure 12) and output plots (figure 13) for LC VCO are shown. From figure 13, we get f_{res}= 7Ghz (from ac analysis), BW=f_h-f_l= 7.393Ghz-6.454 Ghz=0.939Ghz.

Substituting the values in Equation 8 ,we get R_p=329.8Ω.

$$Rp = \frac{fres}{BW\sqrt{\frac{C}{L}}} \qquad (8)$$

therefore G_{tank}=3.032mS. The MOS devices are sized, i.e., the W/L ratio of the NMOS and PMOS devices constituting the *-Gm* core are computed. Schematic and the plot of LC VCO for Oscillation without AC is checked as shown in figure 14.In order to find the tuning range: Varied V_{cont} and checked for the frequency of oscillation. The different values are tabulated as given below in table 1.

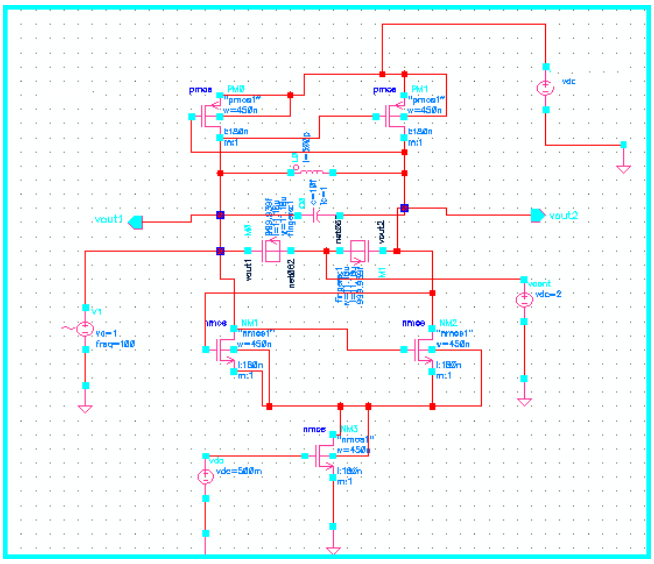

Figure 12 : Schematic for AC analysis of LC VCO

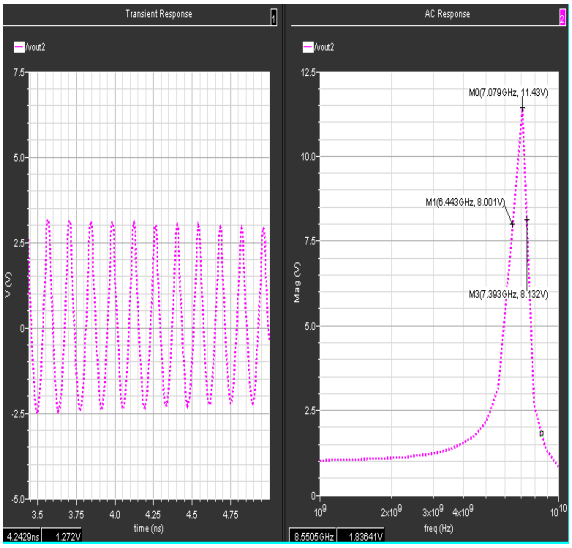

Figure 13 : Plot for transient and AC analysis of LC VCO.

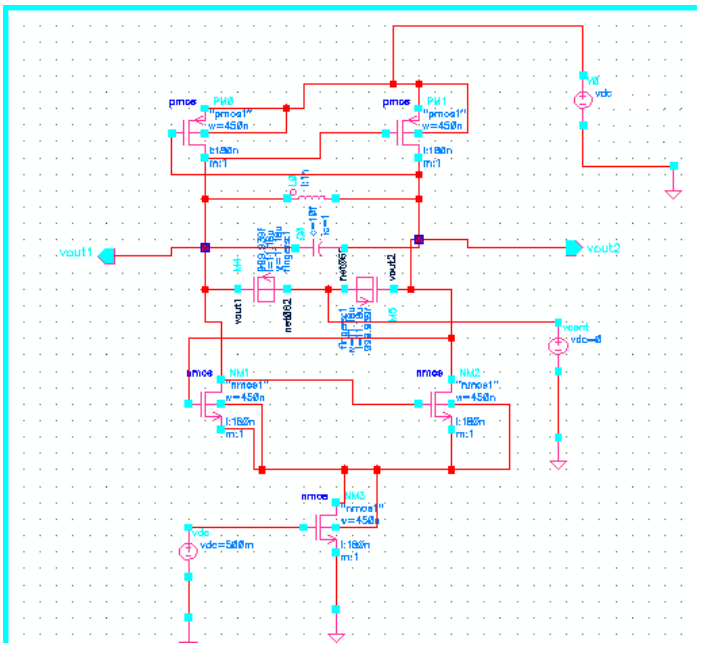

Figure 14 : Schematic of Oscillation without AC of LC VCO

Table 1: Varies V_{cont} the obtained f_{res}

Sl.No	V_{cont}	
1	100mV	6.711Ghz
2	500mV	6.896 Ghz
3	1V	7.092 Ghz
4	1.25V	7.35 Ghz
5	1.35V	7.518 Ghz

D. Result

The designed LC-VCO has a resonating frequency of 7GHz.The designed VCO was linear when the control voltage is in the range of 0.1v to 1.35v. From the transient analysis the bandwidth was observed to be 799MHz and 939MHz was obtained from AC analysis. The linear Gain of the VCO was measured to be 484 MHz/V. The output power P(mw) was 2.25mw. The observed Phase noise at 1MHz is -103.2dbc/Hz and at 10 MHz is -131.5dbc/Hz (figure 15). The resonating frequency was verified using PSS analysis as shown in figure 16, which gives a resonating frequency of 7 GHz. The FOM of the designed VCO is 184.88dbc. Table 2 summarizes simulated results and performances of reported VCOs.

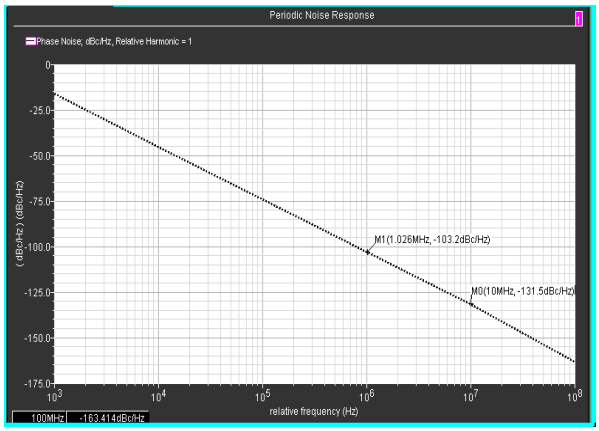

Figure 15: Phase Noise of LC VCO

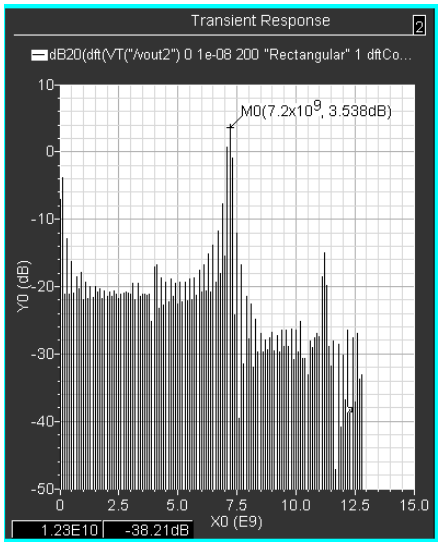

Figure 16: Output of PSS Analysis.

Table 2:Performance comparison with reported VCOs

CMOS Tech	f_{res} (Ghz)	V_{dd} (V)	Phase Noise (dbc/Hz)	Power (mw)	FOM (dbc/Hz)	Ref
0.18µm	5	5	-120.4 @1Mhz	8.1	-189.6	[12]
0.18µm	2	1	-103 @100Khz	1.8	-182.3	[13]
0.35µm	5.2	2.7	-90 @100Khz	0.5	-130.4	[14]
0.18µm	2.4	1.2-V	--106.2 dBc/Hz at 400 kHz	4.4	-176.2	[15]
0.18µm	7	1.8	-131.5 @10Mhz	2.25	-136.98	This work

V. CONCLUSION

In this paper the analysis to build a LC VCO starting from the basic parallel LC resonator to the actual designing of CMOS cross coupled is discussed. The designed CMOS cross coupled LC VCO is designed in a 180nm CMOS technology . The designed LC – VCO with 6.711 GHz - 7.518 GHz is proposed for The IR UWB system that generates short pulses using Indirect IR-UWB method to generate the RF signal. This LC VCO is designed to maintain linearity of the VCO frequency gain for resonating at 7GHz , which uses PMOS capacitors for wide tuning range, using Cadence tools for the given specification. A Cross coupled LC VCO topology is chosen to achieve low phase noise.

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