A Voltage Controlled Oscillator with Inductive Divider Design and Analysis at Frequencies Above 100 GHz

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***Abstract*— Millimeter wave oscillators are of particular interest towards future communications and sensing as frequency multiplication of local oscillator signal is resulting in degraded performance. At high frequencies, the quality (Q) factor of the LC tank is degraded. Thus, a higher transconductance (G_M) size is required to compensate the losses, thereby consuming high power. Numerous techniques have been adopted to reduce the power consumption of a cross-coupled LC voltage controlled oscillator (VCO) and to improve the negative resistance (R_{neg}) associated to it. One of them utilizes inductors in the cross-coupled pair. In this paper, we examine the trade-offs of this inductor to improve negative resistance above 100 GHz. For the analysis, the transistor model is being verified with the simplified small-signal equivalent model. Moreover, we have studied the inductor influence on the transition frequencies of the cross-coupled pair. The restrictions of this technique at high frequencies is investigated. To study the benefits of this technique, an oscillator core is designed and simulated using the 22nm FDSOI CMOS process. It exhibits a tuning range of 5.4% from 125.5 GHz to 132.5 GHz, and phase noise from -101.23 dBc/Hz to -102.0381 dBc/Hz at 10 MHz offset over the entire tuning range. The VCO consumes power of 17 mW. In simulations, an improvement in power consumption by 4.3 mW and phase noise by 1.5 dBc/Hz were achieved when compared to conventional LC Tank VCO.**

Keywords—VCO, CMOS, LC-VCO, inductive divider, tuning range, phase noise, sub-terahertz, voltage-controlled oscillators, mm-wave, radio frequency.

I. INTRODUCTION

Conventional cross-coupled pair VCOs at mm-wave frequencies require large transconductance (G_M) to compensate for the losses incurred by the LC tank due to the low quality factor (Q) of the varactors or capacitors. The Q value affects the phase noise (PN) performance whereas the contribution of the fixed parasitic capacitance (C_{par}) by the active circuitry in the VCO affects the frequency tuning range (FTR), respectively. Moreover, having a large G_M in the circuit is power-hungry and consumes a lot of power to generate negative resistance. Thus, low power, high-performance VCO design is of essence. In the past decade, efforts have been made to design a low voltage, low power i.e. mm-wave CMOS VCO. An effective impedance balancing technique was introduced in [1] by placing an inductor between the gate and drain terminals of the negative G_M cross-coupled pair stage as shown in Fig. 1 (b). The inductor assisted in the improvement of the negative resistance and therefore the size of the G_M transistors in the cross-coupled pair stage was reduced improving power consumption, phase noise and tuning range.

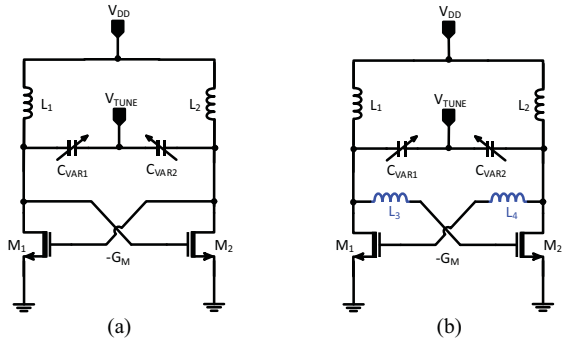

Fig. 1. (a) Conventional cross-coupled LC oscillator (b) An Inductive divider cross-coupled LC oscillator.

In [1], the designed oscillator achieved a tuning range of 8.75 GHz at a center frequency of 64 GHz, consuming 3.16 mW power when operating at a V_{DD} of 0.6V. The same technique was further excelled in the designing of a D-Band VCO operating at 118 GHz with a 7.8% tuning range consuming 5.6 mW [2]. The method is quite useful in the design of a low power mm-wave VCO with improvements in phase noise performance and tuning range. Although the technique is convenient, the possible drawbacks of this technique at high frequencies above 100 GHz hasn't been discussed in the references.

In this paper, we address the limitations and performance challenges in the design and implementation of the inductive divider VCO above 100 GHz. An in-depth analysis is performed to explore the feasibility of this technique to achieve high operational frequency. The paper is organized as follows. In Section II, conventional LC VCO and inductive divider VCO are briefly discussed. The impact of the Q factor, parallel resistive losses (R_p) at high frequencies are examined. In Section III the inductive divider cross-coupled pair is compared with its small signal equivalent model. The negative resistance enhancement parameters and the constraints limiting the performance are discussed in detail. This section also explains the practical implementation of the circuit design and the layout. Simulation results are shown in Section IV, and finally Section V concludes the paper.

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II. Design Consideration for High-Speed VCO

A. Fundamental LC cross-coupled pair topology

The fundamental LC tank cross-coupled VCO is shown in Fig. 1 (a). It consists of two parts, an LC tank, and negative G_M cross-coupled pair. The LC tank acts as a resonator and has losses associated with it. To compensate for the losses, a negative resistance is required. Cross-coupled transistors have an inherited property to generate negative resistance. However, the transistors are usually large and consume a lot of power to generate sufficiently large negative resistance. Designing a fundamental VCO in the high frequency, i.e., D-Band, is a challenge in terms of the performance and trade-off with the tuning range, phase noise, and power consumption need to be balanced against specifications.

B. Quality Factor of the LC tank

The quality factor of the LC tank in the VCO is highly degraded when operating at mm-wave and higher frequencies. The inherently low Q of the varactors degrades the tank Q, consequently affecting the phase noise performance as predicted by the Leeson phase noise model [3]. At high frequencies, the varactor governs the quality factor of the tank. The Q of the LC tank is given as

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{ind}} + \frac{1}{Q_{var}}, \tag{1}$$

where Q_{tank} is the quality factor of the tank, Q_{ind} is the quality factor of the inductor and Q_{var} is the quality factor of the varactor.

The varactor Q degradation over the frequency range is shown in Fig. 2 (a). In order not to use large varactors to avoid Q factor issues, one would inevitably compromise the tuning range achievable in the design. Due to the compromise between phase noise and the tuning range, an optimum balance is essential to achieve higher oscillation frequencies.

To target higher oscillation frequencies, the size of the inductor or varactor in the LC tank is reduced, consequently reducing the parallel resistive losses associated with the tank that is represented by R_p as illustrated in Fig. 2 (b). There is a requirement to have an equal or higher negative resistance R_{neg} to compensate for the losses produced by the tank. To satisfy the oscillation condition, the $|R_{neg}|$ should be equal or smaller than R_p. An example to estimate the parallel resistance (R_p) over the frequency range at different inductance (L) values with the varactor capacitance (C_{var}) kept constant at 24 fF is shown in Fig. 2 (b). The anticipated R_p is around 170-230 Ω. The oscillation frequency is calculated simply as

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_{var}}}. \tag{2}$$

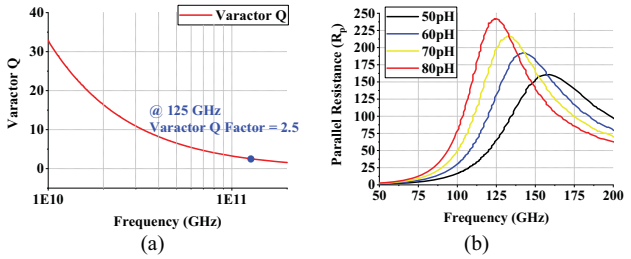

Fig. 2. (a) Quality factor of the varactor over the frequency (b) Parallel resistance R_p at different values of inductance L in the LC tank.

C. Fundamental LC tank inductive divider cross-coupled pair topology

The inductive divider topology is slightly different from the conventional cross-coupled pair topology, as shown in Fig. 1 (b). Since, the transistors in the G_M cross-coupled pair are responsible for producing the negative resistance, an addition of passive element in the cross-coupled pair, i.e., inductors L_3 and L_4 will assist in boosting the negative resistance provided by these transistors. Eventually, the size of the G_M transistors will reduce lowering the parasitic capacitance C_{par} of the G_M cross-coupled pair transistors. The power utilized by these transistors is reduced with improvement in the oscillation frequency f_{osc} of the VCO. In practical design, the oscillation frequency f_{osc} takes into account the total inductance L_T and varactor capacitance C_{var} of the LC tank, the parasitic capacitance C_{par} of the G_M cross-coupled pair transistors and the loaded buffer capacitance C_{buff} is given as:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_T(C_{var}+C_{par}+(2C_{buff}))}}. \tag{3}$$

III. Negative Resistance Enhancement Techniques, Modeling, Limitations and Implementation

The negative resistance R_{neg} provided by the conventional G_M cross-coupled pair, as shown in Fig. 1 (a), is approximately $-2/g_m$ where g_m is the transconductance of the individual transistor. Inherently, the gate and the drain impedances of the transistors M_1 and M_2, are mismatched. The introduction of the inductor in cross-coupled pair in Fig. 3 (a) assists in the conjugate matching of the drain and the gate impedances, thus improving the power efficiency [1]. Moreover, the technique helps in enhancing the negative resistance generated by the cross-coupled pair, which can be shown from the differential small-signal equivalent model of the inductor in the cross-coupled pair stage as in Fig. 3 (b). The estimated real part of the input impedance looking into the cross-coupled pair is given as

$$Z_{in(real)} \approx \frac{-2}{g_m} + \frac{2\omega^2 L_g C_{gs}}{g_m}, \tag{4}$$

where g_m is the transconductance of the transistor, C_{gs} is the gate-to-source capacitance, L_g is the inductor in the cross-coupled pair and ω is the required oscillation frequency.

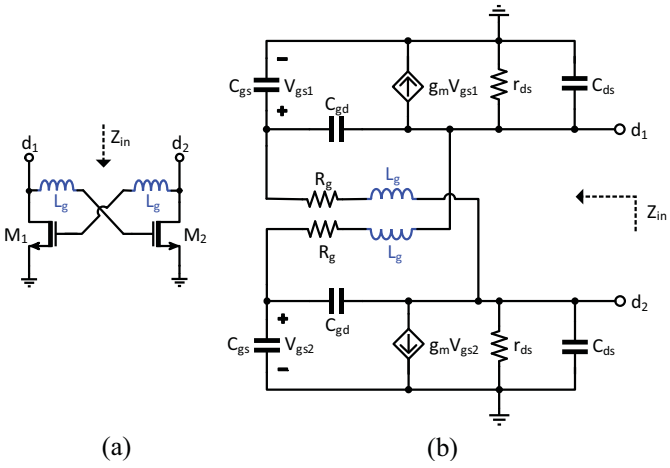

Fig. 3. (a) Transistor Model (b) Small signal equivalent model.

The real part of the impedance of the conventional cross-coupled pair is modified with this technique. The real impedance has a second term, which is a function of the inductor L_g, frequency ω and the gate-to-source capacitance C_{gs}. The parasitic capacitances of the transistors are assumed to be fixed. Theoretically, the parameters that can assist in the improvement of the negative resistance R_{neg} are an increase of inductance value L_g and operational frequency ω. An increase of 18% is expected in the negative resistance theoretically at 130 GHz with an L_g value of 15 pH in Eq. (4).

A. Constraints and Limitations

The behavior of the negative resistance can be extracted from the simplified small-signal equivalent model presented in Fig. 3 (b). Extracted parameters are compared with the process design kit (PDK) transistor model. The comparison of the behavior of the negative resistance R_{neg} over the frequency is shown in Fig. 4 at a fixed L_g value of 15 pH. Both models are in agreement with each other. At low frequencies, the negative resistance is approximately equal to $-2/g_m$. At high frequencies, there is a transition in the negative resistance R_{neg}, and it flips from the negative to positive. This transition is defined as the "maximum attainable oscillation frequency" for the cross-coupled negative resistance cell originally proposed by [4]. This behavior is primarily due to gate resistance r_g. The impedances offered by gate-to-source capacitance C_{gs} becomes comparable to the gate resistance r_g at high frequencies, and a large portion of the voltage at gate appears across r_g rather than C_{gs} leading to inversion. It is worth noting that as the transition frequency approaches, $|R_{neg}|$ drops rapidly, thus making the value of $|R_{neg}|$ even larger than R_p. Therefore, stable oscillation condition cannot be satisfied by limiting the performance at high frequencies. The transition frequency ω_{trans} [5] for the conventional cross-coupled negative resistance cell is a function of r_g and C_{gs} and is given as

$$\omega_{trans} \approx \sqrt{\frac{gm}{2\pi(C_{gs}+C_{gd})r_g C_{gs}}}, \qquad (5)$$

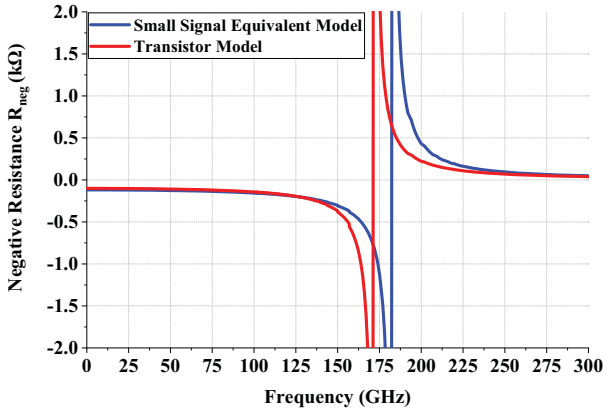

Fig. 4. Negative resistance R_{neg} variation vs. frequency (Transistor Model vs. Small signal equivalent model).

The inductor L_g in cross-coupled pair, as expressed in Eq. (4), has the ability to improve the negative resistance but suffers at high frequencies. This behavior is simulated in the small signal equivalent model by observing the negative resistance over the variation of the inductance L_g at different frequencies from 60 to 140 GHz and is depicted in Fig. 5. There is an improvement in the negative resistance R_{neg}. The decrease in value of negative resistance R_{neg} in the beginning of the curve at each frequency iteration indicates the transition frequency approaching quickly. The variation in the improvement of negative resistance is significantly reduced at a higher frequency, and the negative resistance curve is almost flattened at 140 GHz inductance value of 25 pH. Beyond 25 pH no improvement can be seen. The flattening of the curve at high frequencies demonstrates the limitation of this technique to enhance the negative resistance. To further investigate this, behavior in frequency domain at different inductance L_g values is shown in Fig. 6. It can be seen that the increase in inductance value from 5 to 30 pH shifts the transition frequency from 190 GHz to 160 GHz, indicating that L_g is a direct function of the transition frequency ω_{trans} along with r_g and C_{gs} expressed in Eq. (5). Therefore, higher the value of L_g earlier the transition frequency occurs thus limiting the maximum oscillation frequency. Hence, this justifies the curve flattening behavior at 140 GHz in Fig. 5 with no major improvement in the negative resistance. Layout optimization techniques can be utilized to minimize the dependence of the transition frequency ω_{trans} on r_g and C_{gs}. The appropriate frequency to practice this technique is to make use of the improvement in negative resistance before the curve flattening occurs. For instance in Fig. 5, at 140 GHz the inductance values below 25 pH can be utilized. It is to be noted that there is a slight parasitic capacitance contribution by the inductor L_g itself which is lower compared the R_{neg} it generates [2].

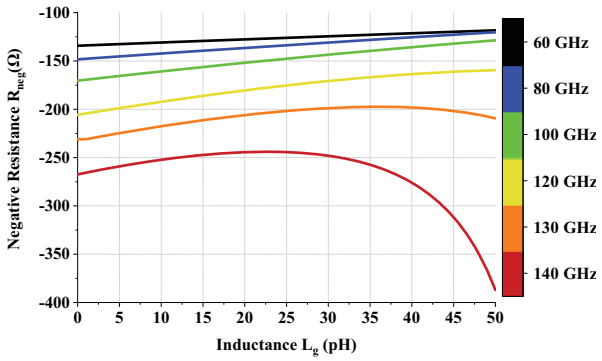

Fig. 5. Negative resistance R_{neg} variation vs. inductance L_g modeled at different frequencies using the small signal equivalent model.

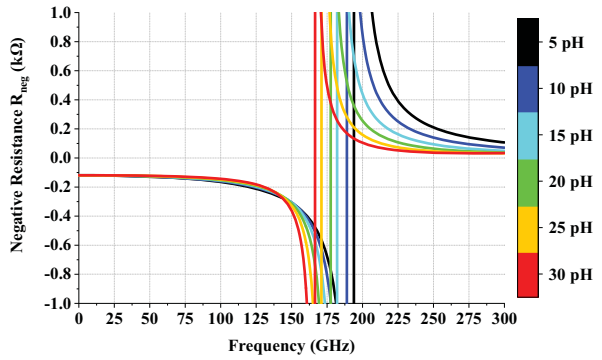

Fig. 6. Negative resistance R_{neg} variation vs. frequency modeled at different inductance L_g values using the small signal equivalent model.

B. Practical implementation aspects

The practical implementation of the inductive divider cross-coupled pair suffers from the performance trade-offs at higher frequencies, as discussed in the previous section. The transistors from the PDK were utilized. An ideal inductor in the cross-coupled pair was used to analyze the behavior. The

performance variation of the negative resistance R_{neg} and parasitic capacitance C_{par} versus the variation of inductor L_g from 1 to 30 pH is investigated in Fig. 7 at different frequencies from 65 to 150 GHz. The negative resistance R_{neg} curve changes its behavior with the increase in frequency. As the frequency increases, the variation in the increase in negative resistance tends to decline as shown in Fig. 7 (a-d) curve flattens at 150 GHz. After 130 GHz, there is hardly any improvement, and a severe decline is observed in the negative resistance. This uncertain behavior with the increase in frequency represents the limitation discussed earlier.

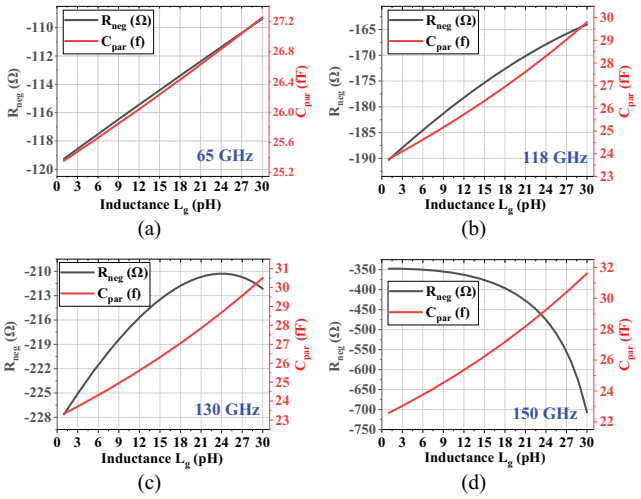

Fig. 7. Negative Resistance (R_{neg}) and parasitic capacitance (C_{par}) versus inductance L_g

C. Layout Implementation

The layout of the oscillator core is realized in a 22nm FDSOI process. The inductor L_g is implemented by the transmission line which is connected to the gate and drain of the transistors in the cross-coupled pair. The negative resistance is extracted by varying the transmission line length, as shown in Fig. 8 which varies the inductance consequently. The variation of the negative resistance is quite low. The inductor in the LC tank is a single turn differential inductor and is utilizing the ultra-thick metal layer. The Q of the inductor is a function of frequency, and high Q is expected from the inductor at high frequencies. The inductor self-resonance frequency and losses were taken into consideration in the design process. Varactor at high frequencies suffers from a low Q. The varactor was selected to have a decent capacitance tuning range and a reasonable quality factor. The varactor is placed in between the two terminals of the inductor. The layout arrangement is shown in Fig. 9. The nominal supply voltage is 0.8V.

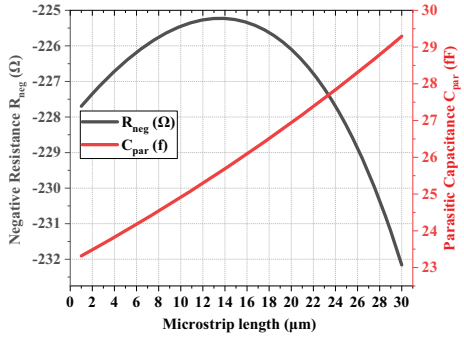

Fig. 8. At 130 GHz (R_{neg} and C_{par} versus Transmission line length (µm))

The simulated oscillator core consumes a DC power of 17.1 mW. It oscillates at a center frequency of 129 GHz with a phase noise of -100.6 dBc/Hz. The tuning range of the oscillator core is observed to be 5.4%, with the tuning voltage range from 0 to 0.8V. The output signal has a voltage swing of 640 mV_{p-p} to 1.6 kΩ load. It is worth noting that output buffers are not included in the circuitry. The buffer circuitry will further reduce the tuning range and the oscillation frequency due to the contribution of the loaded capacitance.

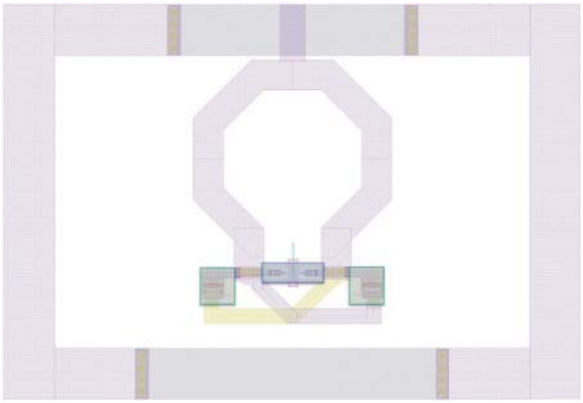

Fig. 9. Inductive divider LC VCO core layout.

IV. Simulation Results

Table I presents a performance summary of the simulated design of the VCO with and without the inductor L_g in the cross-coupled pair. In comparison the inductive divider has a degradation of 4 GHz in the oscillation frequency and 1% decrease in tuning range as compared to the cross-coupled VCO. The degradation reflects the limitations associated with this implementation. However, the inductive divider technique showed considerable improvement of 1.5 dBc/Hz in phase noise and a 4.3 mW improvement in DC power consumption. In Table I, results are also compared to the state-of-the-art oscillator designs at 64 GHz and 118 GHz utilizing a similar inductive divider concept. The VCOs designed with this technique are power efficient with an improvement in phase noise performance.

TABLE I. Performance Summary and Comparisons with the State of the Art

Reference	**[1]**	**[2]**		**This work***	
	90nm	***65nm***		***22nm***	
Topology	Ind. divider LC type	Ind. divider LC type	Ind. divider LC type	Fund. LC	Ind. divider LC type
f_{osc} (GHz)	64	118.3	122.5	133	129
V_{DD}	0.6	1	0.8	0.8	0.8
P_{DC} (mW)	3.16	5.6	2	21.4	17.1
FTR (%)	8.75	4.4	7.8	6.54	5.4
Phase Noise (dBc/Hz)	-95	-83.9	-83	-99.1	-100.6
Phase Noise Offset (MHz)	1	1	1	10	10
Description	Core + Buffer	Core + Buffer	Core + Buffer	Core	Core
FOM_T	-185	-175.7	-174.6	-176.2	-176.53

*Without buffer

V. Conclusion

Here, we presented the limitations and bottlenecks in the design of a D-Band inductive divider LC VCO. The technique is useful in the design of low power VCOs utilizing power matching technique by applying the inductor in the cross-coupled pair. The performance of this technique is compromised at the D-Band frequencies and beyond. The aid in the transition frequency by the addition of the inductor in the G_M cross-coupled pair stage limits the performance of the VCO at these frequencies. The variation in the improvement of the negative resistance decreases as the operational frequency approaches the transition frequency. The prototype VCO core utilizing the technique was designed using a 22nm FDSOI process. The VCO was able to achieve a decent output power and a low power consumption of 17mW with a slight improvement in phase noise. The analyzed technique illustrated is a good choice in the design of low power VCO while taking into consideration the performance constraints involved.

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