# ANALOG PROJECT FOR SEMESTER III - M.TECH

**TITLE : LDO LAYOUT FOR LDO WITH GM/ID METHODOLOGY**

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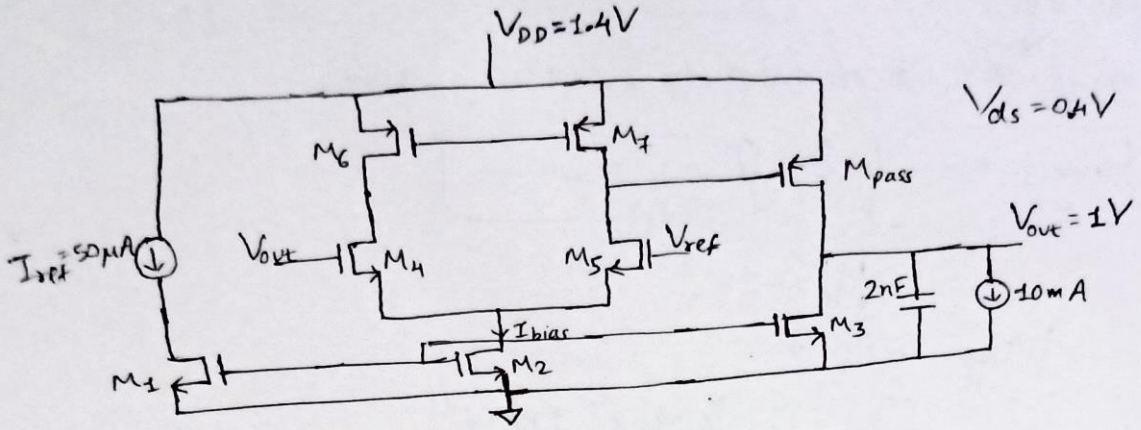
# Theory Calculation for gm/Id Methodology for LDO with Differential Operational Amplifier:

## (#) LDO Layout By $G_m/I_D$ Methodology:




$V_{ds} = 0.4$ & $g_m/I_D = 10 = \frac{2}{V_{ov}}$ ; $V_{ov} \simeq 200mV$

### (##) Sizing of PASSFET:-

(★) S1 $V_{ds} = 0.4V$ & $g_m/I_D = 10$ & 45nm ⟹ For PMOS 1V & gpdk45nm Techplot

$L_{pass} = 45nm$

↳ From Techplot of pmos 1V gpdk045nm. & Using Above values of $V_{ds}$ & $g_m/I_D$

$$\frac{I_D}{W} = 42.1879$$

$$W_{passfet} = \frac{I_{load}}{I_D/W}$$

$$= \frac{10.05mA}{42.1879}$$

$$\rightarrow \boxed{W_{passfet} = 238.22\mu m}$$

→ Also,

$A_{pass} = g_m r_o|_{passfet}$

↓ Through Techplot

$$\boxed{g_m r_o|_{pass} = 19.1957}$$

### (★##) Sizing of Diffamp MOSFET; $M_4$ & $M_5$: NMOS & $M_6$ & $M_7$: PMOS

→ $A_{pass} \cdot A_{diff}$ = DC PSRR

$$A_{diff} = \frac{DC\ PSRR}{A_{pass}}$$

- Let DC PSRR = 45dB because above 45dB PSRR the Techplot values were not available for gpdk045nm. pmos 1V & nmos 1V.

$$A_{diff} = \frac{10^{45/20}}{g_m r_o|_{pass}}$$

$20\log_{10}|Gain| = DC\ PSRR$

$\therefore |Gain| = |A_{diff}| = 10^{\frac{45}{20}} = 10^{2.25}$

$$A_{diff} = \frac{177.828}{19.1957} = \frac{g_m r_o}{2}$$

$$\boxed{A_{diff} = g_m r_o|_{diff} = 18.528}$$

→ $g_m r_o = 18.528$ & $\frac{g_m}{I_D} = 10$

⇓

Through Techplot of NMOS IV & PMOS IV gpdk045nm.

$L_{NMOS}$ (M4 & M5) = 45nm & $L_{PMOS}$ (M6, M7) = 270nm

⇓

Using Techplot

$\left.\frac{I_D}{W}\right|_{\substack{270nm \\ PMOS}} = 16.9973$ : PMOS

$\left.\frac{I_D}{W}\right|_{\substack{45nm \\ NMOS}} = 50.8585$ : NMOS

→ Taking $I_{Bias} = 50\mu A \Longrightarrow \frac{I_{Bias}}{2} = 25\mu A$

$W = \frac{\frac{I_{Bias}}{2}}{I_D/W}$

$W_{NMOS}$ (M4, M5) = 0.492μm ; $W_{PMOS}$ (M6, M7) = 1.471μm → 2.88μm lower limit in virtuoso

$\left(\frac{W}{L}\right)_{NMOS} = \left(\frac{W}{L}\right)_{PMOS}$.

⇓

We get $L_{PMOS}$ (M6, M7) = 263nm ≃ 270nm (Ok).

## (#) Sizing $M_1, M_2, M_3$ Tail, Bias NMOS :-

- $r_o \to \infty$ so $r_o = \frac{1}{\lambda I_D}$ & $I_D$ = constant so $\lambda \propto \frac{1}{L}$

Hence, $r_o \uparrow = \frac{1}{\lambda I_D} \propto L \uparrow$

for $r_o \to \infty$ will take $L_{max} = 720nm$

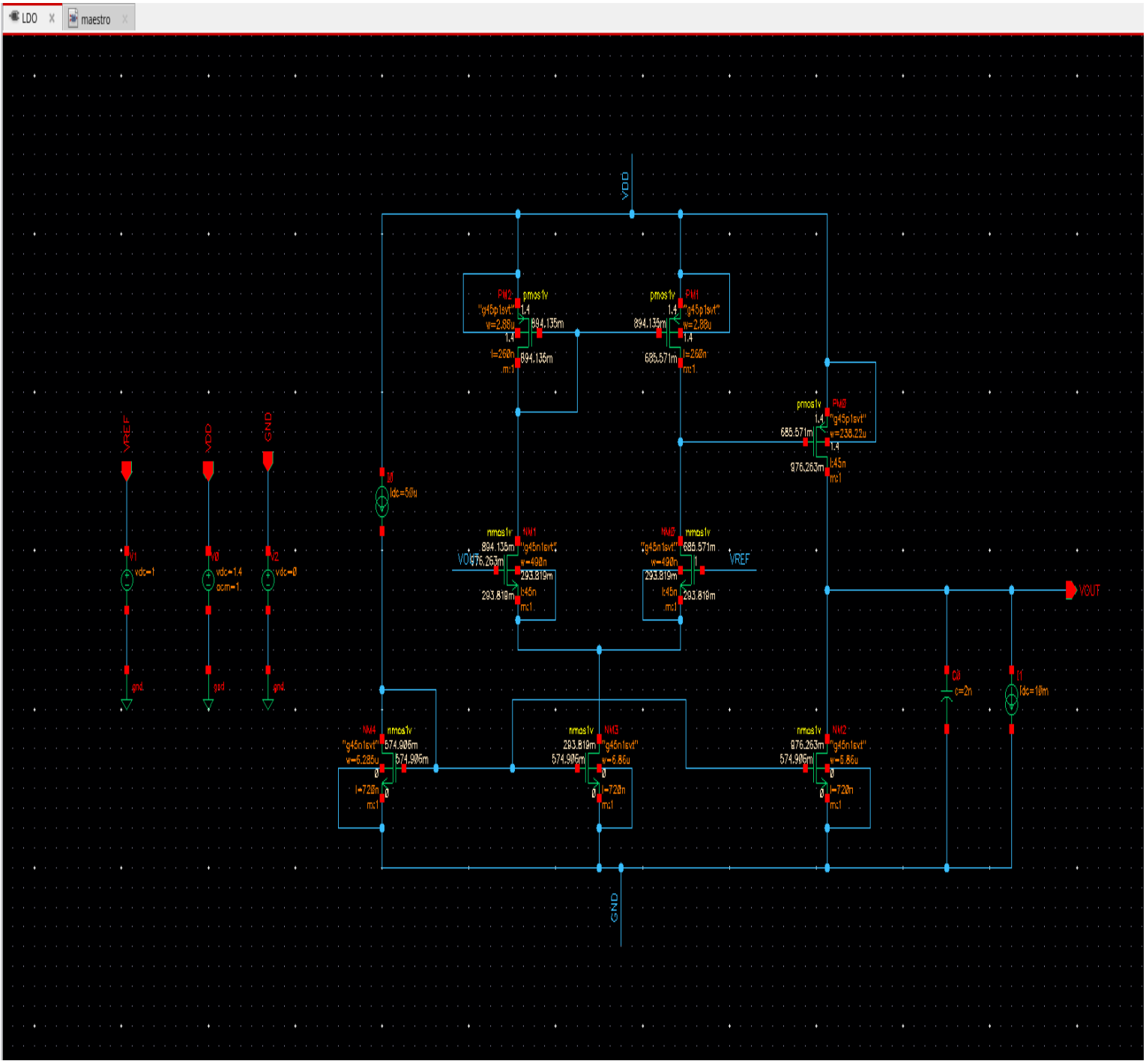
→ Here, $\frac{g_m}{I_D} \simeq 10$ & $I_1, I_2, I_3 = 50\mu A$

→ Techplot $\left.\frac{I_D}{W}\right|_{\substack{NMOS \\ L_{max} = 720nm}} = 7.2868$

$W_{NMOS}$ (M1, M2, M3) $= \frac{I_{Bias}}{I_D/W}$

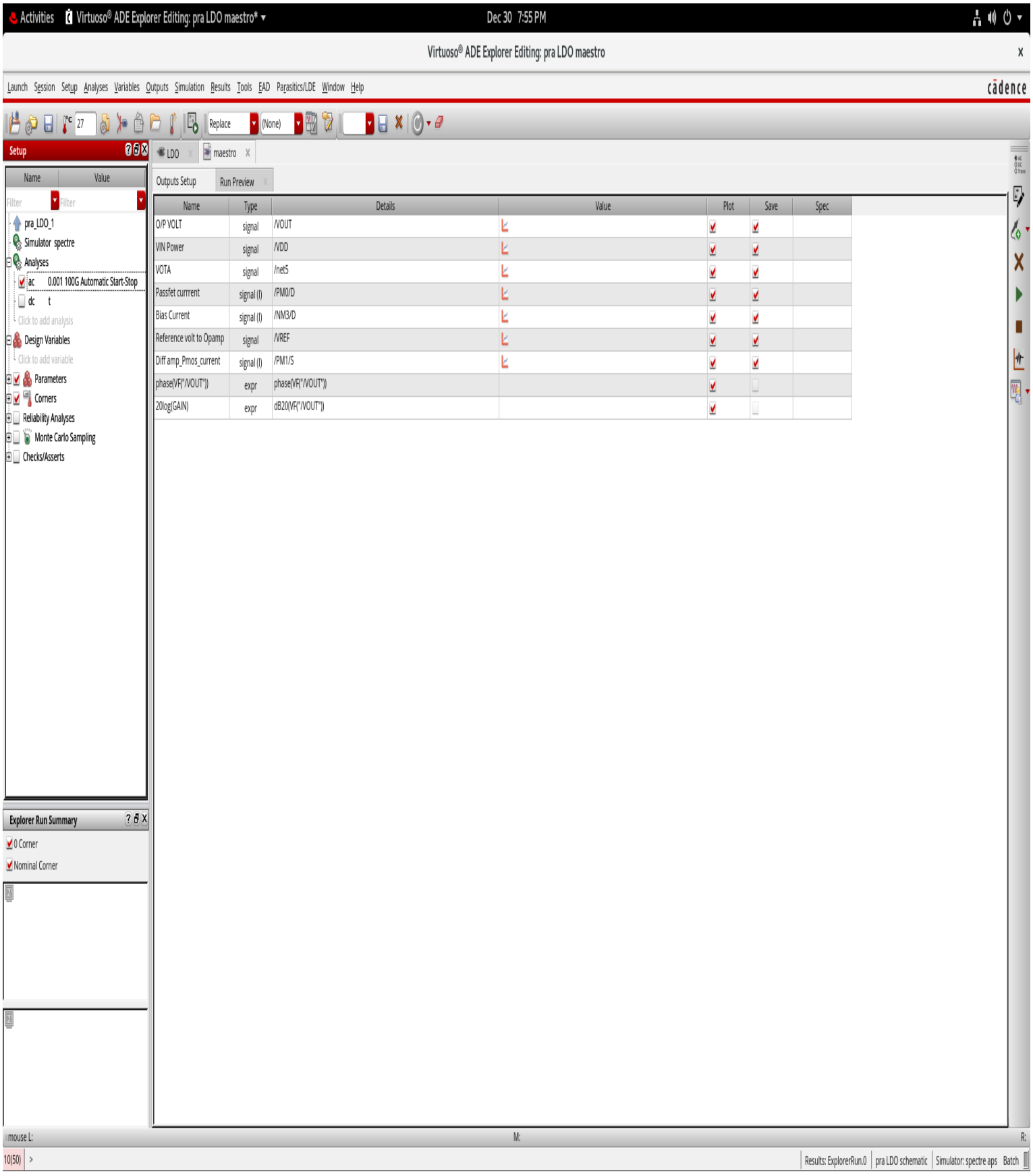
$W_{NMOS}$ (M1, M2, M3) = 6.862μm

# Virtuoso Schematic and DC Operating Point:



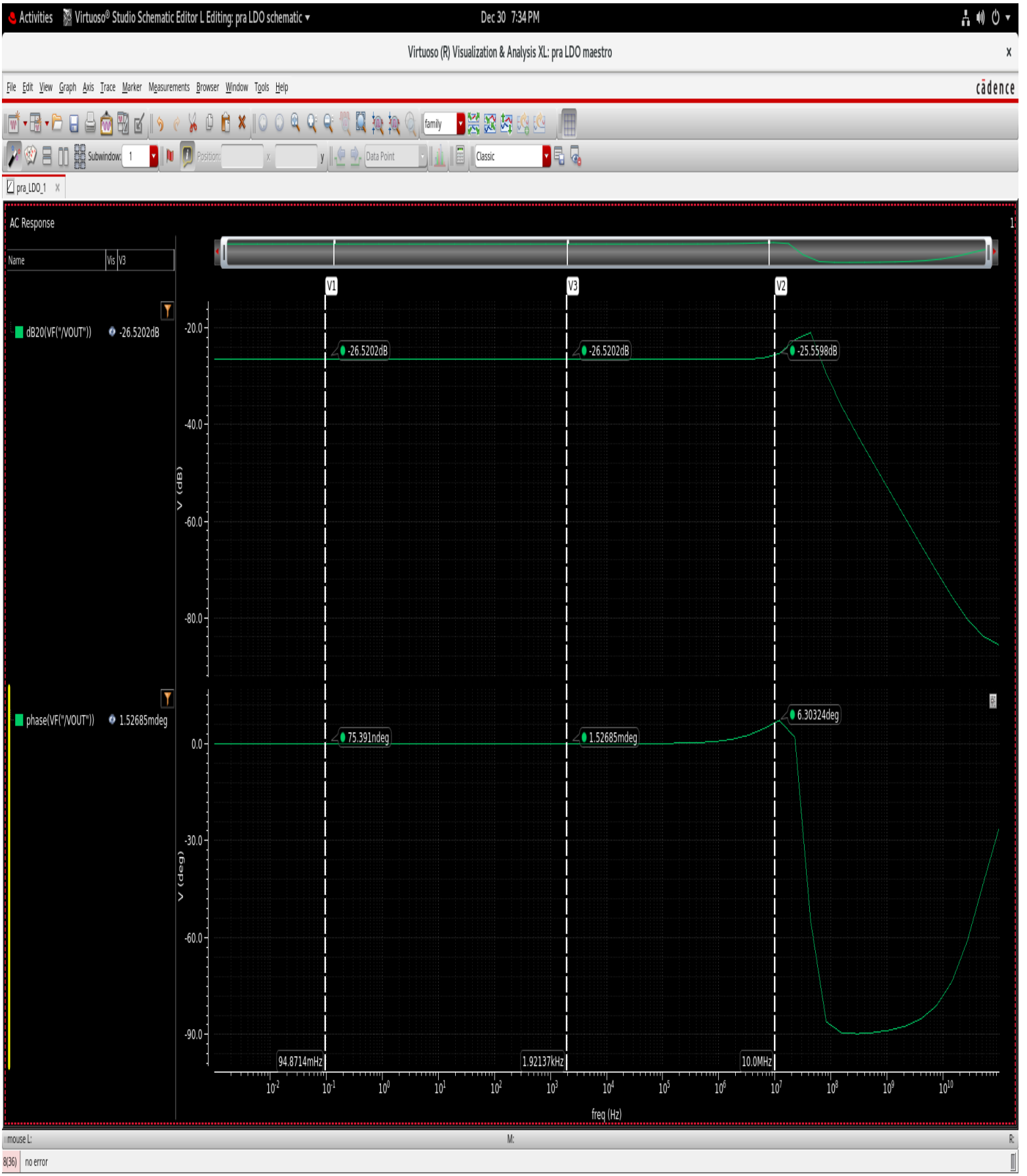

- Through DC Operating point analysis each MOSFET were verified for operating in Saturation that is operating region 2 were checked VOUT=0.976 V, VREF =1 V and VDD=1.4V

# Following Signals were plotted using ADE Explorer maestro:

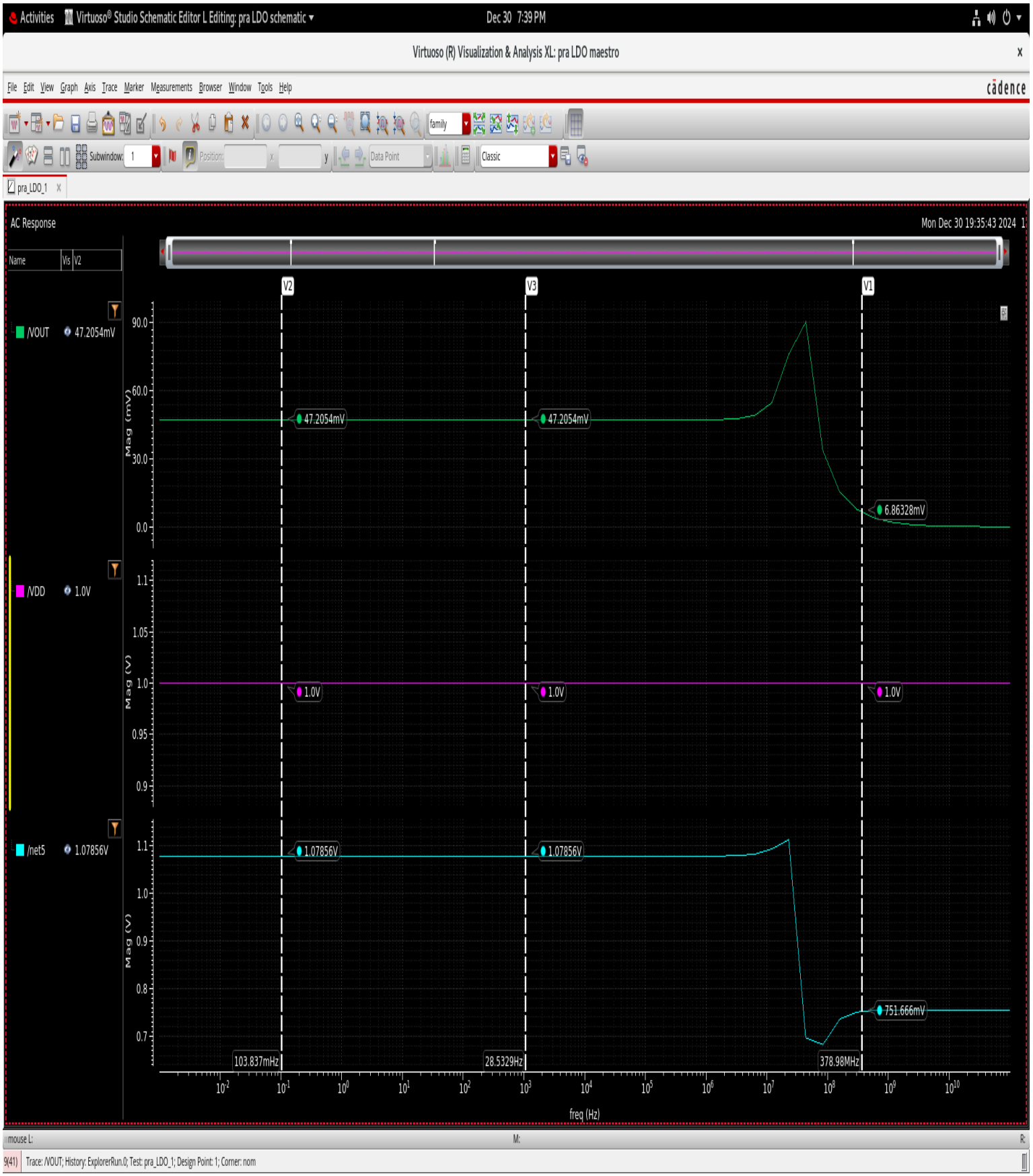


# DC Point operating of Output Volt, VDD, VOTA and VREF:

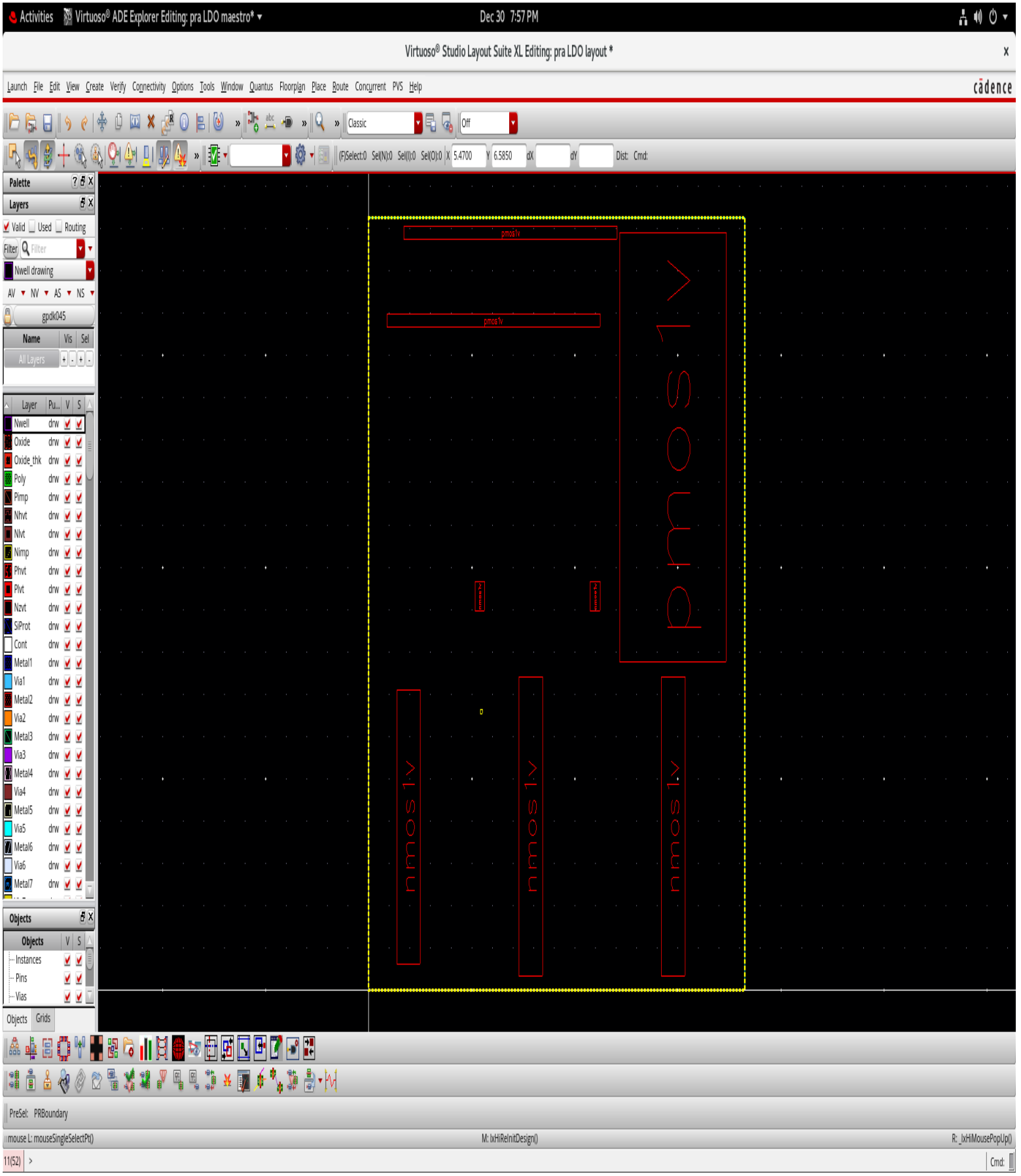
# Plots of PSRR and Phase waveform:



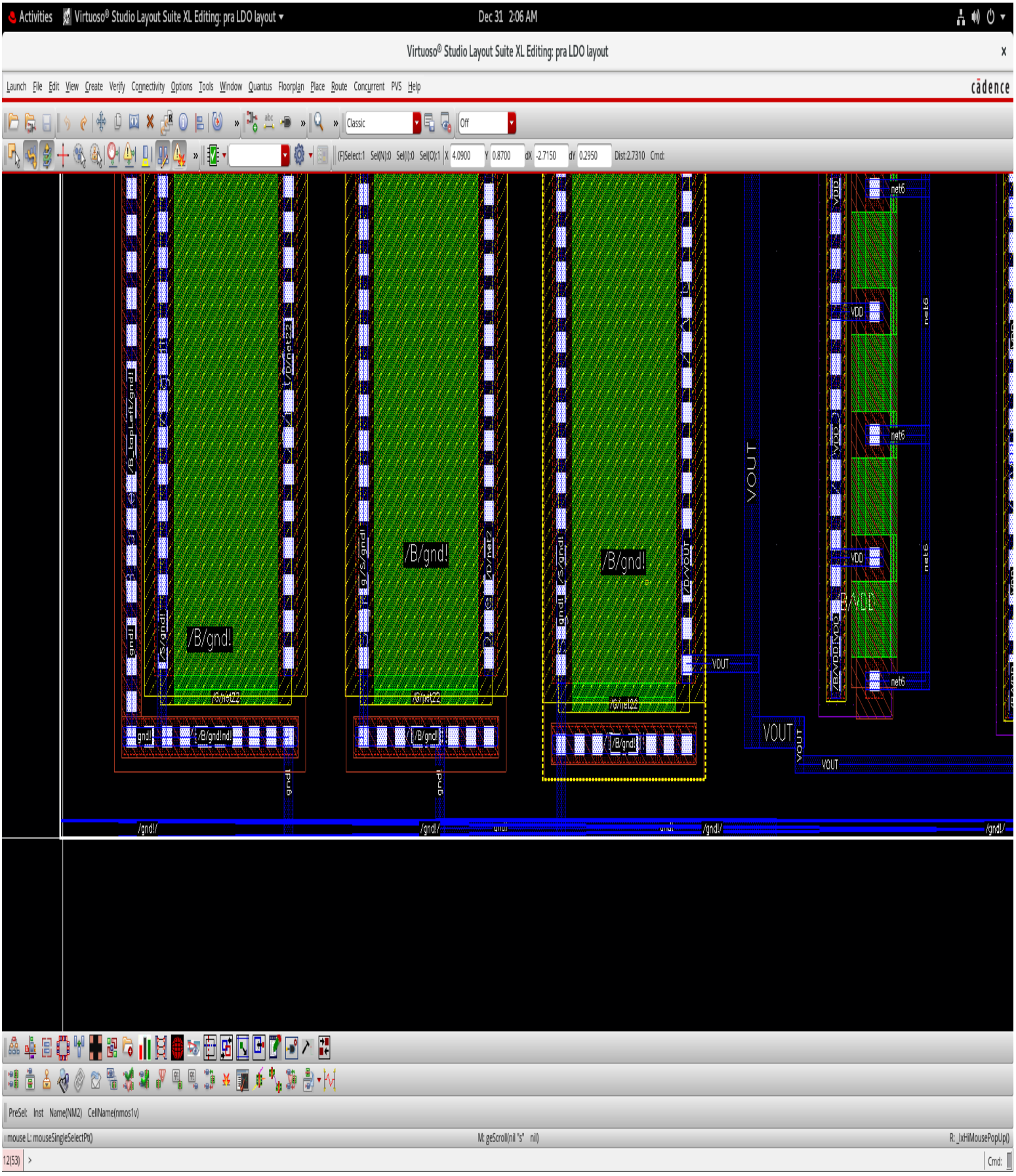
# AC Response plots of VOUT,VDD, VOTA for AC Magnitude = 1V in VDD :



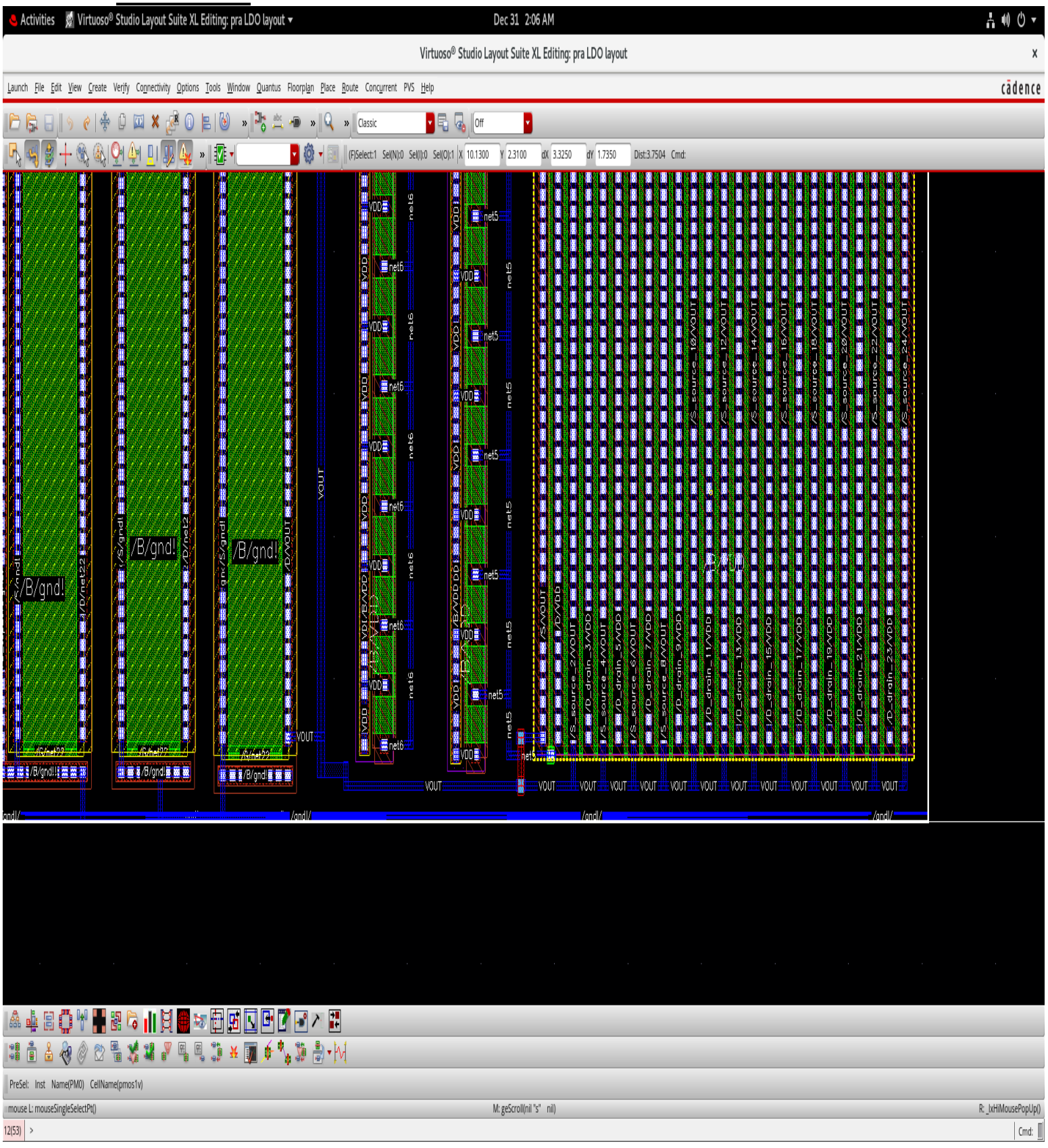
# Layout View of gpdk 45nm for all Components of LDO:



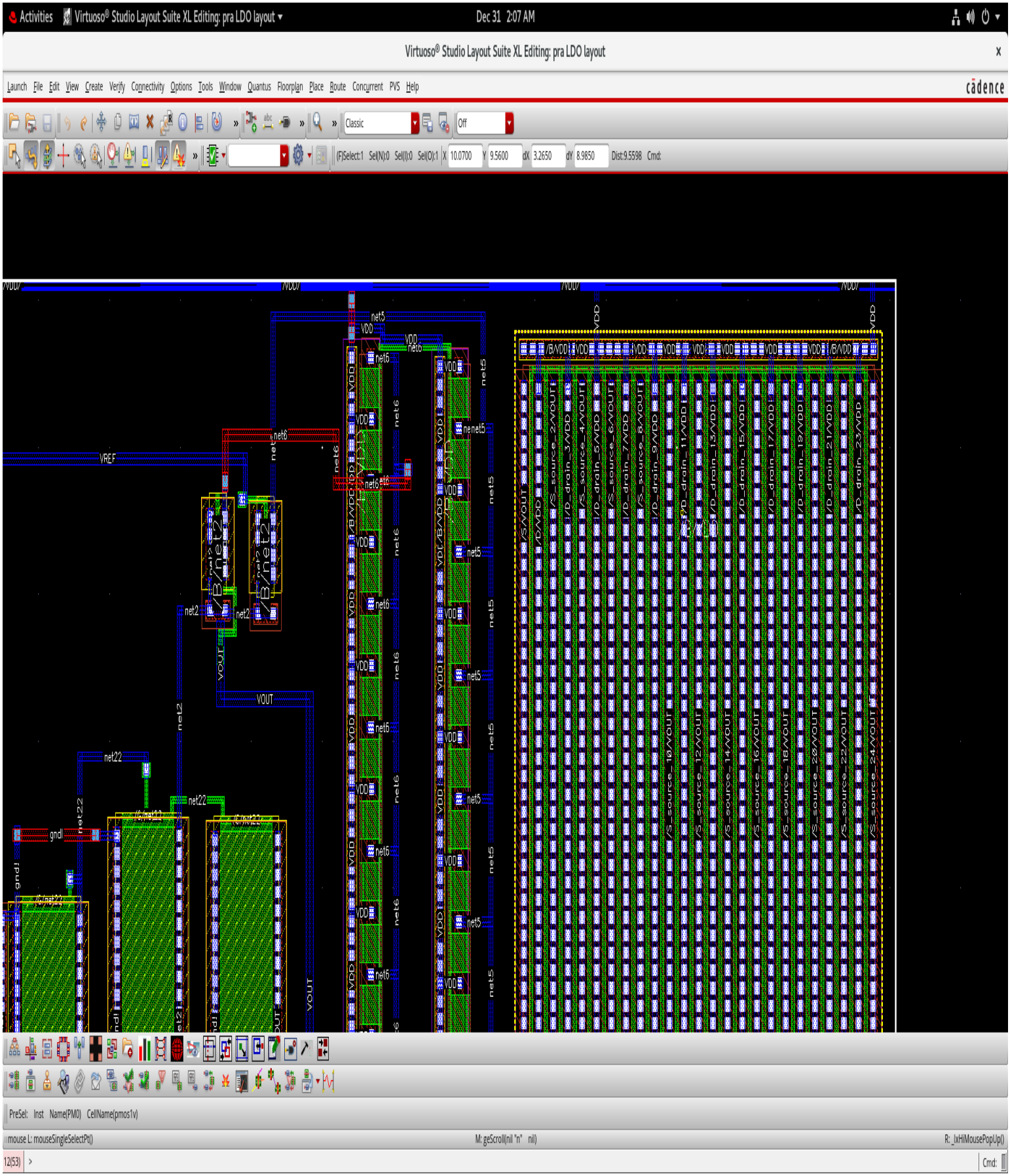
# Zoomed Layout of Bias Current NMOS with L=720 nm



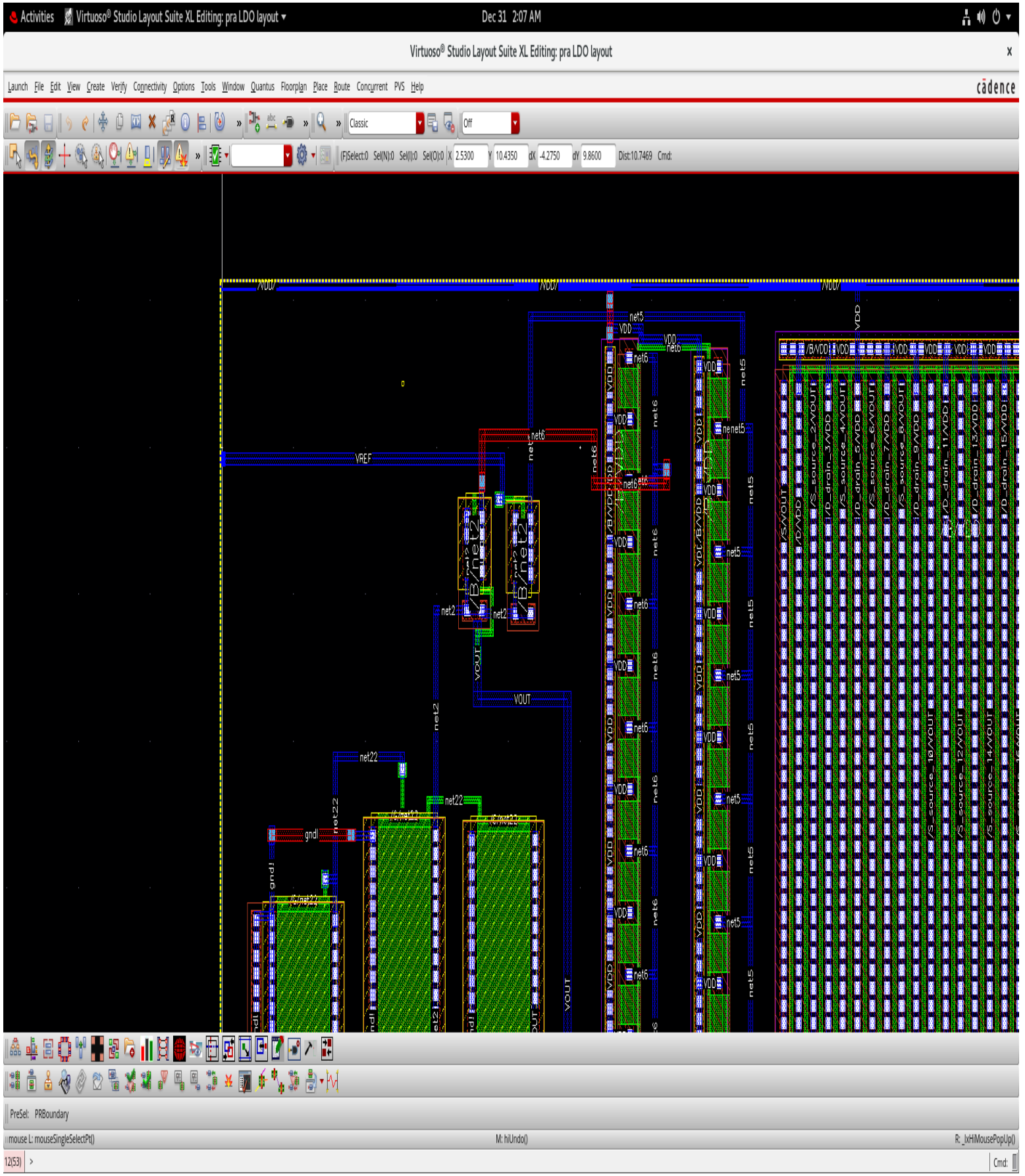
# Zoomed View of Routing of Bias NMOS, Diff AMP PMOS & PASSFET:



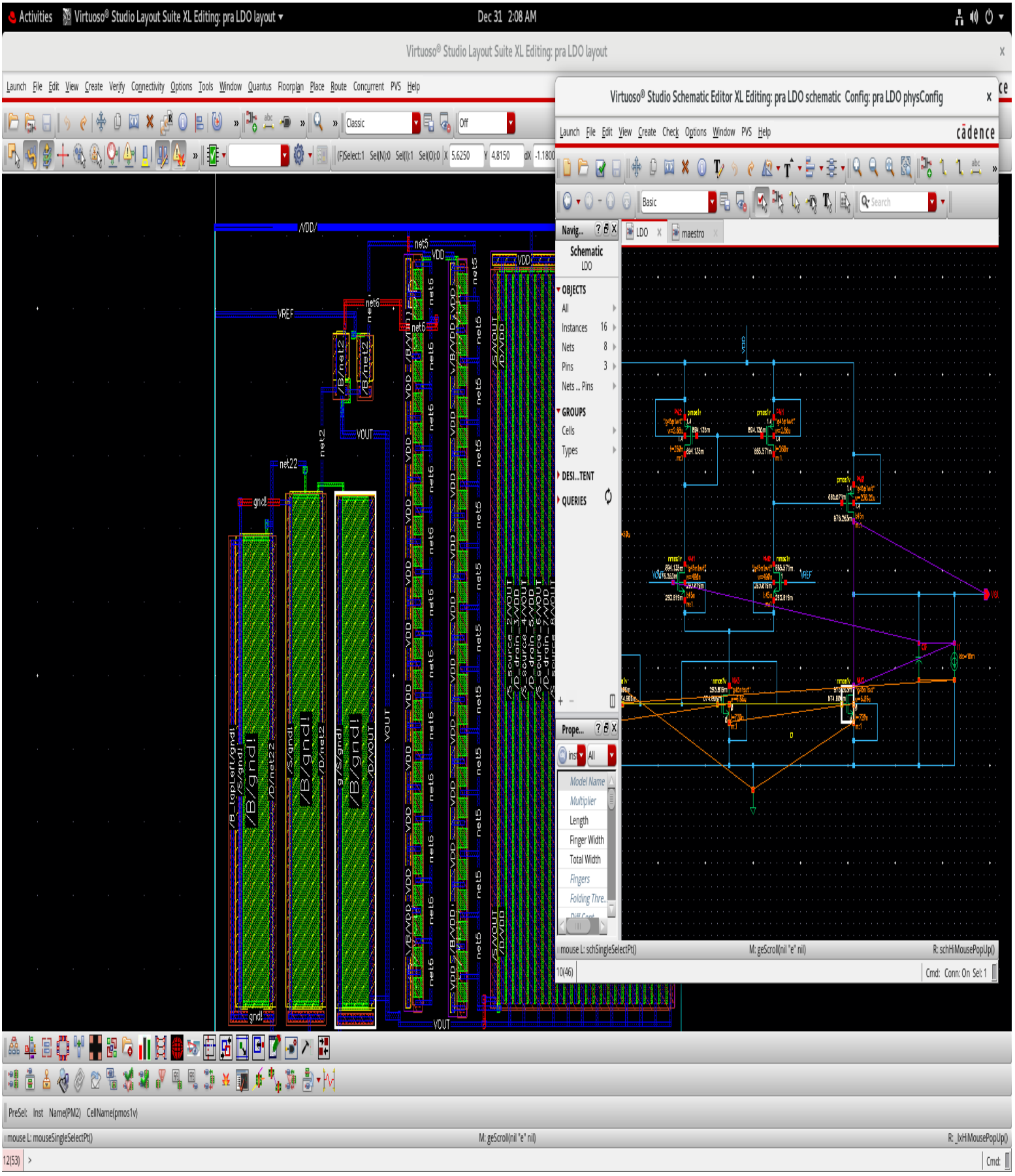
# Zoomed View of PassFet & DiffAMP PMOS L=270 nm



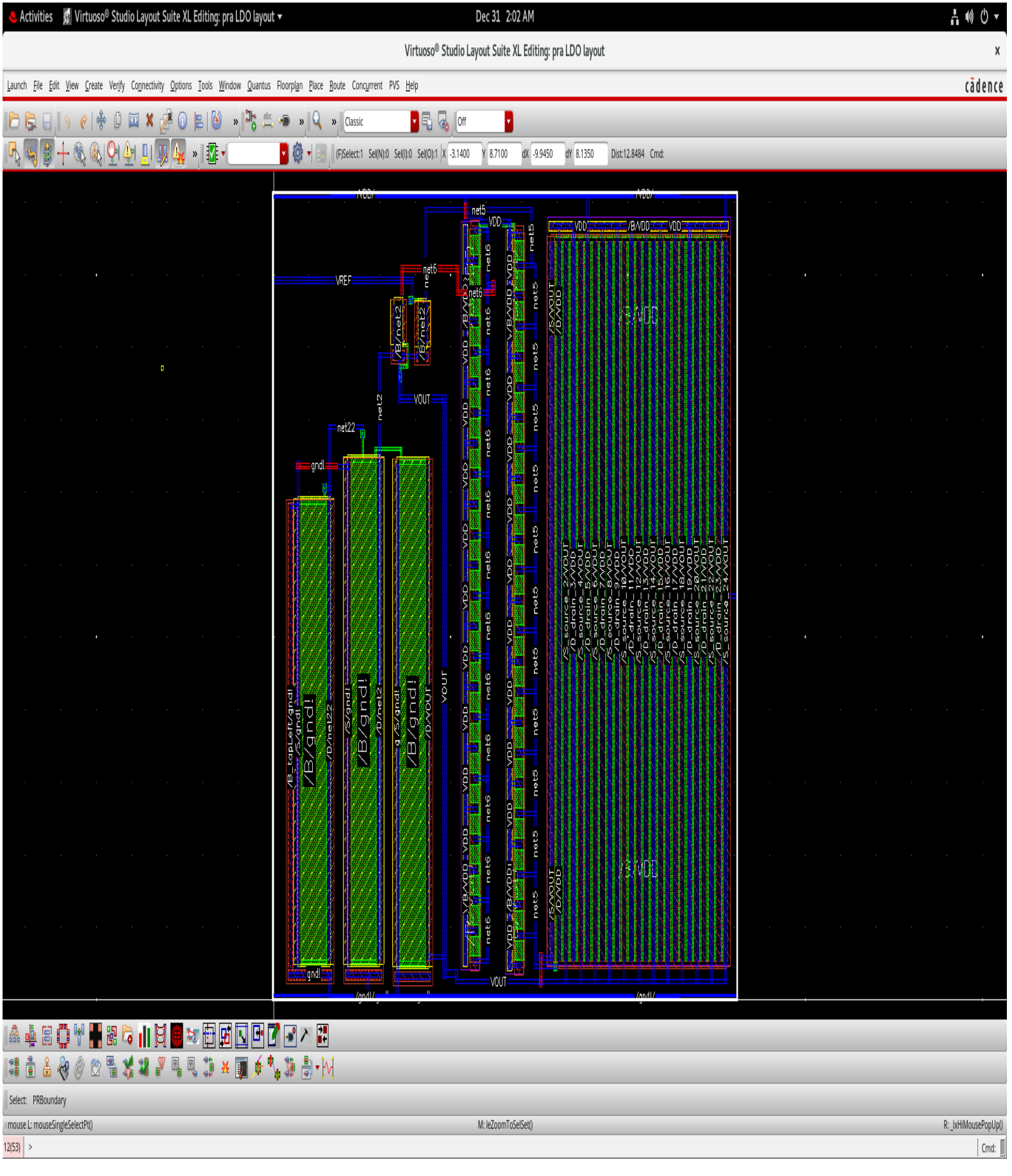
# Zoomed View of Connection DIffamp NMOS with L=45 nm



# # Mapping Schematic and Layout for Bias NMOS of L= 720 nm



# Detailed Layout Routing of all Component of Complete LDO:



# # Points to be Address:

- For NMOS 1V and PMOS 1V gpdk 45nm Technology through Techplots there is limitation of High PSRR values generation in calculation Step 2 of NMOS and PMOS sizing of DIFFAMP
- DRC, LVS Virtuoso window is not taking gpdk045 files, when we try to enter any file in DRC, LVS the particular window will close itself automatically. So, need to resolve by cadence team