

ANALOG PROJECT FOR **SEMESTER III - M.TECH**

TITLE : LDO LAYOUT FOR LDO WITH
GM/ID METHODOLOGY

Under : Prof. Sakshi Arora

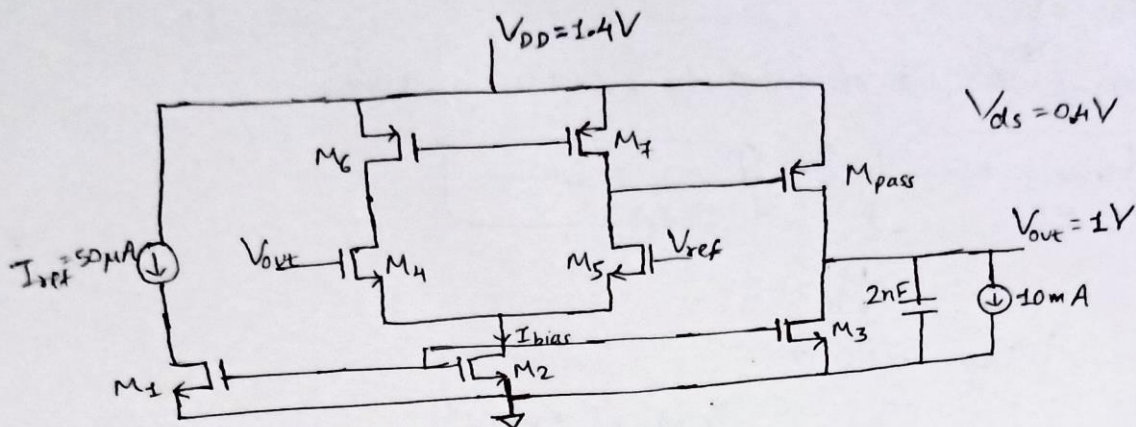
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MTECH EC Final Year - Semester III
(Term I 2025-26)

Differential Operational Amplifier:

⑧ LDO Layout By G_m/I_o Methodology:



$$\boxed{V_{ds} = 0.4} \quad \& \quad \boxed{g_m/I_D = 10 = \frac{2}{V_{ov}}} \quad ; \quad \underline{V_{ov} \approx 200mV}$$

④ Sizing of PASSFET:-

★ **S1** $V_{ds} = 0.4V$ & $g_m/I_D = 10$ & $45nm \Rightarrow$ For PMOS IV & gain $45nm$ technology.

→ From Techplot of pmos 1V $g_{m0} = 45 \text{ nm}$, & Using Above values, of V_{ds} & g_{m0}/I_D

$$\frac{I_0}{W} = 42.1879$$

$$W_{passfet} = \frac{I_{load}}{I_{D/W}}$$

$$= \frac{10.05 \text{ mA}}{42.1879}$$

→ $W_{\text{passfet}} = 238.22 \mu\text{m}$

→ Also,

$$A_{\text{pass}} = g_m r_o |_{\text{passfet}}$$

↓
Through Techplot

$\gamma_{m \gamma_0} = 19.1957$

⊛ Sizing of Diffamp MOSFET; M_4 & M_5 : NMOS
 &
 M_6 & M_7 : PMOS

$$\rightarrow A_{\text{pass}} \cdot A_{\text{diff}} = \text{DC PSRR}$$

$$A_{diff} = \frac{DC, PSRR}{A_{pass}}$$

• Let DC PSRR = 45dB because above 45dB PSRR the Techplot values were not available for $g_{pd} < 0.45 \text{ nm}$. $p_{mos} \pm 1V$ & $n_{mos} \pm 1V$.

$$A_{diff} = \frac{10^{4.5/20}}{g_{n\%pass}}$$

$$A_{diff} = \frac{177.828}{19.1957} = \frac{9.260}{2}$$

$$A_{\text{diff}} = g m^{\gamma_0} |_{\text{diff}} = 18.528$$

$$20 \log |G_{10}| = \text{DC PSRR}$$

$$\therefore |Gain| = |A/\beta| = 10^{\frac{45}{20}} = 10^{2.25}$$

$$\rightarrow \boxed{g_m r_o = 18.528} \quad \& \quad \boxed{\frac{g_m}{I_D} = 10}$$

Through Techplot of NMOS 1V & PMOS 1V gpdk045nm.

$$\boxed{L_{NMOS} = 45nm} \quad \& \quad \boxed{L_{PMOS} = 270nm}$$

M_4, M_5 M_6, M_7

Using Techplot

$$\left. \frac{I_D}{W} \right|_{270nm \text{ PMOS}} = 16.9973 : \text{PMOS}$$

$$\left. \frac{I_D}{W} \right|_{45nm \text{ NMOS}} = 50.8585 : \text{NMOS}$$

$$\rightarrow \text{Taking } I_{Bias} = 50\mu A \Rightarrow \frac{I_{Bias}}{2} = 25\mu A$$

$$W_{diff} = \frac{I_{Bias}}{I_D/W}$$

$$\boxed{W_{NMOS} = 0.492\mu m}$$

M_4, M_5

$$\boxed{W_{PMOS} = 1.471\mu m}$$

M_6, M_7

2.88μm lower limit in virtuoso

$$\left(\frac{W}{L} \right)_{NMOS} = \left(\frac{W}{L} \right)_{PMOS}$$

$$\text{We get } L_{PMOS} = 263nm \approx 270nm \text{ (OK).}$$

⊗ Sizing M_1, M_2, M_3 Tail, Bias NMOS :-

$$\bullet \quad r_o \rightarrow \text{inf} \quad \text{so} \quad r_o = \frac{1}{\lambda I_D} \quad \& \quad I_D = \text{constant}$$

$$\lambda \propto \frac{1}{L}$$

$$\text{Hence, } r_o = \frac{1}{\lambda I_D} \propto L \uparrow$$

$$\text{for } r_o \rightarrow \text{inf} \text{ will take } \boxed{L_{max} = 720nm}$$

$$\rightarrow \text{Here, } \frac{g_m}{I_D} \approx 10 \quad \& \quad I_1, I_2, I_3 = 50\mu A$$

$$W_{NMOS} = \frac{I_{Bias}}{I_D/W}$$

M_1, M_2, M_3

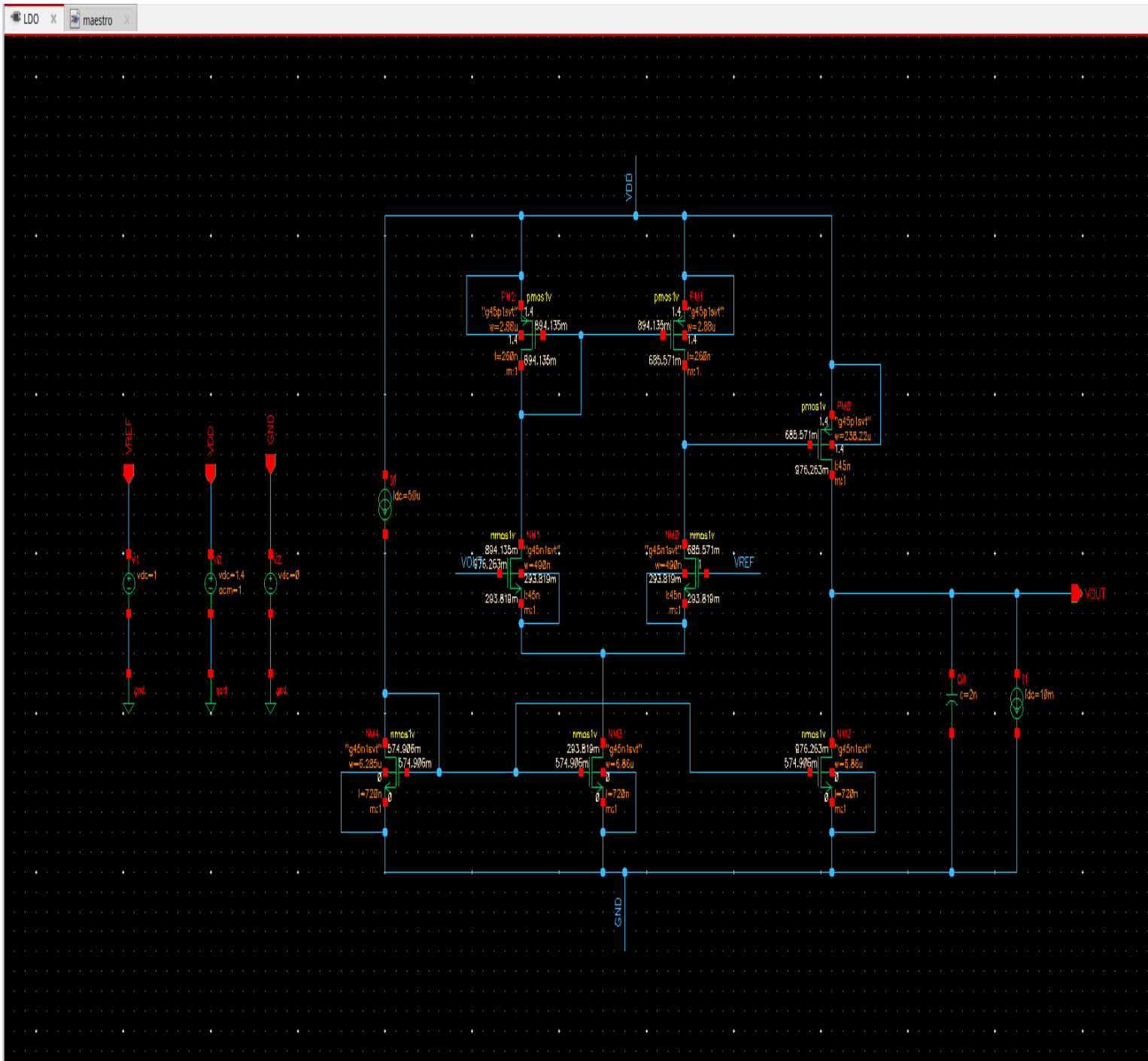
$$\boxed{W_{NMOS} = 6.862\mu m}$$

M_1, M_2, M_3

$$\xrightarrow{\text{Techplot}} \left. \frac{I_D}{W} \right|_{NMOS} = 7.2868$$

$L_{max} = 720nm$

Virtuoso Schematic and DC Operating Point:



- Through DC Operating point analysis each MOSFET were verified for operating in Saturation that is operating region 2 were checked $V_{OUT} = 0.976$ V, $V_{REF} = 1$ V and $V_{DD} = 1.4$ V

Following Signals were plotted using ADE Explorer maestro:

Activities | Virtuoso® ADE Explorer Editing: pra LDO maestro* | Dec 30 7:55 PM

Virtuoso® ADE Explorer Editing: pra LDO maestro

Launch Session Setup Analyses Variables Outputs Simulation Results Tools EAD Parasitics/LDE Window Help

Replace (None)

Setup

filter pra_LDO_1 Simulator spectre Analyses ac 0.001 100G Automatic Start-Stop dc t Click to add analysis Design Variables Click to add variable Parameters Corners Reliability Analyses Monte Carlo Sampling Checks/Asserts

Outputs Setup Run Preview

Name	Type	Details	Value	Plot	Save	Spec
O/P VOLT	signal	/VOUT		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
VIN Power	signal	/VDD		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
VOTA	signal	/net5		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
Passfet current	signal (I)	/PM0/D		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
Bias Current	signal (I)	/NM3/D		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
Reference volt to Opamp	signal	/VREF		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
Diff amp_pmos_current	signal (I)	/PM1/S		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
phase(Vf(/VOUT*))	expr	phase(Vf(/VOUT*))		<input checked="" type="checkbox"/>	<input type="checkbox"/>	
20log(GAIN)	expr	dB20(Vf(/VOUT*))		<input checked="" type="checkbox"/>	<input type="checkbox"/>	

Explorer Run Summary

☒ 0 Corner
☒ Nominal Corner

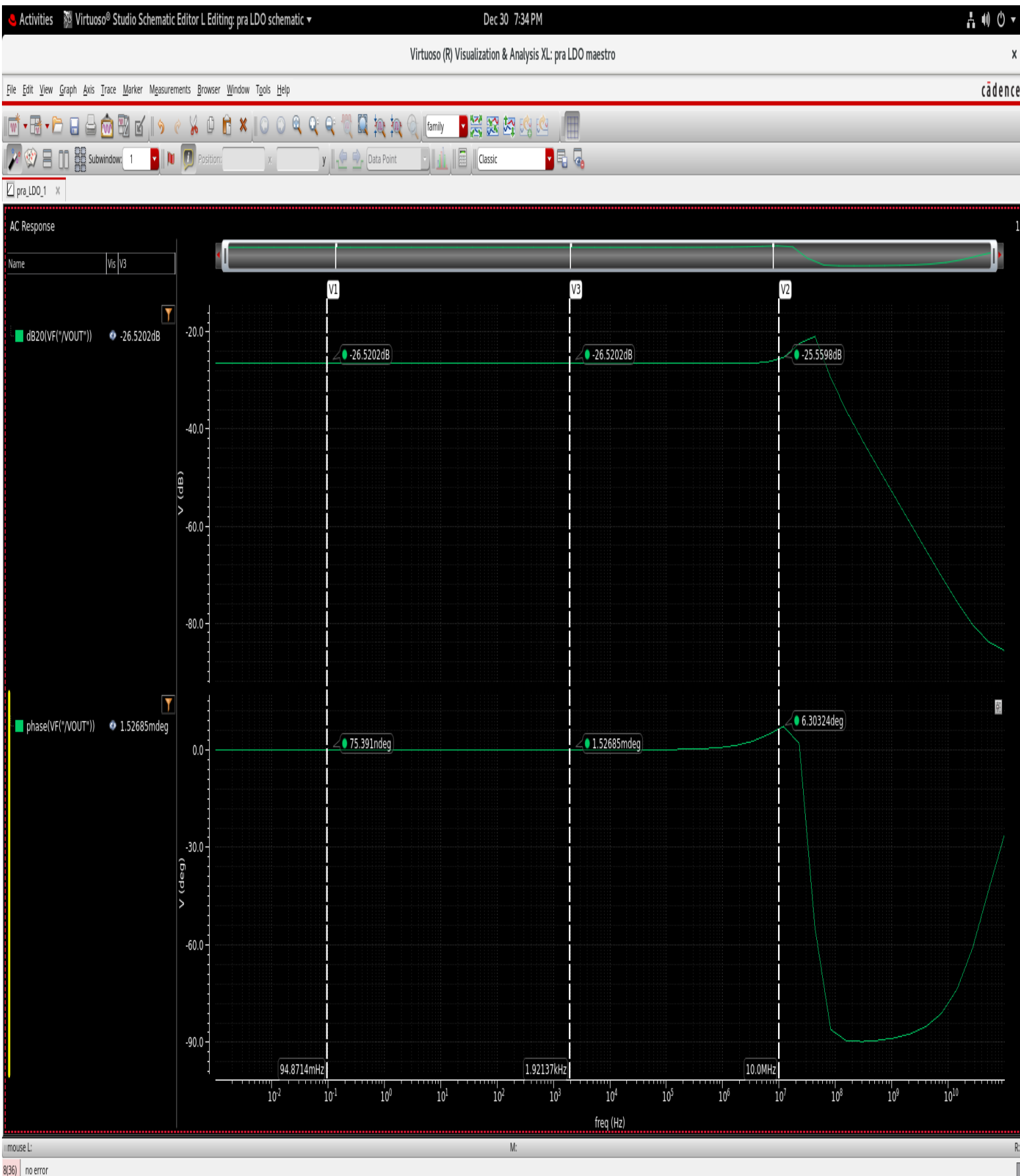
10/50 >

Results: ExplorerRun.0 | pra LDO schematic | Simulator: spectre aps Batch

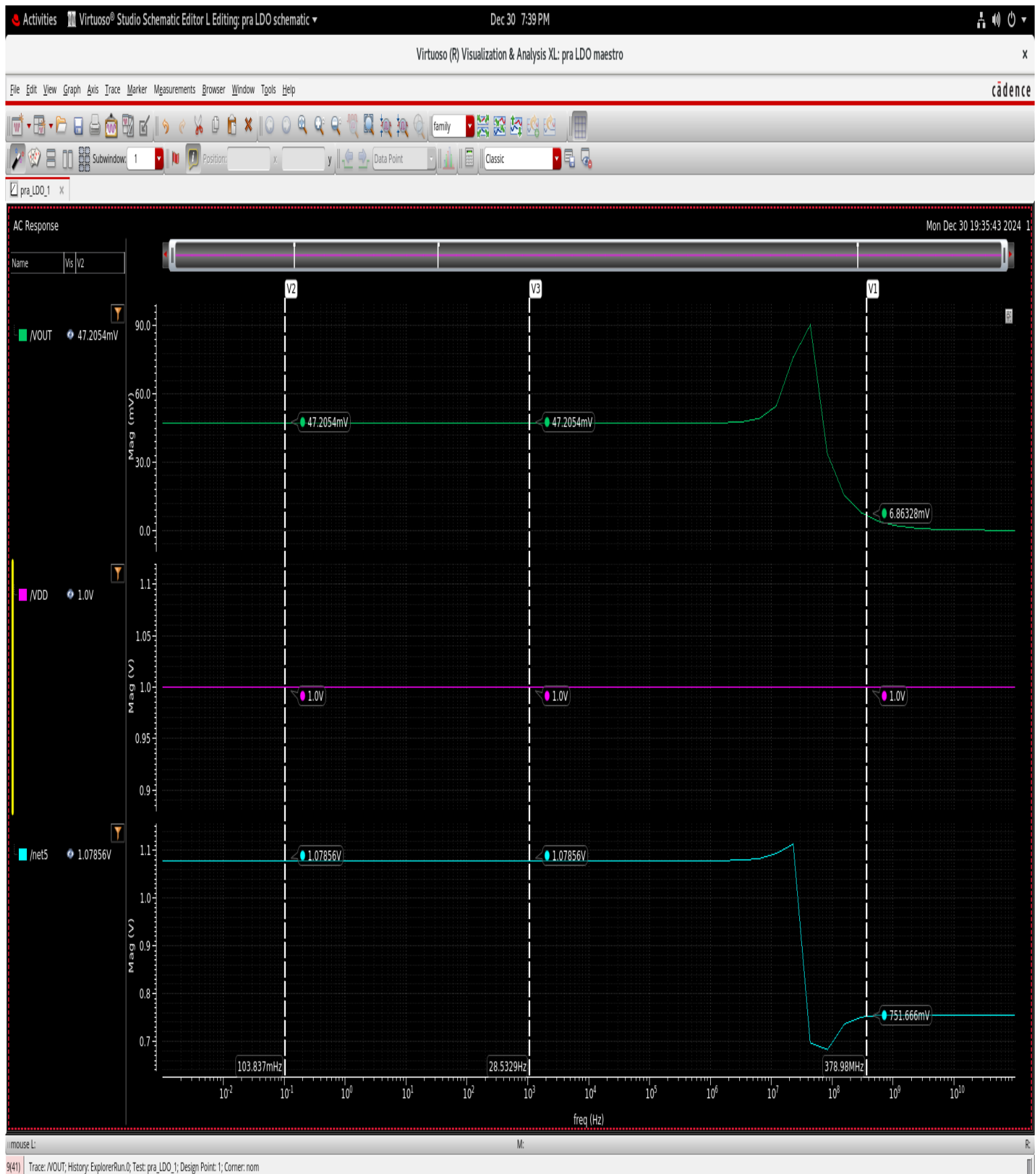
DC Point operating of Output Volt, VDD, VOTA and VREF:



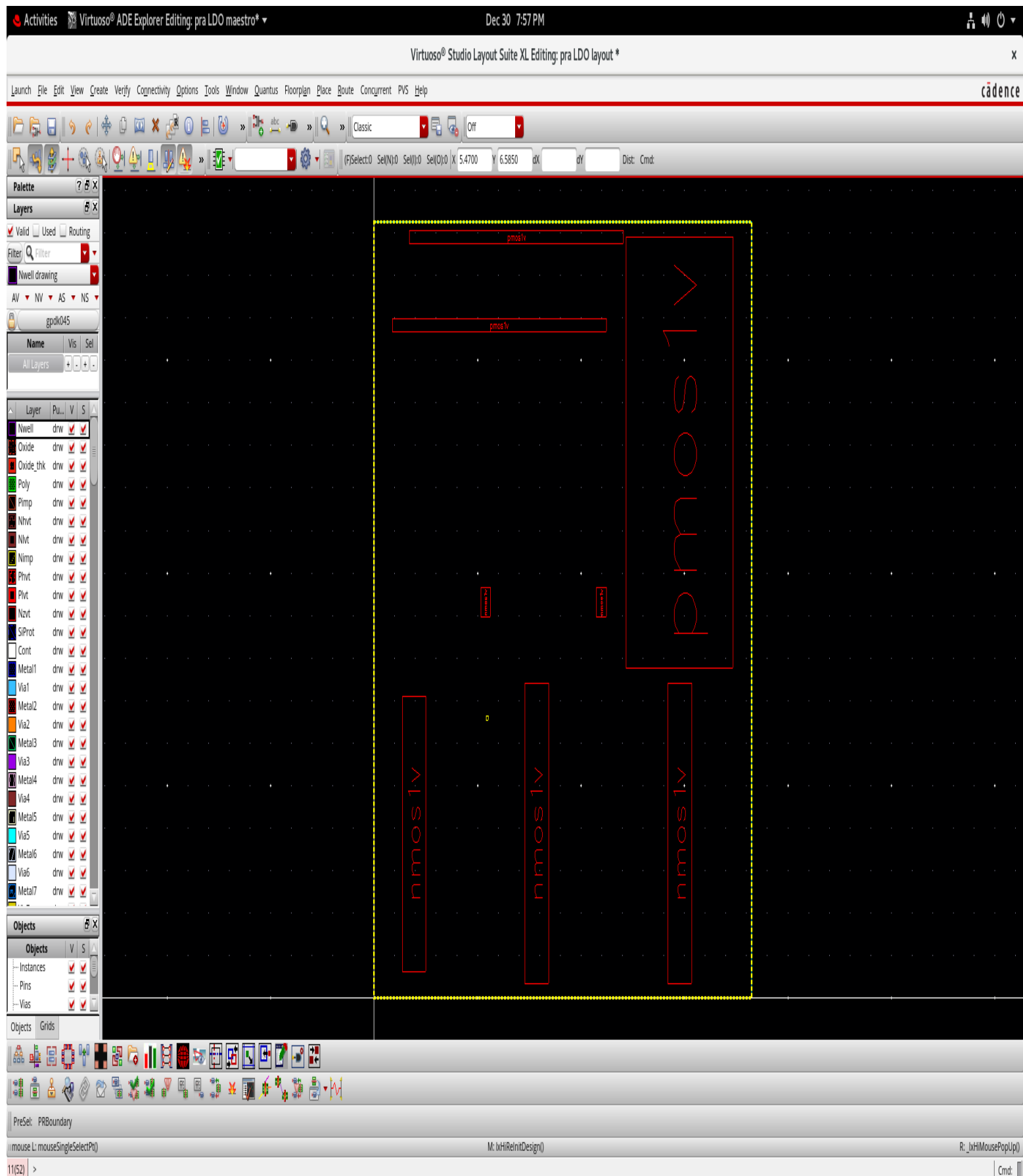
Plots of PSRR and Phase waveform:



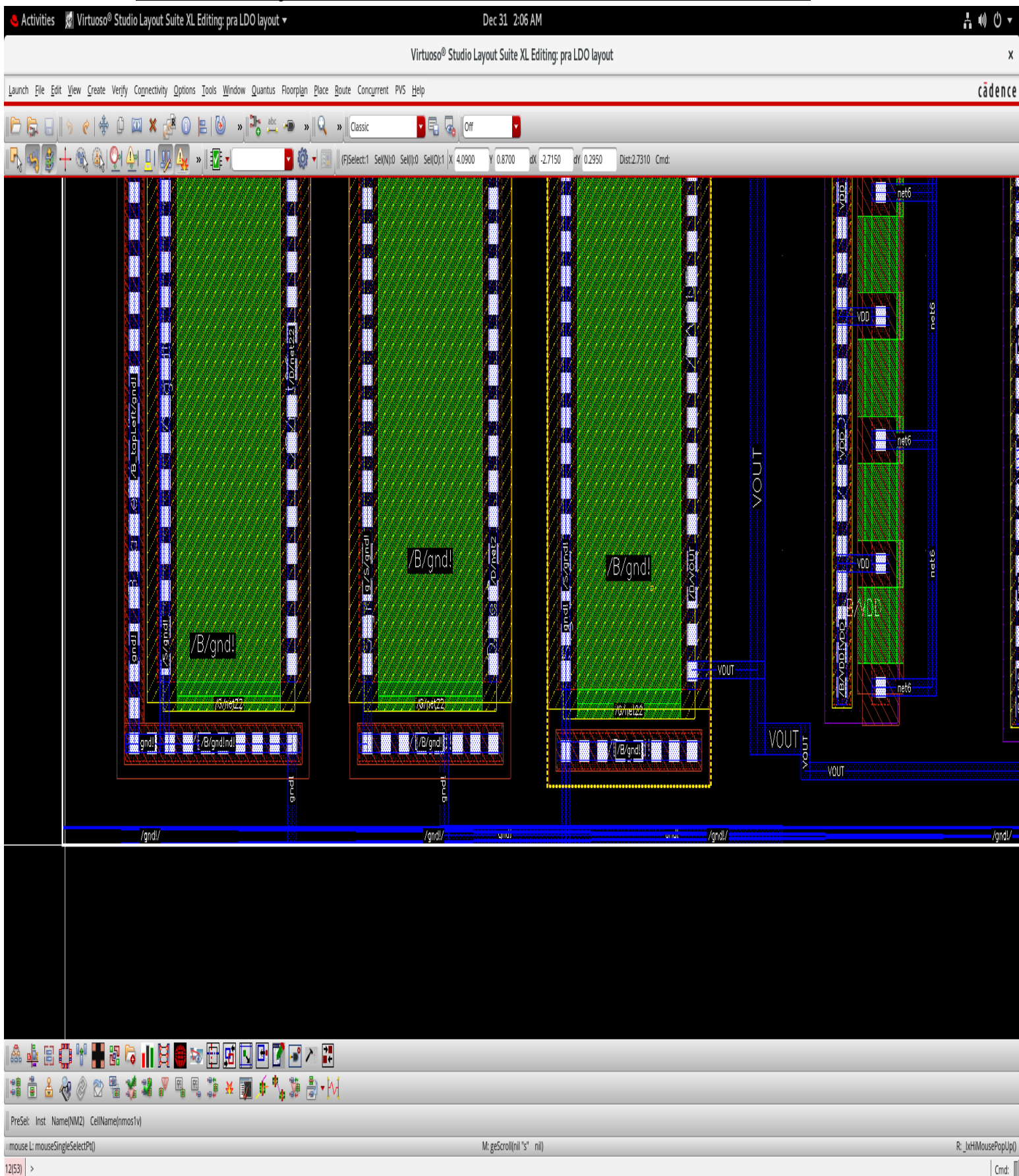
AC Response plots of VOUT,VDD, VOTA for AC Magnitude = 1V in VDD :



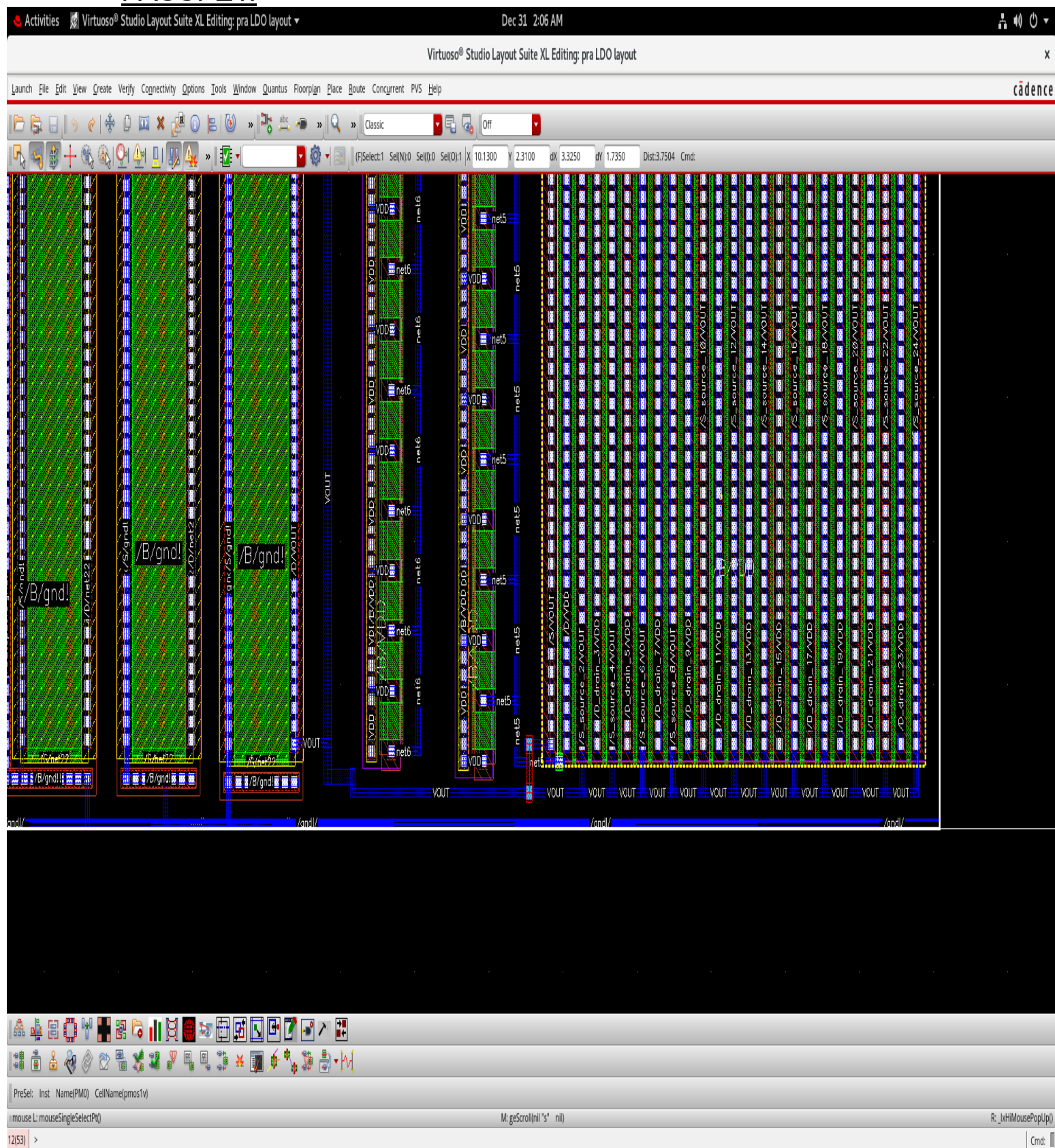
Layout View of gpdk 45nm for all Components of LDO:



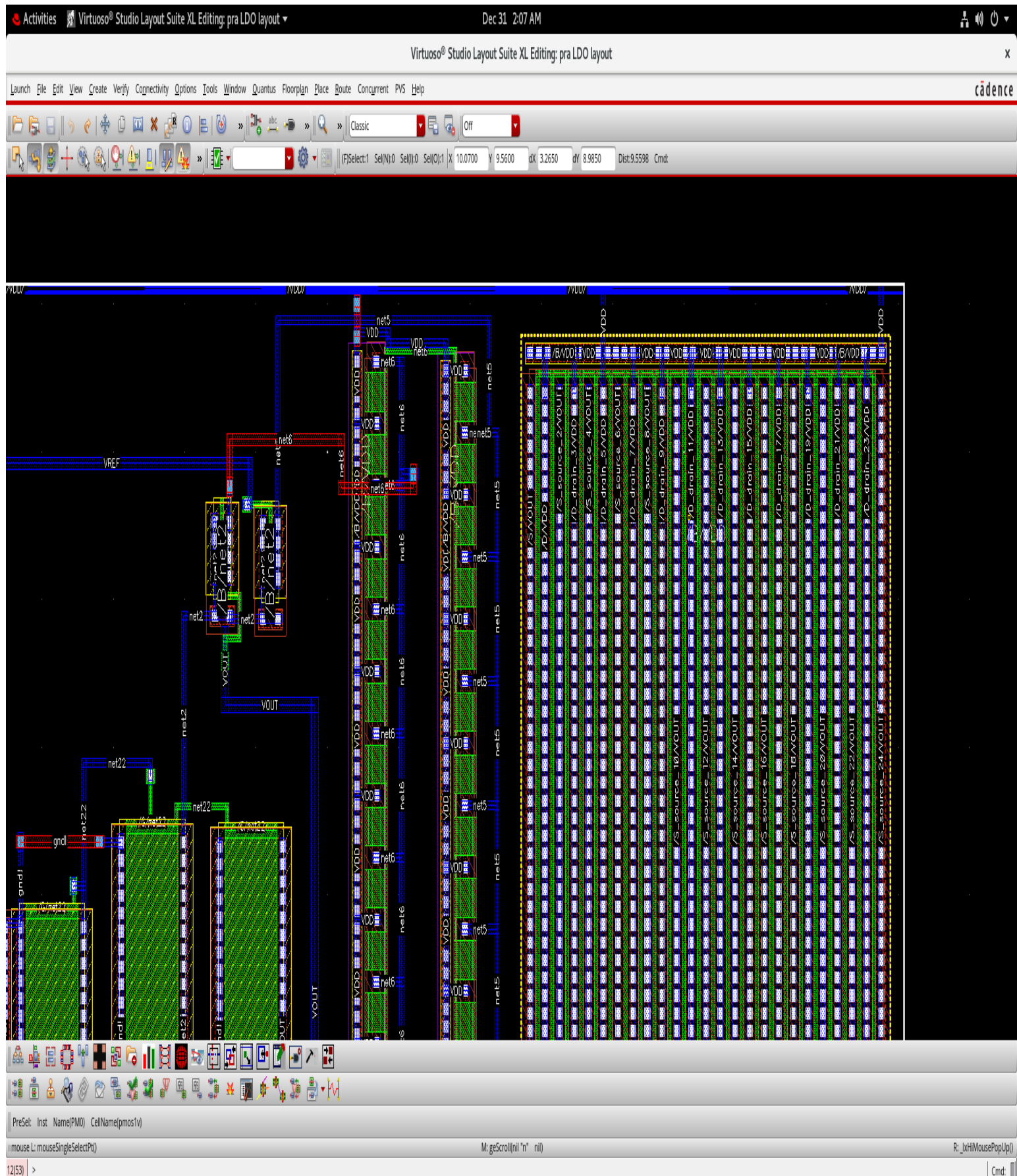
Zoomed Layout of Bias Current NMOS with L=720 nm



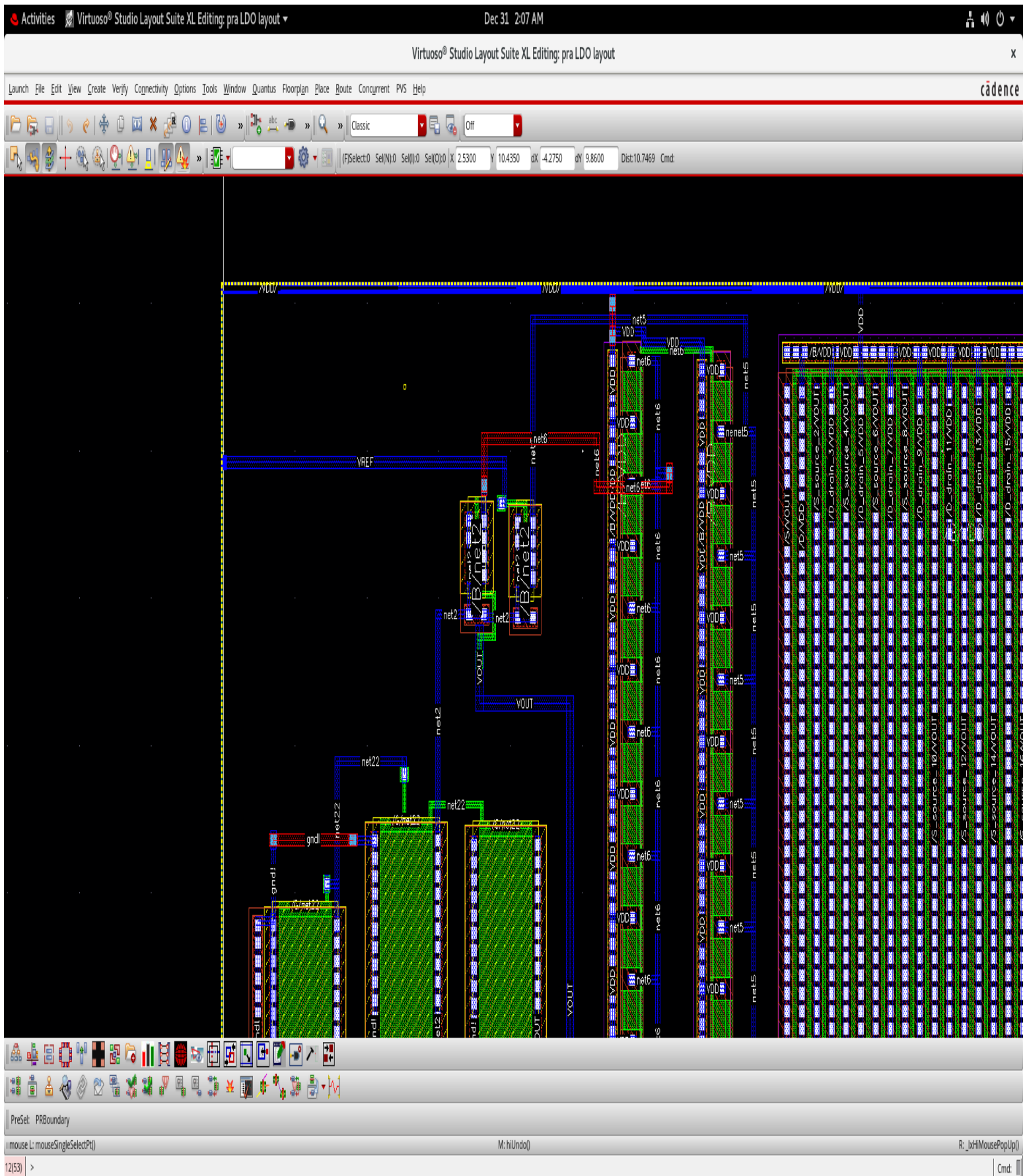
Zoomed View of Routing of Bias NMOS, Diff AMP PMOS & PASSFET:



Zoomed View of PassFet & DiffAMP PMOS L=270 nm



Zoomed View of Connection Diffamp NMOS with L=45 nm



Mapping Schematic and Layout for Bias NMOS of L= 720 nm

Virtuoso® Studio Layout Suite XL Editing: pra LDO layout

Dec 31 2:08 AM

Virtuoso® Studio Schematic Editor XL Editing: pra LDO schematic Config: pra LDO physConfig

Launch File Edit View Create Verify Connectivity Options Tools Window Quantus Floorplan Place Route Concurrent PVS Help

Classic Off

(P)Select:1 Sel(N):0 Sel(I):1 Sel(O):0 X:5.6250 Y:4.8150 dX:-1.1800

Basic Search

NAVIG... ? X

Schematic LDO

OBJECTS

- All
- Instances 16
- Nets 8
- Pins 3
- Nets ... Pins

GROUPS

- Cells
- Types

DESIGN TENT

QUERIES

Prope... ? X

ins All

Model Name

Multiplier

Length

Finger Width

Total Width

Fingers

Folding Thre...

Over Count

mouse L: schSingleSelectPt()

M: geScroll(nil "e" nil)

R: schHIMousePopUp()

10(46)

Cmd: Conn: On Set: 1

PreSel: Inst Name(PM2) CellName(pmos1v)

mouse L: mouseSingleSelectPt()

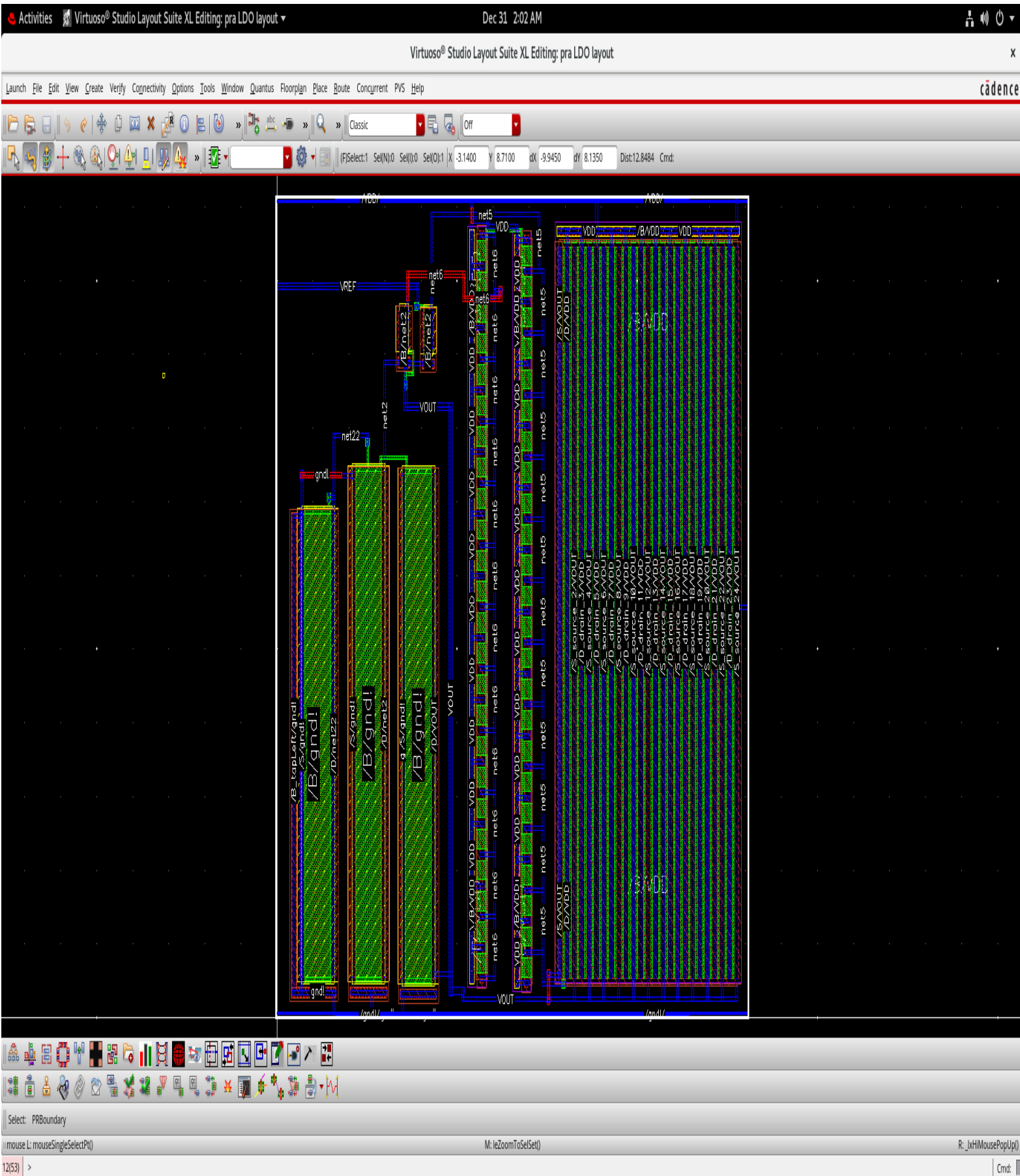
M: geScroll(nil "e" nil)

R: schHIMousePopUp()

12(53)

Cmd:

Detailed Layout Routing of all Component of Complete LDO :



Points to be Address:

- For NMOS 1V and PMOS 1V gpdk 45nm Technology through Techplots there is limitation of High PSRR values generation in calculation Step 2 of NMOS and PMOS sizing of DIFFAMP
- DRC, LVS Virtuoso window is not taking gpdk045 files, when we try to enter any file in DRC, LVS the particular window will close itself automatically. So, need to resolve by cadence team