Lab 01
LPF Simulation and MOSFET Characteristics

Analog IC Design Course – Cādence Tools (Self Study)

Student Information

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Under Guidance and Help of My More Experienced Friends

Labs Provided by **Dr. Hesham Omran** via Master-Micro.com

Thanks to everyone who has helped me,
I pledge to help others as well.

Done during my **Post Graduate MSc. Program** in
Electronics and Electrical Communication Engineering
at the **Faculty of Engineering – Ain Shams University**

Lab 01: LPF Simulation and MOSFET Characteristics

Intended Learning Objectives:[1]

This lab[2] is divided into two parts:

• In Part 1 you will

- Get familiar with Cadence custom IC design tools (Virtuoso Environment).
- Learn the different types of simulations (transient, ac, pole-zero).
- Learn how to run parametric sweeps.

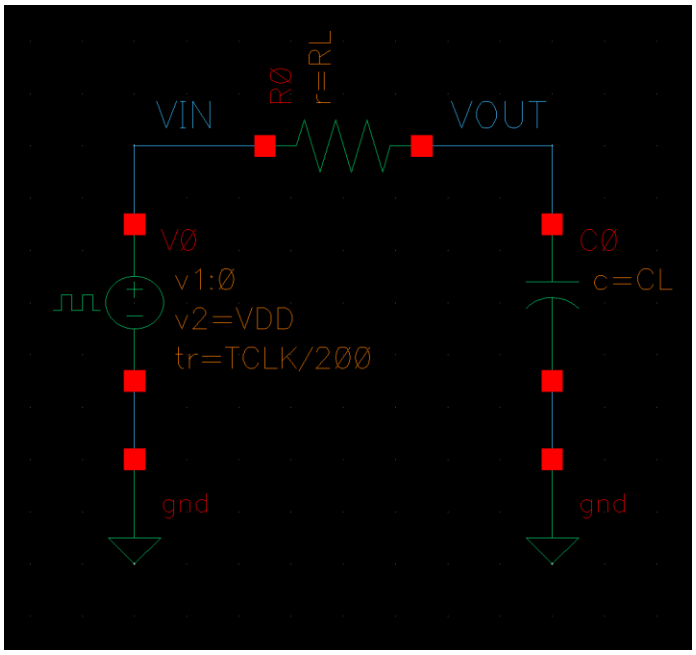
• In Part 2 you will

- Learn the difference between DC and parametric sweeps.
- Compare the behavior of PMOS and NMOS transistors.
- Compare the behavior of short-channel and long-channel MOSFETs.

Part 1: Low Pass Filter Simulation (LPF):

1. Transient Analysis

1) Design a first order low pass filter that has **R = 1kΩ** and **1ns** time constant.



Put RL = 1kΩ

[1] *COLOR CODES:* Orange (steps) -- Blue (output) -- Green (comments / observations) – White (equations).

[2] **Cadence Virtuoso** software on a Linux® Debian 8 Virtual Machine is used.

Then:

$$time\ constant = \tau = RC = 1k\Omega \times C = 1ns$$
$$\therefore C = \frac{1ns}{1k\Omega} = 1pF$$

Put CL = 1pF

2) Apply a square wave input with T_{high} = Pulse Width = 10ns, T_{clk} = Period = 20ns, and T_{rise} = T_{fall} = 100ps.

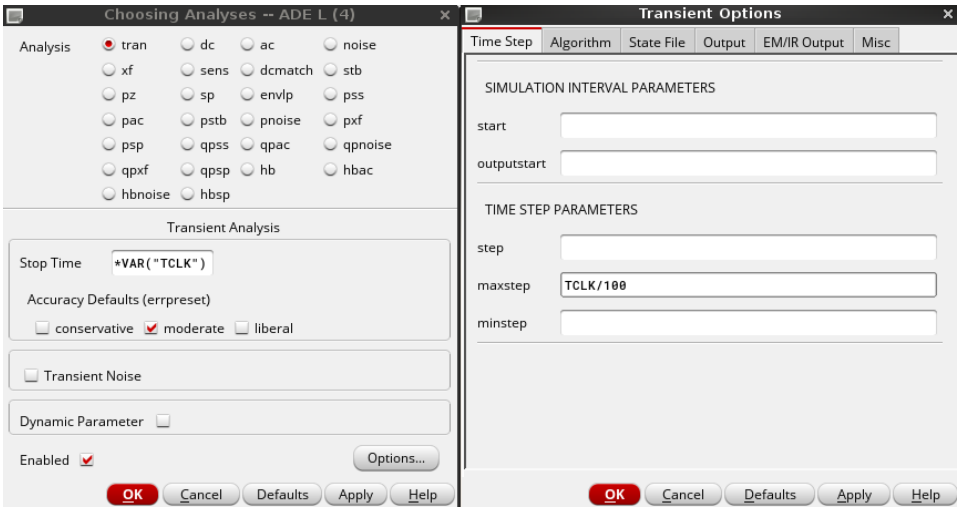
Put TCLK = 20ns

Put Pulse Width = TCLK/2 = 10ns

Put T_{rise} = T_{fall} = T_{CLK}/200 =20ns/200 = 100ps

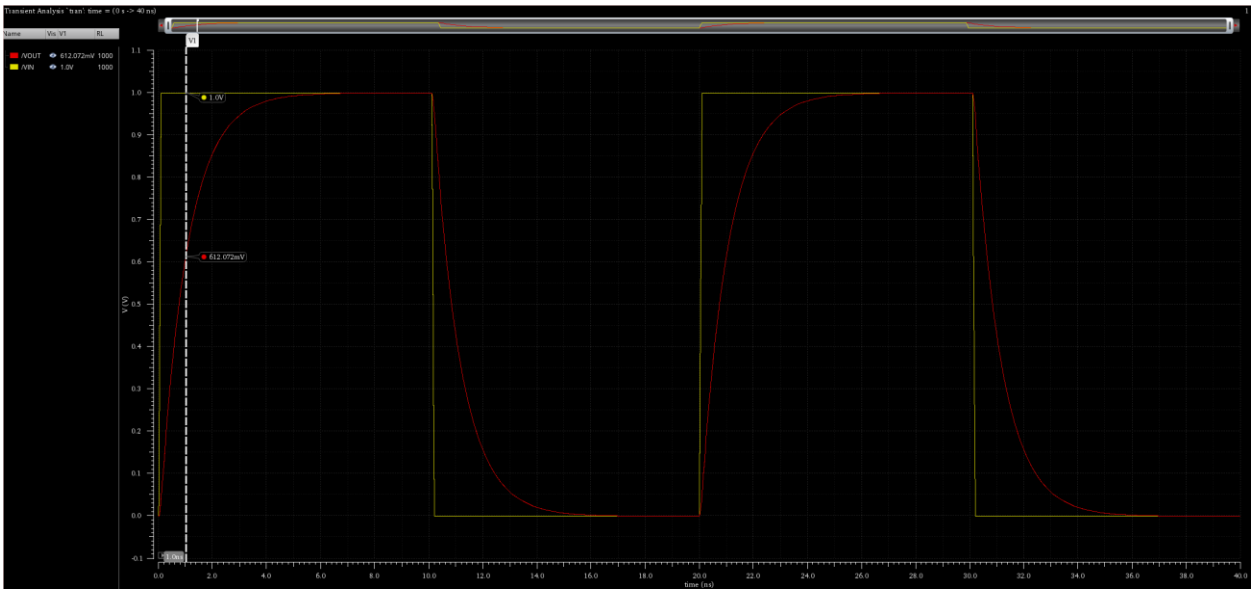
3) Report transient analysis results for two periods (use max time step = T_{clk}/100).

Finally to plot transient analysis we Put VDD = 1V and max time step = TCLK/100



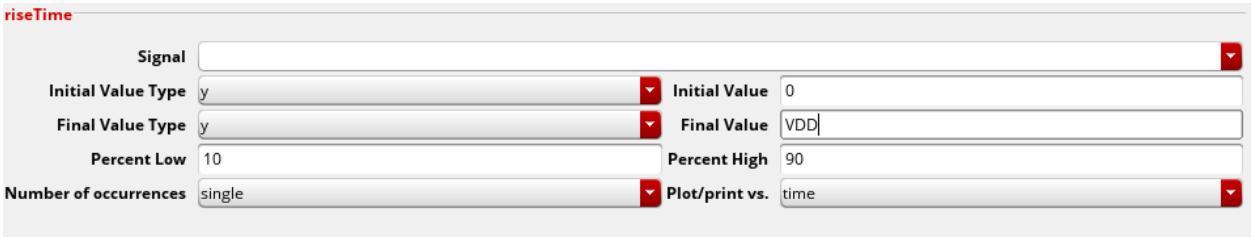
Put stop time = 2*VAR("TCLK"), to get two periods.

Transient Analysis Results:



At $\tau = 1ns$, the voltage is at 61.2%, which is close to theory $= 1 - e^{-1} = 63.21\%$.

4) Calculate rise and fall time (10% to 90%) using Cadence calculator expressions. Export the expressions to adexl.



riseTime(VT("/VOUT") 0 nil 1 nil 10 90 nil "time") = 2.195E-9
fallTime(VT("/VOUT") 1 nil 0 nil 10 90 nil "time") = 2.192E-9

Test	Output	Nominal	Spec	Weight	Pass/Fail
tutorial_rc:rc_tb:2	trise	2.195n			
tutorial_rc:rc_tb:2	tfall	2.192n			

5) Compare simulation with analytical results in a table.

	SIMULATION	THEORETICAL
Trise	2.195ns	2.2* τ = 2.2ns
Tfall	2.192ns	2.2* τ = 2.2ns

Theoretical rise time (and similarly fall time) are calculated from:

$$\because V(t) = V_0\left(1 - e^{-\frac{t}{\tau}}\right)$$

$$\therefore\ 1 - \frac{V(t)}{V_0} = e^{-\frac{t}{\tau}}$$

$$\therefore -\frac{t}{\tau} = ln(1 - \frac{V(t)}{V_0})$$

$$\boldsymbol{t = -\tau \times ln\left(1 - \frac{V(t)}{V_0}\right)}$$

$$\because \frac{V(t_1)}{V_0} = 0.1, \qquad \because \frac{V(t_2)}{V_0} = 0.9$$

$$t_1 = -\tau \times \ln(0.9) = \tau \times \ln\left(\frac{10}{9}\right) = \tau \times (ln10 - ln9)$$

$$t_2 = -\tau \times \ln(0.1) = \tau \times \ln\left(\frac{10}{1}\right) = \tau \times ln10$$

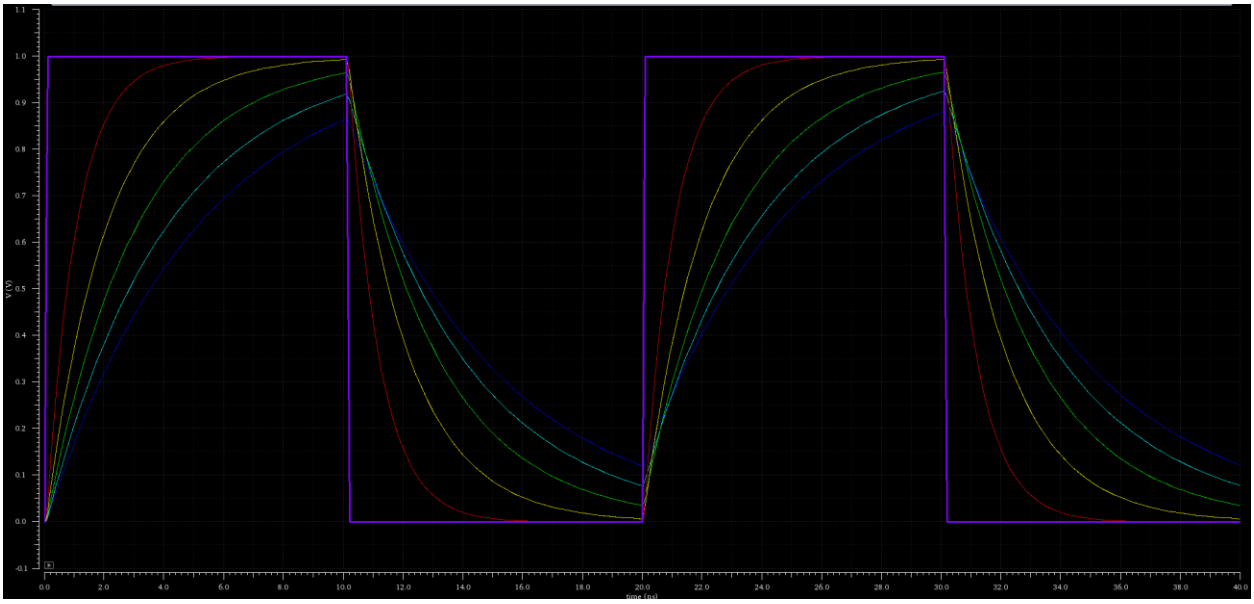
$$\boldsymbol{t_r = t_1 - t_2 = \tau \times (ln10 - ln9) - \tau \times ln10 = \tau \times ln9 \approx 2.197 \times \tau}$$

6) Do parametric sweep for **R = 1: 1: 5kΩ**. Report overlaid results. Comment on the results.

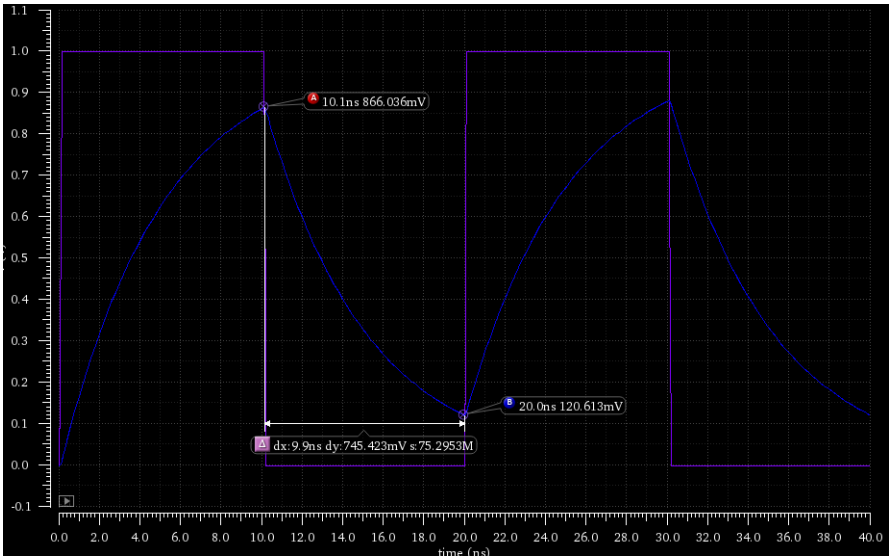
Put RL = 1k, 2k, 3k, 4k, 5k (5 Point Sweeps)

Parameters: RL=1k						
1	tutorial_rc:rc_tb:2	trise	2.195n			
1	tutorial_rc:rc_tb:2	tfall	2.192n			
Parameters: RL=2k						
2	tutorial_rc:rc_tb:2	trise	4.391n			
2	tutorial_rc:rc_tb:2	tfall	4.393n			
Parameters: RL=3k						
3	tutorial_rc:rc_tb:2	trise	6.589n			
3	tutorial_rc:rc_tb:2	tfall	6.589n			
Parameters: RL=4k						
4	tutorial_rc:rc_tb:2	trise	8.787n			
4	tutorial_rc:rc_tb:2	tfall	8.789n			
Parameters: RL=5k						
5	tutorial_rc:rc_tb:2	trise	eval err			
5	tutorial_rc:rc_tb:2	tfall	eval err			

Notice the eval err, as output waveform doesn't reach 10% or 90% of input, therefore calculating trise and tfall with these conditions is meaningless. Notice the following overlaid waveforms.



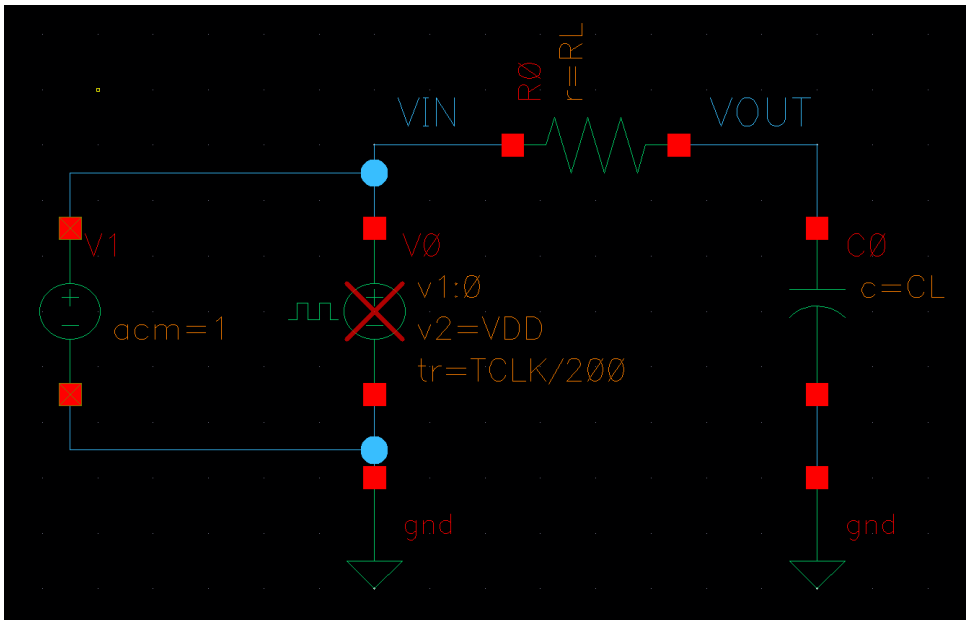
The values of the output signal doesn't reach 10% or 90% of the input signal.



2. AC Analysis

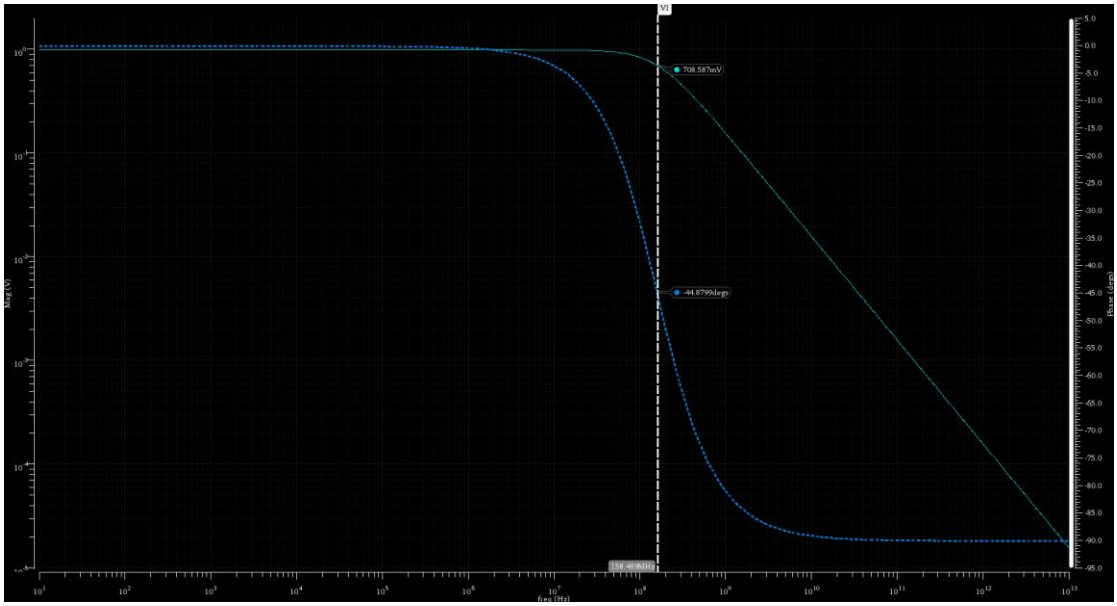
1) Report Bode Plot (magnitude and phase) for the previous LPF.

To do an AC Analysis, **the pulse voltage source has to be changed** into a regular AC source.



Put RL=1k

Bode Plot (Magnitude and Phase) → Note the Marker [V1] at the 3dB BW and -45° phase shift



2) Calculate DC gain and 3dB bandwidth using Cadence calculator expressions. Export the expressions to adexl.

ymax(mag(v("/VOUT" ?result "ac")) 3 "low") = 1.000
bandwidth(mag(v("/VOUT" ?result "ac")) 3 "low") = 158.8E6

3) Compare simulation with analytical results in a table.

	SIMULATION	THEORETICAL
Ao (DC Gain)	1 (0dB)	1
BW (3dB Bandwidth)	158.8 MHz	159.155 MHz (error = 0.2235%)

Theoretical Ao and BW are calculated from:

$$\because V_{out}(s) = \frac{1\backslash sC}{\frac{1}{sC} + R}$$

$$\therefore V_{out}(s) = \frac{1}{1 + sRC}$$

$$\therefore V_{out}(j\omega) = \frac{1/RC}{1\backslash RC + j\omega} = \frac{\omega_c}{\omega_c + j\omega} = \frac{1}{1 + \frac{j\omega}{\omega_c}}$$

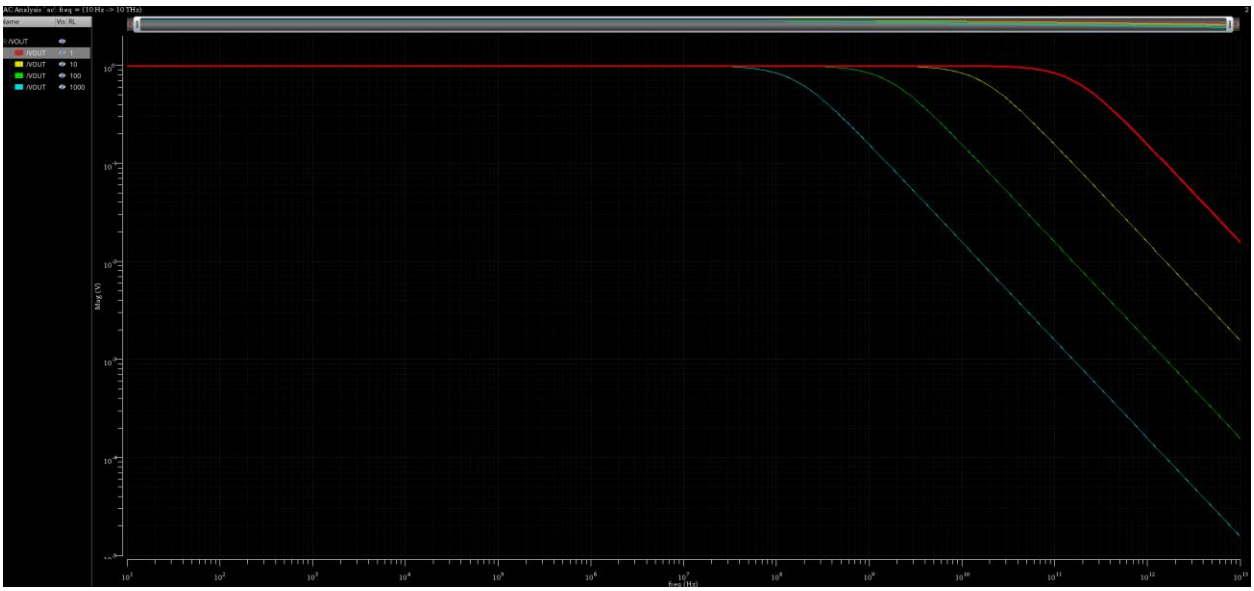
$$\therefore \boldsymbol{|V_{out}(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^2}}}, \qquad \therefore \boldsymbol{\angle V_{out}(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_c}\right)}$$

$$BW = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC} = 159.155\ MHz$$

4) Do parametric sweep for **R = 1, 10, 100, 1000kΩ**. Report overlaid results. Comment on the results.

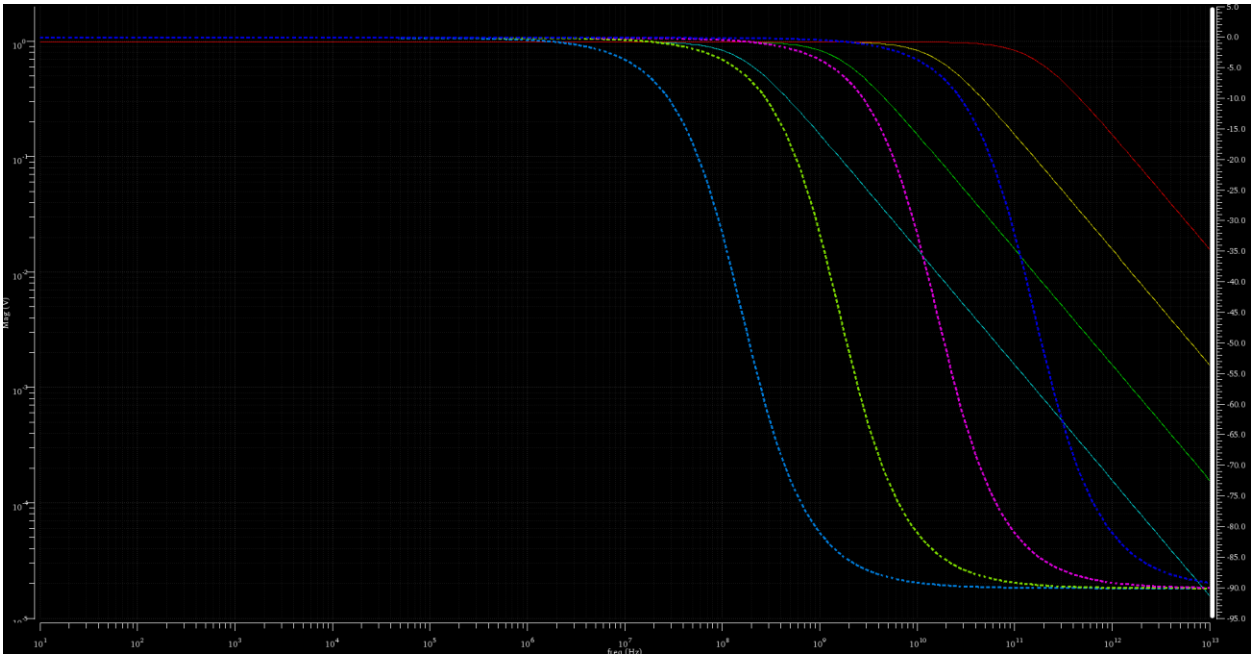
Parameters: RL=1						
1	tutorial_rc:rc_tb:2	BW	158.8G			
1	tutorial_rc:rc_tb:2	Ao	1			
Parameters: RL=10						
2	tutorial_rc:rc_tb:2	BW	15.88G			
2	tutorial_rc:rc_tb:2	Ao	1			
Parameters: RL=100						
3	tutorial_rc:rc_tb:2	BW	1.588G			
3	tutorial_rc:rc_tb:2	Ao	1			
Parameters: RL=1k						
4	tutorial_rc:rc_tb:2	BW	158.8M			
4	tutorial_rc:rc_tb:2	Ao	1			

NOTE: As R decreases, the 3dB-BW increases.



Overlaid Results of the Magnitude and Phase of the Frequency response as a Bode Plot for an R sweep:

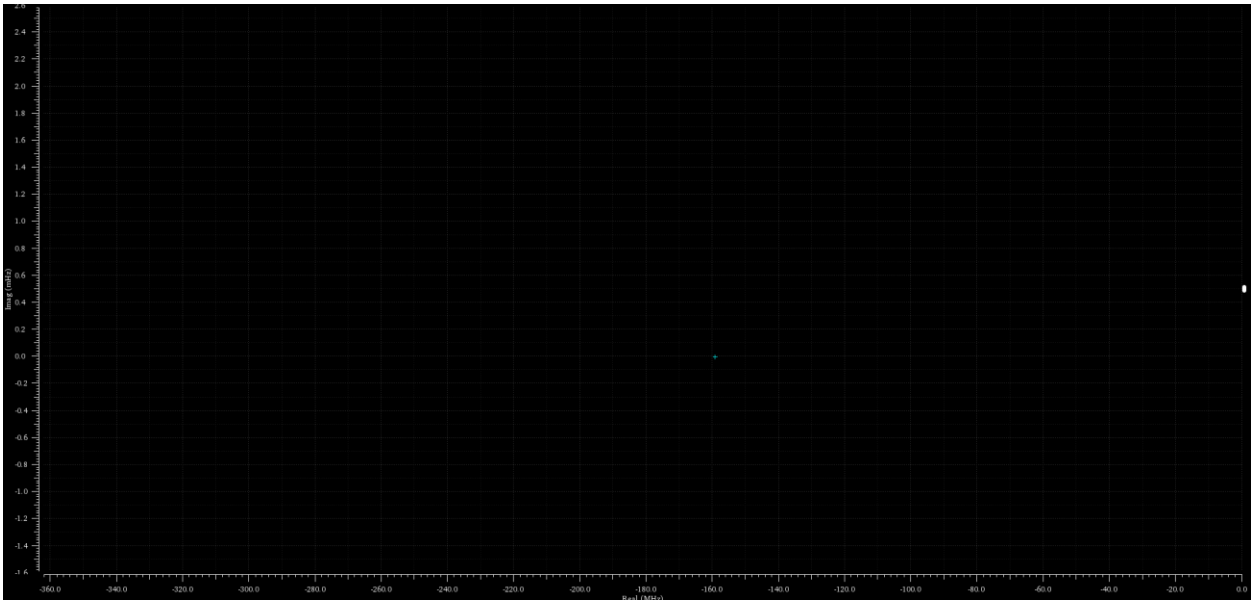
Put R = 1, 10, 100, 1k



3. [Optional] Pole Zero Analysis

1) Report pole zero analysis results.

The pole is at -158MHz for R = 1kΩ

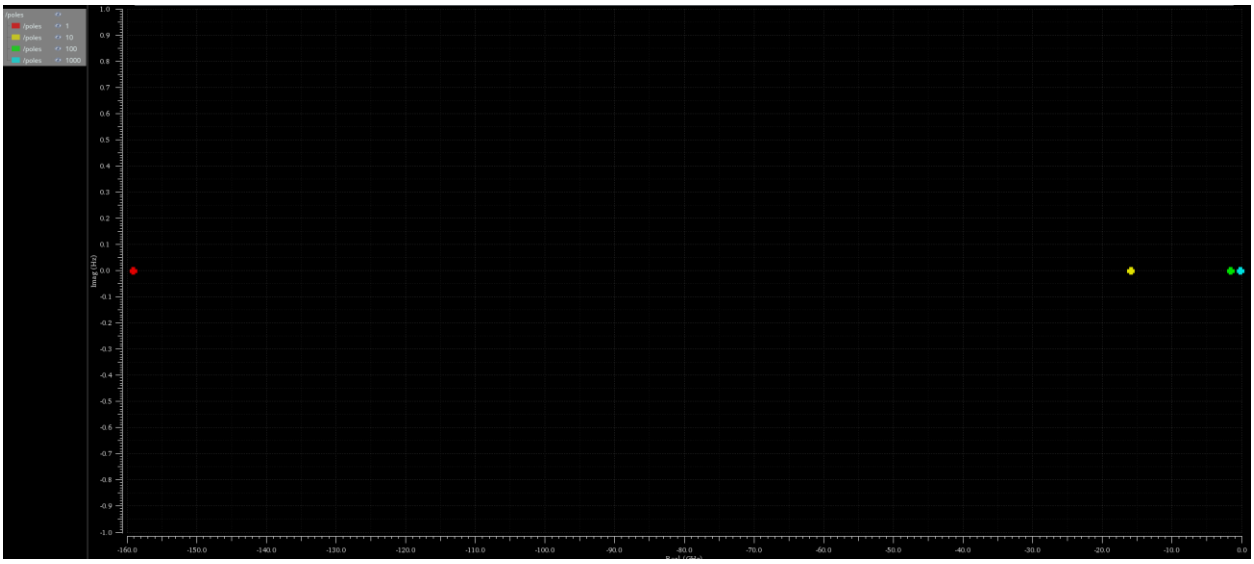


2) Find the pole frequency and compare it with the bandwidth calculated from AC analysis.

Note the pole is at -158MHz which is similar to the theoretical and AC analysis.

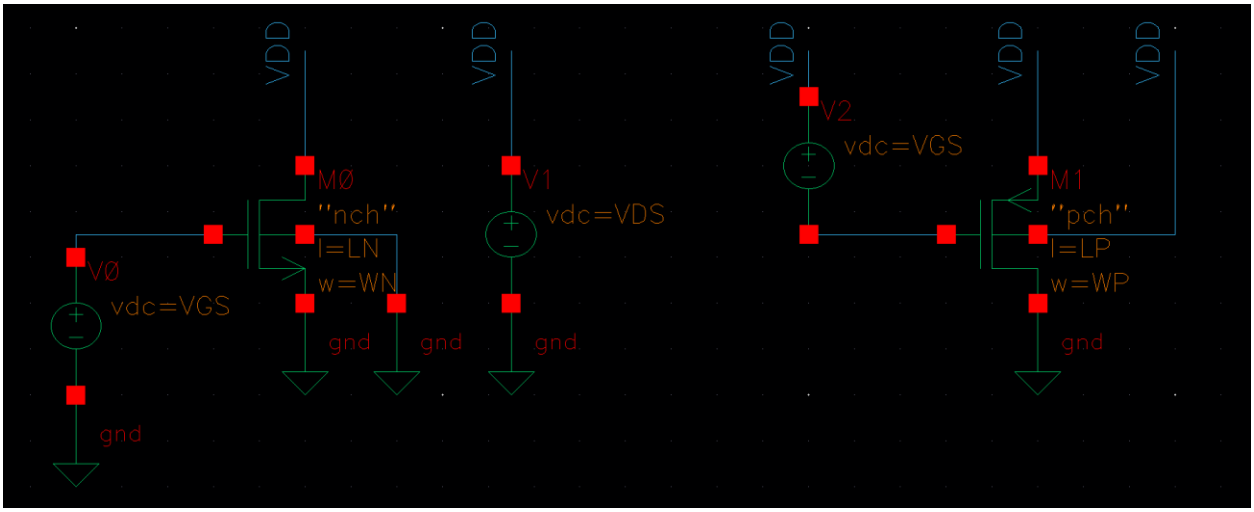
At different values of R:

Note the **Pole Frequency = 159.2E9 (RED – left most pole – at R = 1 ohm)**



Part 2: MOSFET Characteristics

Create a test-bench to characterize NMOS and PMOS devices as shown in the figure below.



1. ID vs VGS

1) Plot ID – VGS characteristics for NMOS and PMOS devices. **Set VDS = VDD**, and **VGS = 0: 10m: VDD**. Use **VDD = 1.2V for 130nm** technology and **VDD = 1.8V for 180nm** technology.

Plot the results overlaid for the following:

- Short channel device: **W = 1µm and L = 200nm**
- Long channel device: **W = 10µm and L = 2µm**.

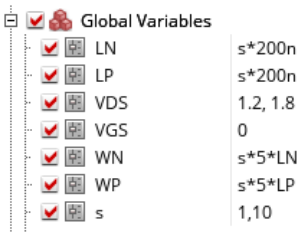
Hint: Set L as a parameter and set W = 5 × L

➔ **Cadence Hint:** Use DC sweep instead of parametric sweep whenever possible. DC sweep is extremely faster, and uses much less resources and disk space. In this question you should **use DC sweep for VGS**.

➔ **Cadence Hint:** To simulate both the short channel and the long channel devices in the same simulation run you can **use parametric sweep**. Define **L** as a parameter (L = 200n, 2u) and define **W** as a function of L (W = 5*L).

Set
VDS = VDD
VDD = 1.2V for 130nm **VDD = 1.8V** for 180nm
VGS = 0: 10m: VDD [DC Sweep]

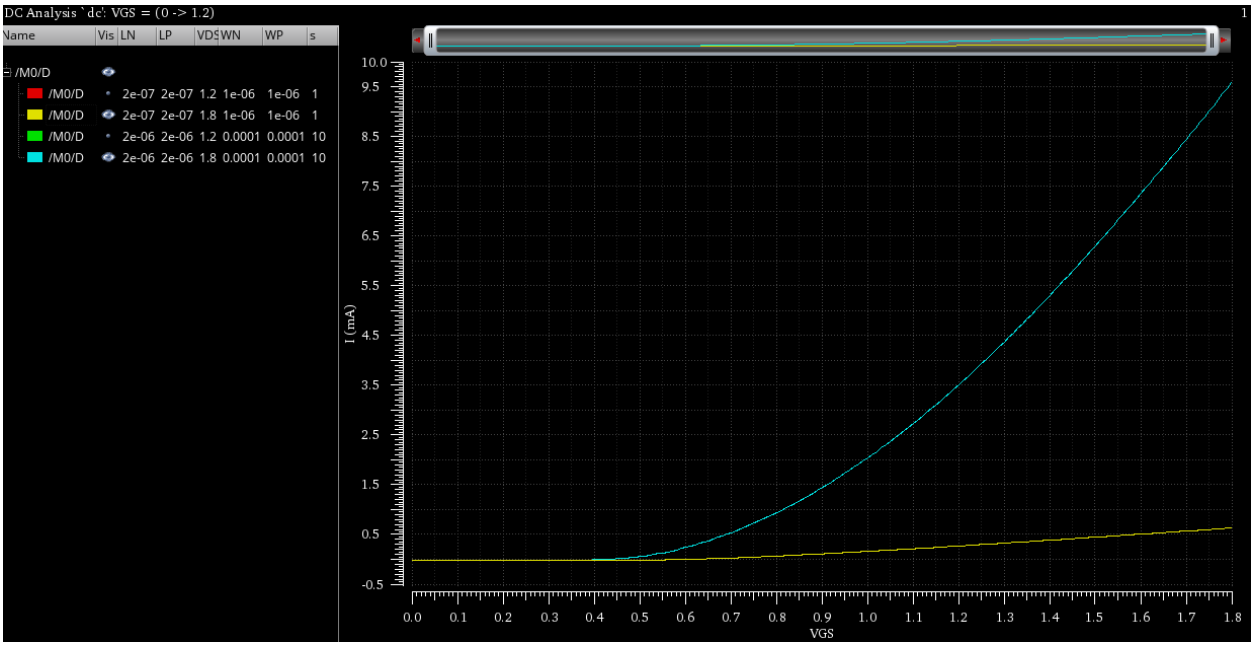
Put **(L = 200n, 2u)** and **(W = 5*L)**. [Parametric Sweep]

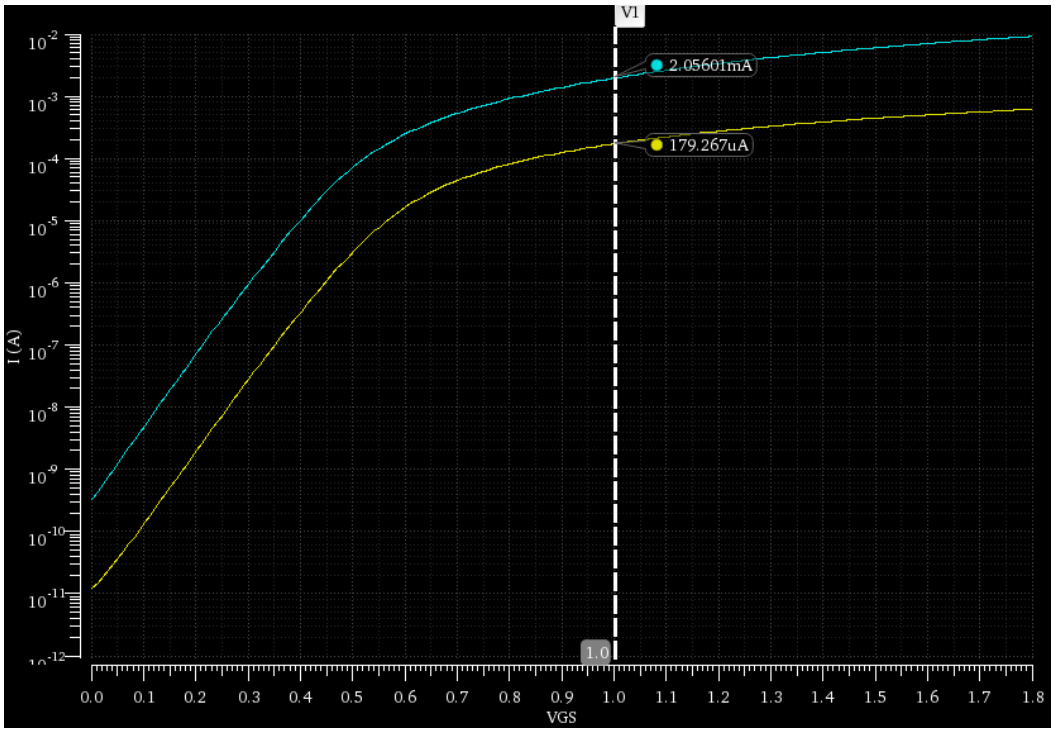


The aim of this variable setup is to finish all required in one run,
then use results browser to choose the required results for the lab.

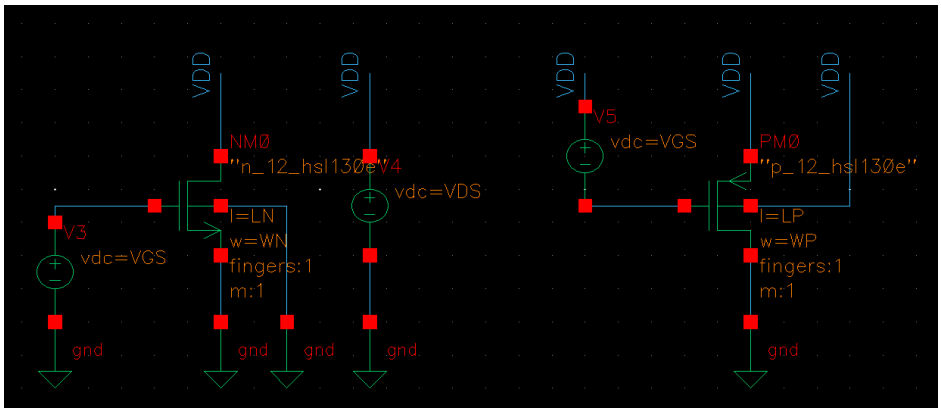
(This run is using *ee214b.sp* library file (Dr. B. Murmann), which is a 180nm technology)

Overlaid Results for Short channel device: W = 1µm and L = 200nm [yellow]
Overlaid Results for Long channel device: W = 10µm and L = 2µm. [cyan]



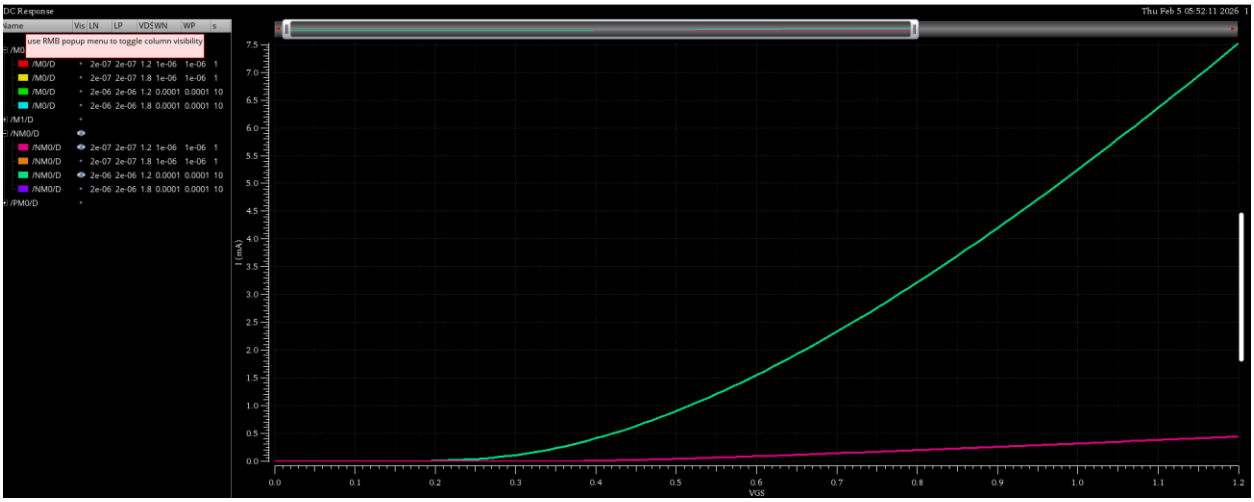


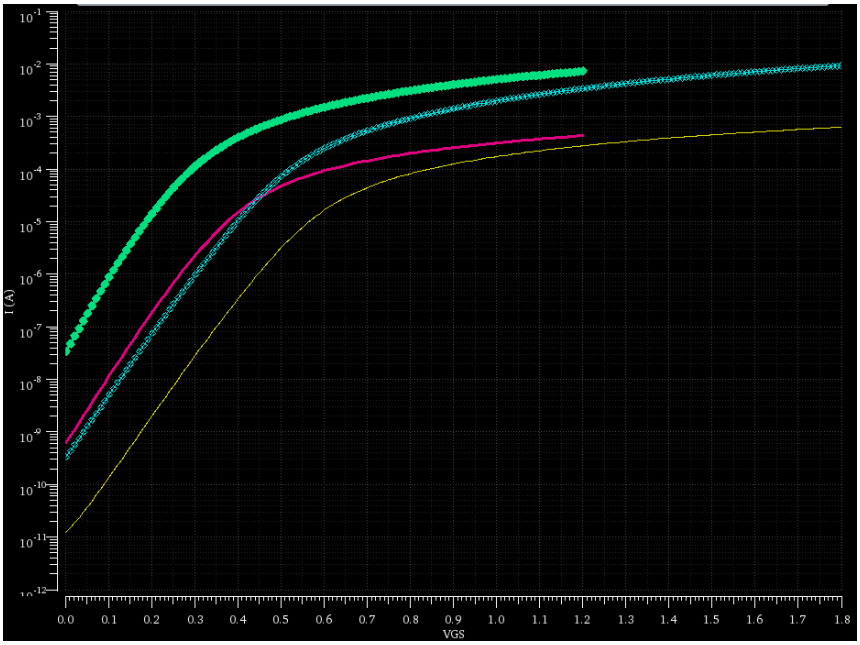
In 180nm technology, VGS is DC Swept to 1.8V. It is noticed that the longer channel is higher in current.



(This run is using *umc13mmrf* library, which is a 130nm technology)

Overlaid Results for Short channel device: W = 1µm and L = 200nm [green]
Overlaid Results for Long channel device: W = 10µm and L = 2µm. [red]





Note that: The long channel (diamond symbol - ◊) is always higher in current due to less short channel effects.

The **130nm technology** (with lesser VDD = 1.2V) is higher in current than the **180nm technology** (with higher VDD = 1.8V), which means higher current with less dynamic power consumption. However, it has considerably much more sub-threshold leakage, which means higher static power consumption.

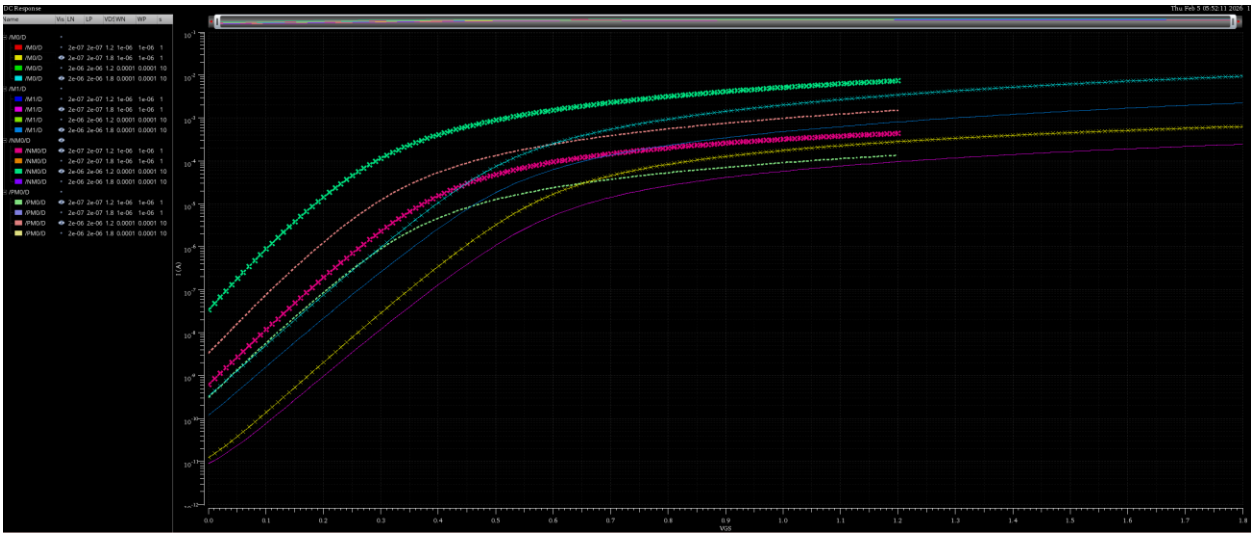
2) Comment on the differences between short channel and long channel results.

- Which one has higher current? Why?
- Is the relation linear or quadratic? Why?

The short channel (for both 130nm and 180nm) has less current than the long channel MOSFET.
The relation is linear for the short channel, and quadratic for the long channel.

3) Comment on the differences between NMOS and PMOS.

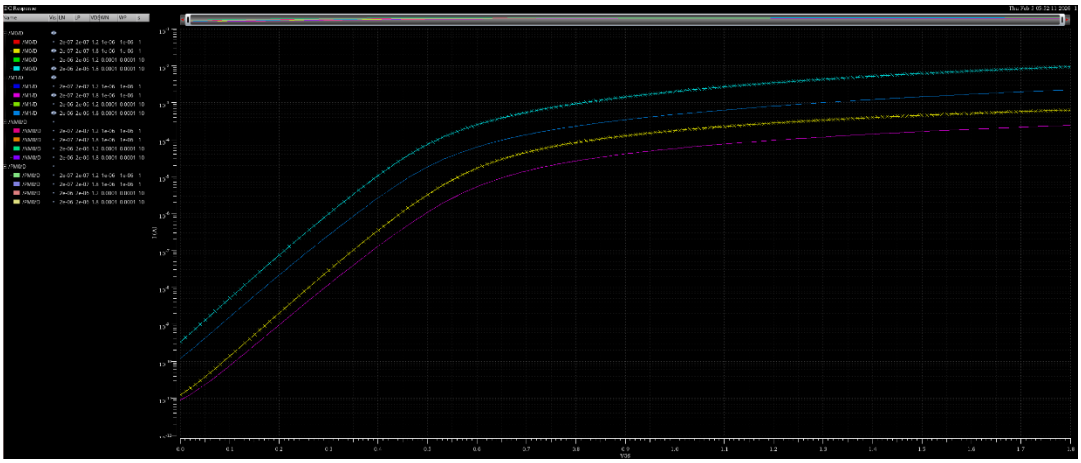
- Which one has higher current? Why?
- What is the ratio between NMOS and PMOS currents at **VGS = VDD**?
- Which one is more affected by short channel effects?



Symbol X: NMOS
Dashed: 130nm technology (VDD = 1.2V)

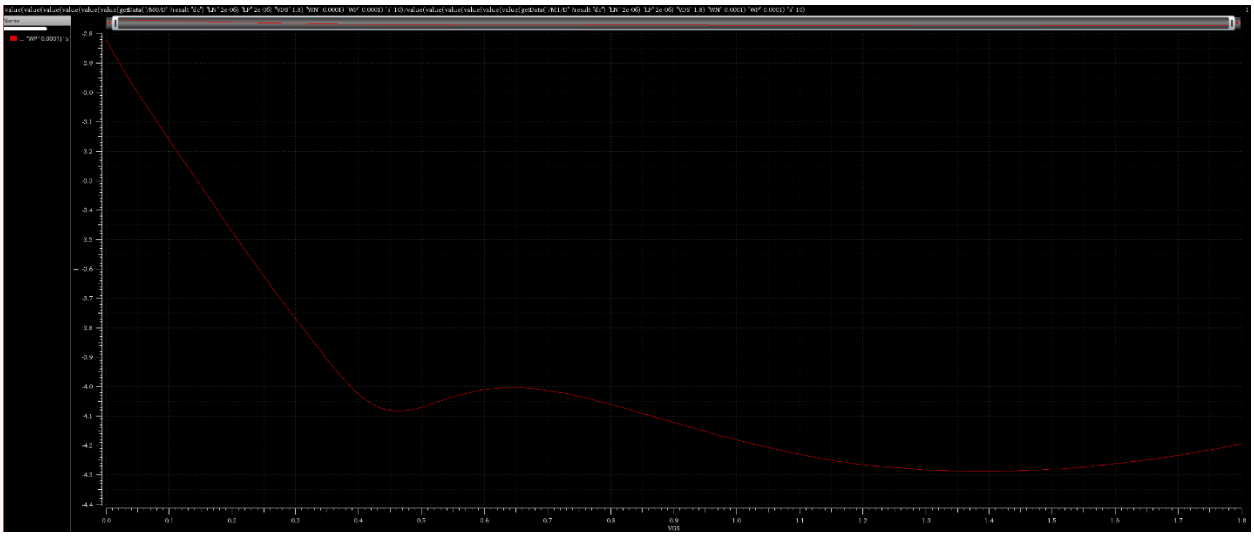
NOTES:

- 130nm technology is always higher in current
- Long channel has higher current
- NMOS current is always higher than PMOS



Note that the PMOS long channel has higher current than NMOS short channel (for 180nm).

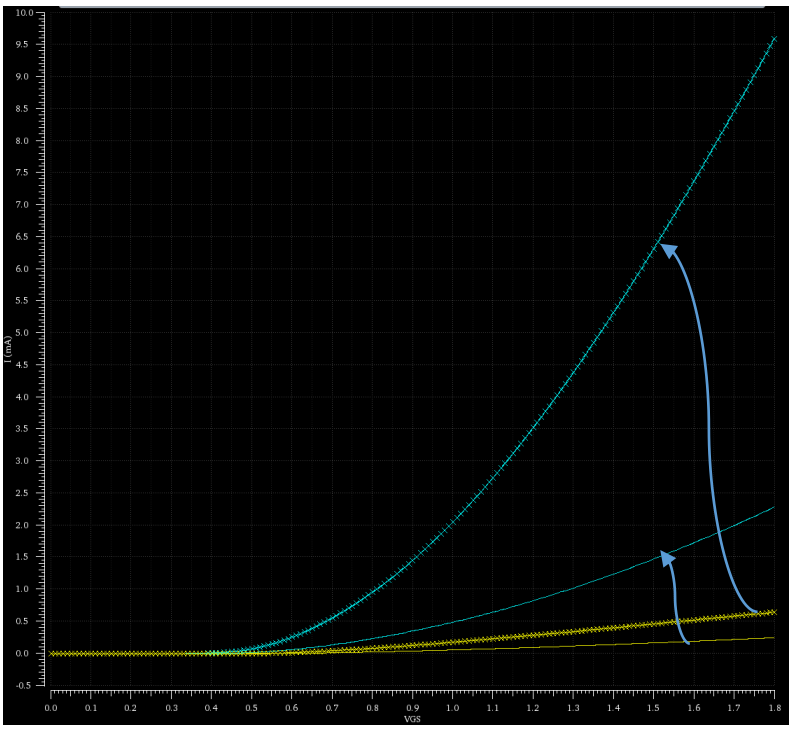
The ratio between NMOS and PMOS can be graphed



NOTE: the ratio between current of NMOS/ PMOS at 1.8V is **4.192**,
which means that the current of NMOS is roughly 4 times higher than that of PMOS.

ALSO it is noted that the **PMOS is LESS affected** by Short Channel Effects.

(THIS NEXT GRAPH IS FOR 180nm technology)



The difference between NMOS (short channel with symbol X-- YELLOW) and NMOS (long channel with symbol X-- CYAN) IS MUCH HIGHER THAN the difference between PMOS (short channel with no symbols -- YELLOW) and PMOS (long channel with no symbols -- CYAN).

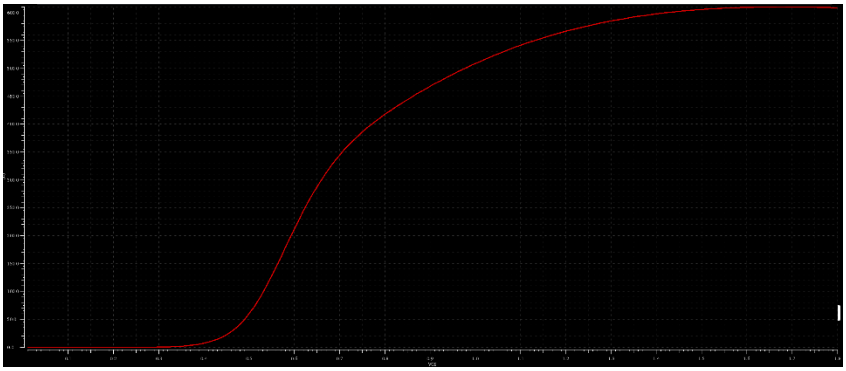
2. gm vs. VGS

1) Plot **gm vs. VGS** for NMOS device. Set **VDS = VDD**, and **VGS = 0: 10m: VDD**. Plot the results overlaid for the following:

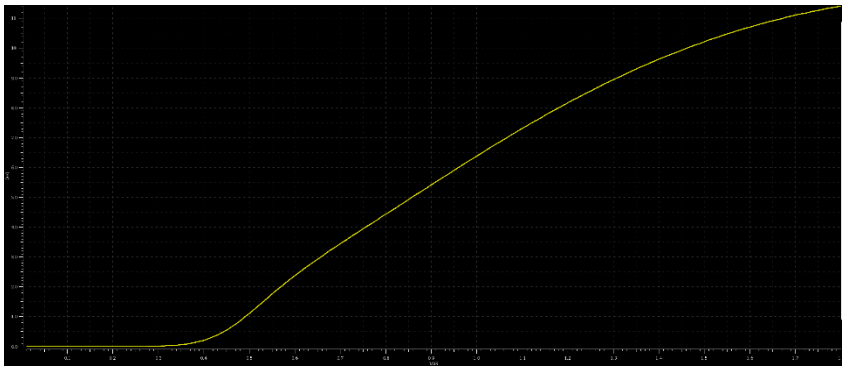
- Short channel device: **W = 1µm and L = 200nm**
- Long channel device: **W = 10µm and L = 2µm**.

Gm is the derivative of ID with respect to VGS. Using the Calculator we can graph $\frac{\partial I_D}{\partial V_{GS}}$. The results are as following:

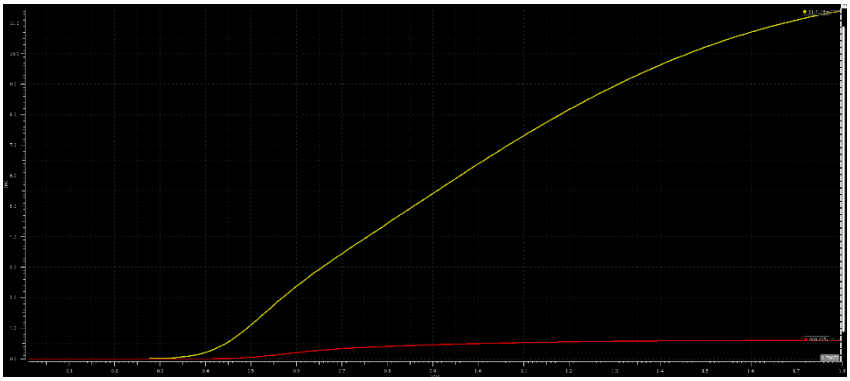
For Short channel in micro Siemens (uS): → max. 611uS



For Long channel in milli-Siemens (mS): → max. 11.5mS



Together for comparison:



2) Comment on the differences between short channel and long channel results.

- Does gm increase linearly? Why?
- Does gm saturate? Why?

➔ **Cadence Hint:** In order to save gm vs DC sweep variable, create an empty text file and write the following statement (without quotes): "save *:gm sigtype=dev". To save all OP point parameters for all transistors use (without quotes): "save *:oppoint sigtype=dev". Add this text file in adexl (Setup -> Model Libraries). You need to do this in every new test-bench whenever you need to save small signal parameters. [NOT in model libraries, but Simulation Files >> Definition Files.]

Gm doesn't increase linearly for both short and long channel, but it is worth noting that the long channel has much higher gm and looks like a more linear relation in certain parts (more linear than short channel).

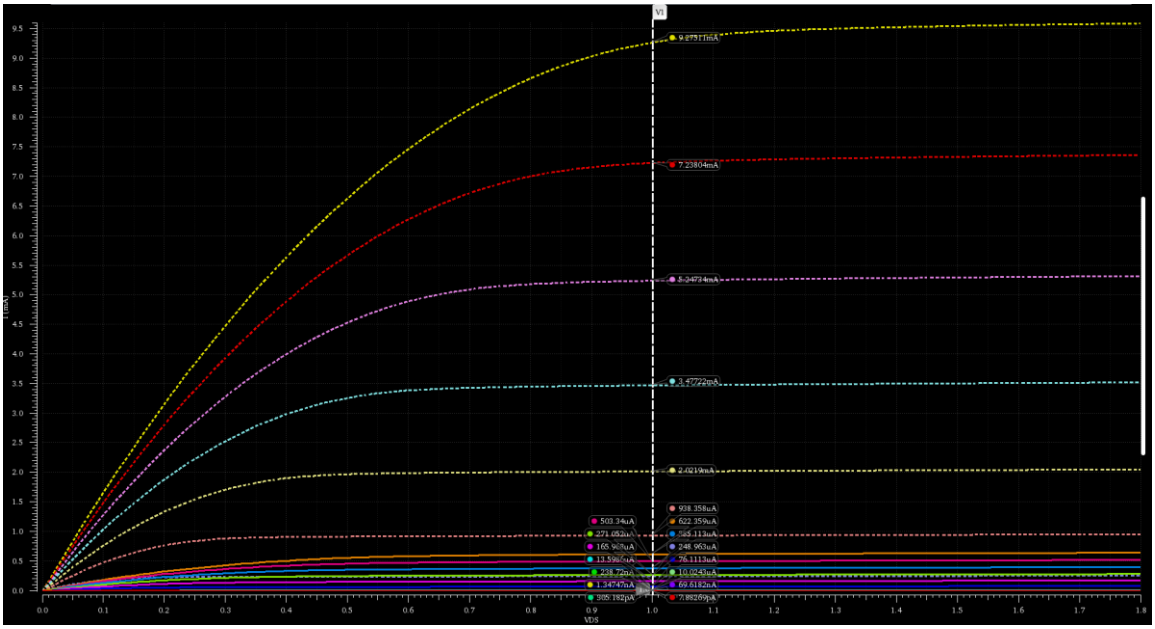
Gm saturates in both cases then starts to decrease a little at the end (as seen in short channel -- RED).

3. ID vs. VDS

1) Plot ID – VDS characteristics **for NMOS device**. Set **VDS = 0: 10m: VDD**, and **VGS = 0: 0.2: VDD** (nested sweep). Plot the results overlaid for the following:

- Short channel device: **W = 1µm and L = 200nm**
- Long channel device: **W = 10µm and L = 2µm**.

➔ **Cadence Hint:** In Mentor Eldo and Synopsys HSPICE you can do nested DC sweep (DC sweep with multiple variables). But in Cadence Virtuoso you can use only one DC sweep variable. Thus, you should use DC sweep for the variable with fine step, i.e., the primary variable (VDS in this case), and parametric sweep for the variable with coarse step, i.e., secondary variable (VGS in this case). Actually, Cadence simulation engine (Spectre) can run nested DC sweeps if you invoke it from the command prompt rather than the GUI.



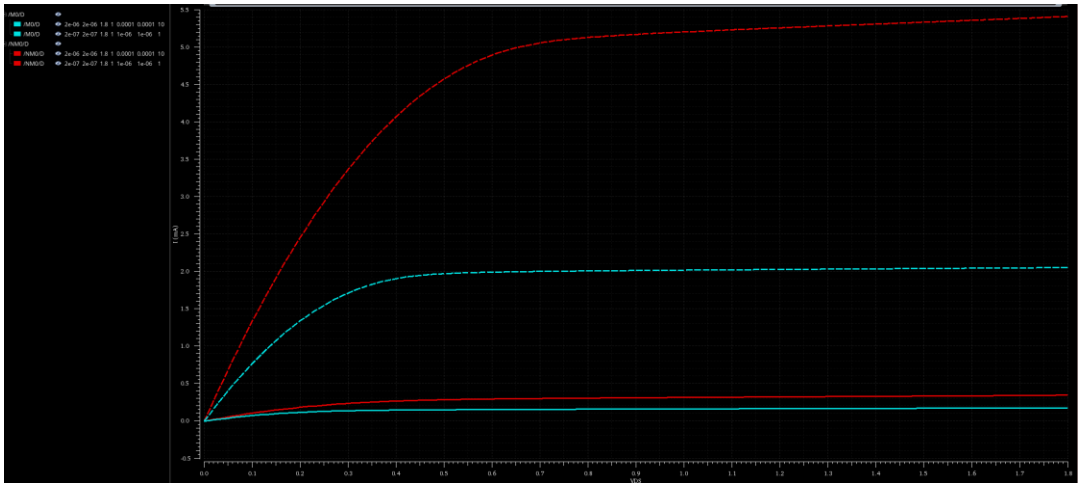
2) Comment on the differences between short channel and long channel results.

- Which one has higher current? Why?
- Which one has higher slope in the saturation region? Why?

DASHED: Long Channel (W = 10µm and L = 2µm).
SOLID: Short Channel (W = 1µm and L = 200nm).

Long channel has higher current for the same W/L. Because longer channel means less short channel effects. This means less velocity saturation, and less mobility degradation. Longer channel is a more ideal MOSFET that is more "square-law" like.

Short Channel has higher slope in saturation region (less r_o, less gate control over channel due to SCEs).



NOTE: the 130nm technology differ from the 180nm technology in more ways than just a less number. The fabrication process is intrinsically very different. This can be reflected in the PDK (Process Design Kit).

It is noted that in 130nm (red) the short channel (solid line) has much less current than the long channel although the same aspect ratio W/L (because of SCEs mainly – beyond the simplistic square law), in fact the relation is not linear or quadratic it's in between (alpha-law).

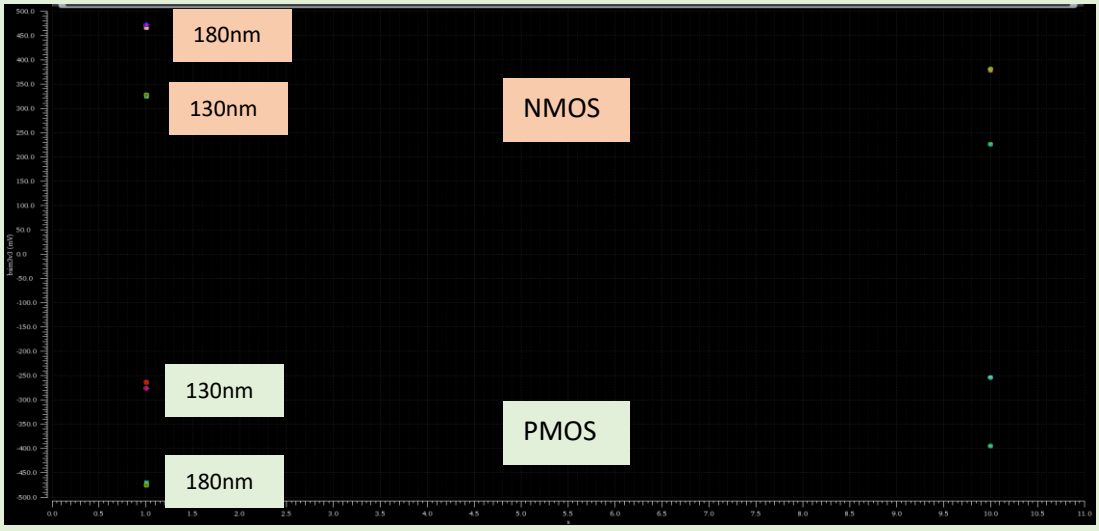
It is noted that in 180nm (cyan) the short channel (solid line) has also much less current than the long channel one for the same reason (SCEs).

Now let's make a more complicated comparison, for the same dimensions for the short channel (L: 200n and W: 1u) but different technologies we notice that the opposite happens. The less technology (130nm) has more current than its peer of the same dimensions but less technology node (180nm). One may only wonder WHY?
To my – very limited – knowledge, as we go down in technology nodes, fabrication process gets much more complex. Techniques of mobility enhancement, stress engineering, band gap engineering, the usage of high-k gate oxides, and many other methods are used to combat the complicated SCEs that – maybe – are of quantum nature which arise due to technology scaling down. These techniques are reflected in the PDK to give such observation (which is logical, that's why scaling down benefits digital design that depends on more current to get higher speeds but harm analog circuits that needs higher r_o to get higher gain). One can only search, ask, and learn more every day.

4. [Optional] gm and ro in Triode and Saturation

1) Plot **gm and ro vs. VDS** for NMOS device. Use **W = 10µm and L = 2µm**, **VDS = 0: 10m: VDD**, and **VGS ≈ VTH + 0.5V**.

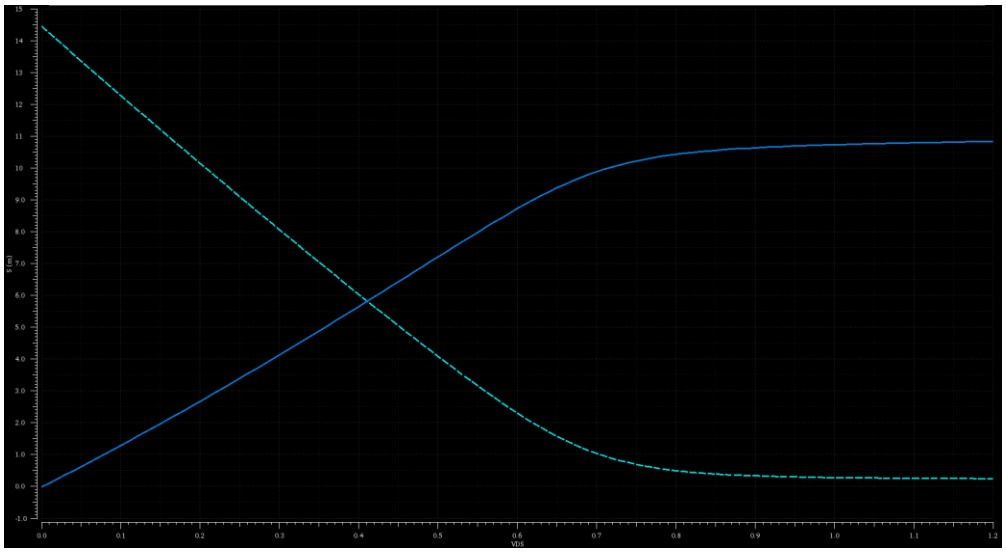
Hint: *You can get an estimate of VTH from the ID vs VGS characteristics, or you can print the operating point parameters of the transistor from DCOP/TRAN in* ***Pyxis*** *(my note: a mentor graphics tool not in cadence).*



Estimation of V_{th}	130nm		180nm	
	Short Channel	Long Channel	Short Channel	Long Channel
NMOS	330 mV	**470 mV**	225 mV	**380 mV**
PMOS	-275 mV	-475 mV	-250 mV	-390 mV

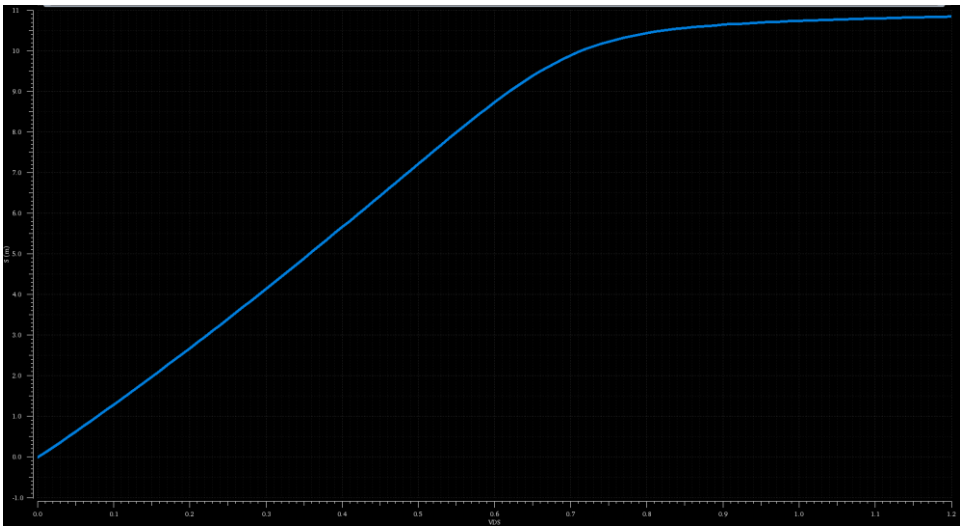
We will use NMOS, Long Channel, in 130nm technology. So Let VGS = 0.5 + VTH (which is 470mV) ≈ 1V.

gm and gds vs. VDS



2) Comment on the variation of **gm vs. VDS**.

- In the first part of the curve, is the relation linear? Why?
- Does gm saturate? Why?
- Where do you want to operate the transistor for analog amplifier applications? Why?



The first part of the curve, the relation is linear (low VDS), then saturates.

The gm is linear at low VDS, because $\boldsymbol{g_m} = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] = \boldsymbol{\mu C_{ox} \frac{W}{L} V_{DS}}$.
The channel is not pinched off, Drain current depends linearly on VDS

The gm saturates at high VDS, due to the pinch off and MOSFET entering saturation region. Notice that gm no longer depends on VDS. $\boldsymbol{g_m} = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH})^2 \right] = \boldsymbol{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$

The transistor for analog amplifier applications is preferred to be operated a little deep into saturation (after the edge of saturation). Because here is the highest intrinsic gain gmro, and the gm is stable.

3) Comment on the variation of **ro vs. VDS**.

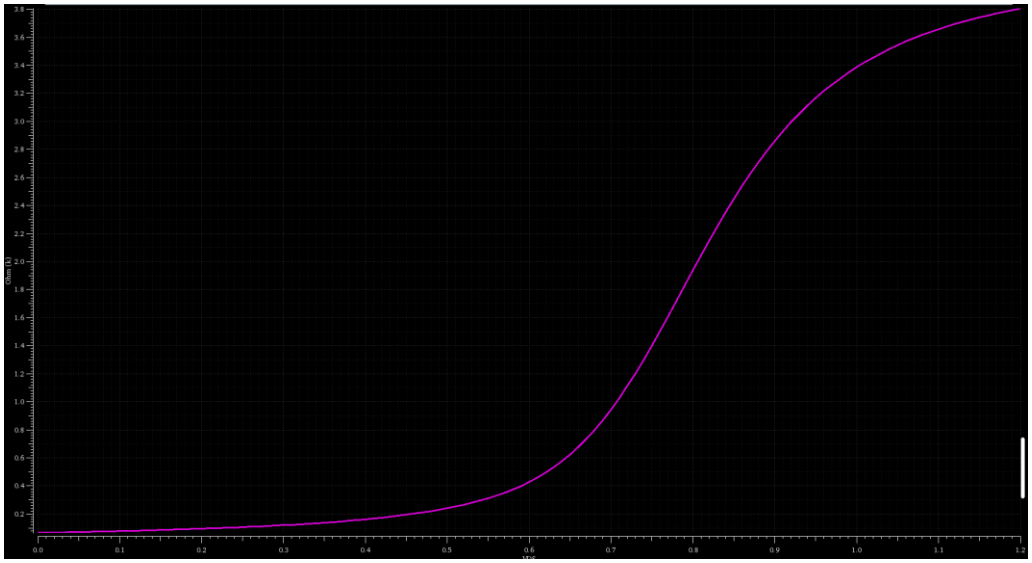
- Does ro saturate just after the transistor enters saturation similar to gm? Why?
- Does ro increase if the transistor is biased more into saturation?
- Should we operate the transistor at the edge of saturation?
- Where do you want to operate the transistor for analog amplifier applications? Why?

Not in the same way ro saturate but a while after the transistor enters saturation not like gm.

ro increase as the transistor is biased more into saturation but gm saturates then decrease so gmro peaks then decreases.

If we require high ro and higher gain, We SHOULD operate the transistor a little deep into saturation not at the edge of saturation (Vov=0.1→0.2)

The transistor for analog amplifier applications is preferred to be operated a little deep into saturation. Because here is the highest intrinsic gain gmro.



Lab Summary

- *In Part 1 I learned*
  - How to run transient simulations.
  - How to run ac-analysis simulations.
  - How to run pole-zero simulations.
  - How to run parametric sweeps.

- *In Part 2 I learned*
  - How to plot the transistors I/V characteristics using DC analysis.
  - How to plot the transistors I/V characteristics using parametric sweeps.
  - The difference in transistor characteristics between an NMOS and a PMOS transistor.
  - The difference in transistor characteristics between a short-channel and a long-channel MOSFET.
  - How the g_m of the transistor behaves vs V_{GS}.
  - How the g_m and r_o of the transistor behave in triode and in saturation.

Acknowledgements

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[END OF LAB]

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