Lab 02
Common Source Amplifier

Analog IC Design Course – Cadence Tools (Self Study)

Student Information

Name	Kerollos Saad Thomas Shokralla	كيرُلُسْ سَعْد تُومَاس شُكرَالله
Email	2501030@eng.asu.edu.eg	
Date	*January **10**, 20**26***	

Under Guidance and Help of My More Experienced Friends

Labs Provided by **Dr. Hesham Omran** via Master-Micro.com

Thanks to everyone who has helped me,
I pledge to help others as well.

Done during my **Post Graduate MSc. Program** in
Electronics and Electrical Communication Engineering
at the **Faculty of Engineering – Ain Shams University**

Lab 02: Common Source Amplifier

Intended Learning Objectives:[1]

In this lab[2] you will:

- Design and simulate a common-source amplifier.
- Learn how to generate and use design charts.
- Investigate gain non-linearity; the variation of the gain with input signal amplitude.
- Study the maximum gain attainable for a resistive-loaded CS amplifier and the effect of supply scaling on max gain.
- Learn how to use feedback to reduce non-linearity (gain linearization).

Part 1: Sizing Chart

1) We would like to design a resistive loaded CS amplifier that meets the specifications below. The design process involves selecting the sizing of the transistor (W and L), the bias point (V_{GS}), and the resistive load (R_D).

Spec	0.13um CMOS	0.18um CMOS
DC Gain	-5	-8
Supply	$1.2\ V$	$1.8\ V$
Current consumption	$100\ \mu A$	$100\ \mu A$

I decided – in this lab – to use the umc13mmrf PDK (Process Design Kit), which is a 130nm process technology, instead of the ee214b.sp file. The reason is a matter of preference.

2) The first design decision is to choose L. Since there is no spec on bandwidth (speed), we may choose a relatively long L to provide large r_o and avoid short channel effects. Note that r_o appears in parallel with R_D. Assume we will choose $L = 2\mu m$.

$$Put\ L\ =\ 2\ \mu m$$

3) We can show that the gain is given by:

$$|Av| \approx\ g_m R_D\ = \frac{2I_D}{V_{ov}} \times R_D\ = \frac{2V_{R_D}}{V_{ov}}$$

[1] *COLOR CODES:* Orange (steps) -- Blue (output) -- Green (comments / observations) – White (equations).

[2] Cadence Virtuoso software on a Linux® Debian 8 Virtual Machine is used.

Interestingly, the gain only depends on the voltage drop across V_{R_D} and V_{ov}. However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula:

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$

However, for a real MOSFET they are not equal. The actual gain is now given by:

$$|Av| \approx \frac{2V_{R_D}}{V^*}$$

This is more like an observation than a step to follow.

The noted idea is that the real MOSFET ≠ Square-Law. Hence, the famous V-star and its relative the g_m/I_D analog design methods. Both are famous ways to design analog circuits based on more accurate and physics-aware simulation data not just the simple square law.

It is rumored that the V-star method is very well known and practiced by those who graduated from Stanford University, while g_m/I_D is practiced by UC Berkley. But I found no proof of that statement.

4) The choice of V_{R_D} is constrained by the output signal swing. Since we usually want to provide large output swing, we choose the common-mode (CM) output level (DC output level) around $V_{DD}/2$. Thus, although increasing V_{R_D} increases the gain, but the choice is limited by the supply voltage which is aggressively scaled down in modern technologies. That's one reason it is difficult to get high gain in modern technologies. Assuming CM output = $V_{R_D} = V_{DD}/2$ and given the DC bias current, determine the value of R_D. Again, it is interesting to note that although the gain equals $g_m R_D$, it actually does not depend on R_D itself, but on the voltage drop across it, i.e., the product $I_D \times R_D$.

"The choice of $\boldsymbol{V_{R_D}}$ is constrained by the output signal swing"

Very interesting statement. Indeed as the drop on the resistive load $\boldsymbol{V_{R_D}}$ increase, the output voltage upper ceil must decrease (voltage divider), this decreases the maximum signal swing. The minimum signal swing will be related to the overdrive voltage V_{ov} and the drop on the degeneration resistance R_S , if present.

$$\because I_D = 100\ \mu A$$
$$\therefore I_D \times R_D = V_{R_D} = \frac{V_{DD}}{2} = \frac{1.2\ V}{2} = 0.6\ V$$
$$\therefore R_D = \frac{0.6\ V}{100\ \mu A} = 6\ k\Omega$$

5) Given A_v and V_{R_D}, calculate the required V^* (again note that $V^* \neq V_{ov}$ for a real MOSFET). Let's name this value V_Q^*.

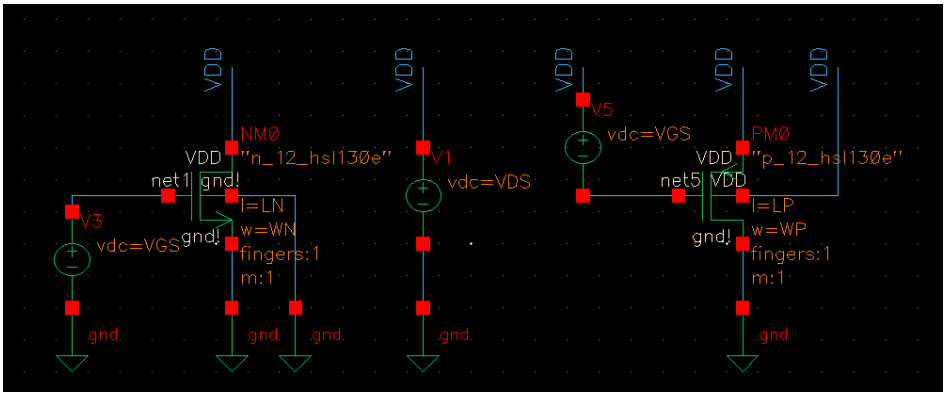
$$\because |Av| \approx g_m R_D = \frac{2I_D}{V^*} \times R_D = \frac{2V_{R_D}}{V^*} \approx \frac{1.2\text{ V}}{V^*} \approx 5\ V/V$$

$$\therefore V_Q^* = \frac{1.2\ V}{5\ V/V} = \frac{6}{25} V = 0.24\ V$$

6) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation.

Create a test-bench for NMOS and PMOS characterization (we will use the PMOS later in Part 2 of this lab). Use $\boldsymbol{W = 10\mu m}$ (we will understand why shortly) and $\boldsymbol{L = 2\mu m}$ (the same L that we chose before).

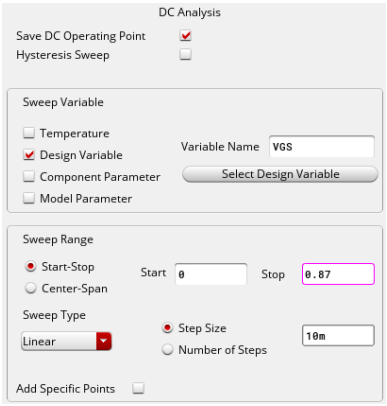
$$Put\ \boldsymbol{W = 10\ \mu m}\ and\ \boldsymbol{L = 2\ \mu m}$$



Remember that we estimated VTH value from DCOP in Lab 1 Part 2 as following (just as a guide – we can sweep till **1.2 V** anyways):

Estimation of V_{th}	130nm	
	Short Channel	Long Channel
NMOS	330 mV	**470 mV**
PMOS	-275 mV	-475 mV

For L = 2um (considered Long Channel), then **V_{th} = 470 mV**



7) Sweep **VGS** from $0\ to\ \approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.

$$V_{TH} + 0.4V \approx 0.87\ V, \qquad V_{DD} = 1.2\ V, \qquad V_{DS} = 0.6\ V$$

8) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov}. Export the expressions to ADE XL.

The Blue Curve is $V_{ov} = V_{GS} - V_{TH}$

(value(v("/net1" ?result "dc") "WP" 1e-05) - pv("NM0" "vth" ?result "dcOpInfo"))

```
(v("NM0:vgs" ?result "dc") - v("NM0:vth" ?result "dc"))
```

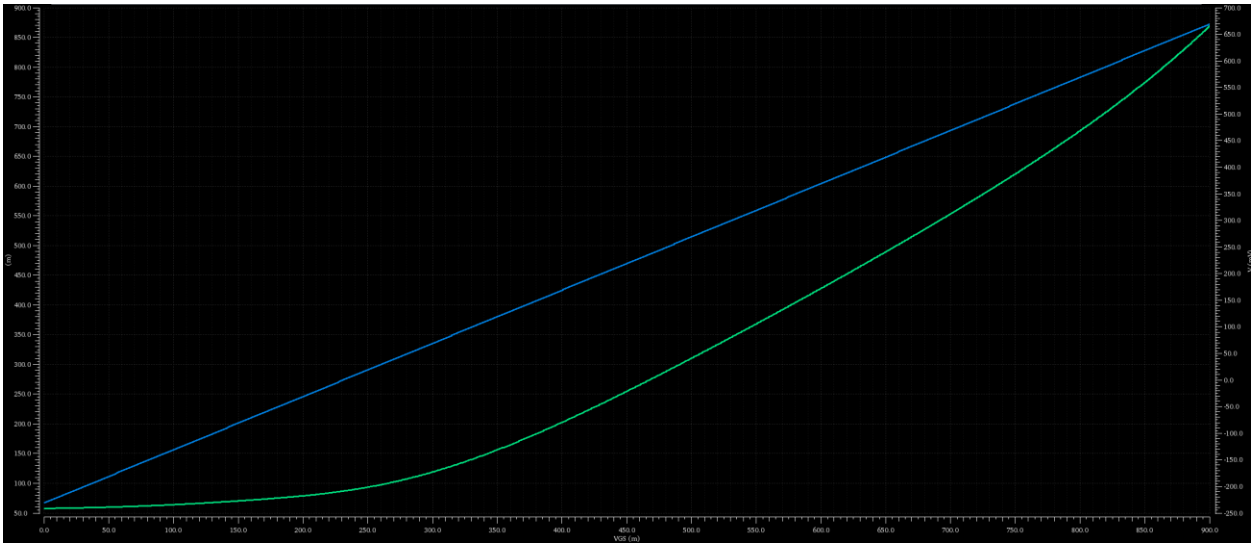
The Green Curve is $V^* = 2I_D/g_m$

((2 * value(i("/NM0/D" ?result "dc" ?resultsDir "./simulation/tutorial_CS/CS_tb/adexl/results/data/Interactive.1/psf/tutorial_CS:CS_tb:1/psf") "WP" 1e-05)) / deriv(value(i("/NM0/D" ?result "dc") "WP" 1e-05)))

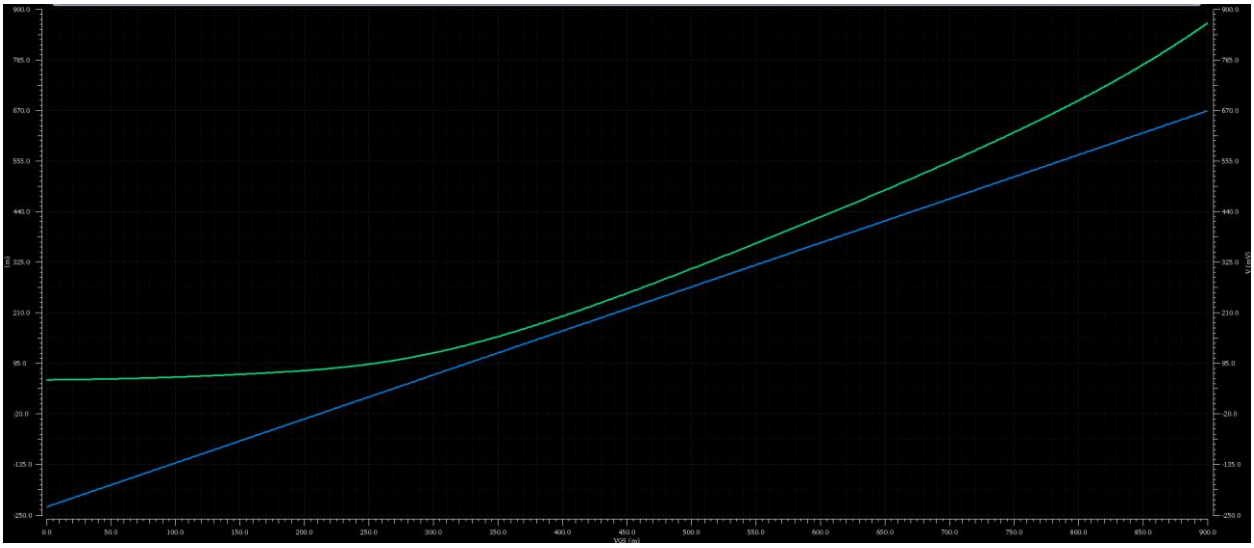
```
(2 / (getData("NM0:gm" ?result "dc") / getData("NM0:id" ?result "dc")))
```

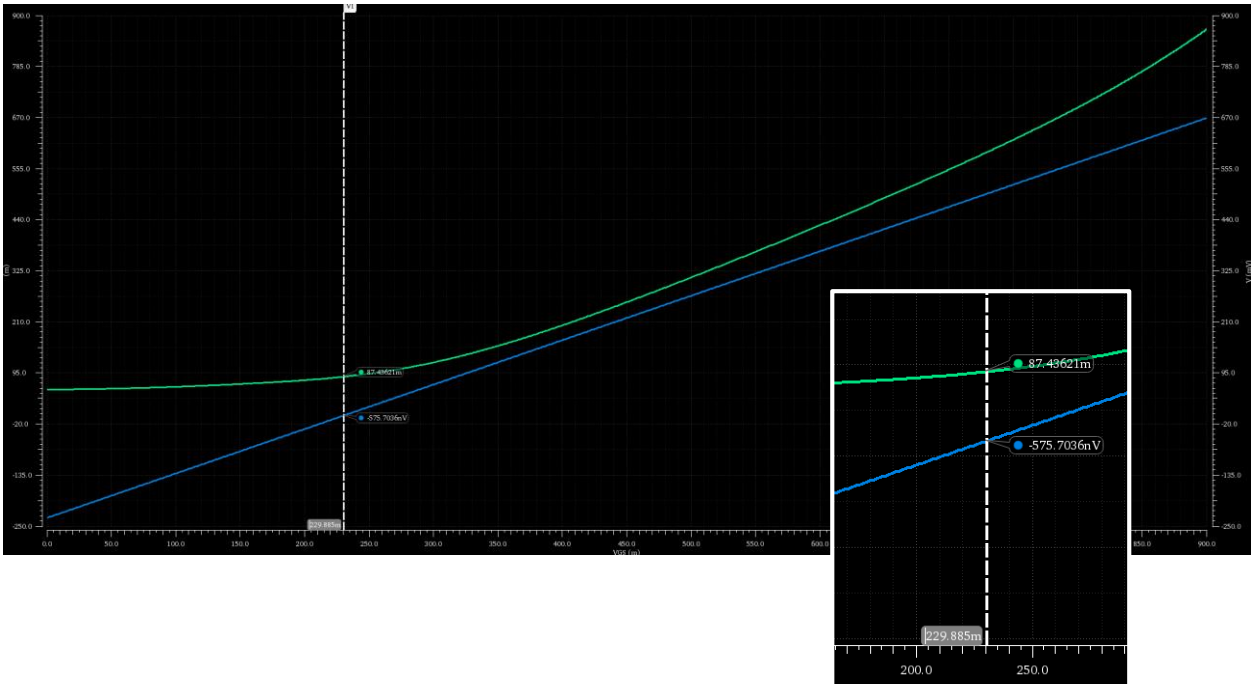
The difference is that V^* takes a lot of factors into consideration, unlike the simple V_{ov} from square law.

9) Plot V^* and V_{ov} overlaid vs. V_{GS}. Make sure the y-axis of both curves has the same range. You will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large V_{ov}: velocity saturation and mobility degradation) or weak inversion (near-threshold and sub-threshold operation) the behavior is quite far from the square-law (although we are using L = 2 μm).



After adjusting the y-axes ranges to be the same (-250mv to 900mv) and x-axis is not changed (0 to 0.9V).





At threshold, $\boldsymbol{V_{ov}} \approx 0$ but $\boldsymbol{V^* = 87.43\ mV}$

At near threshold and sub-threshold the difference is drastic. The $\boldsymbol{V^*}$ method is more accurate and more similar to practice than the simple $\boldsymbol{V_{ov}}$ from square-law.

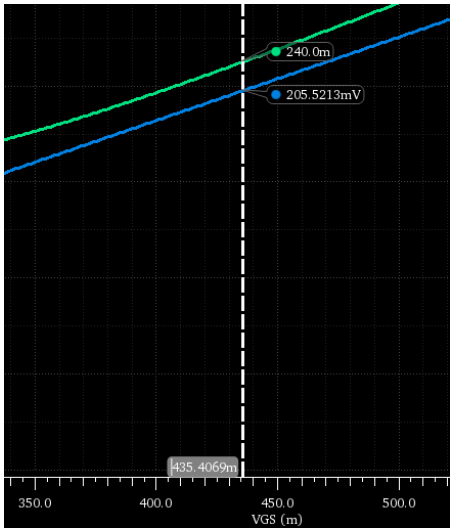
10) On the V^* *and* V_{ov} chart locate the point at which $V^* = V_Q^*$. Find the corresponding V_{ov_Q} and V_{GS_Q}.

Remember that we chose $V_Q^* = \frac{1.2\,V}{5\,V/V} = \frac{6}{25}V = 0.24\,V$,
so we can achieve the required gain (5 V/V)

$$V^* = V_Q^* = 240\ mV$$

$$V_{ov} = V_{ov_Q} = 205.52\ mV$$

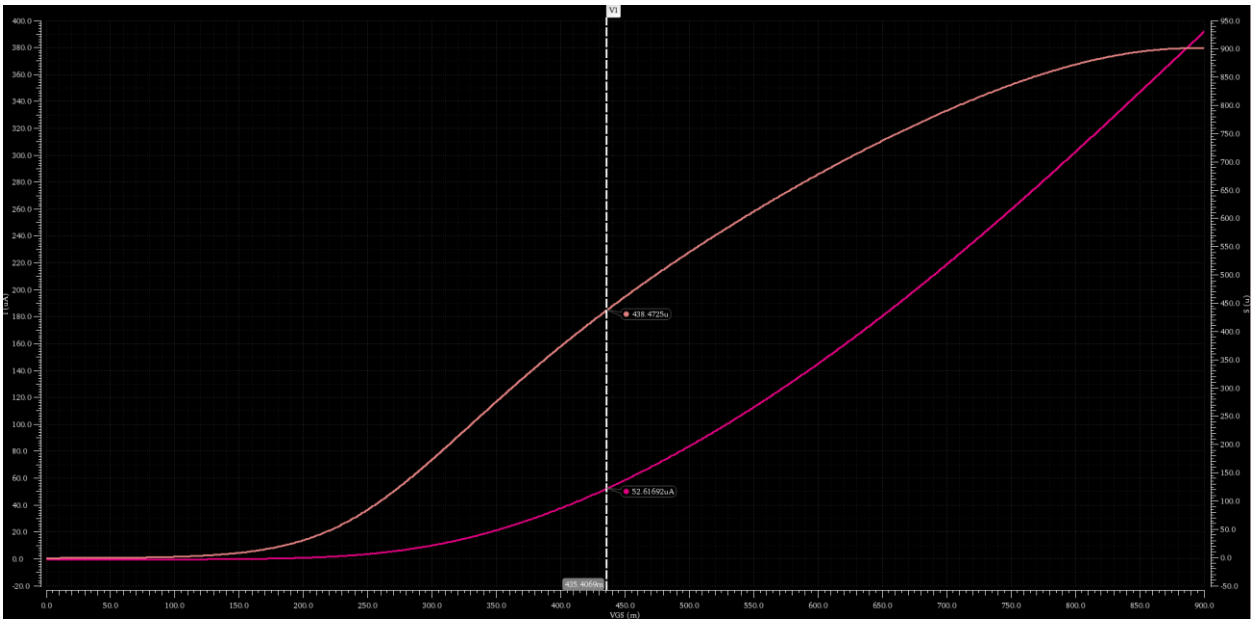
It is noted that $V_{GS} = V_{GS_Q} = 435.4069\ mV$



11) Plot I_D, g_m, *and* g_{ds} vs. V_{GS}. Find their values at V_{GS_Q}. Let's name these values I_{DX}, g_{mX}, *and* g_{dsX}.

$I_{DX} = 52.61692\ \mu A$
$g_{mX} = 438.4725\ \mu S$
$g_{dsX} = 4.5\ \mu S$
$r_o = 222.2\ k\Omega$

vgs	435.4m
ID_n	
vth_n	229.9m
id_n	52.62u
gm_n	438.5u
gds_n	4.5u
Vov_n	
(2ID/Gm)_n	
ro_n	222.2k

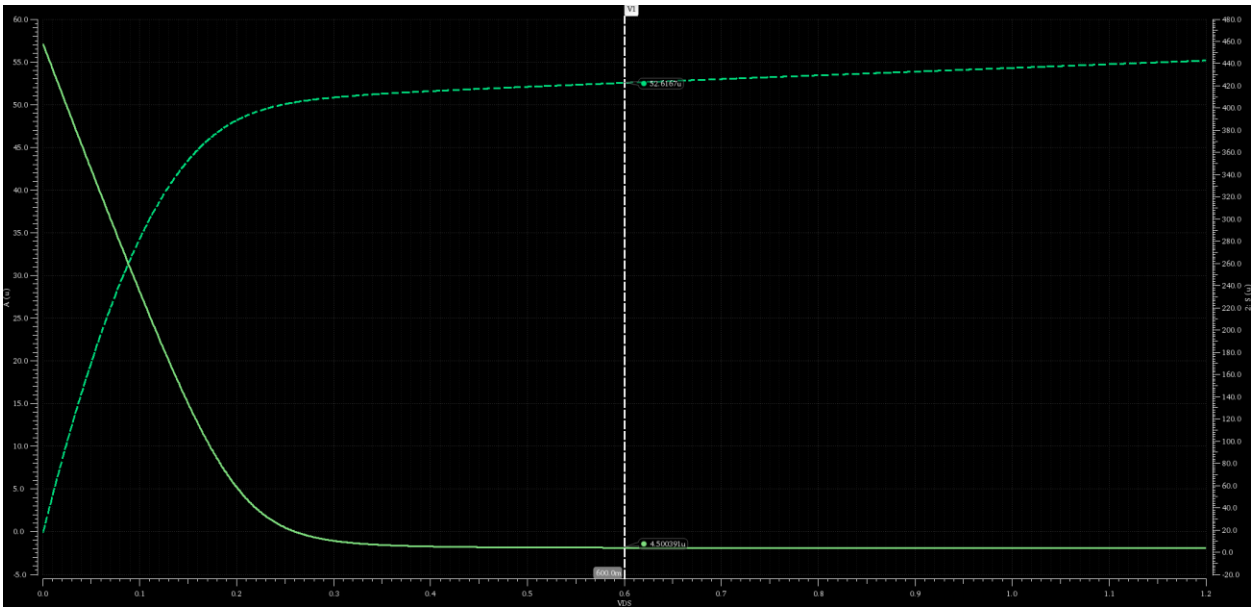


$$\because V_{GS_Q} = 435.4069\, mV$$

$\therefore$The current and trans-conductance can both be plotted vs. V_{GS}.
However, $\boldsymbol{g_{ds}}$ is the slope of $\boldsymbol{I_D\ vs.V_{DS}}$

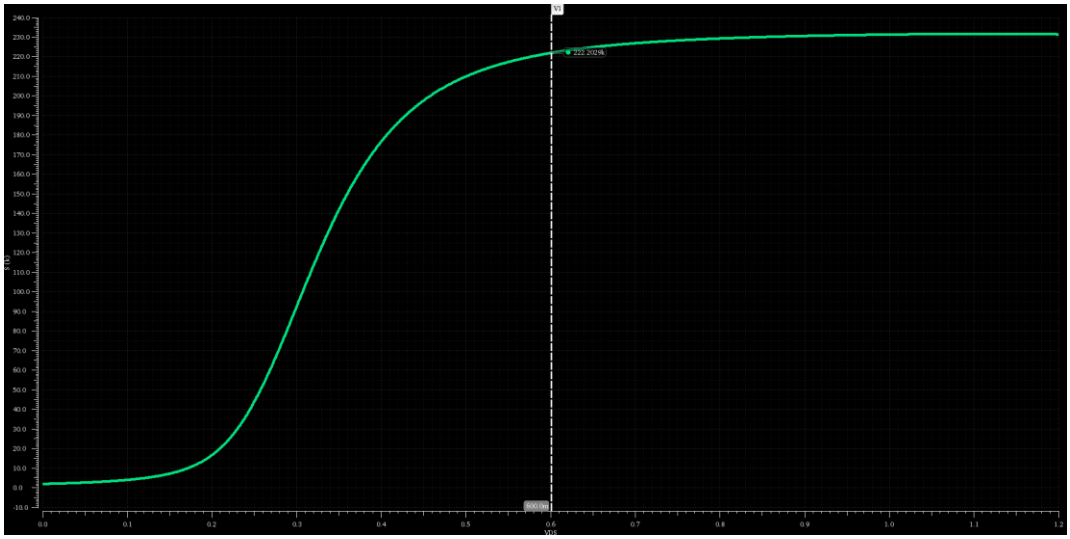
$$\because V_{DS} = V_{DD} \,/\, 2 = 0.6\, V,$$
$$\therefore \boldsymbol{g_{dsX}} \,|_{@\, V_{GS} = 435.4069\, mV, V_{DS} = 0.6\, V} = \mathbf{4.500391\ \mu S}.$$

[The gds curve can be plotted by taking derivative of ID vs. VDS at VGS = 435.4 mV, and it will result in the following curve, yielding the same gds answer at VDS = 0.6 V]



$I_D = 52.6167\ \mu A$. Which is the same (but with measurement errors) to the $I_D\ vs.\ V_{GS}$ curve.

The next curve is the reciprocal of the previous curve, which is the $r_o = 222.2029\ k\Omega$.



A bonus (non-required graph in lab), but still very essential to the understanding of the MOSFET characteristics.

12) Now back to the assumption that we made that W = 10μm. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 100\mu A$ as given in the specs. Calculate W as shown below.

W	$\boldsymbol{I_D}$
10 µm	I_{DX} @ V_Q^* (from the chart)
?	$I_{DQ} = 100\ \mu A$ (from the specs)

$$W = \frac{10\ \mu m \times 100\ \mu A}{I_{DX} \text{ @ } V_Q^* \text{ (from the chart)}}$$

$$W = \frac{10\ \mu m \times 100\ \mu A}{52.62\ \mu A} = 19.0041\ \mu m \approx 20\ \mu m$$

13) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as $\boldsymbol{V_{ov}}$ is constant. On the other hand, $r_o = 1/g_{ds}$ is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross multiplication) and double check that $A_v = -g_m\ (R_D \,||\, r_o)$ meet the required gain spec.

$\boldsymbol{g_{mQ}}$	W @ constant $\boldsymbol{V_{ov}}$
$\mathbf{438.4725\ \mu S}$	$10\ \mu m$
?	$20\ \mu m$

$$\boldsymbol{g_{mQ}} = \frac{\mathbf{438.4725\ \mu S} \times 20\ \mu m}{10\ \mu m} = 876.945\ \mu S$$

$\boldsymbol{g_{dsQ}}$	W ($\boldsymbol{I_D}$)
$\mathbf{4.5\ \mu S}$	$10\ \mu m$
?	$20\ \mu m$

$$\boldsymbol{g_{dsQ}} = \frac{\mathbf{4.5\ \mu S} \times 20\ \mu m}{10\ \mu m} = 9\ \mu S$$

$$r_o = \frac{1}{9\ \mu S} \approx 111.1\ k\Omega$$

Note: $g_m = 438.4725\ \mu S \rightarrow\ g_m = 876.945\ \mu S$
Directly proportional to W (Doubled)

$r_o = 222.2\ k\Omega \rightarrow r_o \approx 111.1\ k\Omega$
Inversely proportional to W (Halved)

REVIEW ON OUR FINAL PARAMETERS:

$$\therefore L = 2\ \mu m, W = 20\ \mu m, V_{DS} = 0.6\ V,$$

$$\boldsymbol{V^* = V_Q^* = 240\ mV}$$
$$\boldsymbol{V_{ov} = V_{ov_Q} = 205.52\ mV}$$

$$V_{GS} = V_{ov} + V_{th} = 435.4069\ mV, \quad V_{th} = 230\ mV$$
$$\therefore g_m = 876.945\ \mu S, \quad g_{ds} = 9\ \mu S, \quad r_o = 111.1\ k\Omega$$

Double-checking that: ($\because R_D = 6\ k\Omega$)

$$\boldsymbol{A_v} = -g_m\ (\boldsymbol{R_D} \,||\, r_o) = -(876.945\ \mu S)(\mathbf{6\ k\Omega} \,||\, 111.1\ k\Omega) = -(876.945\ \mu S)(5692.6\ \Omega) = \mathbf{-4.992}$$

If it is necessary to be higher than 5 we can increase R_D a little (tradeoff with output swing).

$$A_v = -g_m\,(\boldsymbol{R_D} \,||\, r_o) = -(876.945\ \mu S)(\boldsymbol{R_D} \,||\, 111.1\ k\Omega) = -5$$

$$A_v = -g_m \left(\frac{\boldsymbol{R_D} \times r_o}{\boldsymbol{R_D} + r_o}\right) = -(876.945\ \mu S)\left(\frac{\boldsymbol{R_D} \times 111.1\ k\Omega}{\boldsymbol{R_D} + 111.1\ k\Omega}\right) = -5$$

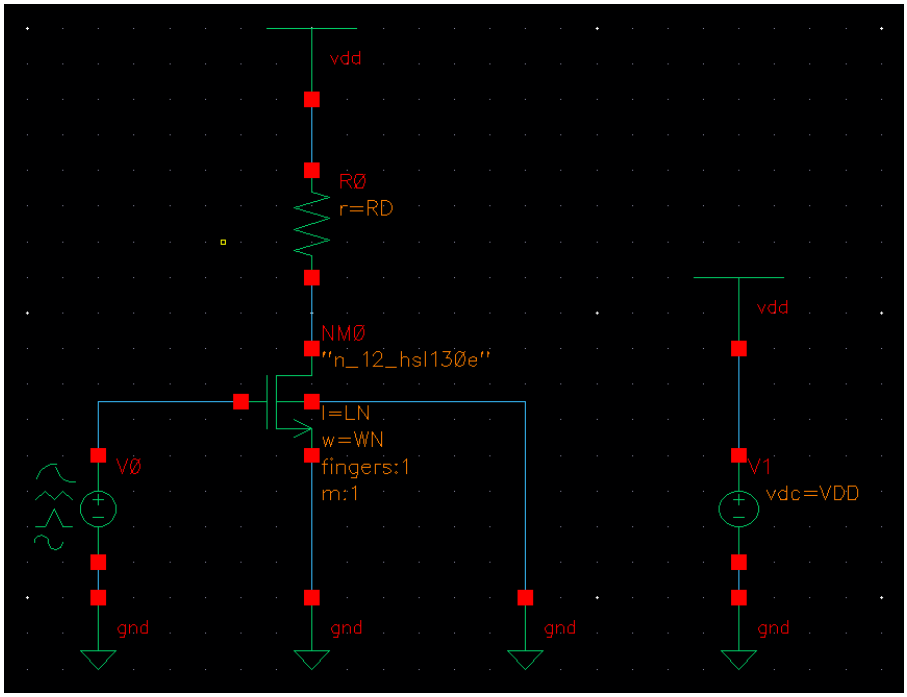
$$\therefore \boldsymbol{R_D} \geq 6010.045\ \Omega$$

$$Let\ R_D = 6.02\ k\Omega, \qquad \therefore A_v = -5.007$$

END OF SIZING AND DESIGN

Part 2: CS Amplifier

1. OP and AC Analysis



1) Create a test-bench for the resistive loaded CS amplifier using $V_{GSQ}, R_D, L,\ and\ W$ that you got from the previous part.

Review On Our Chosen Specs From Part 1

$\boldsymbol{V_{GSQ} = 435.4069mV}$	$\boldsymbol{V_{DD} = 1.2\ V}$	$\boldsymbol{V_{DS} = 0.6\ V}$	$\boldsymbol{V_Q^* = 240\ mV}$
$\boldsymbol{R_D = 6\ k\Omega}$	$L = 2\ \mu m, W = 20\ \mu m$	$\boldsymbol{A_v = -4.992}$	$\boldsymbol{V_{ov_Q} = 205.52\ mV}$
$\therefore g_m = 876.945\ \mu S$	$g_{ds} = 9\ \mu S$	$r_o = 111.1\ k\Omega$	

2) Simulate the **DC OP**. Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part 1. Since we used chart-based design, the results should agree well.

➔ **Cadence Hint:** The "region" meaning is as follows: (0 cut-off, 1 triode, 2 sat, 3 subth, and **4 breakdown**)

Simulator output:

$L = 2\ \mu m, W = 20\ \mu m$

$\boldsymbol{R_D = 6\ k\Omega}$

Output	Nominal
NM0:vgs	435.4m
NM0:vds	559.7m
NM0:vdsat	212.1m
NM0:gm	883.6u
NM0:gmb	119.1u
NM0:vth	228.4m
NM0:id	106.7u
NM0:rout	107.3k
NM0:gds	9.321u
ro_n	107.3k
Avo	-5.021

Part 1 output

$\boldsymbol{V_{GSQ} = 435.4069mV}$

$L = 2\ \mu m, W = 20\ \mu m$

$\boldsymbol{V_{DS} = 0.6\ V}$

$\boldsymbol{V_{ov_Q} = 205.52\ mV}$

$\boldsymbol{V_Q^* = 240\ mV}$

$\therefore g_m = 876.945\ \mu S$

$g_{ds} = 9\ \mu S$

$r_o = 111.1\ k\Omega$

$\boldsymbol{R_D = 6\ k\Omega}$

$\boldsymbol{A_v = -4.992}$

3) Compare r_o and R_D. Is the assumption of ignoring r_o justified in this case? Do you expect the error to remain the same if we use min L?

	Simulator	Part 1 (hand Analysis)	Minimum L = 130nm
Dimensions	$L = 2\mu m, W = 20\mu m$	$L = 2\mu m, W = 20\mu m$	$\boldsymbol{L = min}, W = 20\mu m$
Drain R	$R_D = 6\ k\Omega$	$R_D = 6\ k\Omega$	$R_D = 6\ k\Omega$
Drain-Source R	$r_o = 107.3\ k\Omega$	$r_o = 111.1\ k\Omega$	$r_o = 359.5\ \Omega$
$(R_D \mid\mid r_o)$	$5.6822\ k\Omega$	$5.6925\ k\Omega$	$339.17\ \Omega$
Ignore r_o ?	*Possible*	*Possible*	*Do NOT ignore*

The previous comparison was not necessary because it is intuitive. But I chose to prove it for clarity. **Error is negligible except at minimum L.**

It is also interesting that just decreasing L to its minimum (130 nm for this PDK), will result in a very bad design for an amplifier, naturally.

Interestingly noted, by just decreasing L and leaving every other parameter unchanged, will result in:

- Higher **id**, higher **vth**, much higher **gds** (very low **ro**), lower **gm**, lower **vds**, and a very bad **gain** for an amplifier (-0.6 dB).

Output	Nominal
NM0:vgs	435.4m
NM0:vds	46.57m
NM0:vdsat	87.77m
NM0:gm	2.563m
NM0:gmb	266.4u
NM0:vth	361.1m
NM0:id	192.2u
NM0:rout	359.5
NM0:gds	2.782m
ro_n	359.5
Avo	-869.3m

4) Calculate the intrinsic gain $g_m r_o$ of the transistor.

$$g_m r_o = 883.6046\ \mu S \times 107.3\ k\Omega = 94.79$$

5) Calculate the amplifier gain analytically. What is the relation (≪, ≫) between the amplifier gain and the intrinsic gain?

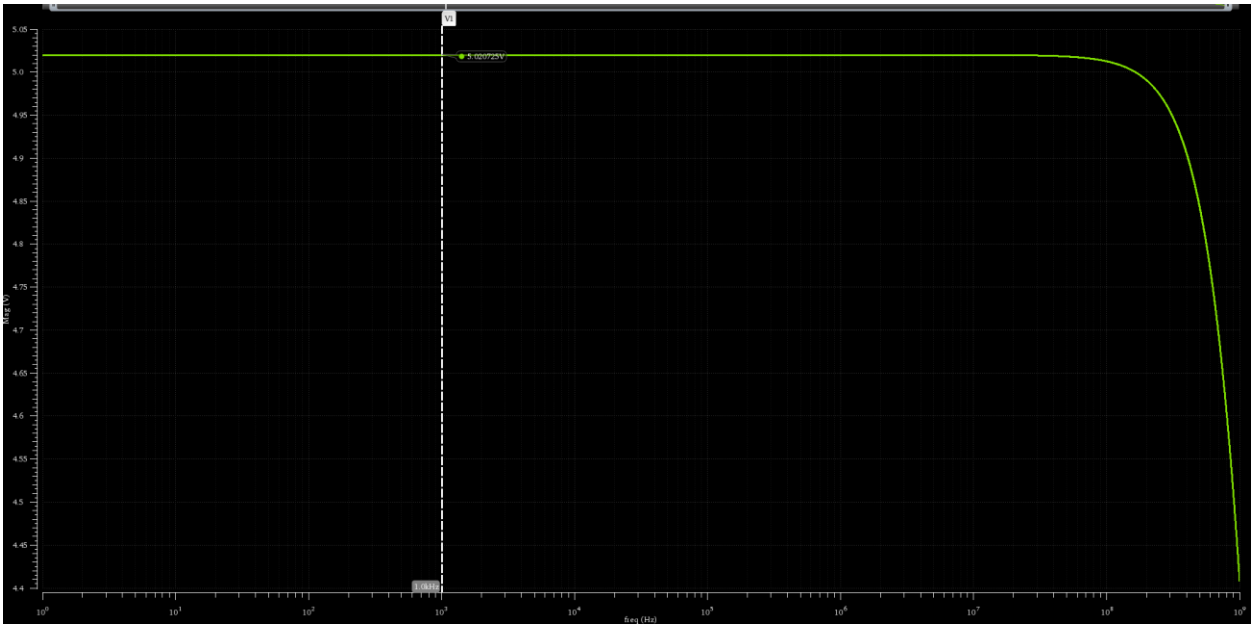
$$\boldsymbol{A_v} = -g_m\ (\boldsymbol{R_D} \,||\, r_o) = -(883.6046\ \mu S)(\mathbf{6\ k\Omega}\ ||107.3\ k\Omega)$$
$$= -(876.945\ \mu S)(5.6822\ k\Omega) = \mathbf{-5.02087}$$

$$\boldsymbol{g_m r_o} = 883.6046\ \mu S \times 107.3\ k\Omega = \mathbf{94.79}$$

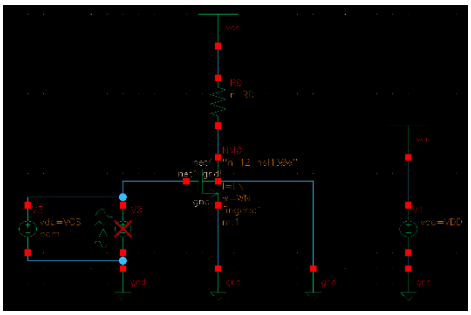
amplifier gain ≪ intrinsic gain

6) Create a new simulation configuration and run **AC analysis** (from 1Hz to 1GHz). Report the **gain vs. frequency**. Annotate the DC gain and make sure it meets the spec.

$$|\boldsymbol{A_v}| = \mathbf{5.0207}$$



It is noted from ac analysis that the DC gain meets the specifications.



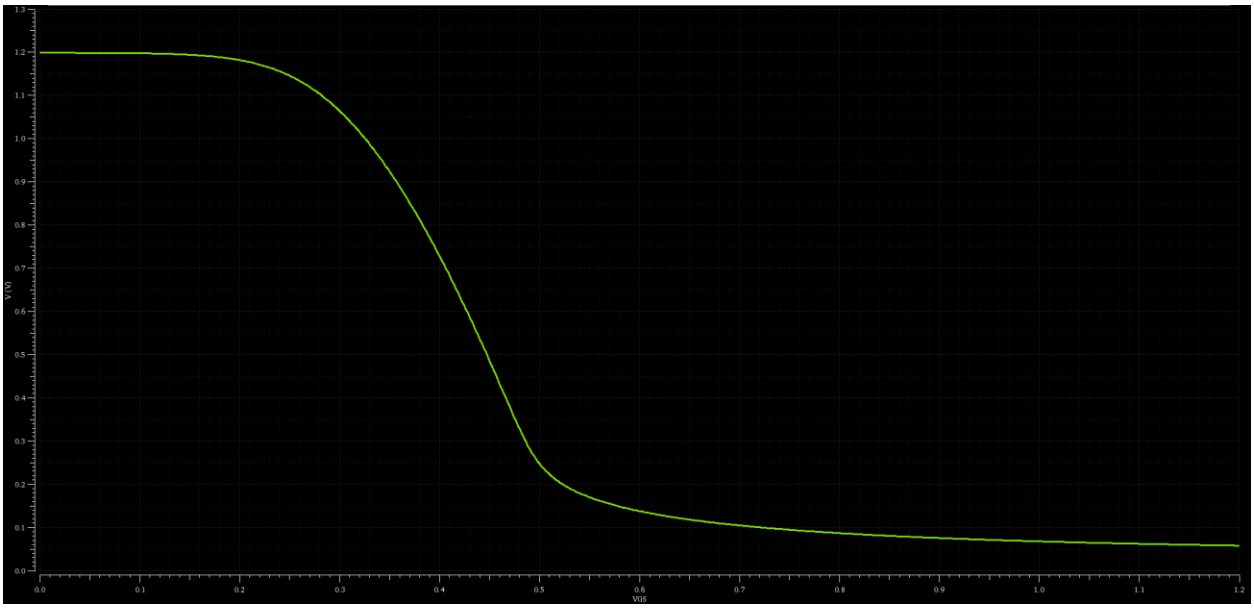
Also, the source was changed in the schematic view to **[vdc]** for the AC analysis to work as follows:

2. Gain Non-Linearity

1) Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to V_{DD} with 2mV step.

DC sweep on $\boldsymbol{V_{GS} = 0: 2mV: V_{DD}}$

2) Report $V_{out}\ vs. V_{in}$. Is the relation linear? Why?



The relation is non-linear. The MOSFET is, in nature, a non-linear device, so it is not expected to have a linear transfer characteristics ($V_{out}\ vs. V_{in}$).

It is noted that there is a section of the transfer characteristics that has nearly linear behavior (0.3:0.5) and especially in small signal approximation the model can be linearized.

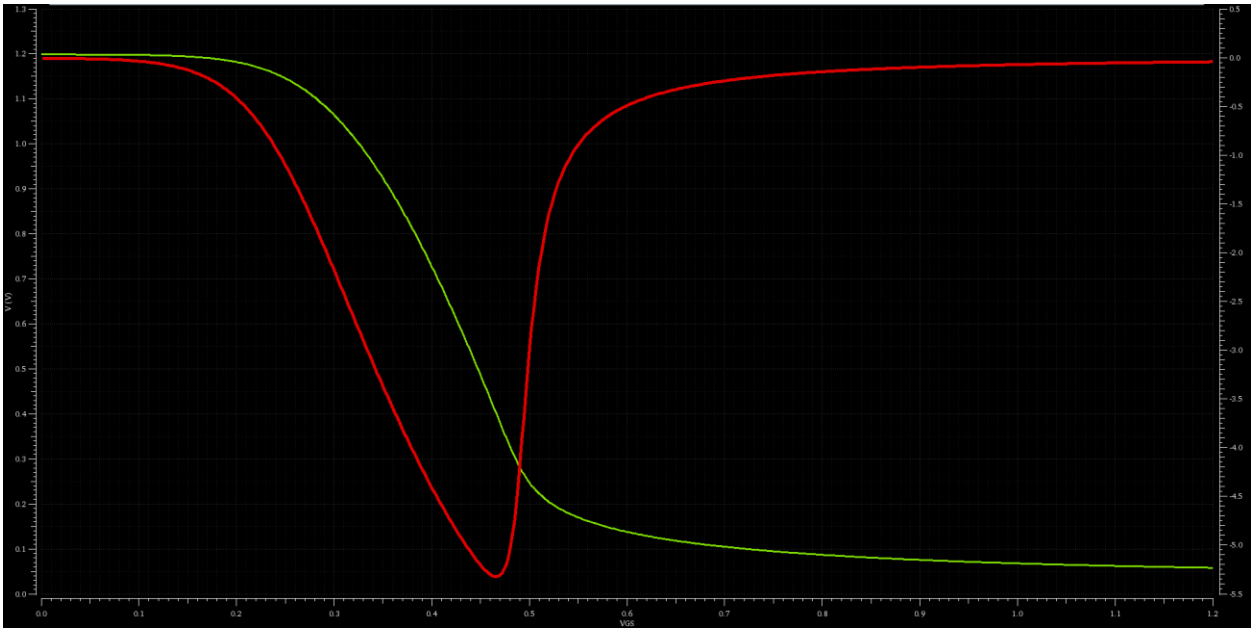
3) Calculate the derivative of V_{out} using calculator. Plot the **derivative vs.** V_{in}. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?

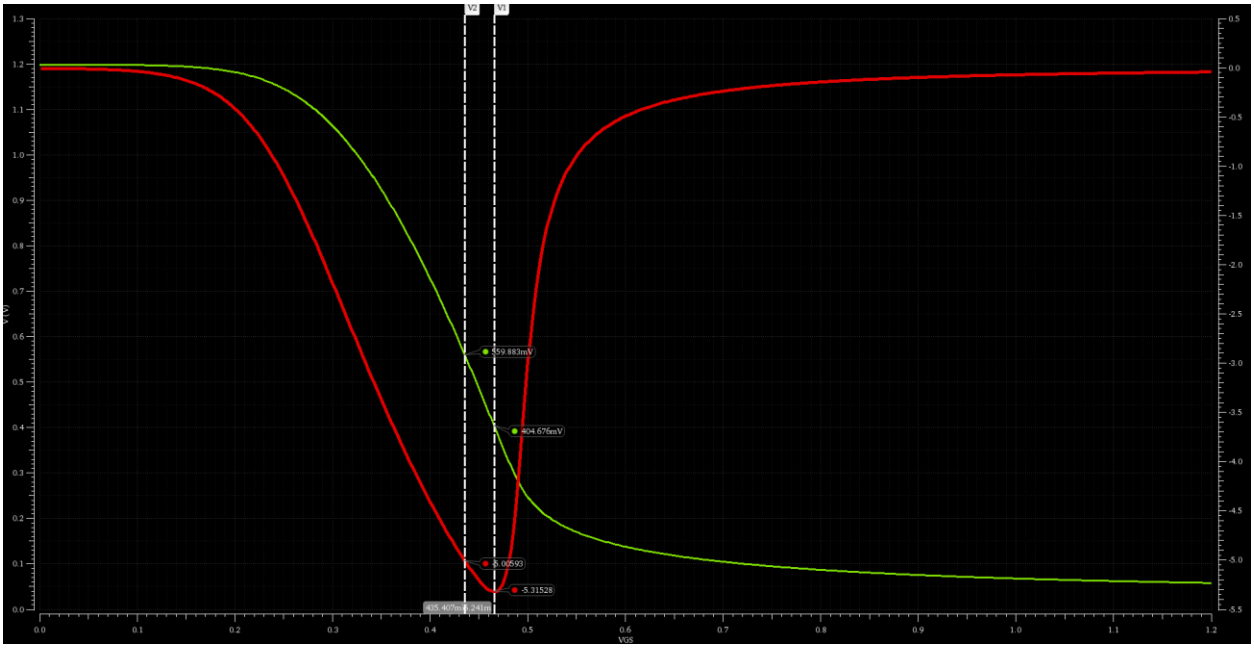
$$A_v = \frac{\boldsymbol{d}V_{out}}{\boldsymbol{d}V_{in}}$$

The derivative of the transfer characteristics results in the small signal gain.

The gain is **non-linear** and is **dependent** on the input V_{GS}, due to the non-linear nature of the MOSFET.

The next two figures shows the non-linearity of the gain.

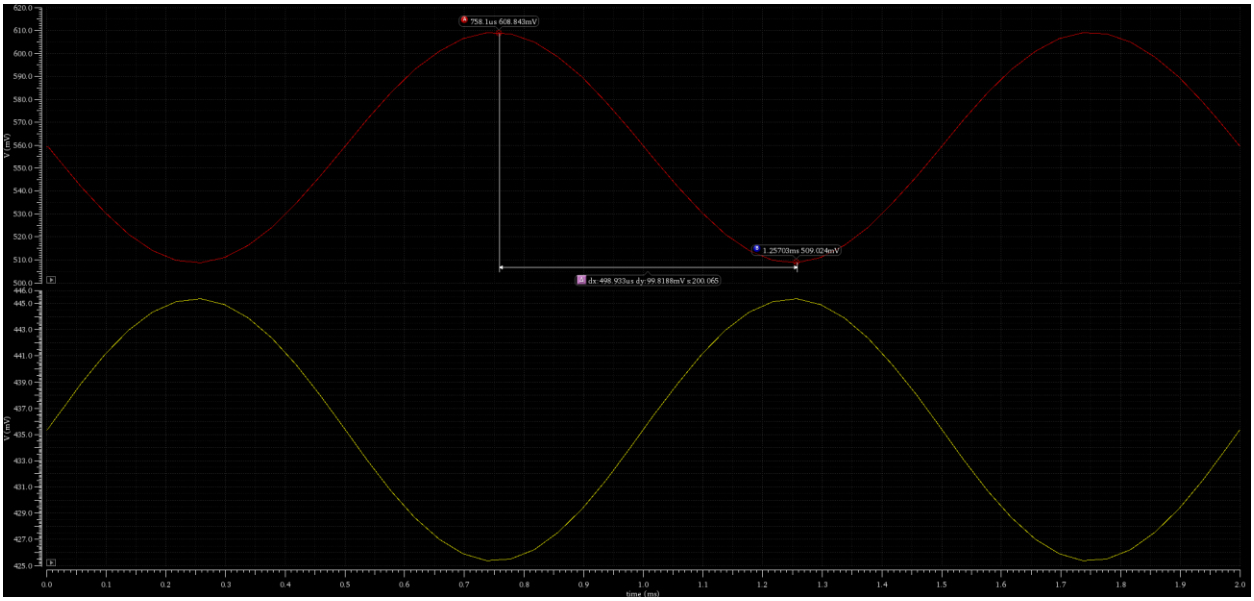




The gain at our chosen $V_{GS} = 435.4069\ mV$, is the same as we calculated before ($A_v = -5$).

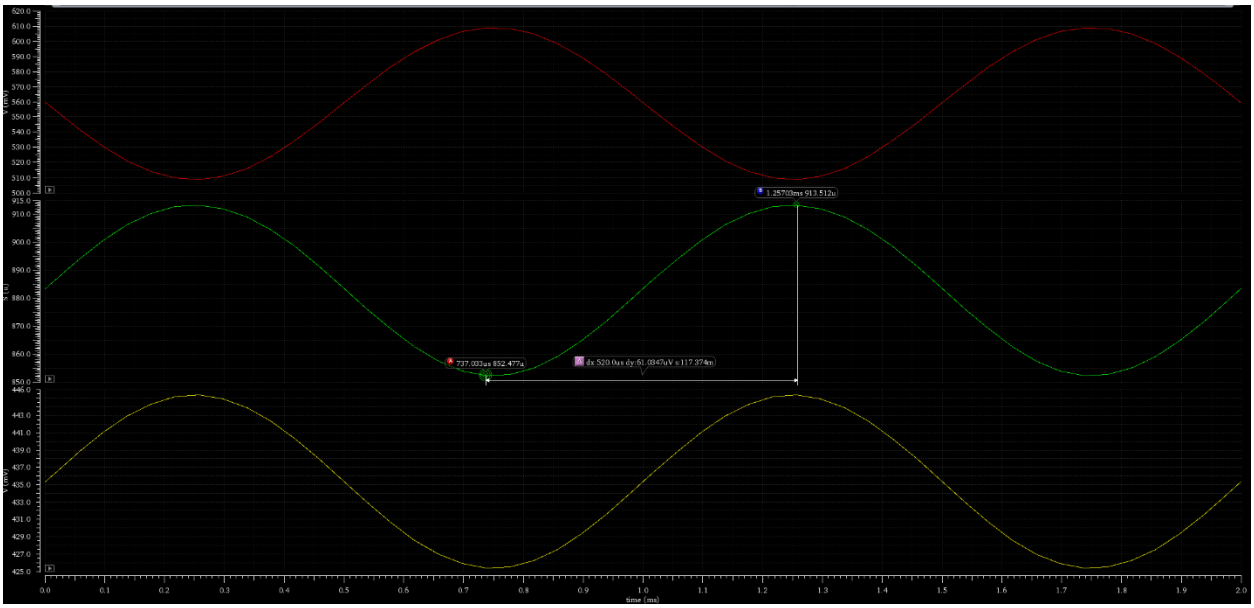
The maximum gain is at $V_{GS} = 468\ mV$, which results in $A_v \approx -5.32$

4) Set the properties of the voltage source to apply a transient stimulus (sine wave of 1 kHz frequency and 10 mV amplitude superimposed on the DC input voltage).



The 20mV p-p of the input was amplified to 100mV p-p in the output with phase difference 180°

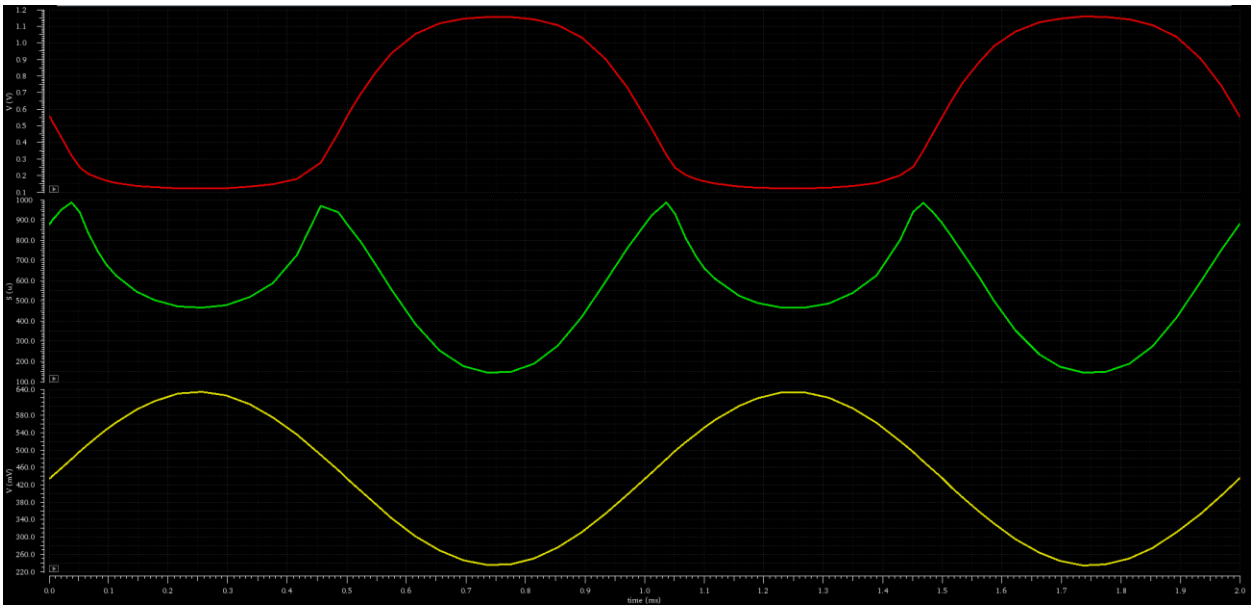
5) Create a new simulation configuration. Run transient simulation for 2ms. Plot g_m **vs. time**. Does g_m vary with the input signal? What does that mean?



The g_m changes in phase with the input, where
at maximum input voltage, g_m reaches maximum of 913.5, and
at minimum input voltage, g_m reaches minimum of 852.5, with difference of 61uS.

This means that the relation of $g_m \; vs. V_{GS}$ is directly proportional. (It is a non-linear relation but with the small signal approximation it can be linearized as we see)

Increasing the amplitude of the AC signal at the input from 20mV p-p to a much higher value (say: 200mV) will introduce the non-linear effects. One such effect is the Distortion of the signal. This can be observed in transient analysis.



As seen, the difference is drastic. The non-linear effects begin to appear due to the – now – invalidity of the small signal linearization approximation.

➔ Cadence Hint: In order to save g_m vs. time, create an empty text file and write the following statement: **`save *:gm sigtype=dev`**. Add this text file in the model libraries. Enable DC simulation.

Actually, this hint is wrong and misleading. The created text file should be added NOT in model libraries, but Simulation Files >> Definition Files. (From sub menu by right clicking the created test in Data View)

This line also has to be added to prevent errors of the program confusing spice with spectre:
`simulator lang = spectre`

6) Is this amplifier linear? Comment.

In the case that the signal (perturbations in the input voltage) is small enough, and hence the small signal approximation is valid, then the amplifier will act linear. However, if the input signal to be increased, the non-linear effects will distort the output signal as seen from the second figure.

3. [Optional] Maximum Gain

1) We want to investigate the variation of **gain vs. R_D**. We will use AC analysis to calculate the small signal gain. Set the **source AC magnitude = 1**. Note that AC analysis is a linear analysis, so we use a magnitude of one such that the output is itself the gain. Keep the **DC value of VGS constant at the DC value you selected in Part 1**.

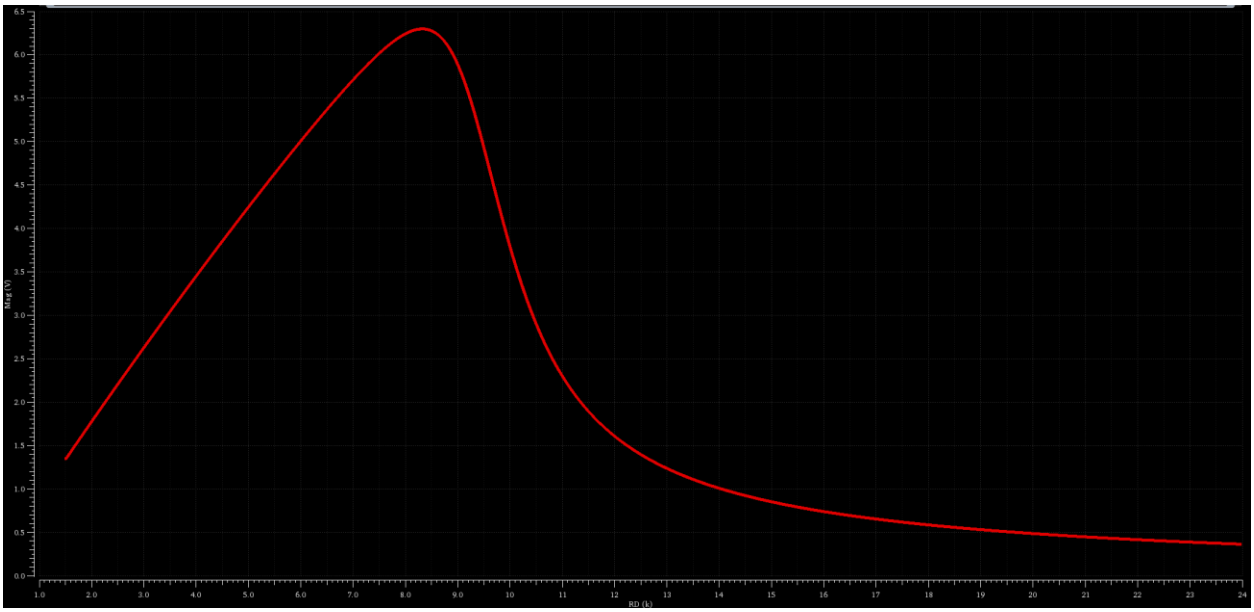
$V_{GS} = 435.4069\ mV$

2) Set AC simulation to sweep design variable (R_D from ¼ the value you selected in Part 1 to 4 times the value you selected in Part 1). Set the **AC simulation frequency at 1 Hz** (single frequency point). The purpose of the AC analysis here is just to get the small signal gain and not to investigate the frequency response.

$$R_D = \frac{6\ k\Omega}{4} : 1\ \Omega : 4 \times 6\ k\Omega$$

A $1\ \Omega$ step is very fine and will take more time, but it will be a more accurate and a smooth curve.

3) Use the calculator to plot the **gain vs. R_D**.



4) You will find that the **gain increases with R_D and then decreases with R_D**. Justify this behavior.

The gain increases with R_D and then decreases. Maximum at [8316.35 Ω, gain = 6.305], then decreases.

Reasoning: As R_D increases, the voltage drop across it V_{R_D} also increases. This results in a less output voltage (V_{DS}), but for the transistor to be in saturation $V_{ov} \leq V_{DS}$, so by increasing R_D, eventually the transistor is **knocked out of saturation** and, of course, will have very bad gain performance.

5) What is the value of $\boldsymbol{R_D}$ that gives the highest gain? What is the highest gain?

$$\boldsymbol{Maximum\ gain} = \mathbf{6.305}, \qquad \boldsymbol{at\ R_D} = \mathbf{8316.35\ \Omega}.$$

6) Analytically calculate the value of $\boldsymbol{R_D}$ that gives the highest gain and the highest gain using the expressions in Part 1. Compare simulation and analysis results.

The highest gain:

$$|\boldsymbol{A_{v,MAX}}| = \frac{d}{d\boldsymbol{R_D}}\ g_m\ (\boldsymbol{R_D} \,||\, r_o) = \frac{d}{d\boldsymbol{R_D}}\ g_m \frac{\boldsymbol{R_D} \times r_o}{\boldsymbol{R_D} + r_o}$$

$$|\boldsymbol{A_{v,MAX}}| = g_m \frac{r_o(\boldsymbol{R_D} + r_o) - \boldsymbol{R_D} \times r_o}{(\boldsymbol{R_D} + r_o)^2} = \frac{g_m r_o^2}{(\boldsymbol{R_D} + r_o)^2} = \frac{883.6046\ \mu S \times (107.3\ k\Omega)^2}{(\boldsymbol{R_D} + 107.3\ k\Omega)^2}$$

Monotonically increasing. This means maximum at infinity. So at $\boldsymbol{R_D} \to \infty$

$$|\boldsymbol{A_{v,MAX}}| = \lim_{\boldsymbol{R_D} \to \infty} g_m \frac{\boldsymbol{R_D} \times r_o}{\boldsymbol{R_D} + r_o} = \frac{g_m r_o}{1}, \qquad (using\ L'Hôpital's\ Rule)$$

So the highest gain possible is the intrinsic gain ($g_m r_o$)

, but $\boldsymbol{R_D}$ *can never be* ∞ , due to the voltage drop on the resistive load.

$$V_{DS} = V_{DD} - I_D R_D$$
$$V_{DS} \geq V_{ov}, \qquad (condition\ of\ saturation)$$
$$\therefore R_D < \frac{V_{DD} - V_{DS,min}}{I_D}$$

$$\therefore \boldsymbol{R_{D,MAX}} = \frac{\mathbf{1.2} - \boldsymbol{V_{DS,min}}}{\mathbf{106.7\ \mu A}}$$

Simulation	Analysis
$\boldsymbol{Maximum\ gain} = \mathbf{6.305}$	$\boldsymbol{Maximum\ gain} = \boldsymbol{g_m r_o}$ $= 883.6046\ \mu S \times 107.3\ k\Omega$ $= \mathbf{94.79}$
$\boldsymbol{at\ R_D} = \mathbf{8316.35\ \Omega}$	$\boldsymbol{at\ R_D} = \infty$, but no voltage drop (which is only possible in case of an ideal current source)

7) What is the available signal swing at the point of maximum gain?

$$\because\ \boldsymbol{R_{D,MAX}} = \mathbf{8316.35\ \Omega} = \frac{\mathbf{1.2} - \boldsymbol{V_{DS,min}}}{\mathbf{106.7\ \mu A}}$$
$$\therefore\ \boldsymbol{V_{DS,min}} = \mathbf{312.645\ mV}, \qquad \boldsymbol{V_{R_D}} = \mathbf{887.35}, \qquad for\ a\ total\ of\ V_{DD} = 1.2\ V$$

$$\therefore \boldsymbol{Output\ Swing_{@MAX\ gain}} = \mathbf{1.2V} - \mathbf{887.35mV} = \mathbf{312.645\ mV}$$

NOTE THAT: $\boldsymbol{Output\ Swing_{p-p\ @\ gain=5}} = \mathbf{1.2V} - \mathbf{0.24} = \mathbf{960\ mV}$

8) Is scaling down the supply voltage good for gain? Comment.

No, scaling down the transistor dimensions forced us to scale down the voltage to a limit. Gain is reduced drastically by reducing V_{DD}.

$$R_D < \frac{V_{DD} - V_{DS,min}}{I_D}$$

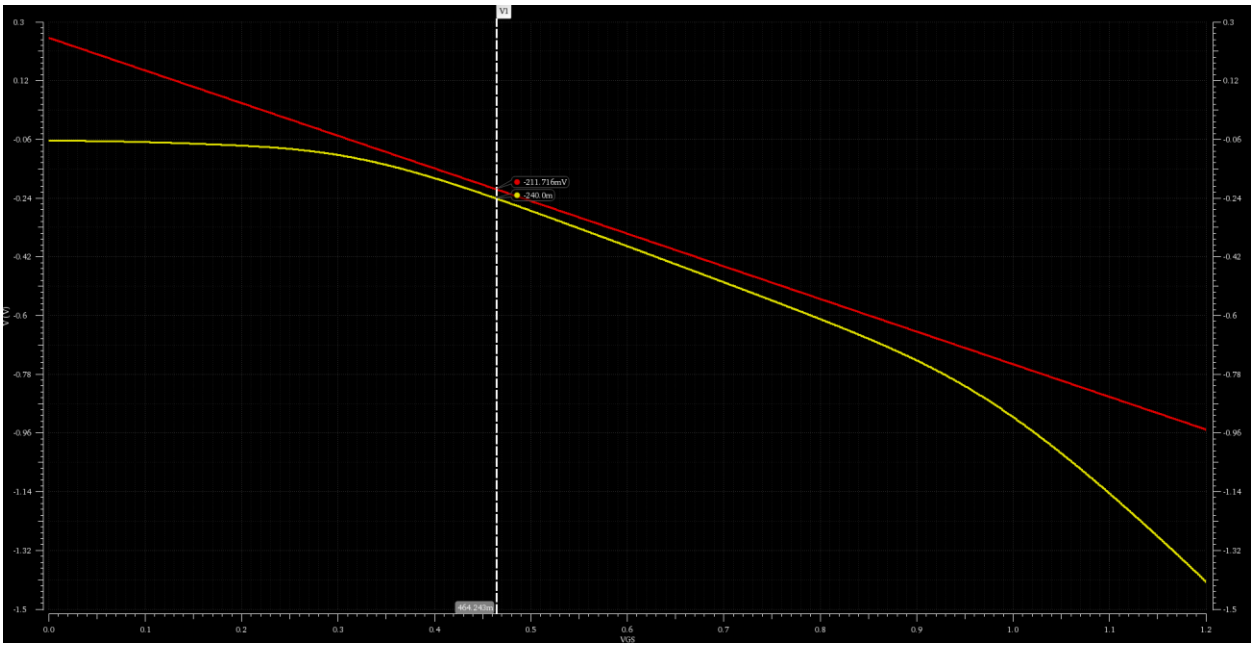
$As\ V_{DD} \uparrow,\ R_D \downarrow$, and hence, gain decreases.

4. [Optional] Gain Linearization (feedback)

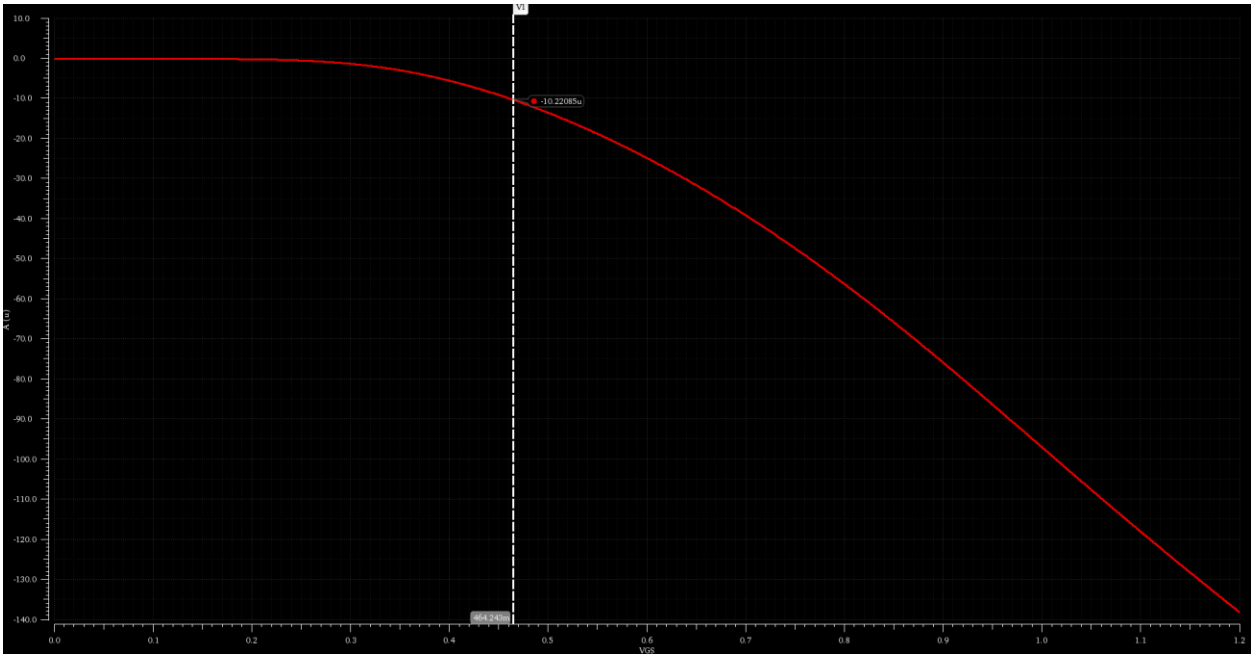
1) We will use feedback to improve the gain non-linearity. We will study feedback in more details later.
2) Create a new schematic and copy the old schematic into it.
3) Replace the resistive load with a PMOS current source (active load) as shown below. Create a sizing chart for the PMOS similar to what we did for NMOS in Part 1 using $\boldsymbol{L = 2\mu m}$ and $\boldsymbol{W = 10\mu m}$ (you may use the same test bench used in Part 1). From the chart, assuming $\boldsymbol{V_Q^*}$ similar to NMOS, determine $\boldsymbol{V_{GSQ}}$ and $\boldsymbol{I_{DX}}$. Using ratio and proportion (cross-multiplication) determine $\boldsymbol{W}$ similar to Part 1. Note that the PMOS load must have the same bias current as the NMOS input device.

Creating a sizing chart for the PMOS: $\boldsymbol{W = 10\ \mu m}\ and\ \boldsymbol{L = 2\ \mu m}$

Assuming $\boldsymbol{V_Q^*}$ similar to NMOS: $\boldsymbol{V_Q^* = 240mV}$, Plot $\boldsymbol{V^*}$ and $\boldsymbol{V_{ov}}$ vs. $\boldsymbol{V_{GS}}$ to get $\boldsymbol{V_{GSQ}}$.



$$\boldsymbol{V_{GSQ} = 464.243m}$$



$$\boldsymbol{I_{DX} = -10.22085\ \mu A}$$

W	$\boldsymbol{I_D}$
10 µm	I_{DX} @ V_Q^* (from the chart)
?	$I_{DQ} = 100\ \mu A$ (from the specs)

$$W = \frac{10\ \mu m \times 100\ \mu A}{I_{DX}\ @\ V_Q^*\ \text{(from the chart)}}$$

Instead of $100\ \mu A$ we will use the same current as the NMOS

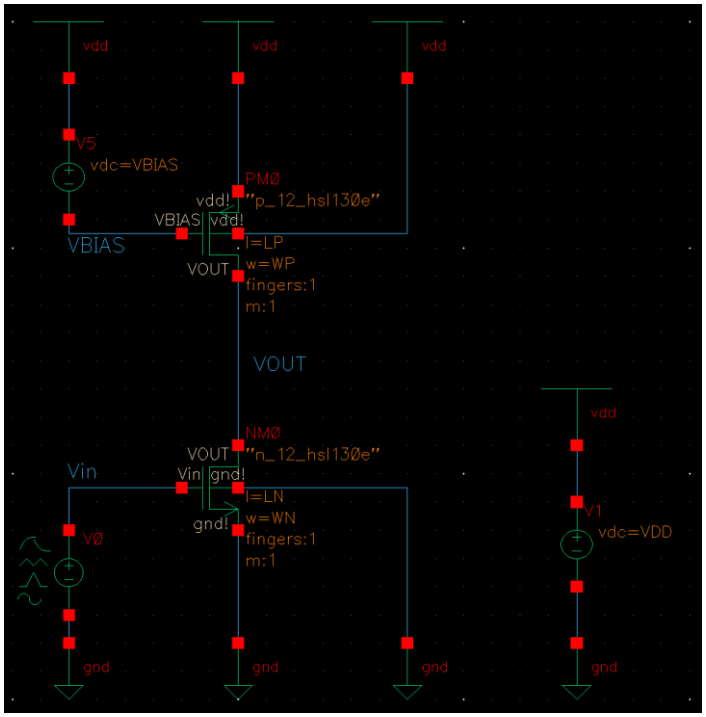
$$W = \frac{10\ \mu m \times 106.7\ \mu A}{\boldsymbol{10.22085\ \mu A}} = 104.3944\ \mu m \approx 105\ \mu m$$

And these are the readings from the first run where $\boldsymbol{V_{GSQ} = 435.4069 mV}$

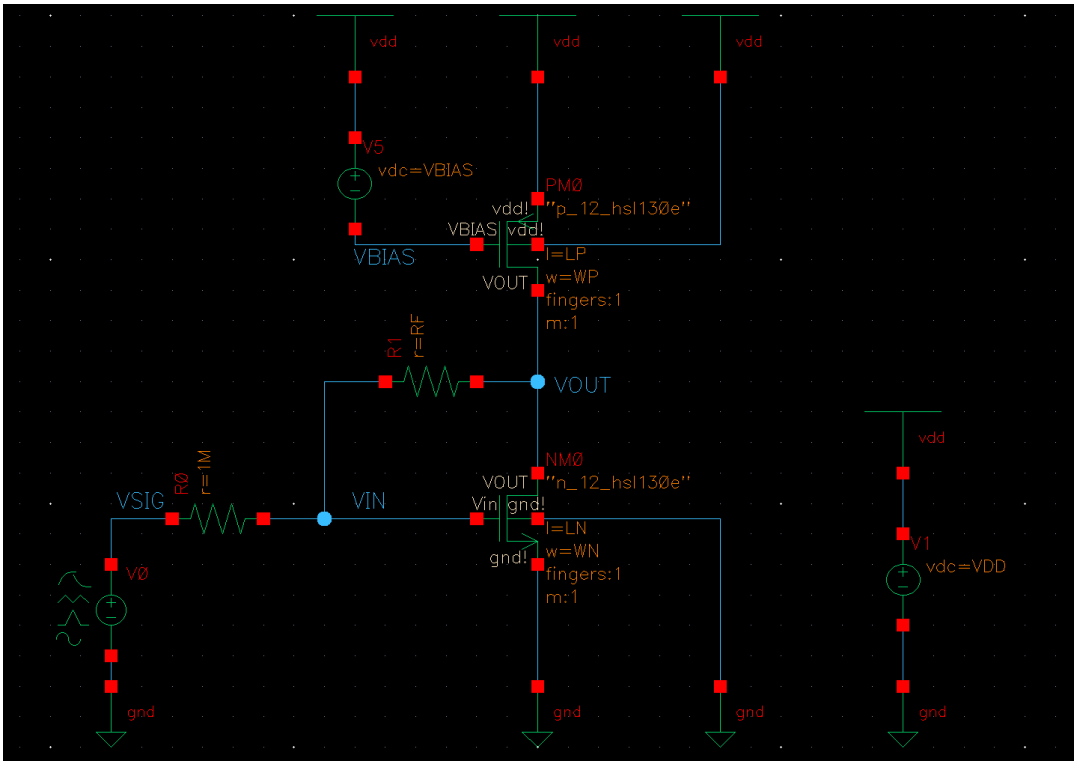
ID_p	
vth_p	-252.5m
id_p	-7.91u
gm_p	75u
gds_p	189.1n
Vov_p	
(2ID/Gm)_p	
ro_p	5.289M

W	$\boldsymbol{I_D}$
10 µm	I_{DX} @ V_Q^* (from the chart)
?	$I_{DQ} = 100\ \mu A$ (from the specs)

4) **Note that** it is better to bias the PMOS using a voltage source between the gate of the PMOS and VDD.



5) Add two resistors: input resistor $(\boldsymbol{R_{in}})$ = 1 M and feedback resistor (R_f). Choose R_f to give a voltage gain approximately equal to $(\boldsymbol{R_f/R_{in}}) = |\boldsymbol{A_v}|$ as given in the specs.



Choosing R_f

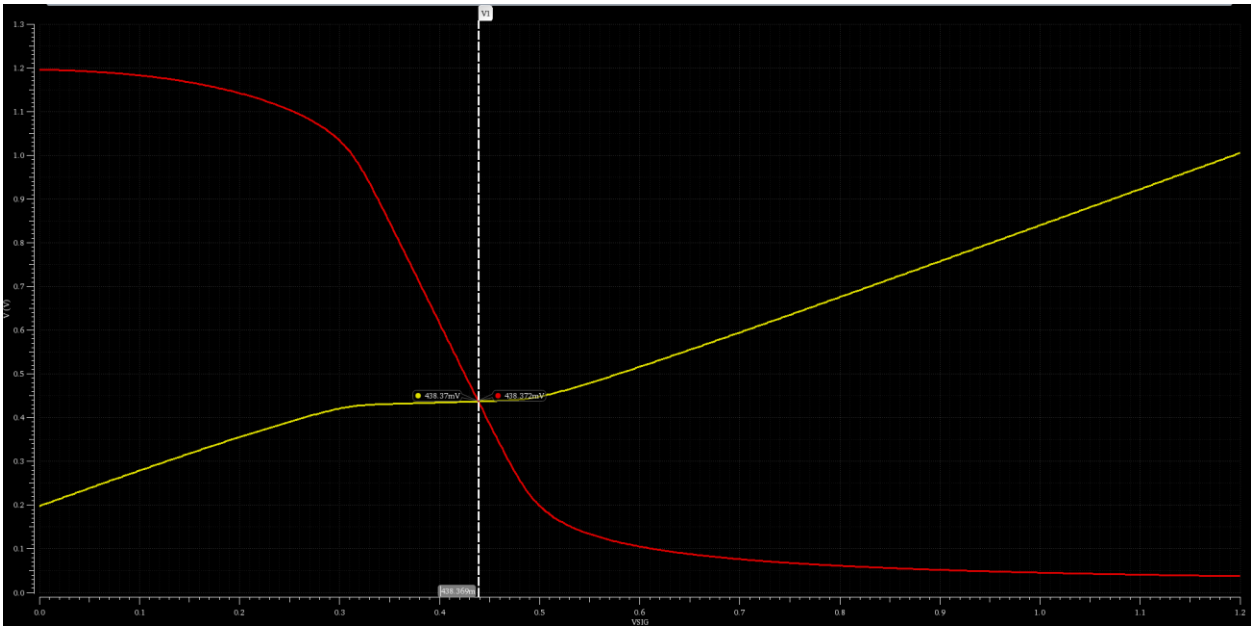
$$\left(\frac{R_f}{R_{in}}\right) = |A_v| = 5 = \frac{R_f}{1\ M\Omega}, \qquad \therefore R_f = 5\ M\Omega$$

Note that $\boldsymbol{V_{GSQ} = 464.243m}$, which is the VBIAS of the PMOS.

6) Perform a DC sweep for the input voltage $(\boldsymbol{V_{SIG}})$ from 0 to $\boldsymbol{V_{DD}}$ with 2mV step.

7) Report $\boldsymbol{V_{IN}}$ and $\boldsymbol{V_{OUT}}$ vs. $\boldsymbol{V_{SIG}}$ (overlaid). At what voltage do the two curves cross? Why?

Hint: Compare this voltage to $\boldsymbol{V_{GS}}$ of M1. The center value of the amplification region is itself $\boldsymbol{V_{GS}}$ of M1. At this point $\boldsymbol{V_{OUT}}$ is also equal to $\boldsymbol{V_{IN}}$ because no current flows in the two resistors.



The two curves cross at 438.37mV

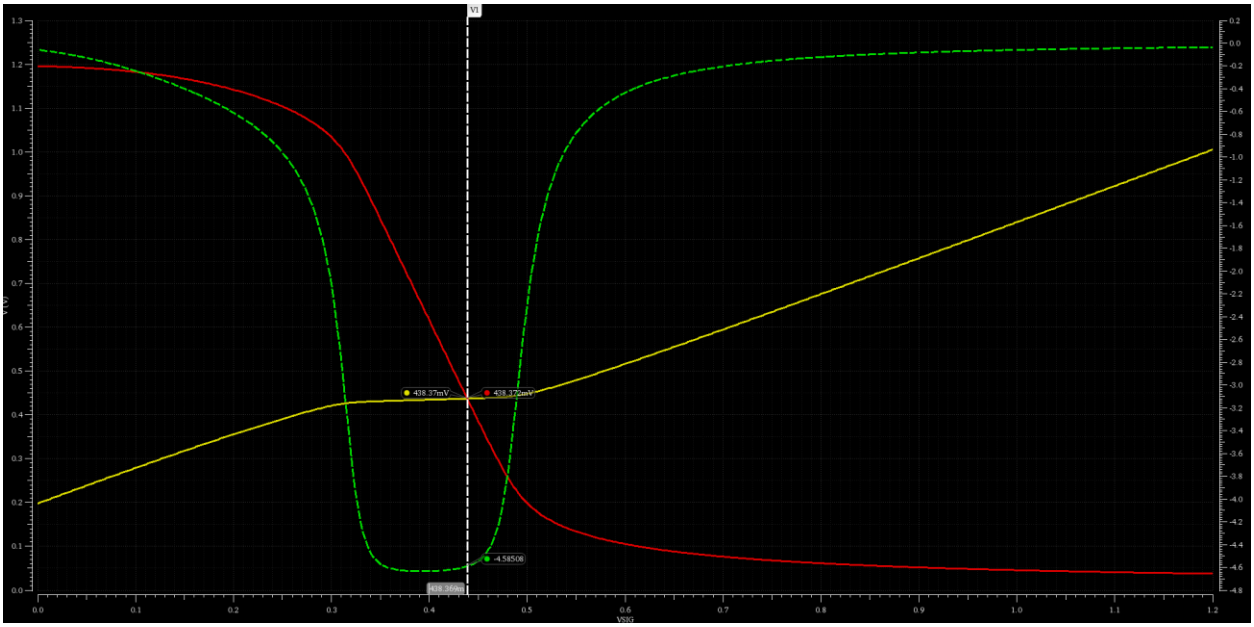
VGS of M1 is 435.4069m

The center value of the amplification region is itself $\boldsymbol{V_{GS}}$ of M1. At this point $\boldsymbol{V_{OUT}}$ is also equal to $\boldsymbol{V_{IN}}$ because no current flows in the two resistors.

8) Is $\boldsymbol{V_{OUT}}$ vs. $\boldsymbol{V_{SIG}}$ linear? Why?

Not at all points, but it is linear in the part we operate at. This is much better and more linear than the no feedback case. It is linear due to the feedback.

9) Calculate the derivative of V_{OUT}. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?



The gain is not linear at all regions but it is noted that g_m is constant at the region we operate in, so the gain is linear in this region. This is due to the feedback.

10) What is value of V_{IN} in the part where the gain is linear?

Voltage V_{IN} is nearly constant at this part. $V_{IN} = between\ 430\ mV\ to\ 440\ mV$

11) Analytically calculate the DC input range over which the gain is linear. Compare your analysis with the simulation result.

Hint: When V_{SIG} deviates from V_{GS1} current flows and V_{OUT} deviates. The amplifier fails when M1 or M2 gets out of saturation ($V_{DS} < V^*$).

You can get the input range by dividing the output range by the gain $\approx \frac{VDD-2V^*}{|A_v|}$

$$Input\ Range_{peak-peak} = \frac{VDD - 2V^*}{|A_v|} = \frac{1.2 - 2(0.24)}{5} = 144\ mV$$

$$Input\ Range_{p-p,Simulation}$$

$$= 2 \times [432.9m - 357.9m]$$

$$= 2 \times 75mV = 150mV$$

The Input range where linearity holds is from about $432\ mV$ to about $358\ mV$.

Lab Summary

- *In Part 1 I learned*
  - How to generate and use design charts for NMOS and PMOS transistors.
  - How to design a resistive-loaded common-source amplifier.
  - How the overdrive voltage of a MOS transistor deviates from the square law in different regions of operation.

- *In Part 2 I learned*
  - How to do ac and DC simulations of a CS amplifier.
  - How the gain of an amplifier changes with the input signal amplitude.
  - How to get the maximum attainable gain of a CS amplifier by changing the load resistor.
  - How to use feedback resistors to reduce gain non-linearity.

Acknowledgements

Thanks to all who contributed to these labs. Special thanks to Dr. Sameh A. Ibrahim for reviewing and editing the labs. If you find any errors or have suggestions concerning these labs, contact Hesham.omran@eng.asu.edu.eg.

[END OF LAB 2]

Kerollos Saad Thomas