

ALTIUM PCB COURSE (JULY 2024)

Variant: 5V / 3V3

7/24/2024
Trial 1

RELEASED 24-JULY-2024

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DESIGN CONSIDERATIONS

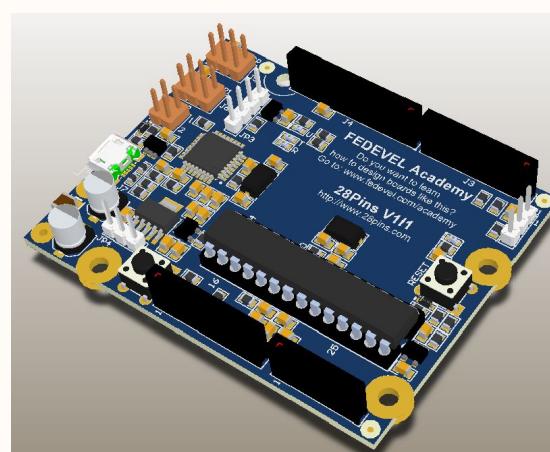
DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.



Would you like to learn how to design boards like this?

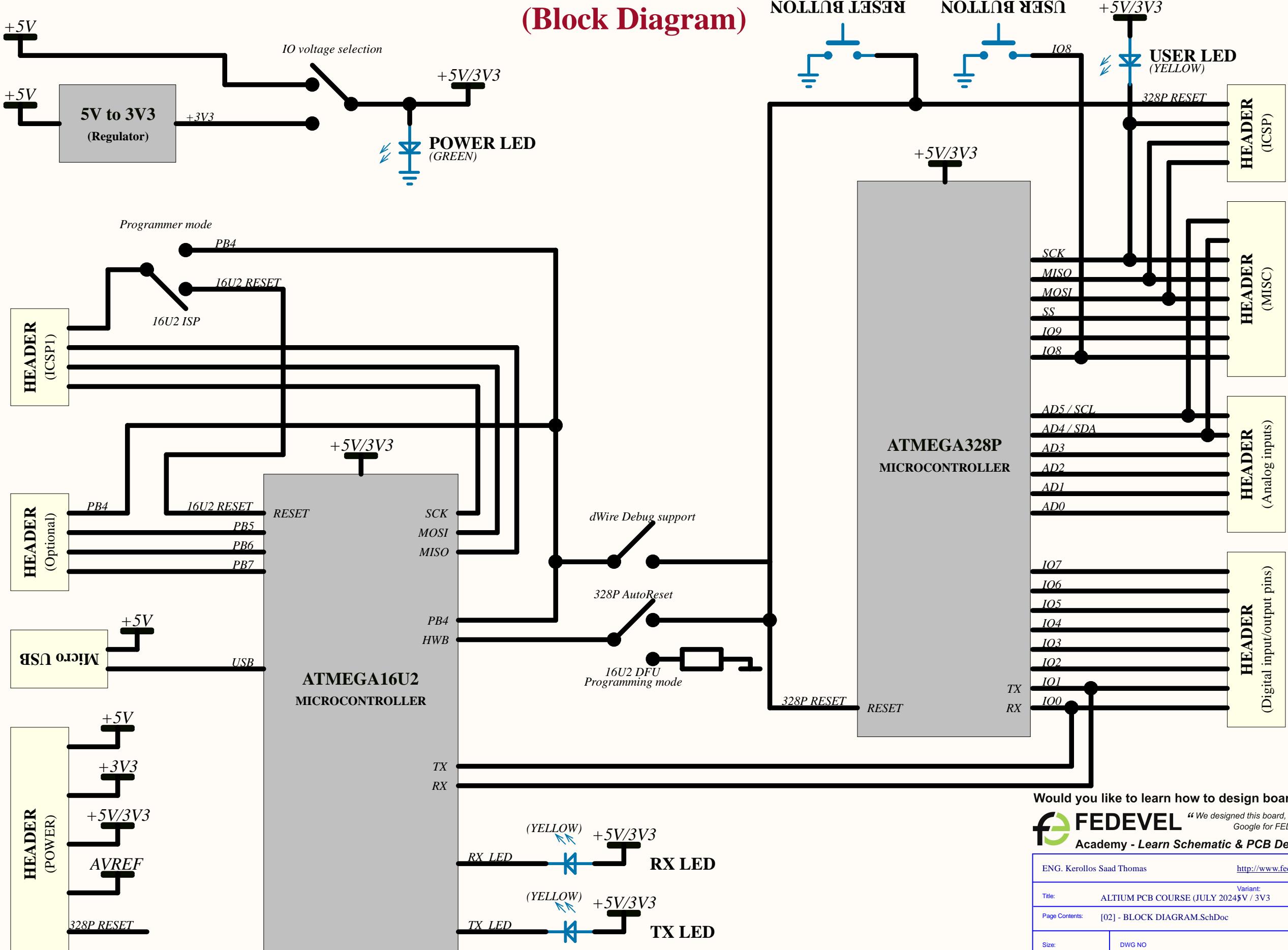
FEDEVEL "We designed this board, so you can learn, Google for FEDEVEL Academy"

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| Title: | ALTIUM PCB COURSE (JULY 2024) 5V / 3V3 |
| Page Contents: | [01] - COVER PAGE.SchDoc Checked by |
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ALTIUM PCB COURSE (JULY 2024)

(Block Diagram)



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| Page Contents: | [02] - BLOCK DIAGRAM.SchDoc |
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| Sheet 2 of 5 | |

28PINS - SCHEMATIC (JULY 2024)

My Version of the 28pins project by FEDEVEL

<https://www.28pins.com/>

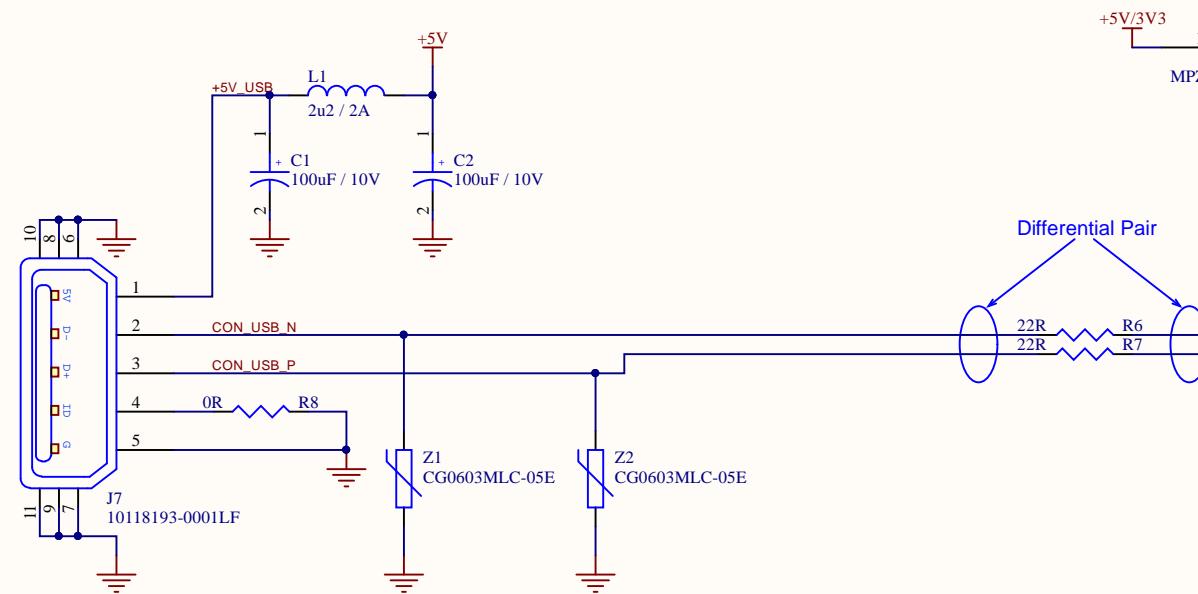
Design Notes

DESIGN NOTE:
This board supports 5V or 3V voltage level on the IO pins:
1) 5V IO - Fit everything as defined in this schematic. NF means, do not fit this component.
2) 3.3V IO - Remove R27, Fit R28. Replace Y1 (change from 16MHz to 10MHz).
3) Both 5V and 3V3 selected through JP4 - Remove R27, Remove R28, Fit JP4. Replace Y1 (change from 16MHz to 10MHz); Replace Y2 (change from 16MHz to 8MHz).
*Note: The 16MHz crystals are not recommended for 3.3V operation. We need to adjust their values, that's why the change.
IMPORTANT: Once you change the crystal value, you may need to re-compile your source code.

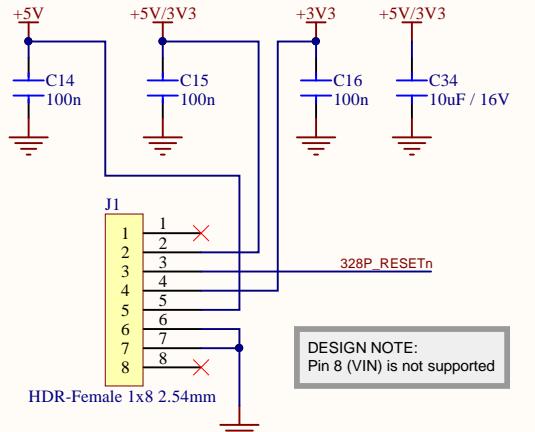
DESIGN NOTE:
About JP3:
1) DebugWire support - Short 1&2. This was added to support possible debugWire debugging (programming) of 328P through 16U2. In this case, the 16U2 crystals are not recommended for 3.3V operation. We need to adjust their values, that's why the change.
2) ISP programmer mode - Short 2&3. In this case, take a cable and connect J5 & J6 together. Upload AVRISP MKII firmware to 16U2 and you can program 328P. Examples of AVRISP MKII firmwares can be found in LUFA project at www.foundwiredude.com/LUFA.php (remap LEDs of the default AVRISP MKII LUFA project to the RX and TX LEDs on the 28Pin board)
3) ISP header - Short 3 & 4. In this mode, the ICSP1 header is used as a standard ISP header to program 16U2 through ISP interface by an ISP programmer.

DESIGN NOTE:
About JP1:
1) AutoReset Enabled - Short 2&3. In this case, 16U2 is used to reset 328P when firmware inside 328P is updated from Arduino IDE.
2) 16U2 DFU mode Enabled - Short 2&3. 16U2 HWIO pin is sampled by 16U2 during RESET. If it pulled low, then after Reset the 16U2 will go into DFU mode (it's the mode when you flash 16U2 firmware through USB and Atmel Flip software: <http://www.atmel.com/tools/flip.aspx>)

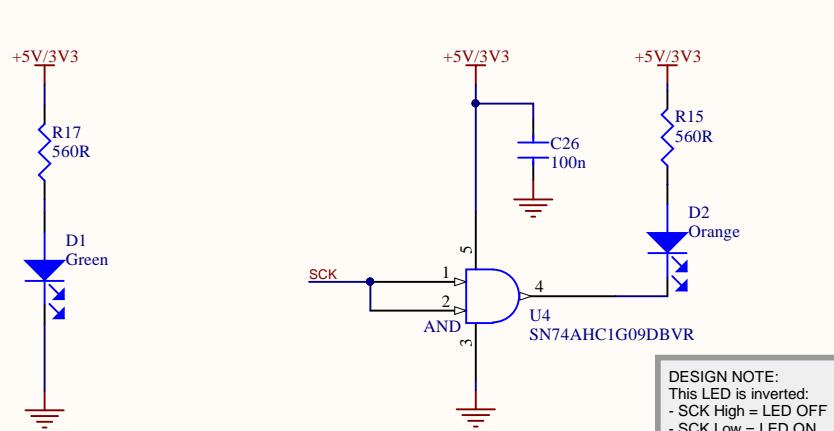
Micro USB



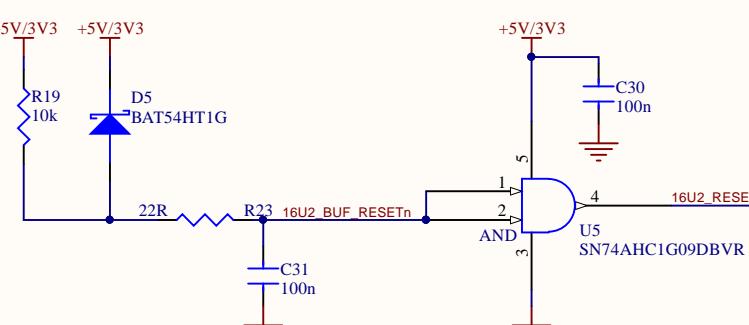
POWER



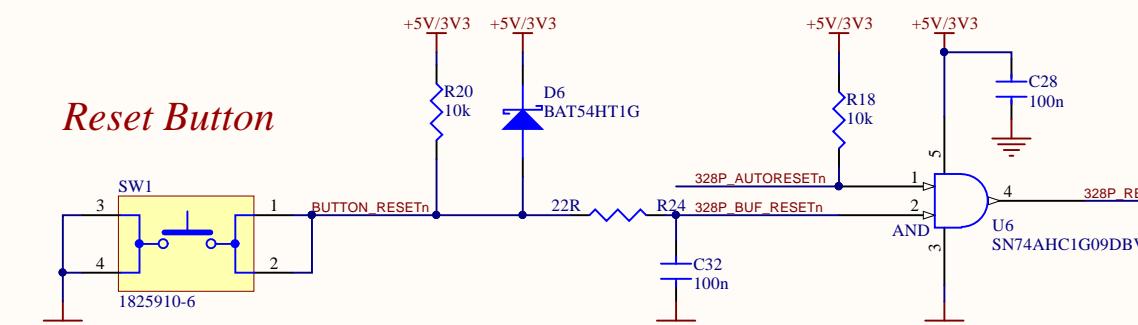
POWER LEDS



RESET (16U2)

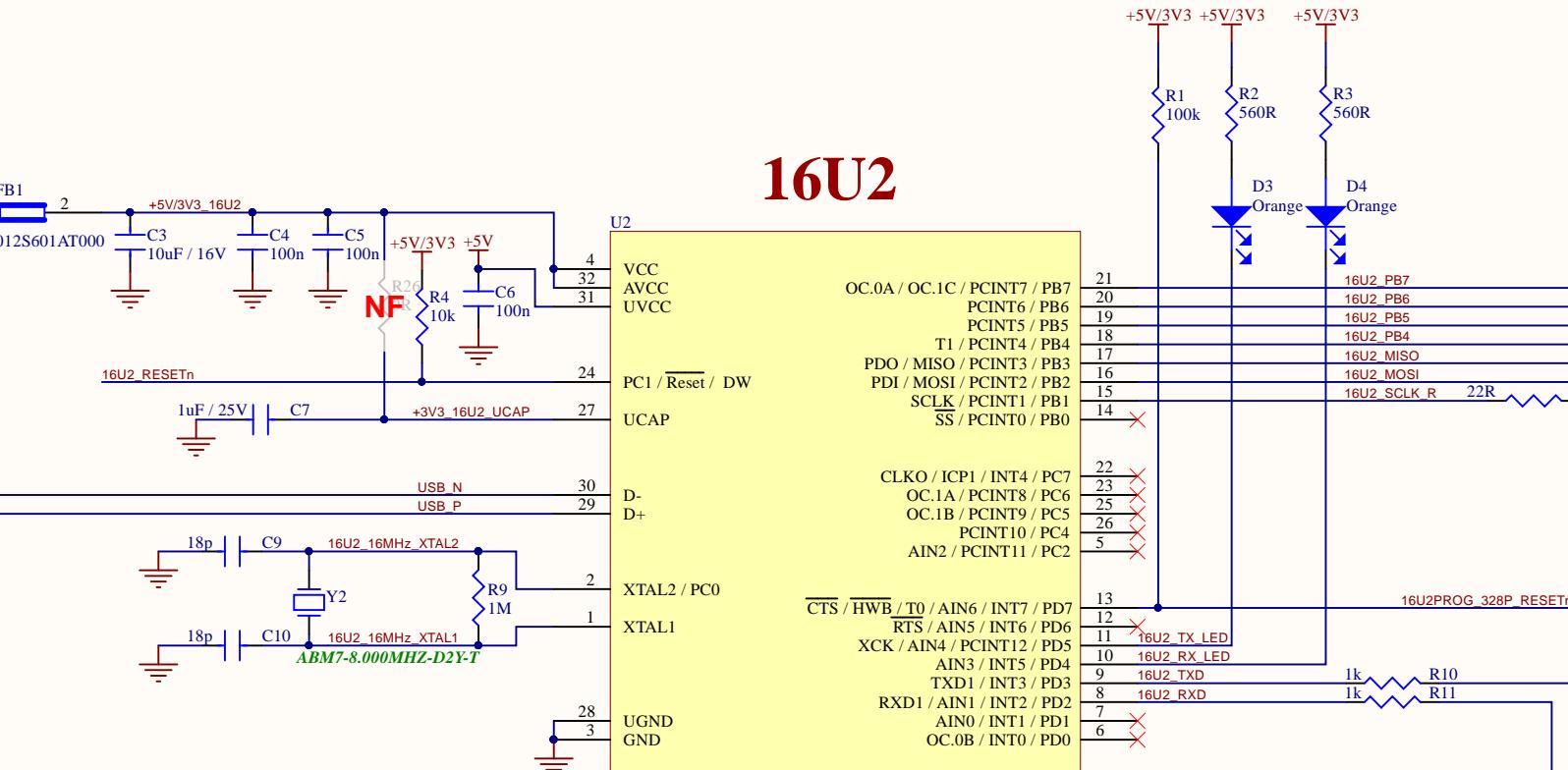


Reset Button

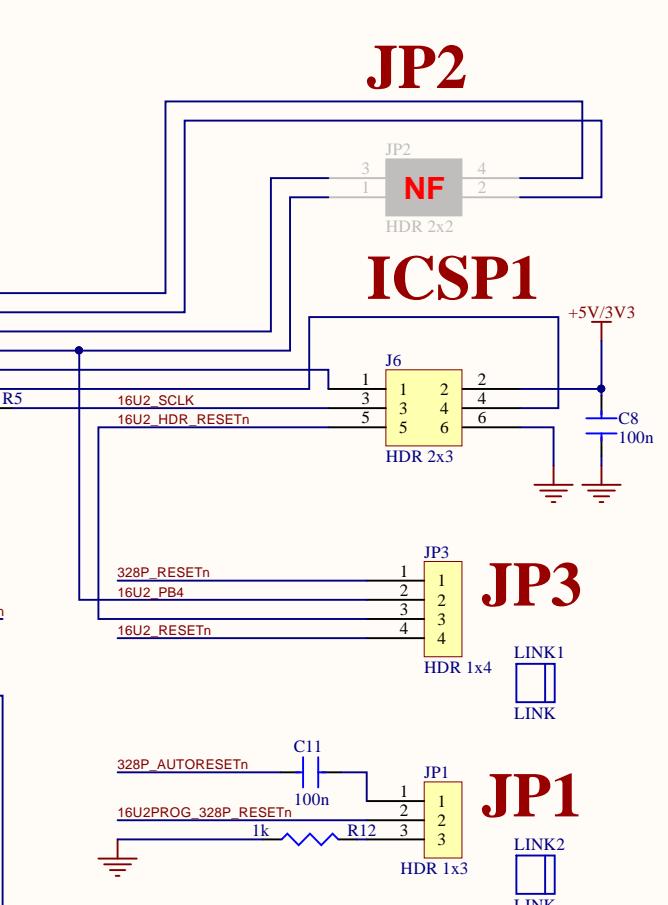


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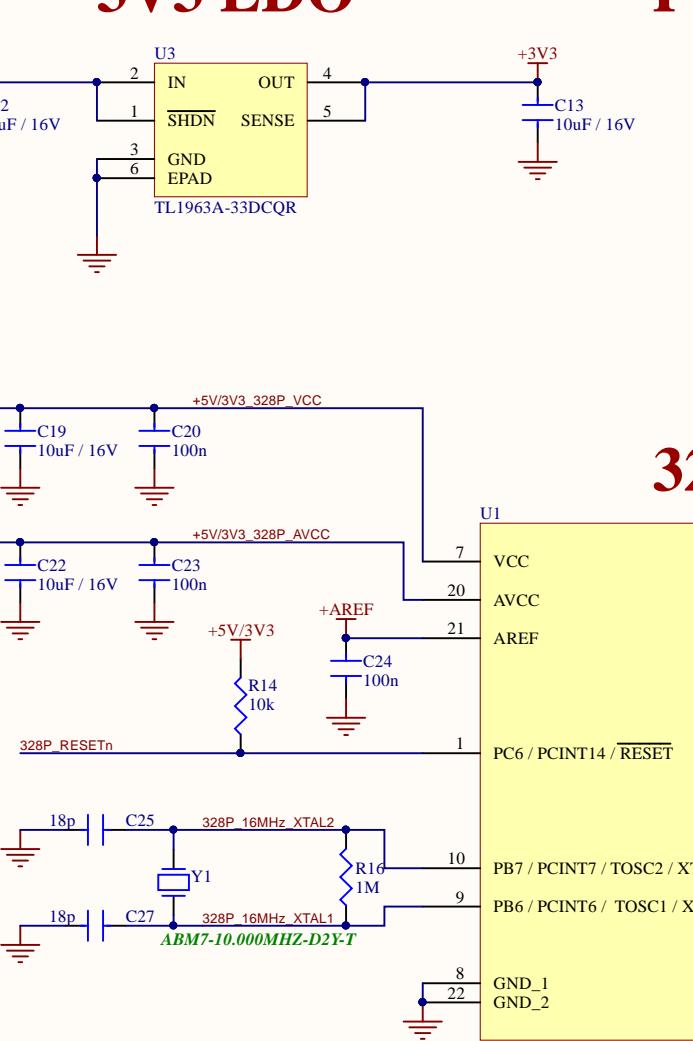
16U2



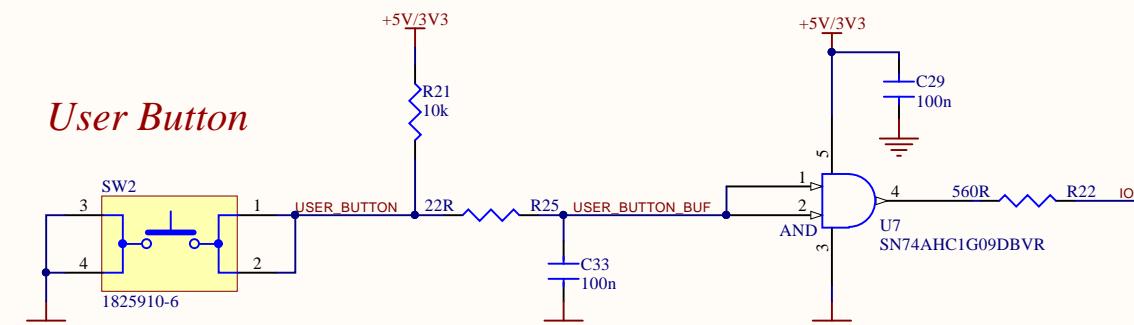
Power Selection



328P



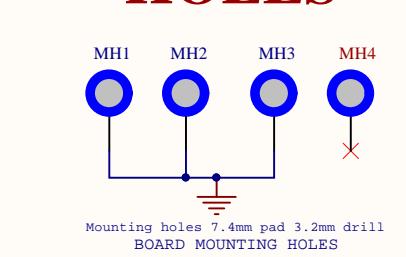
USER BUTTON



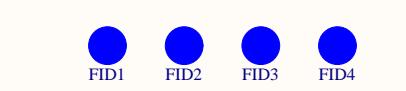
DIP SOCKET



MOUNTING HOLES



FIDUCIALS



LAYOUT NOTE:
1) Route all the POWER tracks with minimum track width 0.4mm.
2) Route all the other tracks by 0.4mm and change them by the end of the design to 0.2mm. To change all of them at once, use this filter '(not InNet(*)) and not InNet("GND") and IsTrack and (OnLayer("L1") or OnLayer("L2"))' and then set 0.2mm width in PCB Inspector panel.

| | |
|---|--|
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| Title: ALTIUM PCB COURSE (JULY 2024) | Variant: 5V / 3V3 |
| Page Contents: [03] - 28PINS SCHEMATIC.SchDoc | Checked by http://www.fedovel.com/designer |
| Size: A2 | DWG NO |
| Date: 7/24/2024 | Designed by www.fedovel.com |
| Sheet 3 of 5 | Trial 1 |

REVISION HISTORY

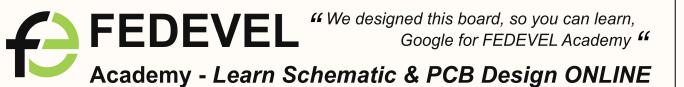
A A

B B

C C

D D

Would you like to learn how to design boards like this?



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| Page Contents: | [04] - REVISION HISTORY.SchDoc |
| Checked by: | |
| Size: | DWG NO |
| Revision: | Trial 1 |
| Date: | 7/24/2024 |
| Sheet 4 of 5 | |

Designator
[01] - COVER PAGE.SchDoc

Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - 28PINS SCHEMATIC.SchDoc

Designator
[04] - REVISION HISTORY.SchDoc

A

A

B

B

C

C

NOTES

Mark Not Fitted Components as
NF

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

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| Page Contents: | 28Pins_Project_VIII Project.SchDoc |
| Checked by: | |
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